AIROC™ Bluetooth® system on chip for automotive applications

CYW89820 is a monolithic, single-chip, Bluetooth® 5.0 compliant, standalone baseband processor system on chip (SoC) with an integrated 2.4 GHz transceiver.

Manufactured using the industry's most advanced 40-nm CMOS low-power process, the CYW89820 employs the highest level of integration, eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth® solutions.

Integrating a transceiver, baseband processor, Arm® Cortex®-M4, and application flash memory on a single die provides the capability to replace function-specific devices with a single design that offers all Bluetooth® modes of operation.

The CYW89820 brings the latest Bluetooth® technology to automotive applications and offers automotive Grade 2 (–40°C to +105°C) ambient operating temperature performance. The CYW89820 is tested to Automotive Electronics Council AEC-Q100 environmental stress guidelines and is manufactured in ISO9001 approved and TS16949 certified facilities.

Features

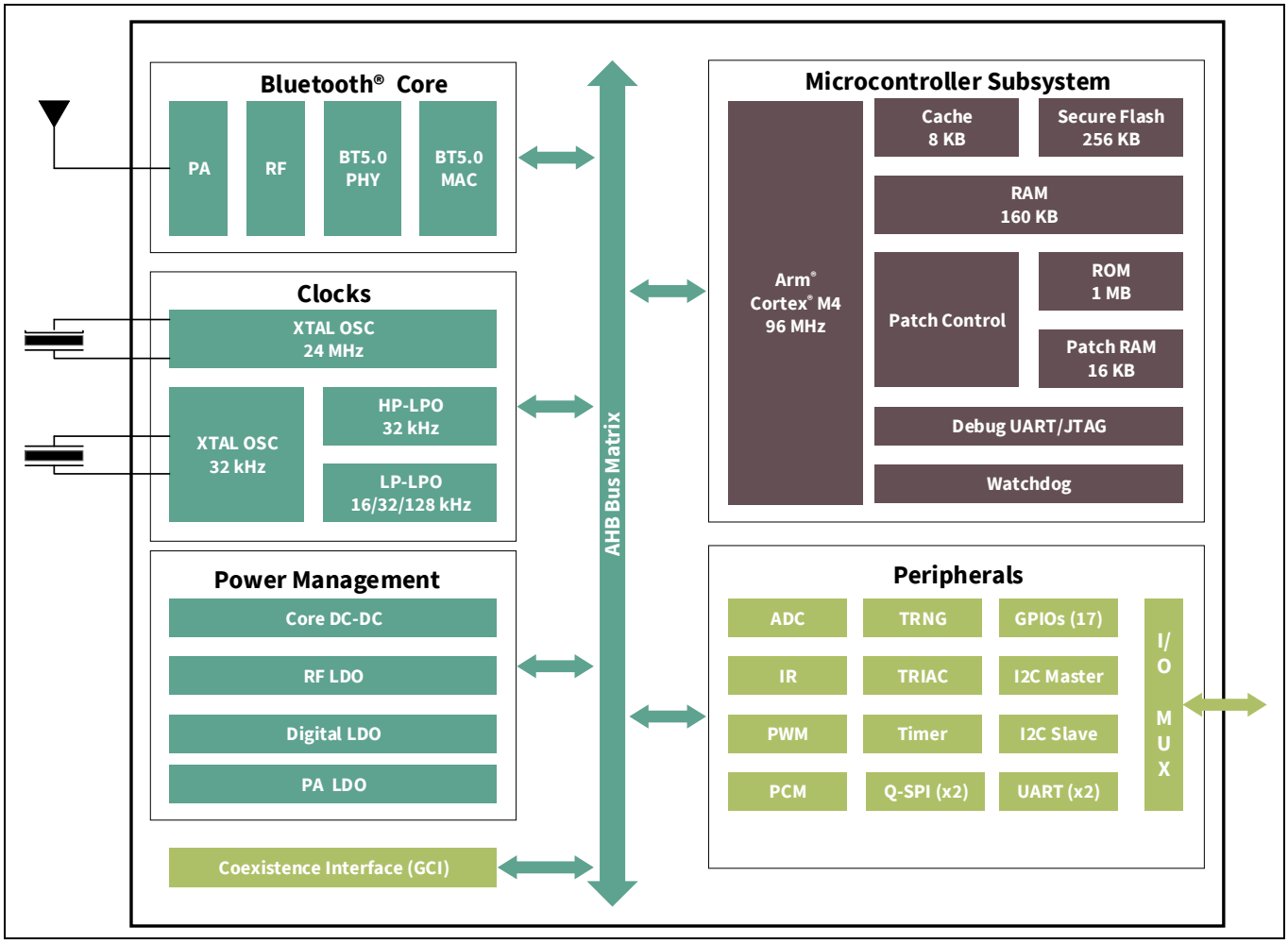
- Bluetooth® subsystem
  - Complies with Bluetooth® Core Specification version 5.0
    - QDID: **151200**
    - Declaration ID: **D043201**
  - Includes support for BR, EDR 2 Mbps and 3 Mbps, eSCO, Bluetooth® LE, and LE 2 Mbps.
  - Programmable TX Power up to 11.5 dBm
  - Excellent receiver sensitivity (–94 dBm for BLE 1 Mbps)
- Microcontroller
  - Powerful Arm® Cortex®-M4 core with a maximum speed of 96 MHz
  - Bluetooth® stack in ROM allowing standalone operation without any external MCU
  - 256-KB on-chip secure flash
  - 176-KB on-chip RA
  - Bluetooth® stack, peripheral drivers, security functions built into ROM (1 MB) allowing application to efficiently use on-chip flash
  - AES-128 and true random number generator (TRNG)
  - Security functions in ROM including ECDSA signature verification
  - Over-the-air (OTA) firmware updates
- Peripherals
  - 17 GPIOs
  - I2C, I2S, UART, and PCM interfaces
  - Quad-SPI interfaces
  - Auxiliary ADC with up to 14 analog channels
  - General-purpose timers and PWM
  - Real-time clock (RTC) and watchdog timers (WDT)
- Power management
  - On chip power-on reset (POR)
  - Integrated buck (DC-DC) and LDO regulators
  - On chip software controlled power management unit
  - On chip 32-kHz LPO with optional external 32-kHz crystal oscillator support

- Wi-Fi coexistence
  - Global Coexistence Interface (GCI) for Infineon Wi-Fi parts
  - Serial Enhanced Coexistence Interface (SECI)
- Supported in ModusToolbox™ software
- OTA firmware update support
- Grade-2 (–40°C to +105°C) operation
- Package types
  - 48-pin WQFN
  - RoHS compliant

Applications

- Automotive
  - Car access and car sharing
  - Keyless entry
  - Passive entry and passive start (PEPS)
  - Remote parking
  - Wireless diagnostics (OBD)
  - Sensors
  - Cable replacement
- Industrial
  - Access control
  - Asset tracking
  - Factory automation
  - Logistics management
  - Sensors

Functional block diagram



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1 Bluetooth® baseband core

The Bluetooth® baseband core (BBC) implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all ACL, SCO, eSCO, LE, and 2 Mbps LE connections. It prioritizes and schedules all RX/TX activities including adv, paging, scanning, and servicing of connections. In addition to these functions, it independently handles the host controller interface (HCI) including all commands, events, and data flowing over HCI. The core also handles symbol timing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), authentication, data encryption/decryption, and data whitening/dewhitening.

Table 1 lists key Bluetooth® features supported by the CYW89820.

Table 1 Key Bluetooth® features supported by CYW89820

Bluetooth® 1.0	**Bluetooth® 1.2**	**Bluetooth® 2.0**
Basic rate	Interlaced scans	EDR 2 Mbps and 3 Mbps
SCO	Adaptive frequency hopping	–
Paging and inquiry	eSCO	–
Page and inquiry scan	–	–
Sniff	–	–
Bluetooth® 2.1	**Bluetooth® 3.0**	**Bluetooth® 4.0**
Secure simple pairing	Unicast connectionless data	Bluetooth® Low Energy
Enhanced inquiry response	Enhanced power control	–
Sniff Subrating	eSCO	–
Bluetooth® 4.1	**Bluetooth® 4.2**	**Bluetooth® 5.0**
Low duty cycle advertising	Data packet length extension	LE 2 Mbps
Dual mode	LE secure connection	Slot availability mask
LE link layer topology	Link layer privacy	High duty cycle advertising

1.1 BQB and regulatory testing support

The CYW89820 fully supports Bluetooth® test mode as described in Part I:1 of the Specification of the Bluetooth® System v3.0. This includes the transmitter tests, normal and delayed loop back tests, and reduced hopping sequence.

In addition to the standard Bluetooth® test mode, the CYW89820 also supports enhanced testing features to simplify RF debugging and qualification. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

1.2 Wi-Fi coexistence support

The CYW89820 includes support for:

- Global Coexistence Interface for use with Infineon Wi-Fi parts
- Serial Enhanced Coexistence Interface (SECI) for use with SECI compatible Wi-Fi parts

2 Microprocessor unit

The CYW89820 includes a Cortex® M4 processor with 1 MB of program ROM, 160 KB of data RAM, 16 KB of patch RAM, and 256 KB of flash. The CM4 has a maximum speed of 96 MHz. The 256 KB of flash is supported by an 8 KB cache allowing direct code execution from flash at near maximum speed and low power consumption.

The CM4 runs all the BT layers as well as application code. The ROM includes LMAC, HCI, L2CAP, GATT, as well as other stack layers freeing up most of the flash for application usage.

A standard serial wire debug (SWD) interface provides debugging support. Refer to the **"Firmware"** on page 21 section for details on the architecture and layers that are included in the ROM.

2.1 Main crystal oscillator

The CYW89820 uses a 24 MHz crystal oscillator (XTAL).

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 1**).

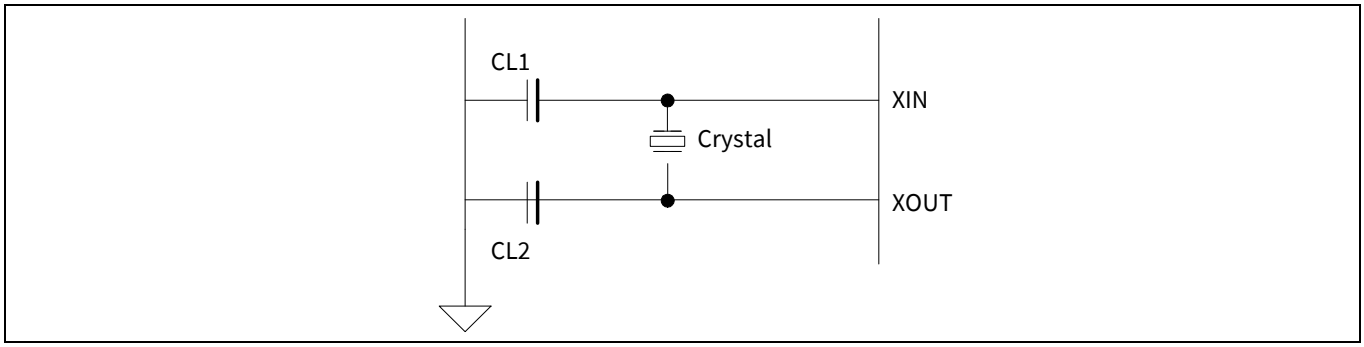


Figure 1 Recommended oscillator configuration

Table 2 Reference crystal electrical specifications

Parameter	Sym	Electrical specification				Note
		Min	Typ	Max	Unit	
Nominal frequency	FL	20	24	40	MHz	–
Oscillation mode	–	Fundamental			–	–
Load capacitance	CL	8			pF	–
Frequency tolerance	–	±10			ppm	at 25°C ±3°C
Frequency stability	–	± 20			ppm	Over operating temperature range (reference 25°C)
Operating temperature	–	–40	–	105	°C	–
Aging	–	±3			ppm	1st year
Drive level	DL	–	100	200	uW	–
Series resonant resistance	Rr	–	–	60	Ω	–
Shunt capacitance	C0	–	–	3	pF	–
Insulation resistance	–	500	–	–	MΩ	at DC 100 V
Storage temperature range	–	–40	–	125	°C	–

2.2 32 kHz crystal oscillator

The CYW89820 includes a 32 kHz oscillator to provide accurate timing during low power operations. **Figure 2** shows the 32 kHz XTAL oscillator with external components and **Table 3** lists the oscillator's characteristics. This oscillator can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The XTAL must have an accuracy of ±250 ppm or better per the BT spec over temperature and including aging. The default component values are: R1 = 10 MΩ and C1 = C2 = ~6 pF. The values of C1 and C2 are used to fine-tune the oscillator.

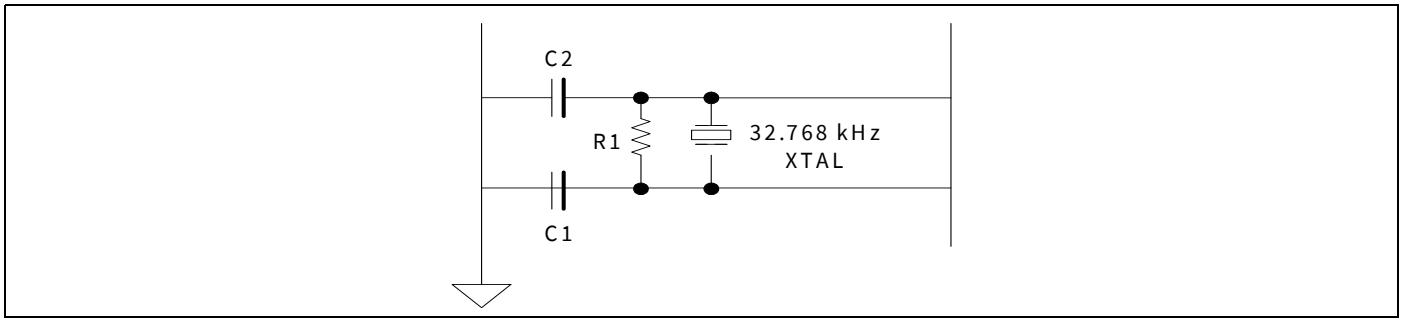


Figure 2 32 kHz oscillator block diagram

Table 3 XTAL oscillator characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Over temperature and aging	–	–	250	ppm
XTAL drive level	P_{drv}	For crystal selection	–	–	0.5	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF

2.3 Low-frequency clock sources

The 32-kHz low-frequency clock (LPO_32K on the following figure) can be obtained from multiple sources. There are two internal low-power oscillators (LPOs), called the LP-LPO and HP-LPO, as well as external crystal connections (OSC32K). The firmware determines the clock source to use among the available LPOs depending on the accuracy and power requirements. The preferred source is the external LPO (OSC32K) because it has good accuracy with the lowest current consumption. Internal LP-LPO has low current consumption and low accuracy whereas HP-LPO has higher accuracy and higher current consumption. The firmware assumes the external LPO has less than 250 PPM error with little or no jitter.

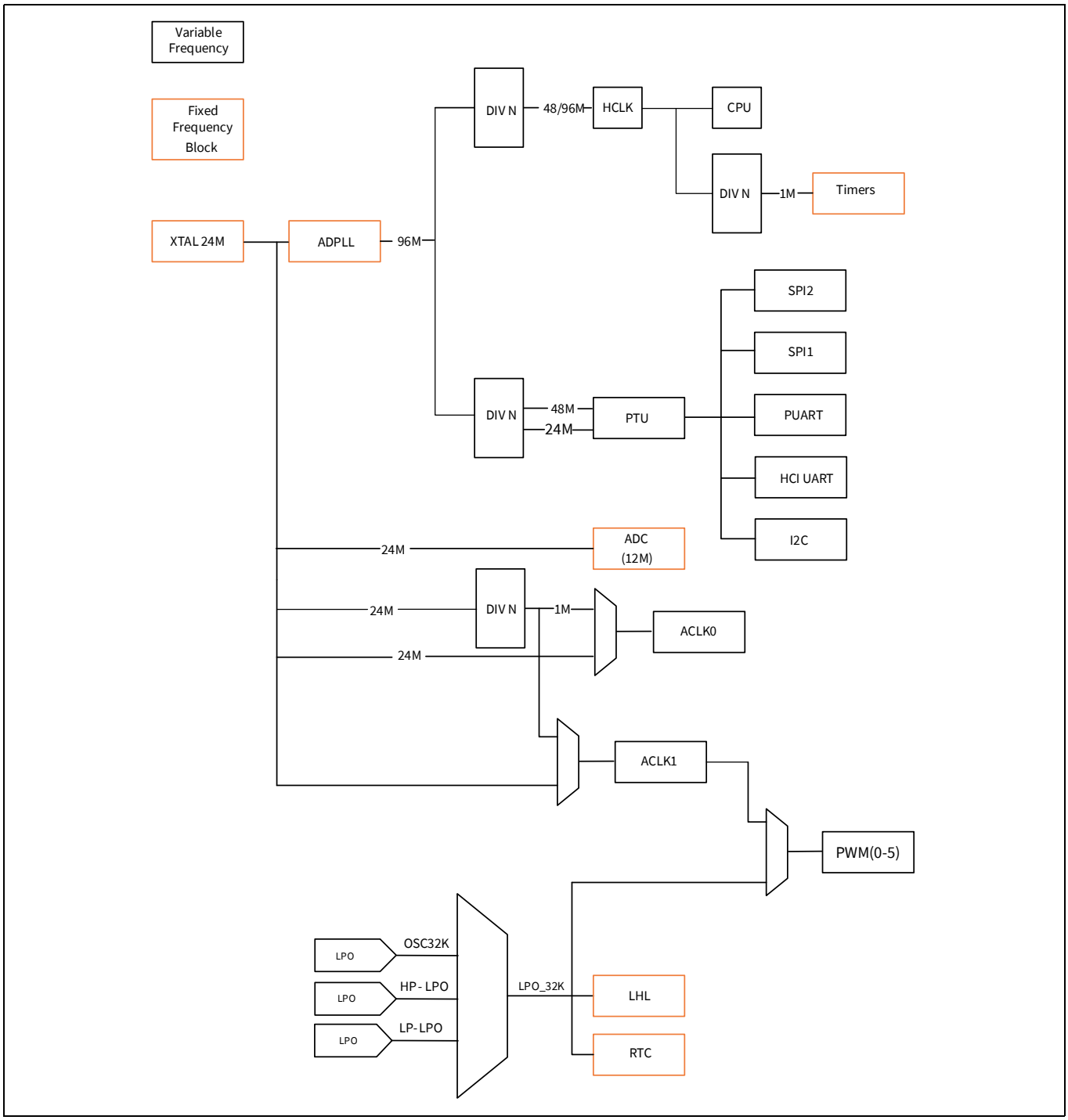


Figure 3 Simplified clock source

2.4 Power modes

The CYW89820 supports the following HW power modes:

- Active mode: Normal operating mode in which all peripherals are available and CPU is active
- Idle mode - CPU is paused: In this mode, the CPU is in “Wait for Interrupt” (WFI) and the HCLK, which is the high frequency clock derived from the main crystal oscillator, is running at a lower clock speed. Other clocks are active and the state of the entire chip is retained.
- Sleep mode: All systems clocks idle except for the LPO. The chip can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIOs. In this mode, CPU is in WFI and the HCLK is not running. The PMU determines if the other clocks can be turned off and does accordingly. State of the entire chip is retained, the internal LDOs run at a lower voltage (voltage is managed by the PMU), and SRAM is retained.
- PDS (Power Down Sleep) mode: Radio powered down and digital core mostly powered down except for RAM, registers, and some core logic. CYW89819 can wake up either after a programmed period of time has expired or if an external event is received via one of the GPIOs.
- ePDS (extended PDS) mode: This is an extension of the PDS Mode. In this mode, only the main RAM and ePDS control circuitry retains power. As in other modes, the CYW89819 can wake up either after a programmed period or upon receiving an external event.
- HID-OFF (Deep Sleep) mode: Core, radio, and regulators powered down. Only the LHL IO domain is powered. In this mode, the CYW89819 can be woken up either by an event on one of the GPIOs or after a certain amount of time has expired. After wakeup, the part will go through full FW initialization although it will retain enough information to determine that it came out of HID-OFF and the event that caused the wake up. LPO and RTC are turned off in this mode. Either an internal LPO or an external input would provide a measure of time.

Transition between power modes is handled by the on-chip firmware with host/application involvement. In general ePDS is the most power efficient mode for most active use cases. HID-OFF generally works for non-connectable beacon type use cases with long advertisement intervals. Refer to the **“Firmware”** on page 21 section for more details.

2.5 Watchdog

CYW89820 includes an onboard watchdog with a period of approx. 4 seconds. The watchdog timer generates an interrupt to the FW after 2 seconds of inactivity and resets the parts after 4 seconds.

2.6 Lockout functionality

The CYW89820 power up with JTAG and SWD access to flash and RAM is disabled. After reset, FW checks OCF for the presence of a security lockout field. If present, FW leaves JTAG and SWD Flash and RAM access disabled and also blocks any HCI commands from reading the raw contents of the RAM or Flash.

The security field can be programmed in the factory after all programming and testing has been done. Refer to the **ModusToolbox™ software** documentation for details on how to enable this feature. This provides an effective way of protecting against any tampering, dumping, probing or reverse engineering of OCF resident user application. The only FW upgrade path in this scenario is the secure OTA update.

2.7 True random number generator

The CYW89820 includes a hardware TRNG. Applications can access the random number generator via the firmware driver. Refer to the **ModusToolbox™ software** documentation for details.

3 Power-on and external reset

Figure 4 shows power-on and reset timing of the CYW89820. After VBAT is applied and reset is inactive, the internal buck turns on, followed by the RF and Digital LDOs. Once the LDO outputs have stabilized, the PMU allows the digital core to come out of reset. As shown in the figure, external reset can be applied at any time subsequent to power up.

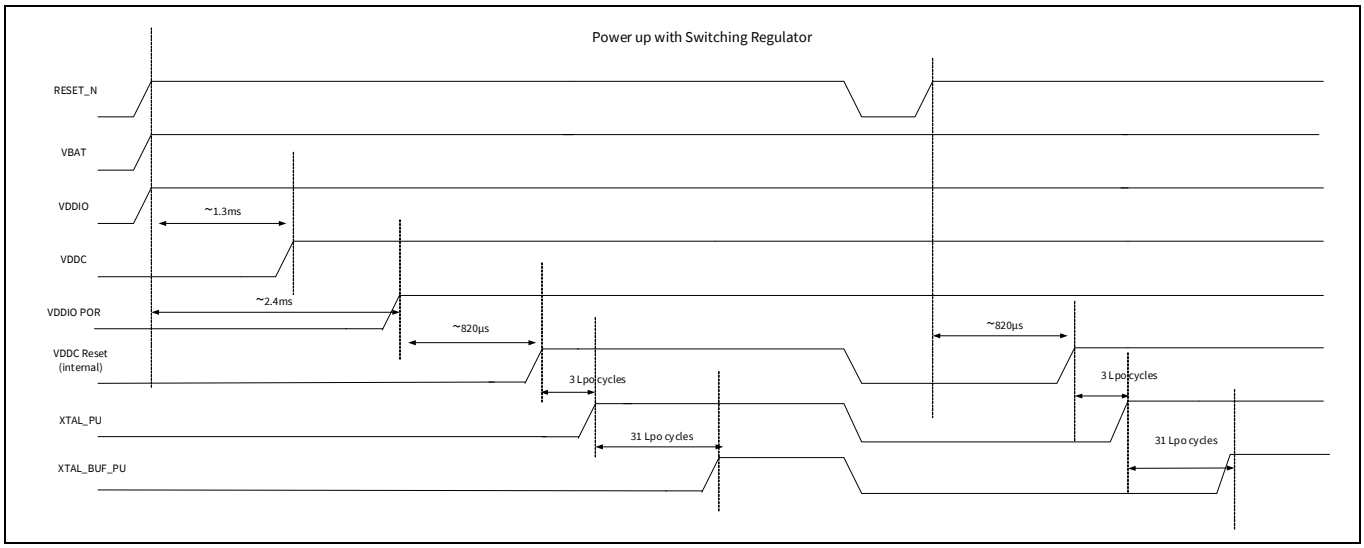


Figure 4 Reset timing

4 Power management unit

Figure 5 shows the CYW89820 power management unit (PMU) block diagram. The CYW89820 includes an integrated buck regulator, a digital LDO for the digital core, and an RF LDO for the Radio. The PMU also includes a brownout detector which places the part in shutdown when input voltage is below a certain threshold.

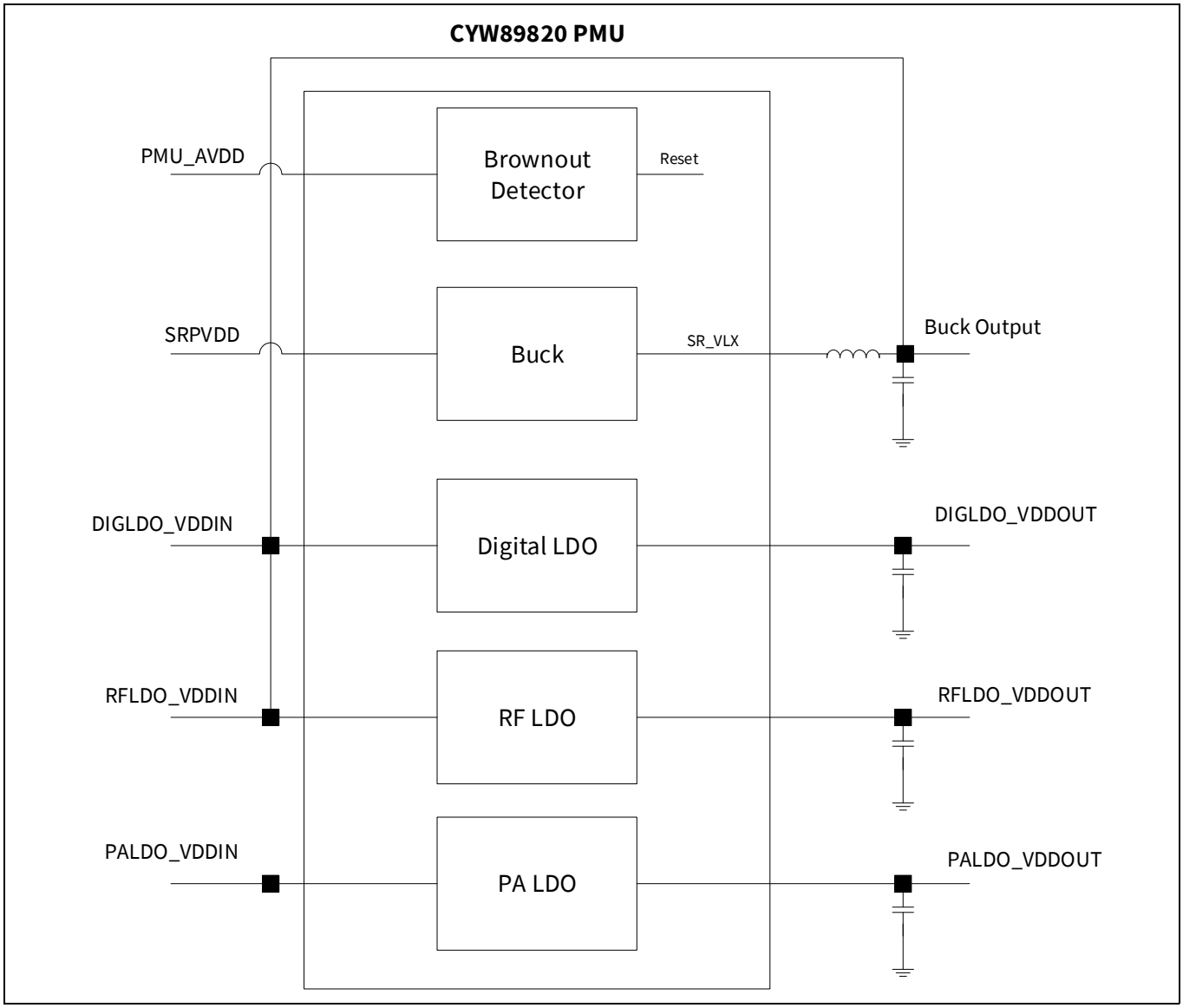


Figure 5 Power management unit

5 Power configurations

CYW89820 supports three power configurations as described in the following table.

Table 4 Power configurations

Configuration	Description
VBAT and VDDIO	VBAT and VDDIO are supplied externally and are used to generate all other supplies on the device. Reset may be left floating as it has an internal pull-up, may be connected to an external RC, or may be driven externally.
External Supplies	PMU is disabled and on-chip regulators are not used. All supplies are provided externally. Reset is driven from the outside.
LDOs and VDDIO	On-chip LDOs are used to generate internal supplies but the on-chip buck is not used. Reset is driven externally.

5.1 Configuration 1 - VBAT and VDDIO

In this configuration the device is provided with two supplies (which can also be tied together). RST_N is either left floating and relies on the internal pull-up to VDDIO to bring the device out of reset or tied to an external RC, or driven externally. All other required supplies are generated on-chip (see the following figure). Note that VDDIO must be supplied at the same time or before VBAT is supplied.

The device may require an external reset when any supply voltages drop below 1 V. POR operation not guaranteed below 1 V.

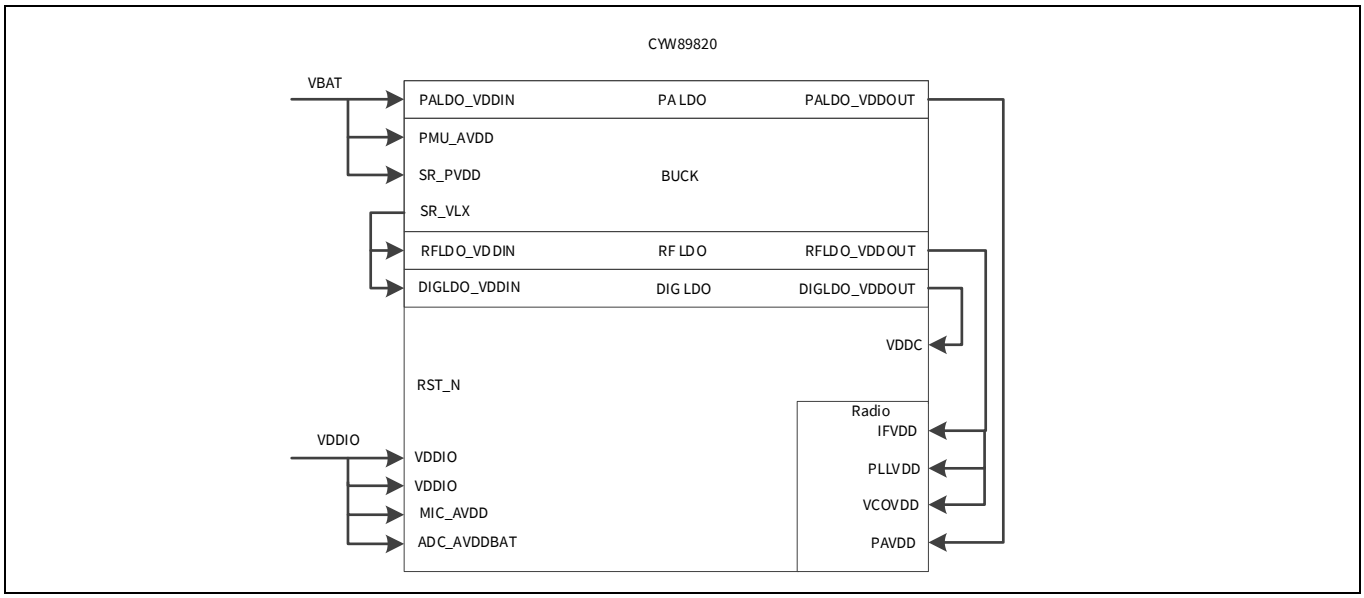


Figure 6 VBAT and VDDIO configuration

5.2 Configuration 2 - External supplies

In this configuration the internal regulators are not used and VBAT is not supplied. VDDIO is supplied along with externally generated core and radio supplies. This is shown in the following figure.

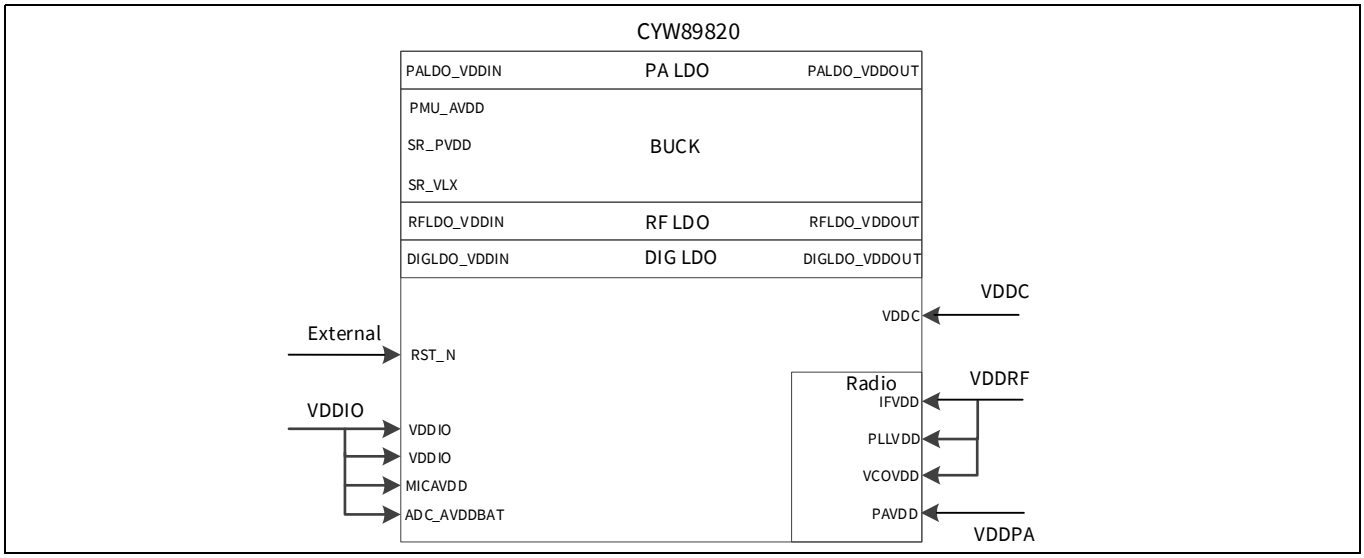


Figure 7 External supplies configuration

Note that VDDIO must be provided simultaneously or before the rest of the supplies and the device must be held in reset until all supplies are within normal operating ranges.

The device may require a reset if any supply goes outside the normal operating range.

5.3 Configuration 3 - LDOs and VDDIO

In this configuration the internal buck regulator is not used. Instead, power is supplied to the internal LDOs which are responsible for supplying the rest of the device.

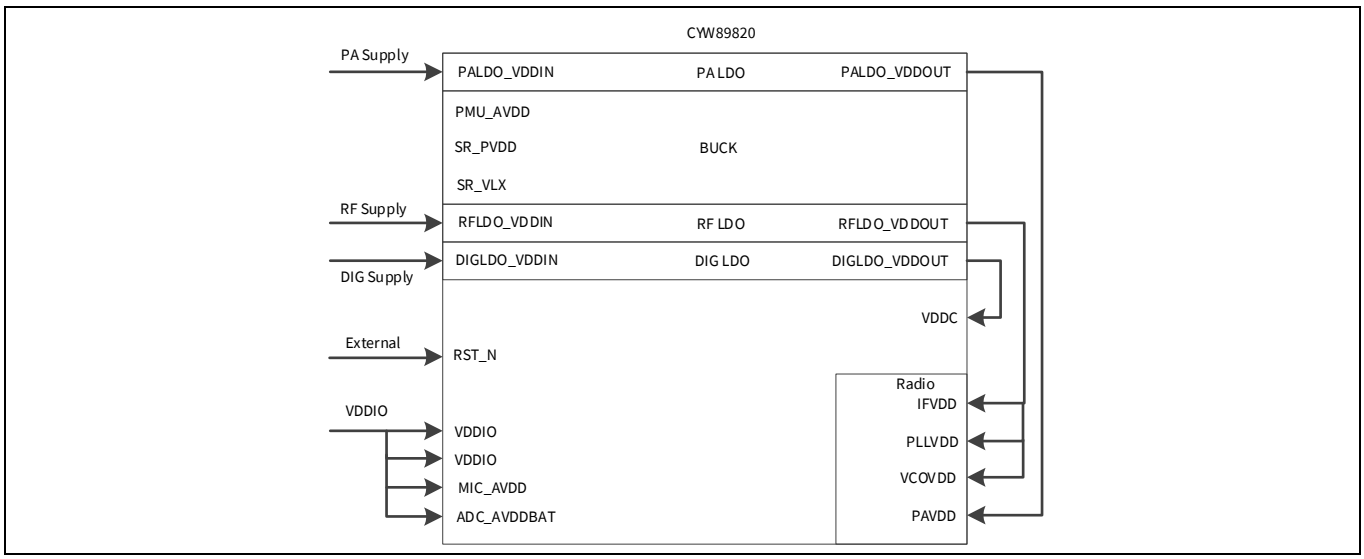


Figure 8 LDOs and VDDIO configuration

Note that VDDIO must be provided simultaneously or before the rest of the supplies and the device must be held in reset until all supplies are within normal operating ranges. The internal LDOs have a small turn-on time (specified later in the datasheet) which should be accounted for before releasing reset.

The device may require a reset if any supply goes outside the normal operating range.

6 Integrated radio transceiver

The CYW89820 has an integrated radio transceiver that has been designed to provide low power operation in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth® Radio Specification 5.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

6.1 Transmitter path

The CYW89820 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

6.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

6.1.2 Power amplifier

The CYW89820 has an integrated power amplifier (PA) that can transmit up to +10.5 dBm for class 1 operation.

6.2 Receiver path

The receiver path uses a low IF scheme to down-convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYW89820 to be used in most applications without off-chip filtering.

6.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

6.2.2 Receiver signal strength indicator

The radio portion of the CYW89820 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

6.3 Local oscillator

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the band. The CYW89820 uses an internal loop filter.

7 Peripherals

7.1 I²C compatible master

The CYW89820 provides a 2-pin I²C compatible master interface to communicate with I²C compatible peripherals. The I²C compatible master supports the following clock speeds:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I²C-compatible speed.)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed.)

The I²C compatible master is capable for doing read, write, write followed by read, and read followed by write operations where read/write can be up to 64 bytes.

SCL and SDA lines can be routed to any of the P1-P37 GPIOs allowing for flexible system configuration. When used as SCL/SDA the GPIOs go into open drain mode and require an external pull-up for proper operation. BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

7.2 Serial peripheral interface

The CYW89820 has two independent SPI interfaces. Both interfaces support single, dual, and Quad Mode SPI operations. Either interface can be a master or a slave. SPI1 has 1040-byte transmit and receive buffers (shared with UART) and SPI2 has 256-byte dedicated transmit and receive buffers. To support more flexibility for user applications, the CYW89820 has optional I/O ports that can be configured individually and separately for each functional pin.

SPI IO voltage depends on VDDO.

7.3 HCI UART interface

The CYW89820 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 3 Mbps. Typical rates are 115200, 921600, 1500000, and 3,000,000 bps although intermediate speeds are also available. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command. The CYW89820 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%. The UART interface CYW89820 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

In HCI Mode, the CYW89820 can wake up the host as needed or allow the host to sleep via the HOST_WAKE signal. The HOST_WAKE signal can be enabled via a vendor specific command.

The FW UART driver allows applications to select different baud rates.

7.4 Peripheral UART interface

The CYW89820 has a second UART that may be used to interface to peripherals. Functionally, the peripheral UART is the same as the HCI UART except for 256 byte TX/RX FIFOs. The peripheral UART is accessed through the I/O ports, which can be configured individually and separately for each functional pin. The CYW89820 can map the peripheral UART to any LHL GPIO.

7.5 GPIO ports

The CYW89820 has 17 general purpose IOs labeled P1-P37. All GPIOs support the following:

- Programmable pull-up/down of approx 45 kΩ
- Input disable, allowing pins to be left floating or analog signals connected without risk of leakage
- Source/sink 8 mA at 3.3 V and 4 mA at 1.8 V
- P26/P27/P28/P29 sink/source 16 mA at 3.3 V and 8 mA at 1.8 V

Most peripheral functions can be assigned to any GPIO. For details, see **Table 6** and **Table 7**.

7.6 ADC

The CYW89820 includes a Σ-Δ ADC designed for audio and DC measurements. The ADC can measure the voltage on 14 GPIO (P1, P9-14, P17-19, P28, P29, P32, P37). When used for analog inputs, the GPIOs must be placed in digital input disable mode to disconnect the digital circuit from the pin and avoid leakage. The internal bandgap reference has ±5% accuracy without calibration. Calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in Direct Current (DC) Mode.

The application can access the ADC through the ADC driver included in the firmware.

7.7 PWM

The CYW89820 has four internal PWMs, labeled PWM0-3.

- Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register is shared among PWM0–3 (read/write). This 18-bit register is used:
  - To enable/disable each PWM channel
  - To select the clock of each PWM channel
  - To invert the output of each PWM channel. The application can access the PWM module through the FW driver.

Figure 9 shows the structure of one PWM channel.

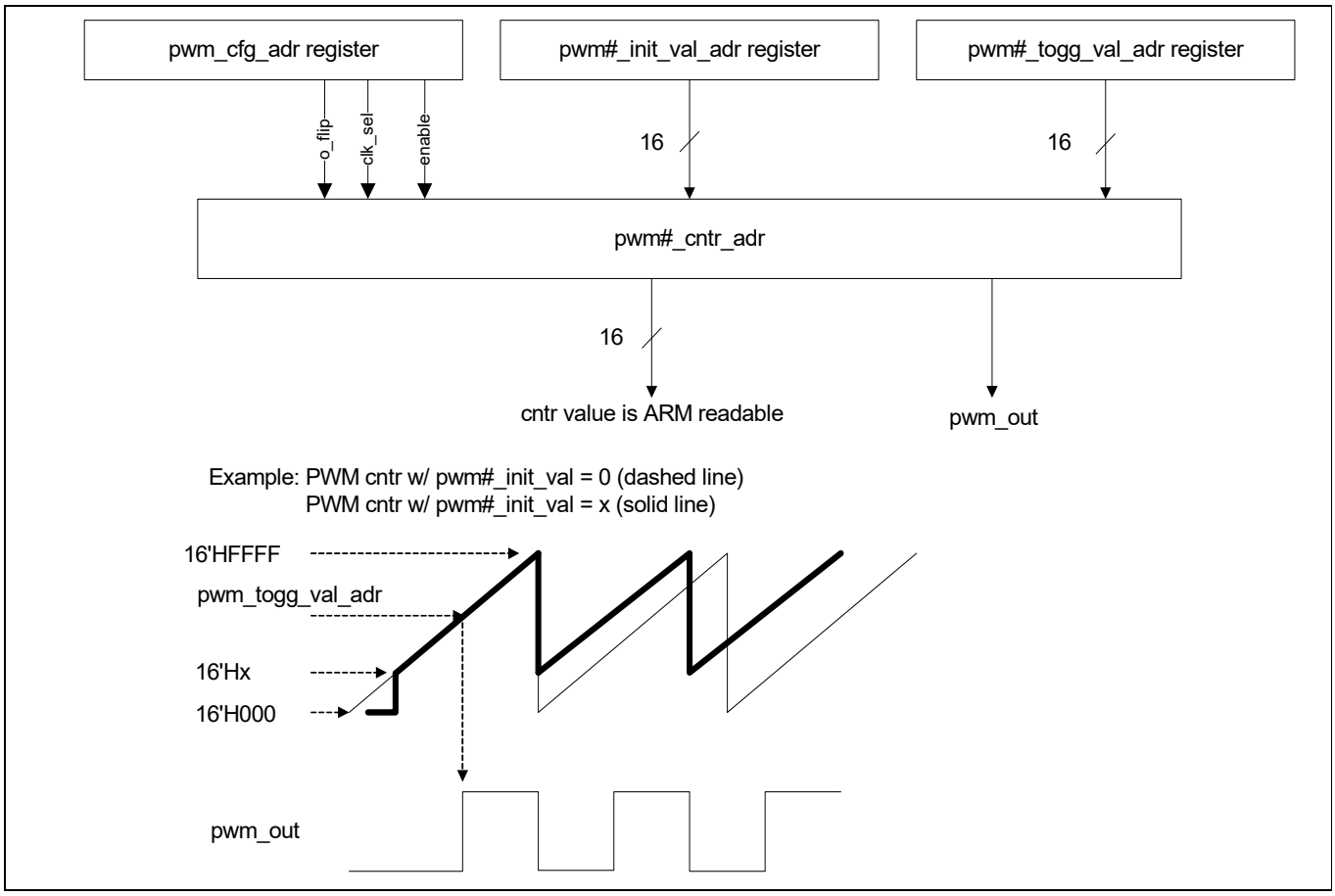


Figure 9 PWM block diagram

7.8 PDM microphone

The CYW89820 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The PDM inputs share the filter path with the aux ADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone takes in a 2.4 MHz clock generated by the CYW89820 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

7.9 I^2S interface

The CYW89820 supports a single I2S digital audio port with both master and slave modes. The I^2S signals are:

- I^2S clock: I^2S SCK
- I^2S word select: I^2S WS
- I^2S data out: I^2S DO
- I^2S data in: I^2S DI

I^2S SCK and I^2S WS become outputs in master mode and inputs in slave mode, while I^2S DO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSN of the left-channel data is aligned with the MSB of the I^2S bus, per I^2S Specifications. The MSB of each data word is transmitted one bit clock cycle after the I^2S WS transition, synchronous with the falling edge of bit clock. Left Channel data is transmitted when I^2S WS is low, and right-channel data is transmitted when I^2S WS is high. Data bits sent by the CYW89820 are synchronized with the falling edge of I^2S SCK and should be sampled by the receiver on the rising edge of the I^2S SCK.

The clock rate in master mode as follows:

- 16 kHz × 16 bits per frame = 256 kHz

The master clock is generated from the reference clock using an N/M clock divider. In the slave mode, any clock rate is supported up to a maximum of 3.072 MHz.

7.10 PCM interface

The CYW89820 includes a PCM interface that can connect to linear PCM codec devices in master or slave mode. In master mode, the CYW89820 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW89820.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Note PCM interface shares HW with the I2S interface and only one can be used at any time. Only audio source (other than SCO) use cases are supported on CYW89820.

7.10.1 Slot mapping

The CYW89820 supports up to three simultaneous full-duplex channels through the PCM Interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.10.2 Frame synchronization

The CYW89820 supports both short- and long-frame synchronization in both master and slave modes. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCGM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.10.3 Data formatting

The CYW89820 may be configured to generate and accept several different data formats. For conventional narrow band speech mode, the CYW89820 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

8 Firmware

The CYW89820 ROM firmware runs on a real time operating system and handles the programming and configuration of all on-chip hardware functions as well as the BT/LE baseband, LMAC, HCI, GATT, ATT, L2CAP, and SDP layers. The ROM also includes drivers for on-chip peripherals as well as handling on-chip power management functions including transitions between different power modes. The ROM also supports OTA firmware update and acts as a root of trust.

The CYW89820 is fully supported by the Infineon ModusToolbox™. ModusToolbox™ releases provide latest ROM patches, drivers, and sample applications allowing customized applications using the CYW89820 to be built quickly and efficiently.

Refer to the **ModusToolbox™ software** documentation for details on the firmware architecture and how to write applications/profiles using the CYW89820.

9 Pin assignments and GPIOs

This section addresses 48-pin WQFN pin assignment and general purpose IOs (GPIOs) for the CYW89820 device.

Table 5. 48-pin WQFN pin assignment

Pin name	Pin number	I/O	Power domain	Description
	WQFN-48			
Baseband supply				
VDDO	31	I	VDDO	I/O pad power supply
VDDO1	6	I	VDDO	I/O pad power supply
VDDO2	39	I	VDDO	I/O pad power supply
ADC_AVDDBAT	36	I	ADC_AVDD	ADC supply
VDDC	8, 30, 41	I/O	VDDC	Baseband core power supply
RF power supply				
IFVDD	24	I	IFVDD	IFPLL power supply
PLLVDD	26	I	PLLVDD	RFPLL and crystal oscillator supply
PAVDD	22	I	PAVDD	PA supply
VCOVDD	25	I	VCOVDD	VCO supply
Onboard LDOs				
PALDO_VDDIN	17	I	–	PA LDO input
PALDO_VDDOUT	18	O	–	PA LDO output
DIGLDO_VDDIN	–	I	–	Internal digital LDO input
DIGLDO_-VDDOUT	21	O	–	Internal digital LDO output
RFLDO_VDDIN	–	I	–	RF LDO input
RFLDO_VDDOUT	19	O	–	RF LDO output
RFLDO_DIGLDO_VDDIN	20	I	–	Internal digital LDO and RF LDO input
SR_PVDD	15	I	–	Core buck input
SR_VLX	14	O	–	Core buck output
PMU_AVDD	16	I	–	PMU supply
Ground pins [1]				
ADC_REFGND	–	I	AVSS	Analog reference ground
VSSC	–	I	VSS	Ground
ADC_AVSS	–	I	AVSS	Analog ground
MIC_AVSS	–	I	AVSS	Microphone analog ground
ADC_AVSSC	–	I	AVSS	Analog ground
PMU_AVSS	–	I	VSS	PMU ground
PLLVSS	–	I	VSS	Ground
PAVSS	–	I	VSS	Ground
VCOVSS	–	I	VSS	Ground
SR_PVSS	–	I	VSS	Ground

Note
1. All grounds in WQFN package connected to ground paddle.

Table 5. 48-pin WQFN pin assignment *(continued)*

Pin name	Pin number	I/O	Power domain	Description
	WQFN-48			
IFVSS	–	I	VSS	Ground
UART				
UART_CTS_N	35	I, PU	VDDO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
UART_RTS_N	34	O, PU	VDDO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
UART_RXD	32	I	VDDO	UART serial input. Serial data input for the HCI UART interface.
UART_TXD	33	O, PU	VDDO	UART serial output. Serial data output for the HCI UART interface.
Crystal				
XTALI	27	I	PLLVDD	Crystal oscillator input. See “The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth® specification. Two external load capacitors are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see **Figure 1**)” for options.
XTALO	28	O	PLLVDD	Crystal oscillator output
XTALI_32K	38	I	VDDO	Low-power oscillator input
XTALO_32K	37	O	VDDO	Low-power oscillator output
CLK_REQ	–	O	N/A	Used for shared-clock application
Other				
RF	23	–	–	RF antenna port
RST_N	12	I	VDDO	Active-low system reset with internal pull-up resistor.
JTAG_SEL	13	–	–	Arm® JTAG debug mode control. Connect to GND for all applications.
GPIOs				
HOST_WAKE	29	O	VDDO	A signal from the CYW89820 device to the host indicating that the Bluetooth® device requires attention.
P1	5	I/O	VDDO	• GPIO: P1 • Keyboard scan input (row): KSI1 • A/D converter input 28 • Peripheral UART: puart_rts • SPI_1: MISO (slave only) • UART1_RXD • Supermux I/O functions as defined in **Table 6** and **Table 7**.

Note
1. All grounds in WQFN package connected to ground paddle.

Table 5. 48-pin WQFN pin assignment *(continued)*

Pin name	Pin number	I/O	Power domain	Description
	WQFN-48			
P2	40	I/O	VDDO	• GPIO: P2 • Keyboard defined in **Table 6** and **Table 7**.
P4	42	I/O	VDDO	• GPIO: P4 • Keyboard scan input (row): KSI4 • Quadrature: QDY0 • SPI_1: MOSI (master only) • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P6	43	I/O	VDDO	• GPIO: P6 • Keyboard scan input (row): KSI6 • Quadrature: QDZ0 • Peripheral UART: puart_rts • PWM2 • Triac control 1 • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P9	46	I/O	VDDO	• GPIO: P9 • Keyboard scan output (column): KSO1 • A/D converter input 26 • External T/R switch control: tx_pd • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P10	47	I/O	VDDO	• GPIO: P10 • Keyboard scan output (column): KSO2 • A/D converter input 25 • External PA ramp control: PA_Ramp • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P11	48	I/O	VDDO	• GPIO: P11 • Keyboard scan output (column): KSO3 • A/D converter input 24 • Supermux I/O functions as defined in **Table 6** and **Table 7**.

Note
1. All grounds in WQFN package connected to ground paddle.

Table 5. 48-pin WQFN pin assignment *(continued)*

Pin name	Pin number WQFN-48	I/O	Power domain	Description
P12	1	I/O	VDDO	• GPIO: P12 • Keyboard scan output (column): KSO4 • A/D converter input 23 • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P13	2	I/O	VDDO	• GPIO: P13 • Keyboard scan output (column): KSO5 • A/D converter input 22 • PWM3 • Triac control 3 • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P14	44	I/O	VDDO	• GPIO: P14 • Keyboard scan output (column): KSO6 • A/D converter input 21 • PWM2 • Triac control 4 • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P17	45	I/O	VDDO	• GPIO: P17 • Keyboard scan output (column): KSO9 • A/D converter input 18 • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P26	9	I/O	VDDO	• GPIO: P26 • Keyboard scan output (column): KSO18 • PWM0 • SPI_1: SPI_CS (slave only) • Optical control output: QOC0 • Triac control 1 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6** and **Table 7**.

Note
1. All grounds in WQFN package connected to ground paddle.

Table 5. 48-pin WQFN pin assignment *(continued)*

Pin name	Pin number	I/O	Power domain	Description
	WQFN-48			
P27	10	I/O	VDDO	• GPIO: P27 • Keyboard scan output (column): KSO19 • PWM1 • SPI_1: MOSI (master only) • Optical control output: QOC1 • Triac control 2 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P28	3	I/O	VDDO	• GPIO: P28 • PWM2 • SCL3 (master and slave) • Optical control output: QOC2 • A/D converter input 11 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P29	4	I/O	VDDO	• GPIO: P29 • PWM3 • SDA3 (master and slave) • Optical control output: QOC3 • A/D converter input 10 • Current: 16 mA sink • Supermux I/O functions as defined in **Table 6** and **Table 7**.

Note
1. All grounds in WQFN package connected to ground paddle.

Table 5. 48-pin WQFN pin assignment *(continued)*

Pin name	Pin number	I/O	Power domain	Description
	WQFN-48			
P32	11	I/O	VDDO	• GPIO: P32 • A/D converter input 7 • Quadrature: QDX0 • Auxiliary clock output: ACLK0 • Peripheral UART: puart_tx • Supermux I/O functions as defined in **Table 6** and **Table 7**.
P37	7	I/O	VDDO	• GPIO: P37 • A/D converter input 2 • Quadrature: QDZ1 • SPI_1: MISO (slave only) • Auxiliary clock output: ACLK1 • BSC: SCL • Supermux I/O functions as defined in **Table 6** and **Table 7**.

Note
1. All grounds in WQFN package connected to ground paddle.

Table 6 GPIO supermux input functions

Input
SWDCK
SWDIO
spiffy1_clk[s]
spiffy1_cs[s]
spiffy1_mosi[s]
spiffy1_miso[m]
spiffy1_io2
spiffy1_io3
spiffy1_int[s]
spiffy2_clk[s]
spiffy2_cs[s]
spiffy2_mosi[s]
spiffy2_miso[m]
spiffy2_io2
spiffy2_io3
spiffy2_int[s]
puart_rx
puart_cts_n
SCL
SDA
SCL2
SDA2
PCM_IN
PCM_CLK
PCM_SYNC
I2S_DI
I2S_WS
I2S_CLK
PDM_IN_Ch_1
PDM_IN_Ch 2

Table 7 GPIO supermux output functions

Output
do_P# (data out of GPIO. For example: P0)
do_PCM_IN
do_PCM_OUT
do_PCM_CLK
do_PCM_SYNC
do_I2S_DO
do_I2S_DI
do_I2S_WS
do_I2S_CLK
do_CLK_REQ
IR_TX
kso0
kso1
kso2
kso3
kso4
kso5
kso6
kso7
kso8
kso9
kso10
kso11
kso12
kso13
kso14
kso15
kso16
kso17
kso18
kso19
do_P# ^ pwm0
do_P# ^ pwm1
do_P# ^ pwm2
do_P# ^ pwm3
do_P# ^ pwm4
do_P# ^ pwm5
aclk0
aclk1

Table 7 GPIO supermux output functions *(continued)*

Output
HID_OFF
pa_ramp
tx_pd
~tx_pd
SWDIO
SDA2
SCL2
puart_tx (uart2_tx)
puart_rts_n (uart2_rts_n)
spiffy1_CLK
spiffy1_CS
spiffy1_MOSI
spiffy1_MISO
spiffy1_IO2
spiffy1_IO3
spiffy2_CLK
spiffy2_CS
spiffy2_MOSI
spiffy2_MISO
spiffy2_IO2
spiffy2_IO3

10 Ball maps

10.1 48-pin WQFN pin map

The CYW89820 48-pin WQFN package is shown in **Figure 11**.

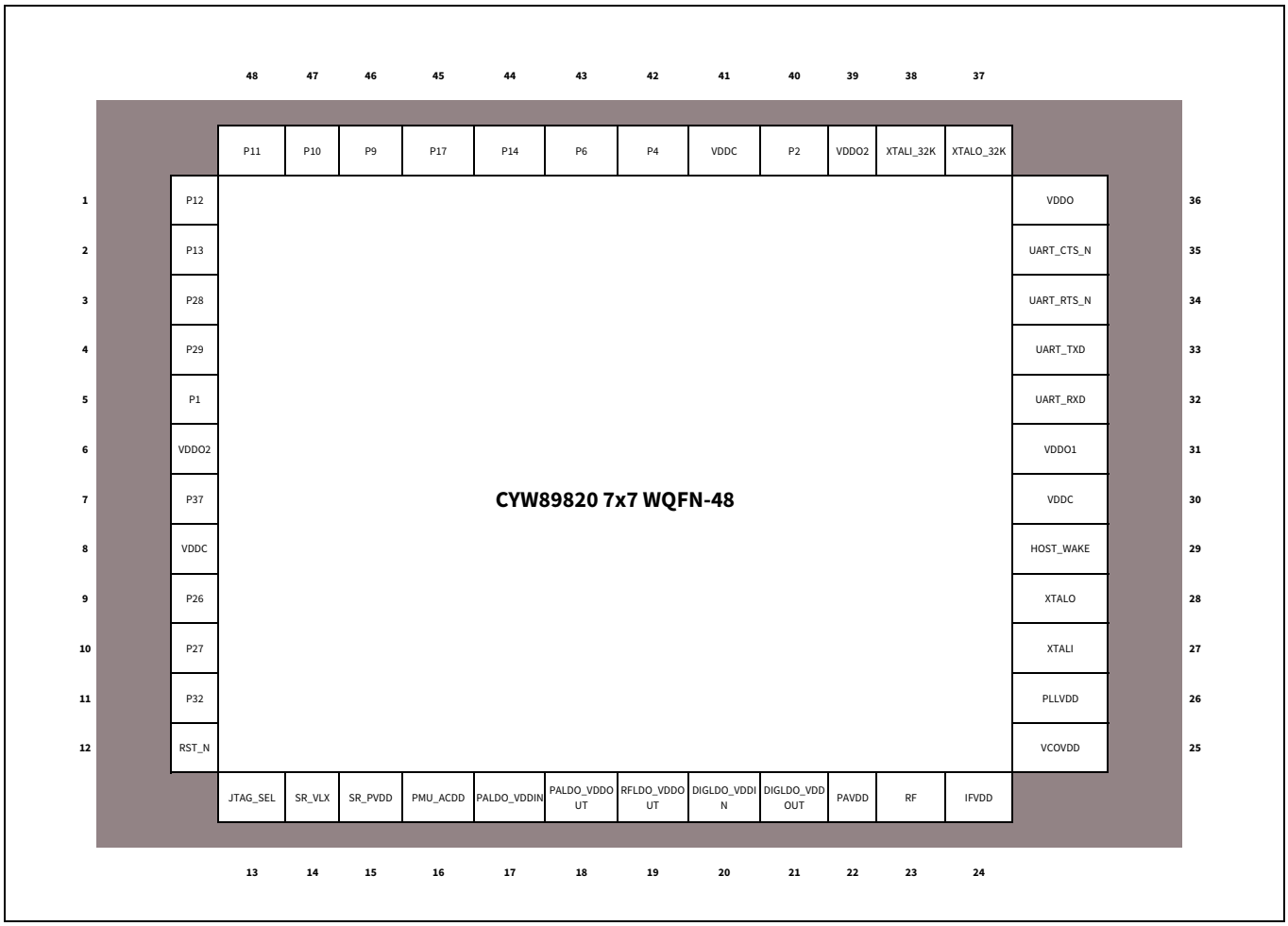


Figure 10 48-pin WQFN pin map

11 Specifications

11.1 Electrical characteristics

The absolute maximum ratings in **Table 8** indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 8 Absolute maximum ratings

Requirement parameter	Specification			Unit
	Min	Nom	Max	
Maximum junction temperature	–	–	125	°C
VDDO1/VDDO2	–0.5	–	3.795	V
IFVDD/PLLVDD/VCOVDD/VDDC	–0.5	–	1.38	
PMUAVDD/SR_PVDD	–0.5	–	3.795	
DIGLDO_VDDIN	–0.5	–	1.65	
RFLDO_VDDIN	–0.5	–	1.65	
PALDO_VDDIN	–0.5	–	3.79	
PAVDD	–0.5	2.5	2.75	

Table 9 ESD/latchup

Requirement parameter	Specification			Unit
	Min	Nom	Max	
ESD Tolerance HBM	–2000	–	2000	V
ESD Tolerance CDM	–500	–	500	
Latch-up	–	200	–	mA

Table 10 Environmental ratings

Characteristic	Value	Unit
Operating Temperature	–40 to +105	°C
Storage Temperature	–40 to +150	

Table 11 Recommended operating conditions

Parameter	Specification			Unit
	Min	Typ	Max	
VDDC	1.045[2]	1.2	1.26	V
IFVDD[4]	1.14	1.2	1.26	
PLLVDD[4]	1.14	1.2	1.26	
VCOVDD[4]	1.14	1.2	1.26	
PAVDD[4]	2.375	2.5	2.625	
VDDO1[3]	1.71	3.0	3.63	
VDDO2[3]	1.71	3.0	3.63	
PMU_AVDD	1.71	3.0	3.63	V
SR_PVDD	1.71	3.0	3.63	
RFLDO_VDDIN	1.26	1.26	1.38	
DIGLDO_VDDIN	1.26	1.26	1.38	
PALDO_VDDIN[4]	2.6	3.0	3.63	V

Notes
2. 1.14 V for >48 MHz operation.
3. VDDO1 must be equal to VDDO2. Recommend that these be provided from the same source.
4. IFVDD, PLLVDD, and VCOVDD must all be equal. Recommend providing from the same supply.PAVDD_VDDIN min. must be greater than V_{out} + 100 mV under max. load current.

11.2 Brown out

The CYW89820 uses an onboard low voltage detector to shut down the part when supply voltage (VDDBAT3V) drops below the operating range.

Table 12 Shutdown voltage

Parameter	Specification			Unit
	Min	Typ	Max	
V_{SHUT}	1.5	1.56	1.7	V

11.2.1 Core buck regulator

Table 13 Core buck regulator

Parameter	Conditions	Min	Typ	Max	Unit
Input supply, VBAT	DC range	1.71	3.0	3.63	V
Output current	Active mode	–	< 60	100	mA
	PDS mode	–	< 60	70	
Output voltage	Active Mode	1.1	1.26	1.4	V
	PDS mode, 40 mV min regulation window.	0.76	0.94 Avg (0.92-0.96)	1.4	
Output voltage accuracy	Active mode, includes line and load regulation. Before trim:	–4	–	+4	%

Note
5. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

Table 13 Core buck regulator *(continued)*

Parameter	Conditions	Min	Typ	Max	Unit
Ripple voltage	Active mode 2.2 µH ± 25% inductor, DCR = 114 mΩ ± 20% 4.7 µF ± 10% capacitor, Total ESR < 20 mΩ	–	3	–	mV
	PDS mode	40	40	–	
Output inductor, L	Refer to the **"Recommended component"** on page 34 section for more details.	1.6[5]	2.2	–	µH
Output capacitor, C_{OUT}		3.0[5]	4.7	–	µF
Input capacitor, C_{IN}		4.0[5]	10	–	
Input supply voltage ramp time	0 to 3.3 V	40	–	–	µs

Note
5. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

11.2.2 Recommended component

Table 14 Recommended component

Parameter	Conditions	Min	Typ	Max	Unit
External inductor, L	2.2 µH ±25%, DCR = 114 mΩ ±20%, ACR < 1Ω (for frequency < 1 MHz)	–	2.2	–	µH
External output capacitor, C_{OUT}	1 µF ±10%, 6.3V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mΩ	0.7	1	1.1	µF
External input capacitor, C_{IN}	For SR_VDDBAT pin Ceramic, X5R, 0402, ESR < 30 mΩ at 4 MHz, +/-20%, 6.3V, 4.7 µF	–	10	–	
External input capacitor	Only use an external input capacitor at VDD_DIGLDO pin if it is not supplied from CBUCK output.	–	1	2.2	

11.2.3 Digital LDO

Table 15 Digital LDO

Parameter	Condition	Min	Typ	Max	Unit
Input supply, DIGLDO_-VDDIN	Min must be met for correct operation	V_{OUT} + 20 mV	1.26	1.4	V
Output voltage, DIGLDO_-VDDOUT	Range	0.9	1.2	1.275	
	Step	–	25	–	mV
	Accuracy after trimming	–2	–	+2	%
Dropout voltage	At max load current	–	–	20	mV
Output current	DC Load	0.075	40	60	mA
Quiescent current	At T ≤ 85°C, V_{IN} = 1.4V	–	–	40	µA
Output load capacitor, C_{OUT}	Total trace + cap ESR must be < 80 mΩ	1.55[6]	2.2	–	µF
Line regulation	1.235 V ≤ V_{IN} ≤ 1.4 V	–	5	10	mV/V
Load regulation	V_{OUT} = 1.2 V, V_{IN} = 1.26 V, 1 mA ≤ I_{OUT} ≤ 25 mA	–	–	0.44	mV/mA

Note
6. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

Table 15 Digital LDO *(continued)*

Parameter	Condition	Min	Typ	Max	Unit
Load step error	I_{OUT} step 1 mA ↔ 20 mA @ 1 µs rise/fall, C_{OUT} = 2.2 µF, V_{IN} = 1.235 V, V_{OUT} = 1.2V	–24	–	+24	mV
Leakage current	Power down Mode, V_{IN} = 1.4 V, Temp = 25°C	–	–	50	nA
	Power down Mode, V_{IN} = 1.4 V, Temp = 125°C	–	–	2	µA
In-rush current	C_{OUT} = 2.2 µF, V_{IN} = 1.4 V, V_{OUT} = 1.2 V	–	–	100	mA
LDO turn on time	C_{OUT} = 2.2 µF, V_{IN} = 1.4 V, V_{OUT} = 1.2 V, I_{OUT} = 20 mA	–	–	120	µs
PSRR	C_{OUT} = 2.2 µF, 1.235 V ≤ V_{IN} ≤ 1.4 V, V_{OUT} = 1.2 V, I_{OUT} = 20 mA f = 1 kHz f = 100 kHz	 25 13	–	–	 dB dB

Note
6. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

11.2.4 Recommended component

Table 16 Recommended component

Parameter	Conditions	Min	Typ	Max	Unit
External input capacitor	Only use an external input capacitor at VDD_DIGLDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

11.2.5 RF LDO

Table 17 RF LDO

Parameter	Conditions	Min	Typ	Max	Unit
Input supply, RFLDO_-VDDIN	Min must be met for correct operation	V_{OUT} + 20 mV	1.26	1.4	V
Output voltage, RFLDO_-VDDOUT	Range	1.1	1.2	1.275	
	Step	–	25	–	mV
	Accuracy after trimming	–2	–	+2	%
Dropout voltage	At max load current	–	–	20	mV
Output current	DC Load	0.075	20	60	mA
Quiescent current	At T ≤ 85°C, V_{IN} = 1.4V	–	–	40	µA
Output load capacitor, C_{OUT}	Total trace + cap ESR must be < 80 mΩ	1.55[7]	2.2	–	µF
Line regulation	1.235 V ≤ V_{IN} ≤ 1.4 V	–	5	10	mV/V
Load regulation	V_{OUT} = 1.2 V, V_{IN} = 1.26 V, 1 mA ≤ I_{OUT} ≤ 25 mA	–	–	0.44	mV/mA
Load step error	I_{OUT} step 1 mA ↔ 20 mA @ 1 µs rise/fall, C_{OUT} = 2.2 µF, V_{IN} = 1.235 V, V_{OUT} = 1.2 V	–24	–	+24	mV
Leakage current	Power down mode, V_{IN} = 1.4 V, Temp = 25°C	–	–	50	nA
	Power down mode, V_{IN} = 1.4 V, Temp = 125°C	–	–	2	µA

Note
7. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

Table 17 RF LDO *(continued)*

Parameter	Conditions	Min	Typ	Max	Unit
In-rush current	C_{OUT} = 2.2 µF, V_{IN} = 1.4 V, V_{OUT} = 1.2 V	–	–	100	mA
LDO turn on time	C_{OUT} = 2.2 µF, V_{IN} = 1.4V, V_{OUT} = 1.2 V, I_{OUT} = 20 mA	–	–	120	µs
PSRR	C_{OUT} = 2.2 µF, 1.235 V ≤ V_{IN} ≤ 1.4 V, V_{OUT} = 1.2 V, I_{OUT} = 20 mA f = 1 kHz f = 100 kHz	25 13	–	–	 dB dB
Noise	C_{OUT} = 2.2 µF, V_{IN} = 1.235 V, V_{OUT} = 1.2 V, I_{OUT} = 20 mA f = 30 kHz f = 100 kHz	–	–	 80 70	 nV√Hz nV√Hz

Note
7. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effects.

11.2.6 PALDO

Table 18 PALDO

Parameter	Conditions	Min	Typ	Max	Unit
Input supply, PALDO_-VDDIN	VDDIN min must be greater than V_{OUT}+100 mV under max load current for proper regulation	2.6	3.0	3.63	V
Output voltage, PALDO_VDDOUT	Range	1.5	2.45	3.0	V
	Step		100		mV
	Accuracy	-4	–	+4	%
HTOL output voltage		–	3.3	–	V
Dropout voltage	At max load current	–	–	100	mV
Output current	DC Load	0	30	60	mA
Quiescent current	At T ≤ 85°C, V_{IN} = 3.3 V	–	–	110	µA
Output load capacitor, C_{OUT}		1.2[8]	2.2	–	µF
Line regulation	2.7 V ≤ V_{IN} ≤ 3.3 V, V_{OUT} = 2.5 V	–	–	25	mV/V
Load regulation	V_{IN} = 3.3 V, V_{OUT} = 2.5 V, 0 mA ≤ I_{OUT} ≤ 30 mA	–	–	1	mV/mA
Load step error	I_{OUT} step 1 mA↔20 mA @ 1 µs rise/fall, C_{OUT} = 2.2 µF, V_{IN} = 3.3 V, V_{OUT} = 2.5 V	-25	–	25	mV
Leakage current	Power-down mode, V_{IN} = 3.6 V, Temp = 25°C	–	–	1.6	µA
	Power-down mode, V_{IN} = 3.6 V, Temp = 125°C	–	–	4.9	µA
In-rush current	C_{OUT} = 2.2 µF, V_{IN} = 3.3 V, V_{OUT} = 2.5 V	–	–	140	mA
LDO turn on time	C_{OUT}=2.2 µF, V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{OUT} = 20 mA	–	–	140	µs
PSRR	C_{OUT}=2.2 µF, V_{IN} = 3.3 V, V_{OUT} = 2.5 V, I_{OUT} = 20 mA f = 1kHz	45	–	–	dB
	f = 100kHz	25	–	–	dB

Note
8. Minimum values represent minimums after derating due to tolerance, temperature, and voltage effect.

11.2.7 Recommended component

Table 19 Recommended component

Parameter	Conditions	Min	Typ	Max	Unit
External output capacitor, Co	Total ESR (trace/cap): 5 m–240 mΩ	0.5	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at VDD_DIGLDO pin if it is not supplied from CBUCK output.	–	1	2.2	

11.2.8 Digital I/O characteristics

Table 20. Digital I/O characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage (VDDO = 3 V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3 V)	V_{IH}	2.4	–	–	
Input low voltage (VDDO = 1.8 V)	V_{IL}	–	–	0.4	
Input high voltage (VDDO = 1.8 V)	V_{IH}	1.4	–	–	
Output low voltage	V_{OL}	–	–	0.4	
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	
Output low current (VDDO = 3 V, V_{OL} = 0.4 V)	I_{OL}	–	–	4.0	mA
Output low current (VDDO = 3 V, V_{OL} = 1.8 V)	I_{OL}	–	–	2.0	
Output high current (VDDO = 3 V, V_{OH} = 2.6 V)	I_{OH}	–	–	8.0	
Output high current (VDDO = 1.8 V, V_{OH} = 1.4 V)	I_{OH}	–	–	4.0	
Input capacitance	C_{IN}	–	–	0.4	pF

11.2.9 Current consumption

Table 21 provides the current consumption measurements taken at input of LDOIN and VDDIO combined (LDOIN = VDDIO = 3.0 V).

Table 21 Current consumption

Operational mode	Conditions	Typ	Unit
HCI	48 MHz with Pause	1.3	mA
	48 MHz without Pause	2.55	
RX	Continuous RX	5.9	
TX	Continuous TX - 10.5 dBm	22.0	
PDS	–	16.5	µA
ePDS	All RAM retained	8.7	
HID-Off (SDS)	32 kHz XTAL on	1.75	

11.3 RF specifications

Note Table 22 and Table 23 apply to single-ended industrial temperatures. Unused inputs are left open.

Table 22 BR/EDR - Receiver RF specifications

Parameter	Mode and conditions	Min	Typ	Max	Unit
Receiver section					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, BDR GFSK 0.1% BER, 1 Mbps	–	–91[9]	–	dBm
	EDR 2M	–	–94	–	dB
	EDR 3M	–	–87.5	–	
Maximum input	–	–20	–	–	dBm
Interference performance					
C/I cochannel	GFSK, BDR GFSK 0.1% BER[10]	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER[10]	–	–	–4.0	
C/I 2 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER[10]	–	–	–31.5	
C/I ≥ 3 MHz adjacent channel	GFSK, BDR GFSK 0.1% BER[10]	–	–	–42.5	
C/I image channel	GFSK, BDR GFSK 0.1% BER[10]	–	–	–24.0	
C/I 1 MHz adjacent to image channel	GFSK, BDR GFSK 0.1% BER[10]	–	–	–35.0	
Out-of-band blocking performance (CW)[11]					
30 MHz to 2000 MHz	BDR GFSK 0.1% BER	–	–10.0	–	dBm
2000 MHz to 2399 MHz	BDR GFSK 0.1% BER	–	–27	–	
2498 MHz to 3000 MHz	BDR GFSK 0.1% BER	–	–27	–	
3000 MHz to 12.75 GHz	BDR GFSK 0.1% BER	–	–10.0	–	
Intermodulation performance[10]					
BT, interferer signal level	BDR GFSK 0.1% BER	–	–	–39.0	dBm
Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–57.0	dBm
1 GHz to 12.75 GHz	–	–	–	–47.0	

Notes

9. The receiver sensitivity is measured at BER of 0.1% on the device interface with dirty TX Off.
10. Desired signal is 10 dB above the reference sensitivity level (defined as –70 dBm).
11. Desired signal is 3 dB above the reference sensitivity level (defined as –70 dBm).
12. Desired signal is –64 dBm Bluetooth®-modulated signal, interferer 1 is –39 dBm sine wave at frequency f1, interferer 2 is –39 dBm Bluetooth®-modulated signal at frequency f2, f0 = 2 * f1 – f2, and |f2 – f1| = n * 1 MHz, where n = 3, 4, or 5. For the typical case, n = 4.

Table 23 BR/EDR - Transmitter RF specifications

Parameter	Min	Typ	Max	Unit
Transmitter section				
Frequency range	2402	–	2480	MHz
BR TX power	–	11.5	–	dBm
BR TX power variation	–	±2	–	dB
EDR 2M TX power	–	2.5	–	dBm
EDR 3M TX power	–	1.5	–	dBm
EDR 2M power variation	–	±2	–	dB
EDR 3M power variation	–	±3	–	dB
Adjacent channel power				
$\|M - N\| = 2$	–	–	–20	dBm
$\|M - N\| \geq 3$	–	–	–40	
Out-of-band spurious emission				
30 MHz to 1 GHz	–	–	–36.0	dBm
1 GHz to 12.75 GHz	–	–	–30.0	
1.8 GHz to 1.9 GHz	–	–	–47.0	
5.15 GHz to 5.3 GHz	–	–	–47.0	
LO performance				
Initial carrier frequency tolerance	–75	–	+75	kHz
Frequency drift				
DH1 packet	–25	–	+25	kHz
DH3 packet	–40	–	+40	
DH5 packet	–40	–	+40	
Drift rate	–20	–	20	kHz/50 µs
Frequency deviation				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	
Channel spacing	–	1	–	MHz

Table 24 Bluetooth® LE RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sensitivity[13]	GFSK, BDR GFSK 0.1% BER 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power	N/A	–	11.5	–	
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[14]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	–	–	%

Notes
13.Dirty TX is Off.
14.At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Table 25 Bluetooth® LE2 RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
RX sensitivity[15]	–	–	–91.5	–	dBm
TX power	–	–	11.5	–	

Note
15.255 packet.

11.4 Timing and AC characteristics

In this section, use the numbers listed in the Reference column of each table to interpret the timing diagrams shown in **Figure 11** through **Figure 16**.

11.4.1 UART timing

Table 26 UART timing specifications

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	

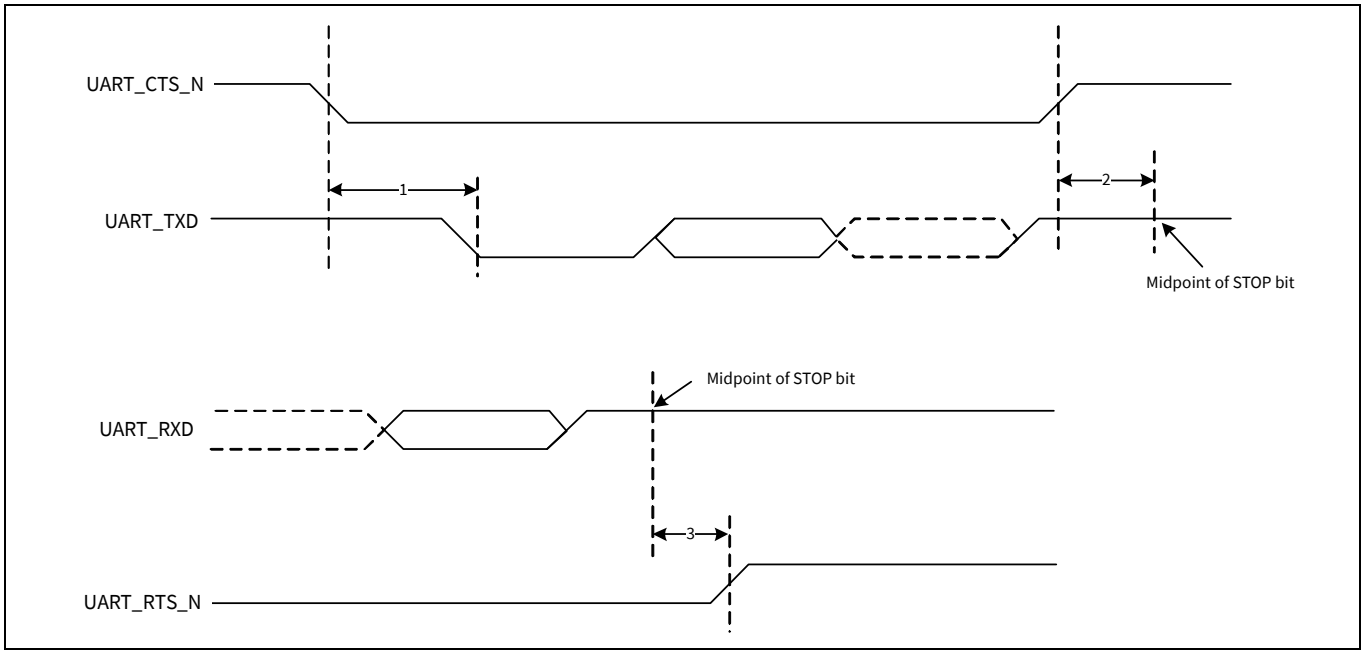


Figure 11 UART timing

11.4.2 SPI timing

The SPI interface can be clocked up to 12 MHz.

Table 27 and **Figure 12** show the timing requirements when operating in SPI mode 0 and 2.

Table 27 SPI mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Setup time for MOSI data lines	6	½ SCK	
3	Idle time between subsequent SPI transactions	1 SCK	–	

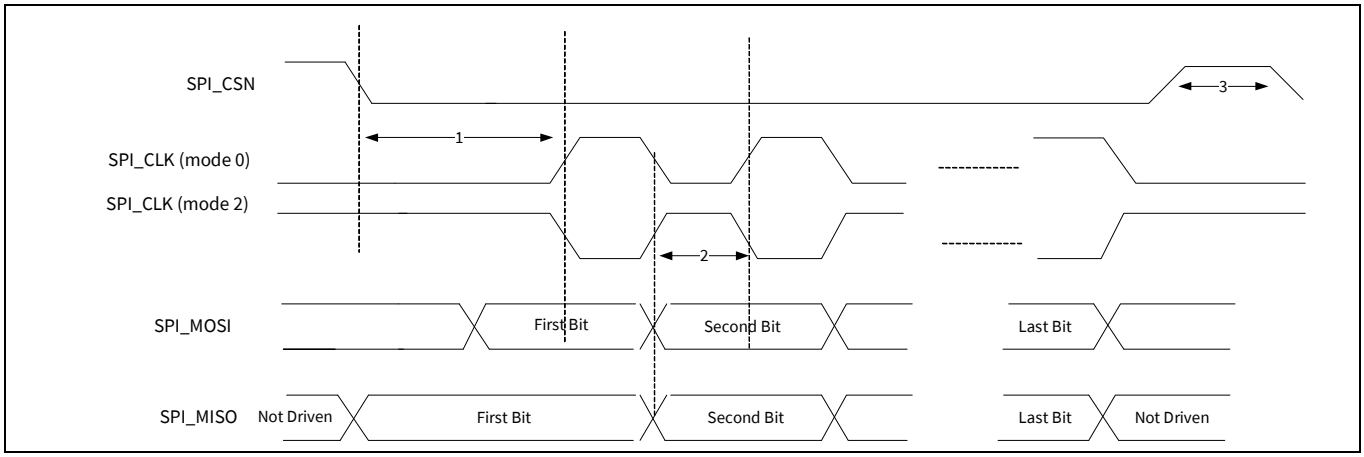


Figure 12 SPI timing, mode 0 and 2

Table 28 and **Figure 13** show the timing requirements when operating in SPI mode 1 and 3.

Table 28 SPI Mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Setup time for MOSI data lines	6	½ SCK	
3	Idle time between subsequent SPI transactions	1 SCK	–	

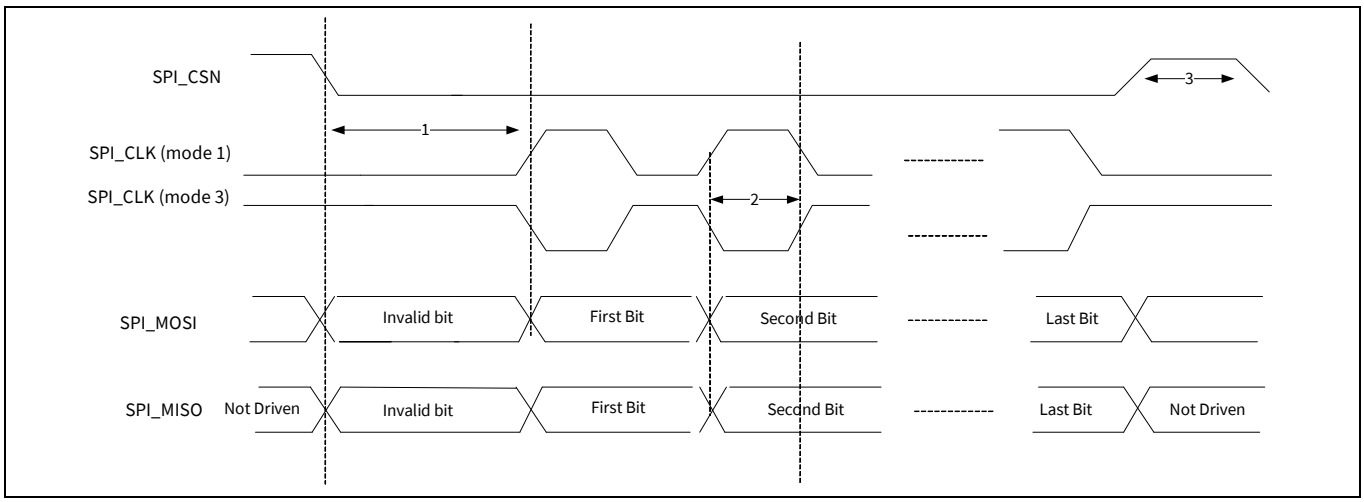


Figure 13 SPI timing, mode 1 and 3

11.4.3 BSC interface timing

The specifications in **Table 29** references **Figure 14**.

Table 29 BSC interface timing specifications (up to 1 MHz)

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[16]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[17]	650	–	

Note

16. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
17. Time that the CBUS must be free before a new transaction can start.

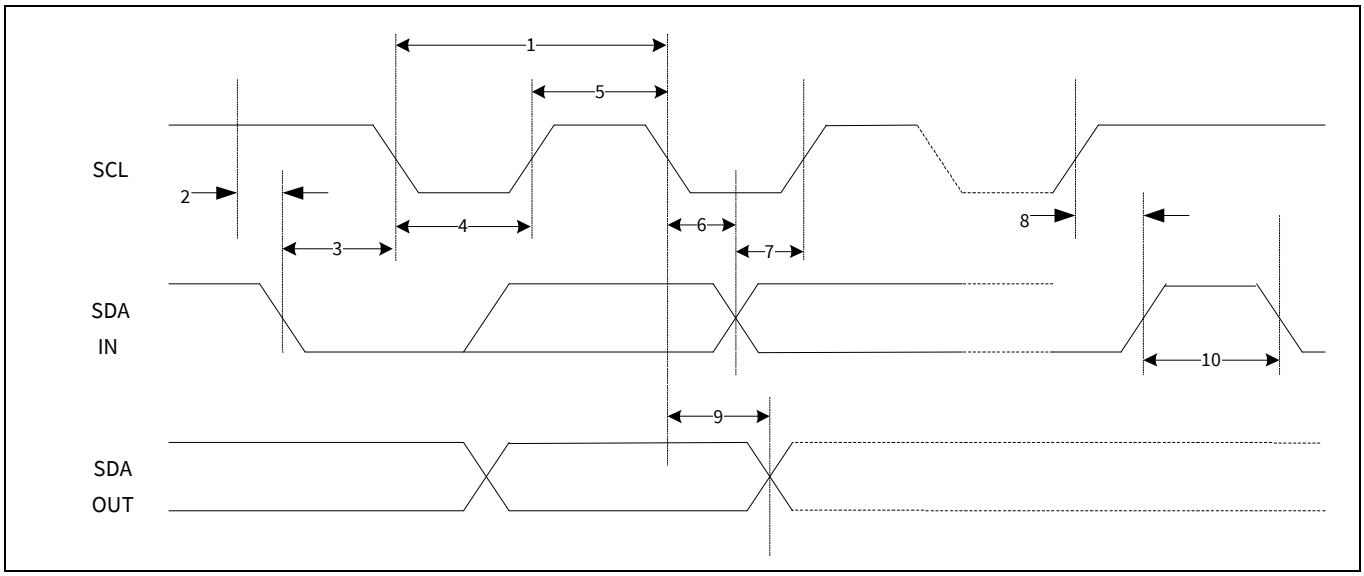


Figure 14 BSC interface timing diagram

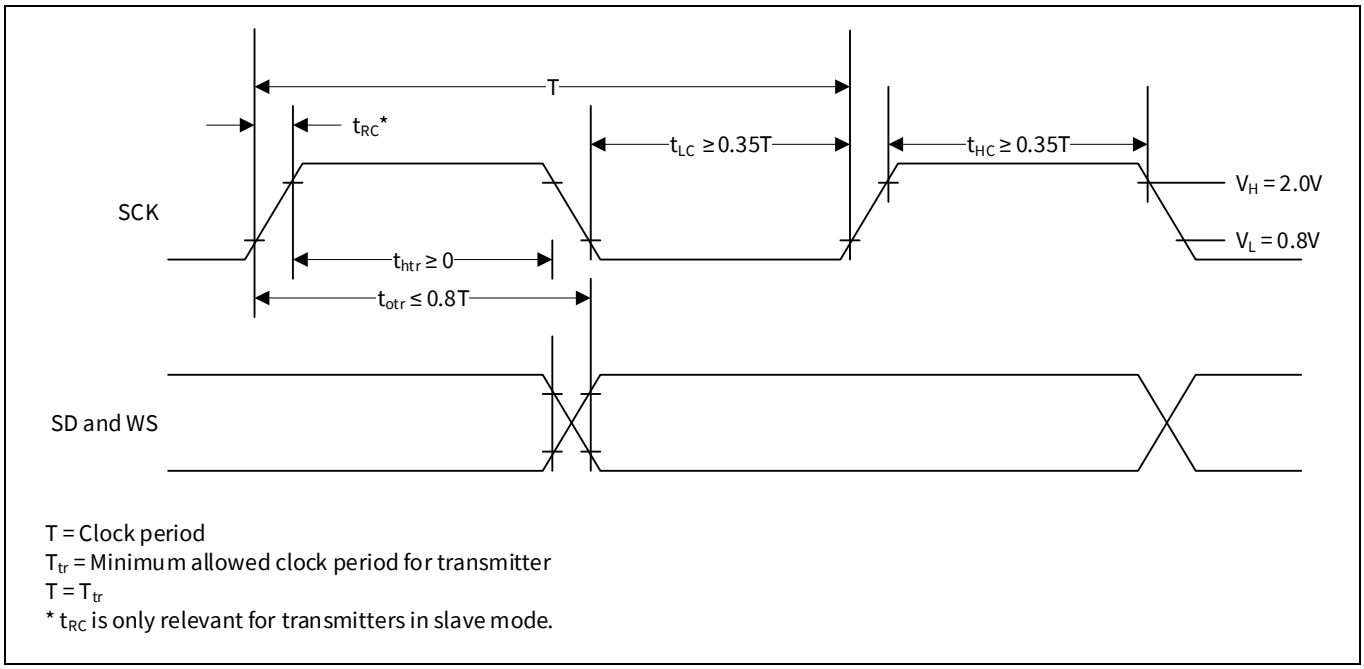
11.4.4 I2S

Table 30. Timing for I^2S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period T	T_{tr}	–	–	–	T_r	–	–	–	[18]
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[19]
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	[19]
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[18]
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	[18]
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	[19]
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	[20]
Hold time t_{htr}	0	–	–	–	–	–	–	–	[19]
Receiver									
Setup time t_{sr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[21]
Hold time t_{hr}	–	–	–	–	$0.2T_{tr}$	–	–	–	[21]

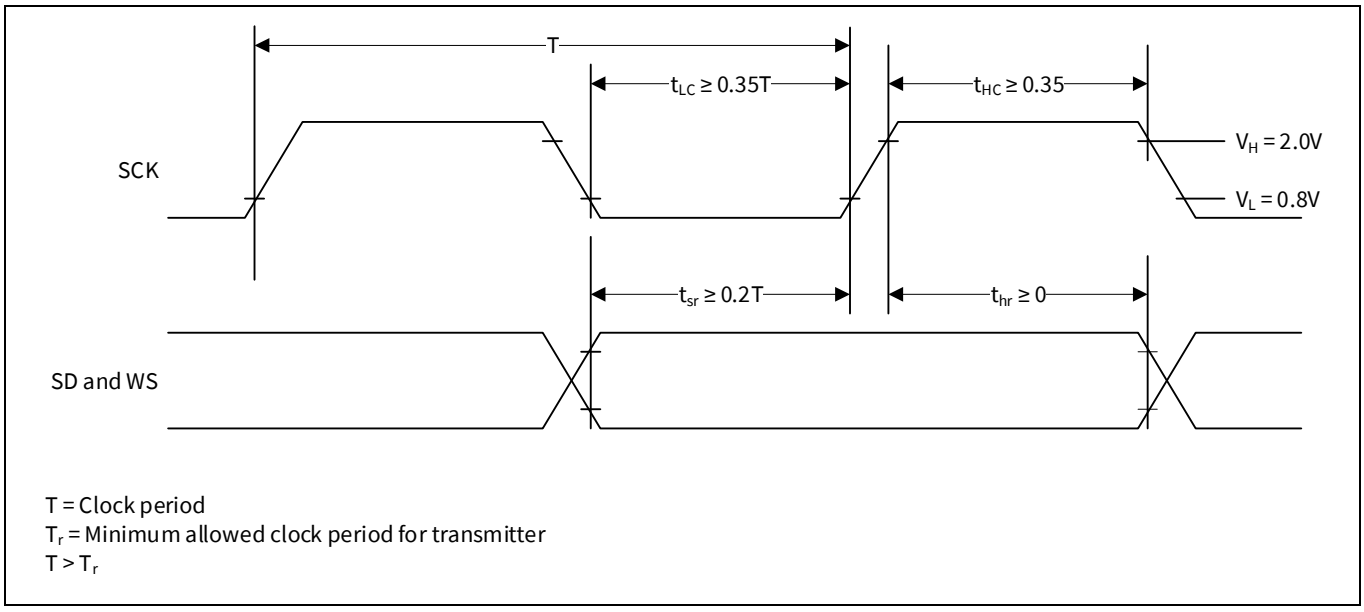
Notes

18. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
19. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
20. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
21. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time tRC is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
22. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
23. The data setup and hold time must not be less than the specified receiver setup and hold time.



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 15 I^2S transmitter timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

Figure 16 I^2S receiver timing

12 Package information

12.1 Package thermal characteristics

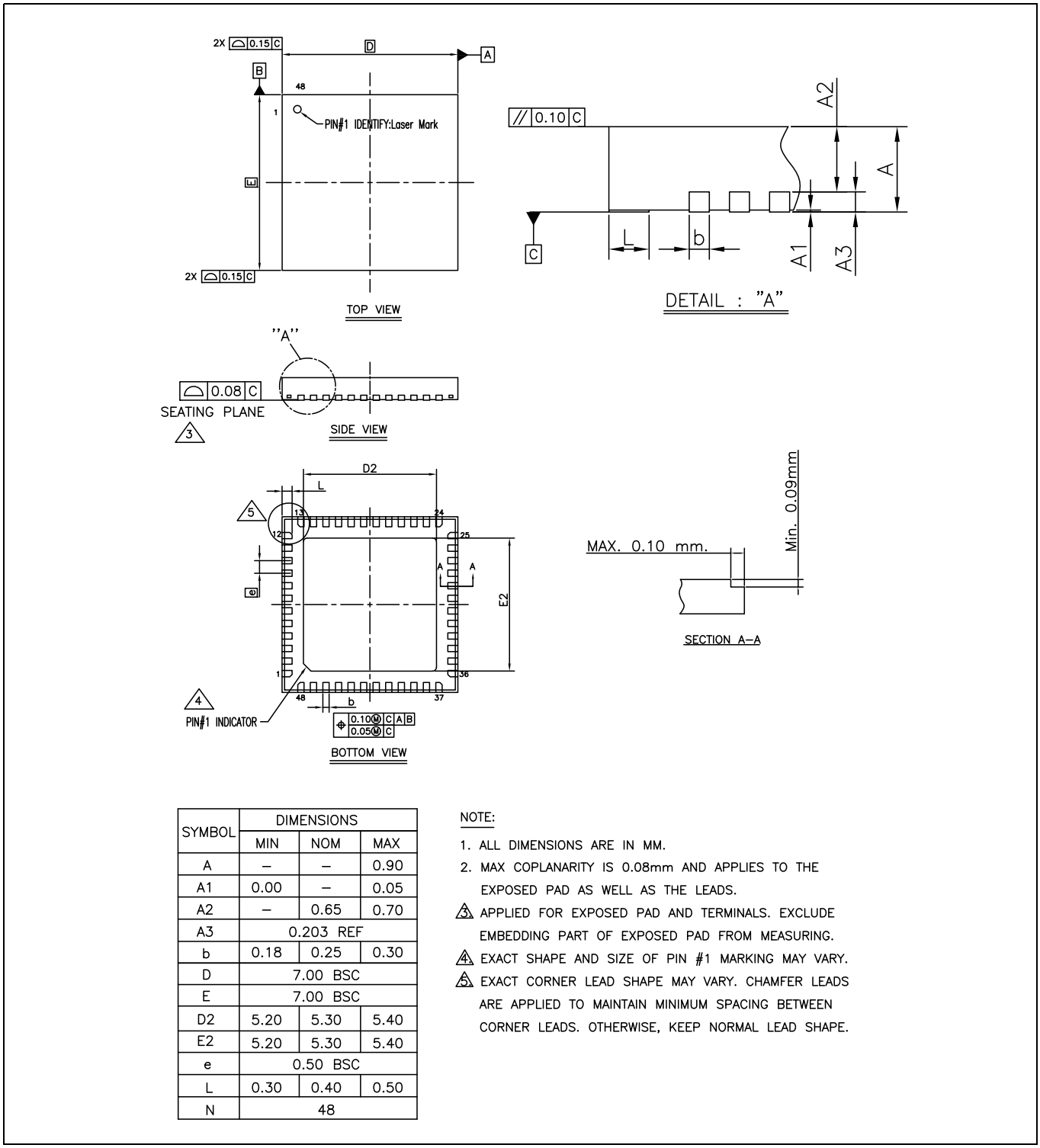
Table 31 Package thermal characteristics

Description	Value	Unit
Ambient air temperature	25	°C
Total power (W)	0.15	W
Board temperature (°C)	N/A	°C
Package-top temperature (°C)	N/A	°C
Maximum junction temperature (°C)	28.2	°C
Ψ_{JB}	3.87	°C/W
Ψ_{JT}	0.1	°C/W
θ_{JA}	21.2	°C/W
θ_{JB}	5.25	°C/W
θ_{JC}	13.1	°C/W
$\theta_{JCbottom}$	2.6	°C/W
Ambient air temperature	105	°C
Total power (W)	0.15	W
Board temperature (°C)	N/A	°C
Package-top temperature (°C)	N/A	°C
Maximum junction temperature (°C)	107.6	°C
Ψ_{JB}	2.63	°C/W
Ψ_{JT}	0.1	°C/W
θ_{JA}	17.5	°C/W
θ_{JB}	5.25	°C/W
θ_{JC}	13.1	°C/W
$\theta_{JCbottom}$	2.6	°C/W

Note: Absolute junction temperature limits are maintained through active thermal monitoring.

13 Packaging diagrams

13.1 48-Pin WQFN package



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	–	–	0.90
A1	0.00	–	0.05
A2	–	0.65	0.70
A3	0.203 REF		
b	0.18	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
D2	5.20	5.30	5.40
E2	5.20	5.30	5.40
e	0.50 BSC		
L	0.30	0.40	0.50
N	48		

NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. MAX COPLANARITY IS 0.08mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.
5. EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

Figure 17 CYW89820 7 mm × 7 mm 48-pin WQFN package

13.2 Tape reel and packaging specifications

Table 32 CYW89820 48-pin WQFN tape reel specifications

Parameter	Value
Quantity per reel	2500 parts
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Pocket pitch	12 mm
Sprocket hole pitch	4 mm

The top-left corner of the CYW89820 package is situated near the sprocket holes, as shown in **Figure 18**.

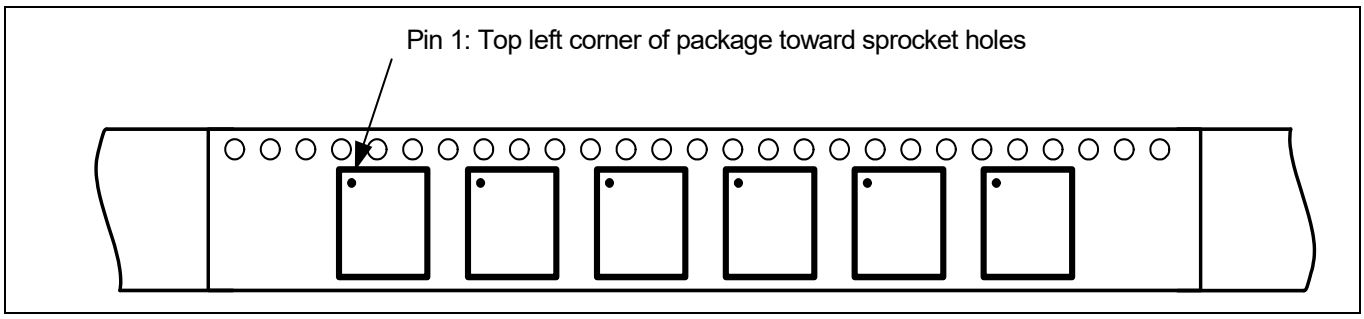


Figure 18 Pin 1 orientation

14 Ordering information

Table 33 Ordering information

Part number	Package	Ambient operating temperature
CYW89820BWMLG	7 mm × 7 mm 48-pin WQFN	–40°C to 105°C
CYW89820BWMLGT	7 mm × 7 mm 48-pin WQFN, tape and reel	–40°C to 105°C

15 Acronyms

Table 34 Acronyms used in this document

Term	Description
ACL	asynchronous connection-less
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
ARM7TDMI-S	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BBC	Bluetooth® Baseband Core
BDR	basic data rate
BLE	Bluetooth® low energy
BR	basic data rate
CMOS	complementary metal oxide semiconductor
CRC	cyclic redundancy check
ECDSA	elliptic curve digital signature algorithm
ED	erroneous data
EDR	enhanced data rate
EIR	extended inquiry response
ePDS	extended power down sleep
eSCO	extended synchronous connection-oriented
EPR	encryption pause resume
FEC	forward error correction
FPU	floating point unit
GAP	generic access profile
GATT	generic attribute profile
GCI	global coexistence interface
GFSK	Gaussian Frequency Shift Keying
GPIO	general-purpose I/O
HCI	host control interface
HEC	header error control
HID	human-interface device
I2C	inter-integrated circuit
I2S	inter-IC sound bus
IF	intermediate frequency
JTAG	Joint Test Action Group
L2CAP	logical link control and adaptation protocol
LC	link control
LCU	link control unit
LDO	low drop out
LE	low energy
LED	light emitting diode

Table 34 Acronyms used in this document *(continued)*

Term	Description
LHL	lean high land
LMAC	Lower MAC
LO	local oscillator
LPO	low power oscillator
LSTO	link supervision time out
MOSI	master out slave in
OBD	on-board diagnostics
OEM	original equipment manufacturer
OCF	on chip flash
OTA	over-the-air
OTP	one-time programmable
PA	power amplifier
PBF	packet boundary flag
PCM	pulse code modulation
PDM	pulse density modulation
PDS	power down sleep
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PWM	pulse width modulation
WQFN	wettable plan quad flat no-lead
QoS	quality of service
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory
RSSI	receiver signal strength indicator
RTC	real time clock
RX/TX	receive/transmit
SCO	synchronous connection-oriented
SDS	Shut Down Sleep
SECI	serial enhanced coexistence interface
SPI	serial peripheral interface
SSP	secure simple pairing
SSR	sniff subrating
SWD	serial wire debug
TRNG	True Random Number Generator
TSSI	transmit signal strength indicator

Table 34 Acronyms used in this document *(continued)*

Term	Description
UART	universal asynchronous receiver/transmitter
WDT	watchdog timer

Revision history

Document revision	Date	Description of changes
**	2018-12-06	New datasheet
*A	2019-25-03	Fixed typo in Page 3
*B	2020-07-15	Added QDID and Declaration ID and updated Programmable TX Power to 11.5 dB in **Features** Added PA LDO in **Functional block diagram** Added **Low-frequency clock sources** and updated **Power modes** section. Added PA LDO in **Power management unit** and **Power configurations** section figures Added **Power configurations** section Added VDDO and ADC_AVDDBAT and updated PALDO_VDDOUT pins in **Table 5**. Added PAVDD parameter value in **Table 8** Updated PAVDD and PALDO_VDDIN values in **Table 11** Updated V_{SHUT} values in **Table 12** Added new section **PALDO** and **Table 18** Updated HCI, RX and ePDS typical values in **Table 21** Updated **Table 22**, **Table 23**, **Table 24**, and **Table 25** in **RF specifications**
*C	2021-04-23	Updated **Table 23**
*D	2021-06-11	Updated **Table 21** to include BR, EDR, and Bluetooth® LE Changed from BLE to Bluetooth® LE and BT to Bluetooth® throughout the document
*E	2021-06-16	Updated to remove Preliminary
*F	2022-01-25	Updated PALDO_VDDIN value in **Table 11** Updated Input Supply, PALDO_VDDIN max value in **Table 18**
*G	2022-09-24	Migrated to Infineon template Updated EDR 2M and 3M TX power parameter values in **Table 23**
*H	2023-04-19	Updated **Table 2**

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