

ADVANCE INFORMATION

CYWB0224ABS/CYWB0224ABM West BridgeTM AstoriaTM

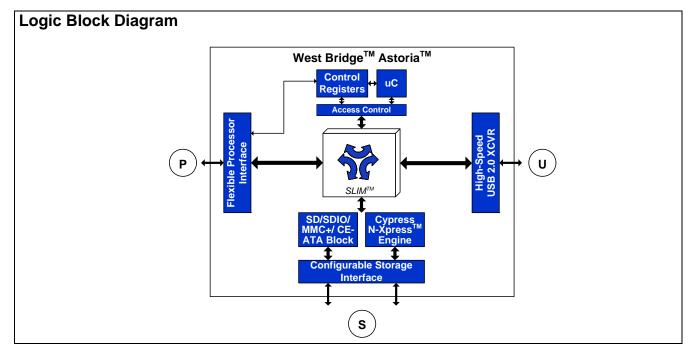
Features

- N-Xpress[™] NAND Controller Technology
 - □ Interleave up to 16 NANDs with 8 Chip Enables (CE#) for x8 or x16 SLC (CYWB0224ABS) or MLC (CYWB0224ABM) NAND flash devices.
 - □ 4-bit Error Correction Coding
 - □ Bad Block Management
 - Static Wear Leveling
- Multimedia Device Support
 - □ Up to 2 SD/SDIO/MMC/MMC+/CE-ATA devices
- SLIM™ Architecture, allowing simultaneous and independent data paths between the processor and USB, and between the USB and Mass Storage.
- Fully backward compatible (including pin to pin) to Antioch (CYWB0124AB)
- High speed USB at 480 Mbps
 - □ USB 2.0 compliant
 - □ Integrated USB 2.0 transceiver, smart Serial Interface Engine
 - ☐ 16 programmable endpoints
- Flexible Processor Interface, which supports:
 - □ Multiplexing and nonMultiplexing Address and Data interface
 - □ SRAM Interface

- □ Pseudo CRAM interface (Antioch Interface)
- ☐ Pseudo NAND Flash interface
- □ SPI (slave mode) interface
- □ DMA slave support
- Ultra low power, 1.8V core operation
- Low Power Modes
- Small footprint, 6x6mm VFBGA
- Supports I2C boot and Processor Boot
- Selectable Clock Input Frequencies
 □ 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Portable Navigation Devices
- Digital Cameras
- POS Terminals
- Portable Video Recorders



Cypress Semiconductor Corporation
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CYWB0224ABS/CYWB0224ABM

Functional Overview

The SLIM™ architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three different interfaces (P-port, S-port and U-port) to connect to each other independently.

With this architecture, a device using Astoria is connected to a PC through a USB, without disturbing any of the functions of the device. The device can still access Mass Storage when the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a www.DataSPC accesses a Mass Storage device independent of the main processor, or enumerates access to both the Mass Storage and the main processor at the same time.

In a handset using SLIM architecture, the user can do the following:

- Use the phone as a thumb drive.
- Download media files to the phone with all the functionalities still available on the phone.
- Use the same phone as a modem to connect the PC to the internet.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all transactions between the P-Port, S-Port, and the U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports NAND, SD, SDIO, MMC+, and CE-ATA devices at the S-Port. For the NAND device, the 8051 firmware follows the Smart Media algorithm to support the following:

- Physical to Logical Management
- ECC Correction support
- Wear Leveling
- NAND Flash bad blocks handling

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers allow the system to specify some behaviors of Astoria. For example, it can mask certain status registers from raising an interrupt. The status registers convey the status of Astoria, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface may be configured to pseudo NAND interface to support the processor's NAND interface. In addition, this interface may be configured to support the slave SPI interface. This ensures straightforward electrical communi-

cation with the processor, which may have other devices connected on a shared memory bus. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses are performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by using a DMA protocol or using an interrupt to the main processor. These two modes are configured by the external processor.

As a DMA slave, Astoria generates a DMA request signal to notify the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for a read or write operation. It then performs the appropriate read or write operations on the buffer through the processor interface. As a result, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the Interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write, and it performs the appropriate read or write operations through the processor interface.

USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in Full-Speed USB mode in addition to High-Speed USB. The USB interface consists of the USB transceiver. The USB interface can access and be accessed by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Mass Storage Support (S-Port)

The S-Port may be configured in three different modes, which simultaneously support the following:

- An SD/SDIO/MMC+/CE-ATA port and a x8 NAND port
- Two SD/SDIO/MMC+/CE-ATA ports
- Up to eight Chip Enable (CE#) for x8 or x16 NAND flash access port

These configurations are controlled by the 8051 firmware. The 16-bit NAND interface is used only when there is no other Mass Storage device connected to the S-Port.

N-Xpress NAND Controller (S-Port)

Astoria, as part of its Mass Storage management functions, can fully manage the SLC and MLC NAND flash devices. The embedded 8051 manages the actual reading and writing of the NAND, along with its required protocols. It performs standard NAND management functions, such as ECC and wear leveling. The Astoria supports single bit ECC for the SLC and 4-bit ECC for MLC NAND flash. SLC NAND flash devices are supported by CYWB0244ABS. CYWB0244ABM supports both SLC and MLC NAND flash devices.

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SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured through firmware to support SD/SDIO/MMC+/CE-ATA, this interface supports the following:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1.
- SD Memory Card Specification Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.
- SD Memory Card Specification Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006.
- SD Specifications Part E1 SDIO specification, Version 1.10, he August 18, 2004.
- CE-ATA Specification CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005

West Bridge Astoria provides support for 1-bit and 4-bit SD and SDIO cards; 1-bit, 4-bit and 8-bit MMC; MMC+ cards, and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command, which is handled by API.

Table 1. Astoria Pin Assignments

	Pin Name				10	Pin Description	Power Domain		
	Non-multiplexing	Multiplexing	SRAM	PNAND	SPI	10	Fill Description	1 Ower Domain	
	CLK	CLK		Ext pull up	SCK	ı	Clock/SPI clock		
	CE#	CE#	CE#	CS#	SS#	I	Chip Enable/NAND Chip Select/SPI Slave Select		
	A0	Ext pull up	A0	CLE#	Ext pull up	ı	Address Bus 0/PNAND Command Latch	PVDDQ VGND	
	A1	Ext pull up	A1	RB#	Ext pull up	Ю	Address Bus 1/PNAND Ready_Buy		
	A[3:2]	set A[3:2] = 01	A[3:2]	set A[3:2] = 00	set A[3:2] = 10	ı	Addr. Bus [3:2]		
	A4	Ext pull up	A4	WP#	Ext pull up	ı	Addr. Bus 4/NAND Write Protect		
	A5	SCL	A5	SCL	SCL	Ю	Address Bus 5/I2C clock		
—	A6	SDA	A6	SDA	SDA	Ю	Address Bus 6/I2C data		
P-PORT	A7]	Ext pull up	A7	set A7 to 0 - LBD set A7 to 1 - SBD	Ext pull up	I	Addr. Bus 7		
급	DQ[0]	AD[0]	DQ[0]	IO[0]	SDI	Ю	SPI Input/Data Bus 0		
	DQ[1]	AD[1]	DQ[1]	IO[1]	SDO	Ю	SPI Output/Data Bus 1		
	DQ[15:2]	AD[15:2]	DQ[15:2]	IO[15:2]	Ext pull up	Ю	Data Bus		
	ADV#	ADV#		ALE#	Ext pull up	ı	Address Valid		
	OE#	OE#	OE#	RE#	Ext pull up	ı	Output Enable		
	WE#	WE#	WE#	WE#	Ext pull up	ı	Write Enable		
	INT#	INT#	INT#	INT#	SINT	0	Interrupt Request		
	DRQ#	DRQ#	DRQ#	DRQ#	N/C	0	DMA Request		
	DACK#	DACK#	DACK#	DACK#	Ext pull up	ı	DMA Acknowledgement		
ort	D+					IO/Z	USB D+		
Ģ	D-					IO/Z	USB D-	UVDDQ UVSSQ	
U-P	UVALID					0	External USB Switch Control		





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Table 1. Astoria Pin Assignments (continued)

Non-multiplexing Multiplexing SRAM PNAND SPI	Power Domain	
SDIO and NAND Configuration SD_D[7:0] NAND_D[7:0] NAND_D[7:0] SD_D[7:0] IO SD Data bus/NAND Upper IO bus SD_D[7:0] SD_D[7:0] SD_D[7:0] IO SD Clock/NAND CE8#/NAND R/B4# SD_CK NAND_CE8#/NAND_R/B4# SD_CK SD_CK IO SD Clock/NAND CE8#/NAND R/B4# SD_CMD NAND_R/B4# SD_CMD IO SD Command, NAND CE7#, or NAND_R/B3# SD_CMD NAND_R/B3# SD_CMD IO SD Command, NAND CE7#, or NAND_R/B3# SD_POW NAND_R/B3# SD_POW IO SD Power Control/NAND CE6# SD_POW SD_POW IO SD Power Control/NAND CE6# SD_WP SD_WP IO GPIO (SD Write Protection Microswitch) or NAND_CE5# NAND_CE5# NAND_CE5# NAND_CE5# SD_Data Bus SD_CMD IO NAND Lower IO bus/2 nd SD Data Bus SD_CMD SD_POW IO SD Power IO bus/2 nd SD Data Bus SD_CMD SD_CMD IO SD Power IO bus/2 nd SD Data Bus SD_CMD SD_CMD IO SD Power IO bus/2 nd SD Data Bus SD_CMD SD_CMD	ei Dolliaili	
PD[7:0] (ĞPIO)		
AND_R/B4# NAND_CE8# / NAND_R/B4# SD_CMD PC-3 (GPIO) / NAND_CE7# / NAND_R/B3# SD_POW NAND_CE6# SD_POW NAND_CE6# SD_POW NAND_CE6# SD_WP NAND_CE6# SD_WP PC-1 (GPIO) / NAND_CE6# SD_WP SD	SSVDDQ VGND	
NAND_R/B3# NAND_CE7# / NAND_R/B3# NAND_R/B3# NAND_R/B3# V NAND_R/B3# NAND_R/B3# V NAND_R/B3# V NAND_R/B3# V NAND_CE6# SD_POW NAND_CE6# SD_POW IO SD Power Control/NAND CE6# SD_WP NAND_CE6# SD_WP IO GPIO (SD Write Protection Microswitch) or NAND_CE5# NAND_IO[7:0] NAND_IO[7:0] NAND_IO[7:0] PB[7:0] (GPIO) IO NAND Lower IO bus/2 nd SD Data Bus		
NAND_CE6# SD_WP NAND_CE5# SD_WP PC-1 (GPIO) / NAND_CE5# SD_WP IO GPIO (SD Write Protection Microswitch) or NAND_CE5# NAND_IO[7:0] NAND_IO[7:0] NAND_IO[7:0] PB[7:0] (GPIO) IO NAND Lower IO bus/2 nd SD Data Bus		
NAND_IO[7:0] NAND_IO[7:0] SD2_D[7:0] NAND_IO[7:0] PB[7:0] (GPIO) IO NAND Lower IO bus/2 nd SD Data Bus		
NAND_IO[7:0] NAND_IO[7:0] SD2_D[7:0] NAND_IO[7:0] PB[7:0] (GPIO) IO NAND Lower IO bus/2 nd SD Data Bus		
The state of the s		
NAND_CLE NAND_CLE SD2_CLK NAND_CLE PA-6 (GPIO) IO CMD Latch Enable/2 nd SD Clock		
NAND_ALE NAND_ALE SD2_CMD NAND_ALE PA-7 (GPIO) IO Address Latch Enable/2 nd SD CMD		
NAND_CE# NAND_CE# SD2_POW NAND_CE# PC-0 (GPIO) IO Chip Enable/2 nd SD Power Control		
	NVDDQ VGND	
NAND_WE# NAND_WE# N/C NAND_WE# N/C O Write Enable	VOND	
NAND_WP# NAND_WP# PA-5 (GPIO) NAND_WP# PA-5 (GPIO) IO Write Protect		
NAND_R/B# NAND_R/B# I Ready/Busy/2 nd SD WP		
NAND_CE2# NAND_CE2# SD2_WP NAND_CE2# PC-2 (GPIO) IO Chip Enable 2		
RESETOUT / NAND_R/B2# RESETOUT NAND_R/B2# / RESETOUT IO RESET OUT/NAND Busy/Ready RESETOUT	GVDDQ VGND	
GPIO[1] / NAND_CE3#		
RESET# I RESET		
WAKEUP I Wake Up Signal		
	XVDDQ	
XTALOUT O Crystal Out	VGND	
XTALSLC[1:0] I Clock Select 0 and 1	21/200	
INANDERS 1 S POR Configuration	GVDDQ VGND	
TEST[2:0] I Test Configuration		
PVDDQ PWR Processor interface VDD		
SNVDDQ PWR NAND VDD		
UVDDQ PWR USB VDD		
SSVDDQ PWR SDIO VDD		
GVDDQ PWR Miscellaneous IO VDD		
AVDDQ PWR Analog VDD XVDDQ PWR Crystal VDD		
XVDDQ PWR Crystal VDD		
VDD PWR Core VDD		
VDD33 PWR Independent 3.3V nominal		
UVSSQ PWR USB GND		
AVSSQ PWR Analog GND		
VGND PWR Core GND		

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Ordering Information

Ordering Code	Package Type	NAND Flash Support	Available Clock Input Frequencies (MHz)
CYWB0224ABS-BVXI	100 VFBGA – Pb-Free	Support SLC NAND Flash only	19.2, 24, 26, 48
CYWB0224ABM-BVXI	100 VFBGA – Pb-Free	Support SLC and MLC NAND Flash	19.2, 24, 26, 48

Package Diagram

 $\overline{\mathbf{A}}$

В

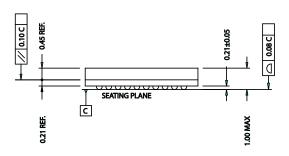
Figure 1. 100 VFBGA (6 x 6 x 1.0 MM) BZ100A

A1 CORNER

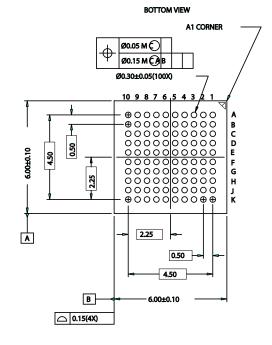
1 2 3 4 5 6 7 8 9 10

A B C D D E F G H J K K

TOP VIEW



6.00±0.10



REFERENCE JEDEC MO-195C PKG. WEIGHT: TBD (NEW PKG.)

51-85209 *B



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CYWB0224ABS/CYWB0224ABM

Document History Page

Document Title: CYWB0224ABS/CYWB0224ABM West Bridge TM Astoria TM Document Number: 001-11710						
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change		
**	567055	See ECN	VSO	New data sheet		
*A	1830226	See ECN	VSO/AESA	In the Feature list, adding the bullets of "N-Xpress Controller Technology" and "Multimedia Device Support" In the Feature list, removed the bullet of "Mass Storage device support" Update the bullet of Application Update Logic Block Diagram. Updated the section of "NAND Port" to N-Xpress NAND Controller" Updated the pin Assignment Table Fix the typo of VGAN in pin Assignment Table		

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