CYWB0320ABX-FDXI
CYWB0321ABX-FDXI

West Bridge®: Arroyo USB and Mass Storage Peripheral Controller

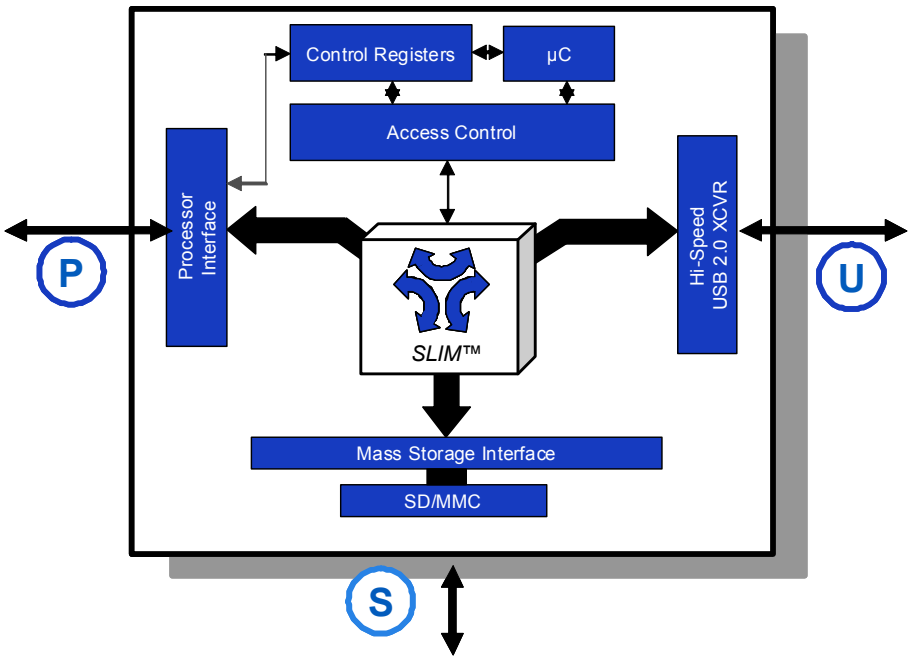
Features

- Multimedia device support
  - Support next-gen SD, SDHC, SDIO, and MMC+
- Simultaneous link to independent multimedia (SLIM®) architecture, enabling simultaneous and independent data paths between the processor and USB, and between the USB and mass storage.
- High speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB 2.0 transceiver, smart Serial Interface Engine
  - 16 programmable endpoints
- Flexible processor interface, which supports:
  - SPI (slave mode) interface
  - Multiplexing and nonmultiplexing address and data interface
  - SRAM interface
  - Pseudo CRAM interface
  - Pseudo NAND Flash interface
  - DMA slave support
- Ultra low power, 1.8 V core operation
- Low power modes
- Small footprint, 3.9 × 3.9 mm, 0.4 mm pitch, WLCSP
- Supports USB Boot, I^2C Boot and Processor Boot
- Clock input frequency
  - 19.2 MHz
  - 26 MHz

Applications

- Cellular phones
- Portable media players
- Personal digital assistants
- Portable navigation devices
- Digital cameras
- POS terminals
- Portable video recorders

Logic Block Diagram



Errata: For information on silicon errata, see "Errata" on page 50 and "Errata" on page 51. Details include trigger conditions, devices affected, and proposed workaround.

Contents

Functional Overview

The SLIM Architecture

The SLIM architecture enables three different interfaces (P-port, S-port, and U-port) to connect to each other independently.

With this architecture, a device using Arroyo is connected to a PC through a USB, without disturbing any of the device functions. The device can still access mass storage when the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC accesses a mass storage device independent of the main processor, or enumerates access to both the mass storage and the main processor at the same time.

You can do the following in a handset using SLIM architecture:

- Use the phone as a thumb drive.
- Download media files to the phone with all the functionalities still available on the phone.
- Use the same phone as a modem to connect the PC to the internet.

8051 Microprocessor

The 8051 microprocessor embedded in Arroyo does basic transaction management for all transactions between the P-Port, S-Port, and the U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports SD, SDHC, SDIO, and MMC+ devices at the S-Port.

Configuration and Status Registers

The West Bridge® Arroyo device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers enable the system to specify some behaviors of Arroyo. For example, it can mask certain status registers from raising an interrupt. The status registers convey the status of Arroyo, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface also can be configured to a pseudo NAND interface to support the processor's NAND interface. In addition, this interface can be configured to support SPI slave. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses can be performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Arroyo. These endpoints serve as buffers for data between each pair of ports; for example, between the processor port and the USB port. The processor writes and reads to these buffers through the memory interface.

Access to these buffers is controlled by using a DMA protocol or using an interrupt to the main processor. These two modes are configured by the external processor.

As a DMA slave, Arroyo generates a DMA request signal to notify the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Arroyo for the specific buffers ready for a read or write operation. It then performs the appropriate read or write operations on the buffer through the processor interface. As a result, the external processor only deals with the buffers to access a storage device connected to Arroyo.

In the Interrupt mode, Arroyo communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Arroyo for the specific buffers ready for read or write, and it performs the appropriate read or write operations through the processor interface.

USB Interface (U-Port)

In accordance with the USB 2.0 specification, Arroyo can operate in both full speed and high speed USB modes. The USB interface consists of the USB transceiver. The USB interface can access and be accessed by both the P-Port and the S-Port.

The Arroyo USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Mass Storage Support (S-Port)

The S-Port may be configured to support the following:

- Next-gen SD/SDIO/eMMC+ port

When Arroyo is configured through firmware to support SD/SDIO/MMC+, this interface supports the following:

- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.
- SD Specifications - Part E1 SDIO specification, Version 1.10, August 18, 2004.
- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1.

West Bridge Arroyo supports 1-bit and 4-bit SD and SDIO cards; 1-bit, 4-bit, and 8-bit MMC; MMC+ cards. For the SD, SDIO, and MMC/MMC Plus, this block supports one card for one physical bus interface. Arroyo supports SD commands including the multisector program command that is handled by API

Clocking

Arroyo enables connection of an external clock at the XTALIN pin. The power supply level at the crystal supply XVDDQ determines whether a crystal or a clock is provided. If XVDDQ is detected to be 1.8 V, Arroyo assumes that a clock input is provided. For a crystal to be connected, XVDDQ must be 3.3 V.

Note Clock inputs at 3.3 V level are not supported.

The 81-pin WLCSP supports 19.2 MHz and 26 MHz external clock input. The crystal or clock frequency selection is shown in Table 1 on page 4.

The XTALIN frequency is independent of the clock and data rate of the 8051 microprocessor or any of the device interfaces (including P-Port and S-Port). The internal PLL applies the proper clock multiply option depending on the input frequency.

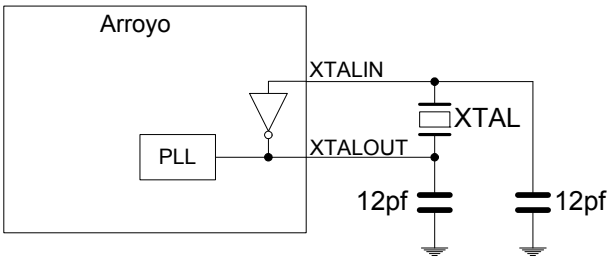
For applications that use an external clock source to drive XTALIN, the XTALOUT, pin must be left floating. The external clock source must also stop high or low and not toggle, to achieve the lowest possible current consumption. The requirements for an external clock source are shown in Table 3.

Arroyo has an on-chip oscillator circuit that uses an external 26 MHz (±150 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 1 mW drive level
- 12 pF (5% tolerance) load capacitors 150 ppm

Note CYWB0321ABX-FDXI does not support crystal.

Figure 1. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 1. CYWB0320ABX-FDXI Clock Selection

XTALSLC	Freq	Crystal/Clock
NA	26 MHz	Clock or Crystal

Table 2. CYWB0321ABX-FDXI Clock Selection

XTALSLC	Freq	Crystal/Clock
0	19.2 MHz	Clock
1	26 MHz	Clock

Table 3. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn (AVDDQ)	Supply Voltage Noise at Frequencies < 50 MHz	–	20	mV p-p
PN_100	Input Phase Noise at 100 Hz	–	–75	dBc/Hz
PN_1k	Input Phase Noise at 1 kHz Offset	–	–104	dBc/Hz
PN_10k	Input Phase Noise at 10 kHz Offset	–	–120	dBc/Hz
PN_100k	Input Phase Noise at 100 kHz Offset	–	–128	dBc/Hz
PN_1M	Input Phase Noise at 1 MHz Offset	–	–130	dBc/Hz
	Duty Cycle	30	70	%
	Maximum Frequency Deviation	–	150	ppm
	Overshoot	–	3	%
	Undershoot	–	–3	%

Power Domains

Arroyo has multiple power domains that serve different purposes within the chip.

VDDQ: This refers to a group of five independent supply domains for the digital I/Os. The nominal voltage level on these supplies are 1.8 V, 2.5 V, or 3.3 V. Specifically, the four separate I/O power domains are:

- PVDDQ – P-Port Processor interface I/O
- SSVDDQ – S-Port SD interface I/O
- GVDDQ – Other miscellaneous I/O

UVDDQ: This is the 3.3 V nominal supply for the USB I/O and some analog circuits. It also supplies power to the USB transceiver.

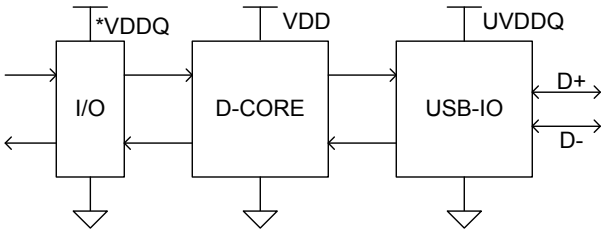
VDD: This is the supply voltage for the logic core. The nominal supply voltage level is 1.8 V. This supplies the core logic circuits. The same supply must also be used for AVDDQ.

AVDDQ: This is the 1.8 V supply for PLL and USB serializer analog components. The same supply must also be used for VDD. Maximum permitted noise on AVDDQ is 20 mV p-p.

XVDDQ: This is the clock I/O supply; 3.3 V for XTAL or 1.8 V for an external clock.

Noise guideline for all supplies except AVDDQ is maximum 100 mV p-p. All I/O supplies of Arroyo must be ON when a system is active even if Arroyo is not in use. The core VDD can also be deactivated at any time to preserve power, provided there is a minimum impedance of 1 kΩ between the VDD pin and ground. All I/Os tristate when the core is disabled.

Figure 2. Arroyo Power Supply Domains



Power Supply Sequence

The power supplies are independently sequenced without damaging the part. All power supplies must be up and stable before the device operates. If the supplies are not stable, the remaining domains are in low power (standby) state.

Power Modes

In addition to the normal operating mode, Arroyo contains several low power states when normal operation is not required.

Normal Mode

Normal mode is the mode in which Arroyo is fully functional. In this mode data transfer functions described in this document are performed.

Suspend Mode

This mode is entered internally by 8051 (external processor only initiates entry into this mode through Mailbox commands). This mode is exited by the D+ bus going low, GPIO[0] going to a pre-determined state or by asserting CE# LOW.

In Arroyo's suspend mode:

- The clocks are shut off.
- All I/Os maintain their previous state.
- Core power supply must be retained.
- The states of the configuration registers, endpoint buffers, and the program RAM are maintained. All transactions must be complete before Arroyo enters suspend mode (state of outstanding transactions are not preserved).
- The firmware resumes its operation from where it was suspended, since the program counter is not reset.
- Only inputs that are sensed are RESET#, GPIO[0]/SD_CD, GPIO[1], SD_D3, D+, and CE#. The last three are wake up sources (each can be individually enabled or disabled).
- Hard Reset can be performed by asserting the RESET# input, and Arroyo is initialized.

Standby Mode

Standby mode is a low power state. This is the lowest power mode of Arroyo while still maintaining external supply levels. This mode is entered through deassertion of the WAKEUP input pin or through internal register settings. To leave this mode, assert WAKEUP, CE#, and RESET#; and change the state of GPIO[0]/SD_CD, GPIO[1], or SD_D3.

In this mode all configuration register settings and program RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed in values. Therefore, the external processor must ensure that the required data is read before putting Arroyo into the standby mode.

In the standby mode:

- The program counter is reset on waking up from standby mode.
- All outputs are tristated and I/O is placed in input only configuration. Values of I/Os in standby mode are listed in the pin assignments table.
- Core power supply must be retained.
- Hard Reset can be performed by asserting the RESET# input, and Arroyo is initialized.
- PLL is disabled.

Core Power Down Mode

The core power supply VDD is powered down in this state. AVDDQ is tied to the same supply as VDD and is hence, also powered down. Neither the endpoint buffers, configuration registers nor program RAM maintain state. It is required that all VDDQ power supplies (except AVDDQ) are on and not power downer down in this mode. When UVDDQ is powered down, D+/D– can't be driven by external device.

The core power down mode has two power down options:

- Core only power down – VDD power down.
- Core and USB power down – VDD and UVDDQ are both powered down.

In these power down options, the endpoint buffers, configuration registers, or the program RAM do not maintain state. It is necessary to reload the firmware on exiting from this mode. It is required that all VDDQ power supplies are on and not powered down in this mode.

Pin Assignments

Table 4. CYWB0320ABX-FDXI WLCSP Package Pin Assignments

	Pin Name									Pin Description	Power Domain
	Ball #	Pseudo CRAM Interface	I/O	SRAM Interface [1]	I/O	ADM (Address/Data Multiplexing)	I/O	PNAND	I/O		
P-Port	J3	CE#	I	CE#	I	CE#	I	CE#	I	CE#	PVDDQ VGND
	E2	A7	I	A7	I	External Pull Up	I	A7 => 1:SBD A7 => 0: LBD	I	A7	
	H1	A6	I	A6	I	SDA	I/O	SDA	I/O	A6 or SDA	
	F2	A5	I	A5	I	SCL	I/O	SCL	I/O	A5 or SCL	
	G2	A4	I	A4	I	External Pull Up	I	WP#	I	A4 or WP#	
	J1	A3	I	A3	I	External Pull Low	I	External Pull Low	I	A3	
	H2	A2	I	A2	I	External Pull Up	I	External Pull Low	I	A2	
	J2	A1	I	A1	I	External Pull Up	I	R/B#	O	A1 or R/B#	
	H3	A0	I	A0	I	External Pull Up	I	CLE	I	A0 or CLE	
	F3	DQ[15]	I/O	DQ[15]	I/O	AD[15]	I/O	I/O[15]	I/O	D15, AD15, or IO15	
	J4	DQ[14]	I/O	DQ[14]	I/O	AD[14]	I/O	I/O[14]	I/O	D14, AD14, or IO14	
	H4	DQ[13]	I/O	DQ[13]	I/O	AD[13]	I/O	I/O[13]	I/O	D13, AD13, or IO13	
	G4	DQ[12]	I/O	DQ[12]	I/O	AD[12]	I/O	I/O[12]	I/O	D12, AD12, or IO12	
	J5	DQ[11]	I/O	DQ[11]	I/O	AD[11]	I/O	I/O[11]	I/O	D11, AD11, or IO11	
	H5	DQ[10]	I/O	DQ[10]	I/O	AD[10]	I/O	I/O[10]	I/O	D10, AD10, or IO10	
	J6	DQ[9]	I/O	DQ[9]	I/O	AD[9]	I/O	I/O[9]	I/O	D9, AD9, or IO9	
	G6	DQ[8]	I/O	DQ[8]	I/O	AD[8	I/O	I/O[8]	I/O	D8, AD8, or IO8	
	H6	DQ[7]	I/O	DQ[7]	I/O	AD[7]	I/O	I/O[7]	I/O	D7, AD7, or IO7	
	J7	DQ[6]	I/O	DQ[6]	I/O	AD[6]	I/O	I/O[6]	I/O	D6, AD6, or IO6	
	F6	DQ[5]	I/O	DQ[5]	I/O	AD[5]	I/O	I/O[5]	I/O	D5, AD5, or IO5	
	J8	DQ[4]	I/O	DQ[4]	I/O	AD[4]	I/O	I/O[4]	I/O	D4, AD4, or IO4	
	H7	DQ[3]	I/O	DQ[3]	I/O	AD[3]	I/O	I/O[3]	I/O	D3, AD3, or IO3	
	G7	DQ[2]	I/O	DQ[2]	I/O	AD[2]	I/O	I/O[2]	I/O	D2, AD2, or IO2	
	H8	DQ[1]	I/O	DQ[1]	I/O	AD[1]	I/O	I/O[1]	I/O	D1, AD1, or IO1	
	H9	DQ[0]	I/O	DQ[0]	I/O	AD[0]	I/O	I/O[0]	I/O	D0I, AD0, or IO0	
	G8	ADV#	I		I	ADV#	I	ALE	I	Address Valid	
	F8	OE#	I	OE#	I	OE#	I	RE#	I	Output Enable	
	G9	WE#	I		I	WE#	I	WE#	I	WE#	
Int	A7	INT#	O		O	INT#	O	INT#	O	INT Request	GVDDQ VGND
	D6	DRQ	O		O	DRQ	O	DRQ	O	DMA Request	
	C6	DACK	I		I	DACK	I	DACK	I	DMA ACK	
U-Port	D9	D+							I/O/Z	USB D+	UVDDQ UVSSQ
	E9	D–							I/O/Z	USB D–	
	D7	NC							I/O/Z	Left floating	
	E7	NC							I/O/Z	Left floating	

Note
1. Errata: When Arroyo is configured to use SRAM for P-port interface, OE should be asserted simultaneously with CE. If this is not possible, OE should be asserted prior to CE. Otherwise, data can be dropped when external processor reads the Arroyo through SRAM interface. For more information, see the "Errata" on page 50 and "Errata" on page 51.

Table 4. CYWB0320ABX-FDXI WLCSP Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
	S-Port Interface		I/O		
S-Port	C4	SD_D[7]	I/O	SD Data or GPIO	SSVDDQ VGND
	A2	SD_D[6]	I/O	SD Data or GPIO	
	B3	SD_D[5]	I/O	SD Data or GPIO	
	C5	SD_D[4]	I/O	SD Data or GPIO	
	B4	SD_D[3]	I/O	SD Data or GPIO	
	A4	SD_D[2]	I/O	SD Data or GPIO	
	B5	SD_D[1]	I/O	SD Data or GPIO	
	A5	SD_D[0]	I/O	SD Data or GPIO	
	A3	SD_CLK	O	SD Clock or GPIO	
	A1	SD_CMD	I/O	SD CMD or GPIO	
	E1	PB[7] (GPIO)	I/O	GPIOI	
	D1	PB[6] (GPIO)	I/O	GPIOI	
	D2	PB[5] (GPIO)	I/O	GPIOI	
	C1	PB[4] (GPIO)	I/O	GPIOI	
	C2	PB[3] (GPIO)	I/O	GPIOI	
	D3	PB[2] (GPIO)	I/O	GPIOI	
	B1	PB[1] (GPIO)	I/O	GPIOI	
	B2	PB[0] (GPIO)	I/O	GPIOI	
	G1	TESTTREE	O	Test Mode	
	F1	SCAN (Ext Pull-Low)	I	Test Mode (Ext Pull-Low)	
Other	A6	SD_CD	I	SD CD	GVDDQ VGND
	B7	RESET#	I	RESET	
	E5	WAKEUP	I	Wake Up Signal	
Conf	C7	TEST[2]	I	Test Cfg 2	GVDDQ VGND
	E6	TEST[1]	I	Test Cfg 1	
	A8	TEST[0]	I	Test Cfg 0	
CLK	B9	XTALIN	I	Clock IN	XVDDQ VGND
	A9	XTALOUT	O	Clock OUT	
Power	F4, J9	PVDDQ	Power	Processor I/F VDD	
	E8	UVDDQ	Power	USBVDD	
	D5	SSVDDQ	Power	SDIO VDD	
	B6	GVDDQ	Power	Misc I/O VDD	
	C8	AVDDQ	Power	Analog VDD	
	D8	XVDDQ	Power	Crystal VDD	
	E4, G5, F7, F9	VDD	Power	Core VDD	
	C9	UVSSQ	Power	USB GND	
	B8	AVSSQ	Power	Analog GND	
	C3, D4, E3, F5, G3	VGND	Power	Core GND	

Table 5. CYWB0321ABX-FDXI WLCSP Package Pin Assignments

	Pin Name					Pin Description	Power Domain
	Ball #	PNAND	I/O	SPI [2]	I/O		
P-Port	J2	Ext pull low	I	SCK	I	Clock	PVDDQ VGND
	J4	CE#	I	SS#	I	CE# or SPI Slave Select	
	G5	SDA	I/O	SDA	I/O	I2C data	
	H2	SCL	I/O	SCL	I/O	I2C clock	
	J1	WP#	I	Ext pull up	I	PNAND WP	
	H3	A[3] (Ext pull low)	I	A[3] (Ext pull up)	I	A[3]	
	F5	A[2] (Ext pull low)	I	A[2] (Ext pull low)	I	A[2]	
	J3	RB#	O	Ext pull up	I	PNAND R/B#	
	H4	CLE	I	Ext pull up	I	PNAND CLE	
	J6	I/O[7]	I/O	Ext pull up	I	IO7	
	H6	I/O[6]	I/O	Ext pull up	I	IO6	
	J7	I/O[5]	I/O	Ext pull up	I	IO5	
	J8	I/O[4]	I/O	Ext pull up	I	IO4	
	H7	I/O[3]	I/O	Ext pull up	I	IO3	
	G7	I/O[2]	I/O	Ext pull up	I	IO2	
	H8	I/O[1]	I/O	SDO	O	IO1 or SPI SDO	
	H9	I/O[0]	I/O	SDI	I	IO0 or SPI SDI	
	G8	ALE	I	Ext pull up	I	Address Valid	
	F8	RE#	I	Ext pull up	I	Output Enable	
	G9	WE#	I	Ext pull up	I	WE#	
Int	A7	INT#	O	SINT#	O	INT Request	GVDDQ VGND
U-Port	D9	D+			I/O/Z	USB D+	UVDDQ UVSSQ
	E9	D–			I/O/Z	USB D–	
	D7	NC			I/O/Z	Left floating	
	E7	NC			I/O/Z	Left floating	

Note
2. Errata: When Arroyo is configured to use SPI for Processor-Port (P-Port) interface, transfers from U-Port to P-Port may intermittently fail after wakeup from STANDBY mode. Workaround for this problem is added in SDK version 1.0 or later. For more information, see the "Errata" on page 50 and "Errata" on page 51.

Table 5. CYWB0321ABX-FDXI WLCSP Package Pin Assignments (continued)

	Pin Name					Pin Description	Power Domain
	Ball #	SDIO	I/O	GPIO only Configuration	I/O		
S-Port	B2	SD_D[7]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO	SSVDDQ VGND
	A2	SD_D[6]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO	
	C3	SD_D[5]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO	
	B3	SD_D[4]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO	
	B4	SD_D[3]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO	
	C4	SD_D[2]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO	
	C5	SD_D[1]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO	
	B5	SD_D[0]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO	
	A3	SD_CLK	O	PC-7 (GPIO)	I/O	SD Clock	
	D4	SD_CMD	I/O	PC-3 (GPIO)	I/O	SD CMD	
	A1	SD_POW	O	PC-6 (GPIO)	I/O	SD POW	
	A5	SD_WP	I	Unused	I	SD WP, GPIO	
	E2	SD_RSV	I/O	PB[7] (GPIO)	I/O	Connect to SSVDDQ with 10K pull up resister	SSVDDQ VGND
	D1	SD_RSV	I/O	PB[6] (GPIO)	I/O		
	E3	SD_RSV	I/O	PB[5] (GPIO)	I/O		
	D2	SD_RSV	I/O	PB[4] (GPIO)	I/O		
	C1	SD_RSV	I/O	PB[3] (GPIO)	I/O		
	D3	SD_RSV	I/O	PB[2] (GPIO)	I/O		
	C2	SD_RSV	I/O	PB[1] (GPIO)	I/O		
	B1	SD_RSV	I/O	PB[0] (GPIO)	I/O		
	G2	SD_RSV	I	Unused	I		
	F2	NC	O	PA-7 (GPIO)	I/O	Left floating	
	G3	NC	O	PC-0 (GPIO)	I/O		
	H1	NC	O	N/C	O		
	E1	NC	O	N/C	O		
	F3	NC	O	PA-5 (GPIO)	I/O		
	G4	NC	O	PA-6 (GPIO)	I/O		
	G1	NC	O	PC-2 (GPIO)	I/O		
Other	B7	RESETOUT	O	RESETOUT	O	RESETOUT	GVDDQ VGND
	B6	PC-5 (GPIO[1])	I/O O	PC-5 (GPIO[1])	I/O	GPIO, SD2 CD4	
	A6	PC-4 (GPIO[0]) or SD_CD	I/O I O	PC-4 (GPIO[0])	I/O	GPIO, SD1 CD	
	C7	RESET#			I	RESET	
	D6	WAKEUP			I	Wake Up Signal	
Conf	A9	XTALSLC				Clock Select	GVDDQ VGND
	A8	TEST[2]			I	Test Cfg 2	
	F7	TEST[1]				Test Cfg 1	
	D8	TEST[0]				Test Cfg 0	
CLK	B9	XTALIN			I	Clock IN	VGND

Table 5. CYWB0321ABX-FDXI WLCSP Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Power	H5, J9	PVDDQ	Power	Processor I/F VDD	
	F1	SSVDDQ	Power	SDIO VDD	
	E8	UVDDQ	Power	USB VDD	
	A4	SSVDDQ	Power	SDIO VDD	
	C6	GVDDQ	Power	Misc I/O VDD	
	C8	AVDDQ	Power	Analog VDD	
	E5, F4, F6, F9	VDD	Power	Core VDD	
	C9	UVSSQ	Power	USB GND	
	B8	AVSSQ	Power	Analog GND	
	D5, E4, E6, G6, J5	VGND	Power	Core GND	

Figure 3. CYWB0320ABX-FDXI WLCSP Ball Map - Top View

	1	2	3	4	5	6	7	8	9	
A	SD_CMD	SD_D[6]	SD_CLK	SD_D[2]	SD_D[0]	GPIO[0]	INT#	TEST[0]	XTALOUT	A
B	NAND_IO[1]	NAND_IO[0]	SD_D[5]	SD_D[3]	SD_D[1]	GVDDQ	RESET#	AVSSQ	XTALIN	B
C	NAND_IO[4]	NAND_IO[3]	VGND	SD_D[7]	SD_D[4]	DACK#	TEST[2]	AVDDQ	UVSSQ	C
D	NAND_IO[6]	NAND_IO[5]	NAND_IO[2]	VGND	SSVDDQ	DRQ#	NC	XVDDQ	D+	D
E	NAND_IO[7]	A[7]	VGND	VDD	WAKEUP	TEST[1]	NC	UVDDQ	D-	E
F	SCAN	A[5]	DQ[15]	PVDDQ	VGND	DQ[5]	VDD	OE#	VDD	F
G	TESTTREE	A[4]	VGND	DQ[12]	VDD	DQ[8]	DQ[2]	ADV#	WE#	G
H	A[6]	A[2]	A[0]	DQ[13]	DQ[10]	DQ[7]	DQ[3]	DQ[1]	DQ[0]	H
J	A[3]	A[1]	CE#	DQ[14]	DQ[11]	DQ[9]	DQ[6]	DQ[4]	PVDDQ	J
	1	2	3	4	5	6	7	8	9	

POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDD/AVDDQ
	VGND/AVSSQ
	PVDDQ
	XVDDQ

Figure 4. CYWB0321ABX-FDXI WLCSP Ball Map – Top View

	1	2	3	4	5	6	7	8	9	
A	SD_POW	SD_D[6]	SD_CLK	SSVDDQ	SD_WP	GPIO[0]	INT#	TEST[2]	XTALSLC	A
B	SD_RSV	SD_D[7]	SD_D[4]	SD_D[3]	SD_D[0]	GPIO[1]	RESETOUT	AVSSQ	XTALIN	B
C	SD_RSV	SD_RSV	SD_D[5]	SD_D[2]	SD_D[1]	GVDDQ	RESET#	AVDDQ	UVSSQ	C
D	SD_RSV	SD_RSV	SD_RSV	SD_CMD	VGND	WAKEUP	NC	TEST[0]	D+	D
E	NC	SD_RSV	SD_RSV	VGND	VDD	VGND	NC	UVDDQ	D-	E
F	SSVDDQ	NC	NC	VDD	A[2]	VDD	TEST[1]	RE#	VDD	F
G	NC	SD_RSV	NC	NC	SDA	VGND	IO[2]	ALE	WE#	G
H	NC	SCL	A[3]	CLE	PVDDQ	IO[6]	IO[3]	IO[1]	IO[0]	H
J	WP#	Pull-Low	R/B#	CE#	VGND	IO[7]	IO[5]	IO[4]	PVDDQ	J
	1	2	3	4	5	6	7	8	9	

POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDD/AVDDQ
	VGND/AVSSQ
	PVDDQ

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Supplied (Industrial) ..... –40 °C to +85 °C

Supply Voltage to Ground Potential
VDD, AVDDQ .....–0.5 V to +2.0 V
GVDDQ, PVDDQ, SSVDDQ, UVDDQ, and XVDDQ .....–0.5 V to +4.0 V

DC Input Voltage to Any Input Pin .....1.89 V to 3.6 V

(Depends on I/O supply voltage. Inputs are not overvoltage tolerant.)

DC Voltage applied to Outputs in High Z State ..... –0.5 V to VDDQ + 0.5 V

Static Discharge Voltage (ESD) from JESD22-A114 .....> 2000 V

Latch up current .....> 200 mA

Maximum Output Short Circuit Current for all I/O Configurations. (Vout = 0 V) .....–100 mA

Operating Conditions

T_A (Ambient Temperature Under Bias)
Industrial ..... –40 °C to +85 °C

VDD, AVDDQ Supply Voltage .....1.7 V to 1.9 V

UVDDQ Supply Voltage .....3.0 V to 3.6 V

PVDDQ, GVDDQ, SSVDDQ Supply Voltage .....1.7 V to 3.6 V

XVDDQ (Crystal I/O) Supply Voltage .....3.0 V to 3.6 V

XVDDQ (Ext. Clock I/O) Supply Voltage .....1.7 V to 1.9 V

DC Characteristics

Table 6. DC Specifications for All Voltage Supplies

Parameter	Description	Conditions		Min	Typ	Max	Unit
VDD	Core Voltage Supply			1.7	1.8	1.9	V
AVDDQ	Analog Voltage Supply			1.7	1.8	1.9	V
XVDDQ	Crystal Voltage Supply			3.0	3.3	3.6	V
XVDDQ	Clock Voltage Supply			1.7	1.8	1.9	V
PVDDQ [3]	Processor Interface I/O			1.7	1.8, 2.5, 3.3	3.6	V
GVDDQ [3]	Miscellaneous I/O Voltage Supply			1.7	1.8, 2.5, 3.3	3.6	V
SSVDDQ [3, 4]	S-Port SD I/O Voltage Supply			1.7	1.8, 2.5, 3.3	3.6	V
UVDDQ [5]	USB Voltage Supply			3.0	3.3	3.6	V
V_{IH1}[6]	Input HIGH Voltage 1	All ports except USB, 2.0 V ≤ V_{CC} ≤ 3.6 V		0.625 × V_{CC}	–	V_{CC} + 0.3	V
V_{IH2}[6]	Input HIGH Voltage 2	All ports except USB, 1.7 V ≤ V_{CC} < 2.0 V		V_{CC} – 0.4	–	V_{CC} + 0.3	
V_{IL}	Input LOW Voltage			–0.3	–	0.25 × V_{CC}	V
V_{OH}	Output HIGH Voltage	I_{OH}(MAX) = –0.1 mA		0.9 × V_{CC}	–	–	V
V_{OL}	Output LOW Voltage	I_{OL}(MIN) = 0.1 mA			–	0.1 × V_{CC}	V
I_{IX}	Input Leakage Current	All I/O signals held at VDDQ		–1	–	1	µA
I_{OZ}	Output Leakage Current	All I/O signals held at VDDQ		–1	–	1	µA
I_{CC} Core	Operating Current of Core Voltage Supply (VDD) and Analog Voltage Supply (AVDDQ)	WLCSP package, outputs tristated		–	–	115	mA
I_{CC} Crystal	Operating Current of Crystal Voltage Supply (XVDDQ) [7]	WLCSP package		–	–	N/A	
I_{CC} USB	Operating Current of USB Voltage Supply (UVDDQ) [7]	Operating and terminated for high speed mode		–	–	25	mA
I_{SB1}	Total Standby Current of Arroyo when Device is in Suspend Mode	1. *VDDQ = 3.3 V nominal (3.0–3.6 V) 2. Outputs and Bidirs high or floating[7] 3. XTALOUT floating 4. D+ floating, D– grounded 5. Device in suspend mode	25 °C	TBD	TBD	TBD	
			85 °C	TBD	TBD	TBD	

Notes
3. Interfaces with a voltage range are adjustable with respect to the I/O voltage and supports multiple I/O voltages.
4. The SSVDDQ I/O voltage can be dynamically changed (for example, from high range to low range) as long as the supply voltage undershoot does not surpass the lower minimum voltage limit. SSVDDQ and SNVDDQ levels for SD modes: 2.0 V–3.6 V, MMC modes: 1.7 V–3.6 V.
5. When U-Port is in a disabled state, UVDDQ can go down to 2.4 V, provided UVDDQ is still the highest supply voltage level.
6. V_{CC} = pertinent VDDQ value.
7. The Outputs and Bidirs that are forced low in standby mode can increase I/O supply standby current beyond specified value.
   Active Current Conditions:
   -UVDDQ: USB transmitting 50% of the time, receiving 50% of the time.
   -PVDDQ/SNVDDQ/SSVDDQ/GVDDQ: Active current depends on I/O activity, bus load and supply level.

Table 6. DC Specifications for All Voltage Supplies (continued)

Parameter	Description	Conditions		Min	Typ	Max	Unit
I_{SB2}	Total Standby Current of Arroyo when Device is in Standby Mode	1. *VDDQ = 3.3 V Nominal (3.0–3.6 V) 2. Outputs and Bidirs High or Floating [7] 3. XTALOUT Floating 4. D+ Floating, D– Grounded	25 °C	–	–	52	µA
			85 °C	–	–	450	µA
I_{SB3}	Total Standby Current of Arroyo when Device is in Core Power Down Mode	1. Outputs and Bidirs High or Floating [7] 2. XTALOUT Floating 3. D+ Floating, D– Grounded 4. Core Powered Down	25 °C	–	–	28	µA
			85 °C	–	–	139	µA

Table 7. Capacitance

Parameter	Description	Conditions	Typ	Max	Unit
C_{IN}	Input Pin Capacitance, Except D+/D–	TA = 25 °C, f = 1 MHz, $V_{CC} = V_{CCIO}$	–	9	pF
	Input Pin Capacitance, D+/D–		–	15	
C_{OUT}	Output Pin Capacitance		–	10	pF

AC Timing Parameters

P Port Interface

PCRAM Non Multiplexing Asynchronous Mode

Table 8. Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
	Interface Bandwidth (MBPS)	–	66.7	MBps
t_{AA}	Address to Data Valid	–	30	ns
t_{OH}	Data Output Hold from Address Change	3	–	ns
t_{EA}	Chip Enable to Data Valid	–	30	ns
t_{AADV}	ADV# to Data Valid Access Time	–	30	ns
t_{AVS}	Address Valid to ADV# HIGH	5	–	ns
t_{AVH}	ADV# HIGH to Address Hold	2 [8]	–	ns
t_{CVS}	CE# Low Setup Time to ADV# HIGH	5	–	ns
t_{VPH}	ADV# HIGH Time	15 [9]	–	ns
t_{VP}	ADV# Pulse Width LOW	7.5	–	ns
t_{OE}	OE# LOW to Data Valid	–	22.5	ns
t_{OLZ}	OE# LOW to Low Z	3	–	ns
t_{OHZ}	OE# HIGH to High Z	0	22.5	ns
t_{LZ}	CE# LOW to Low Z	3	–	ns
t_{HZ}	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
t_{CW}	CE# LOW to Write End	30	–	ns
t_{AW}	Address Valid to Write End	30	–	ns
t_{AS}	Address Setup to Write Start	0	–	ns
t_{ADVS}	ADV# Setup to Write Start	0	–	ns
t_{WP}	WE# Pulse Width	22	–	ns
t_{WPH}	WE# HIGH Time	10	–	ns
t_{CPH}	CE# HIGH Time	10	–	ns
t_{AVS}	Address Valid to ADV# HIGH	5	–	ns
t_{AVH}	ADV# HIGH to Address Hold	2 [8]	–	ns
t_{CVS}	CE# LOW Setup Time to ADV# HIGH	5	–	ns
t_{VPH}	ADV# HIGH Time	15 [9]	–	ns
t_{VP}	ADV# Pulse Width LOW	7.5	–	ns
t_{VS}	ADV# LOW to End of Write	30	–	ns
t_{DW}	Data Setup to Write End	18	–	ns
t_{DH}	Data Hold from Write End	0	–	ns
t_{WHZ}	Write to DQ High Z Output	–	22.5	ns
t_{OW}	End of Write to Low Z Output	3	–	ns

Notes
8. In applications where back-to-back accesses are not performed on different endpoint addresses, the minimum t_{AVH} spec. can be relaxed to 0 ns.
9. In applications where access cycle time is at least 60 ns, t_{VPH} can be relaxed to 12 ns.

Figure 5. Non Multiplexing Asynchronous Pseudo CRAM mode Single Read Timing Parameters

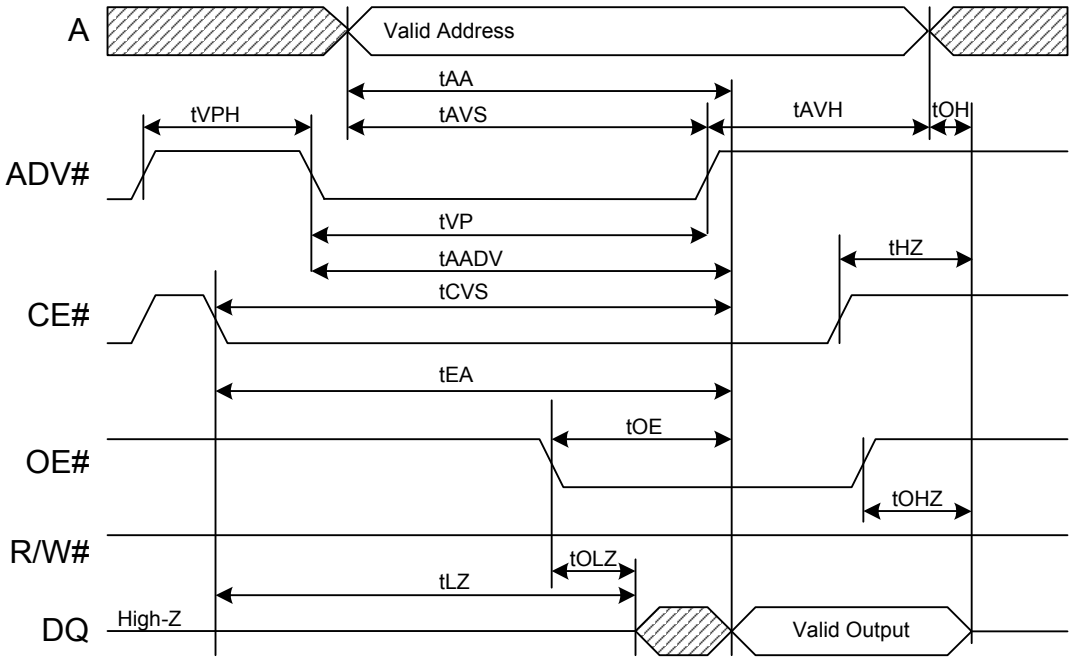


Figure 6. Non Multiplexing Asynchronous Pseudo CRAM Mode Back to Back Read Timing Parameters

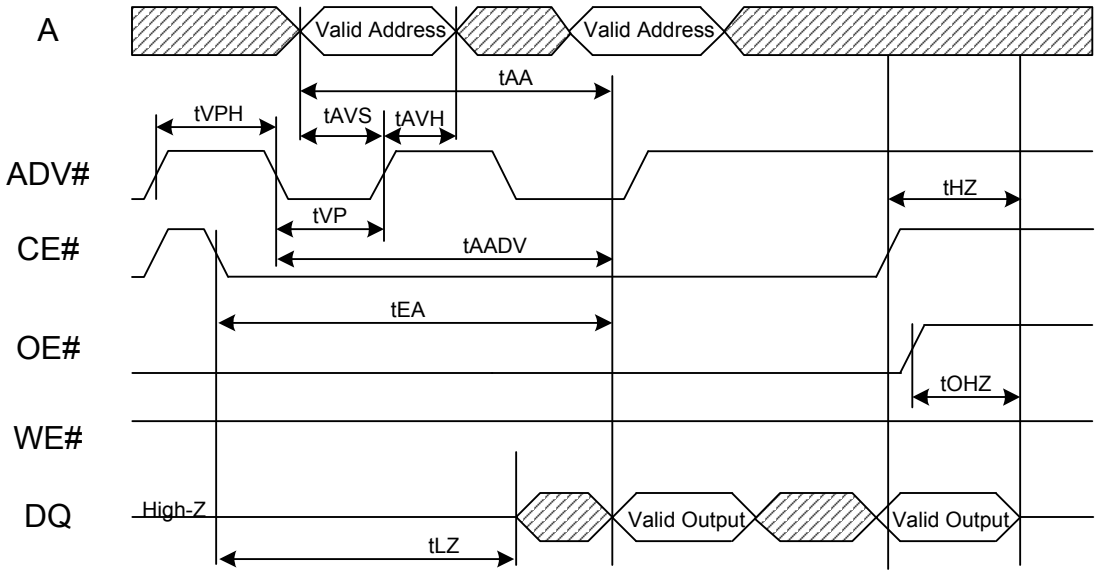


Figure 7. Non Multiplexing Asynchronous Pseudo CRAM mode Back to Back Write Timing Parameters

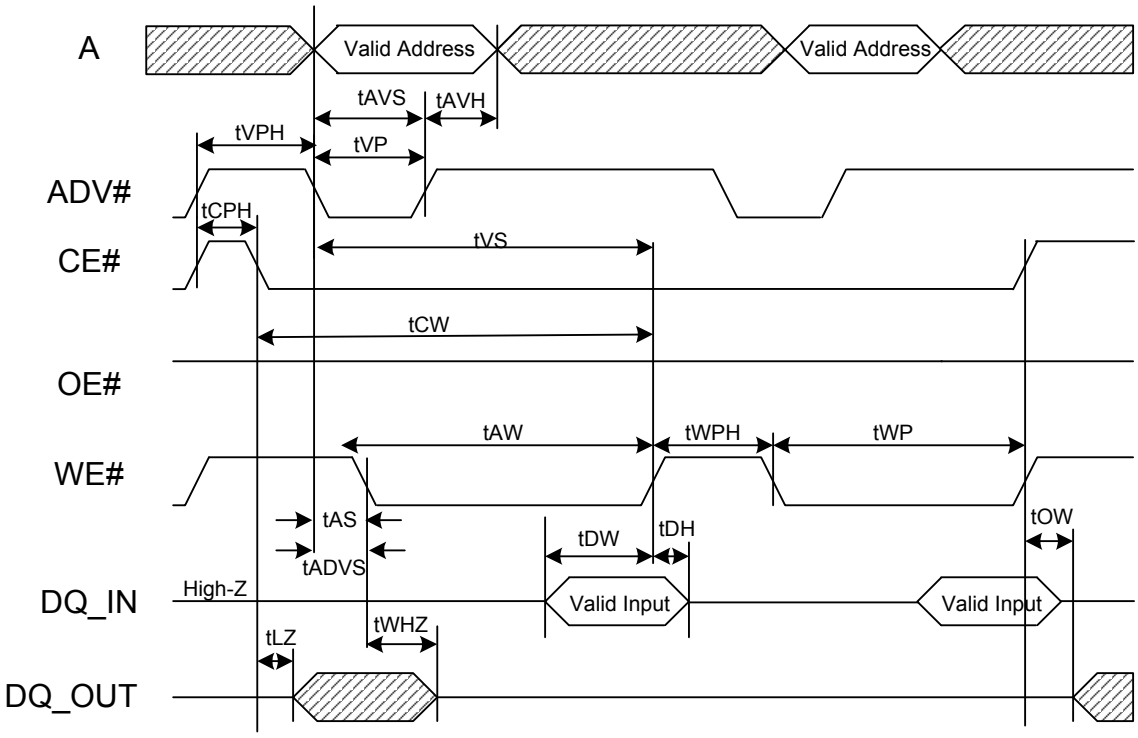


Figure 8. Non Multiplexing Asynchronous Pseudo CRAM Mode Read to Write Timing Parameters

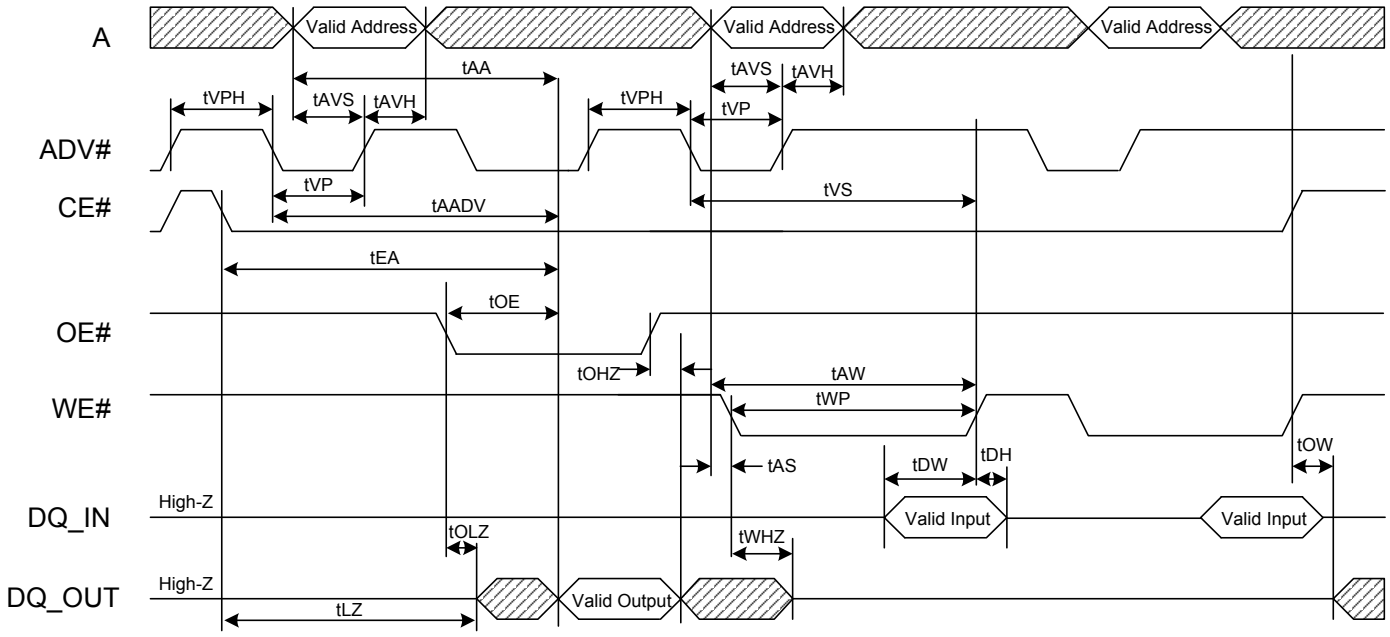
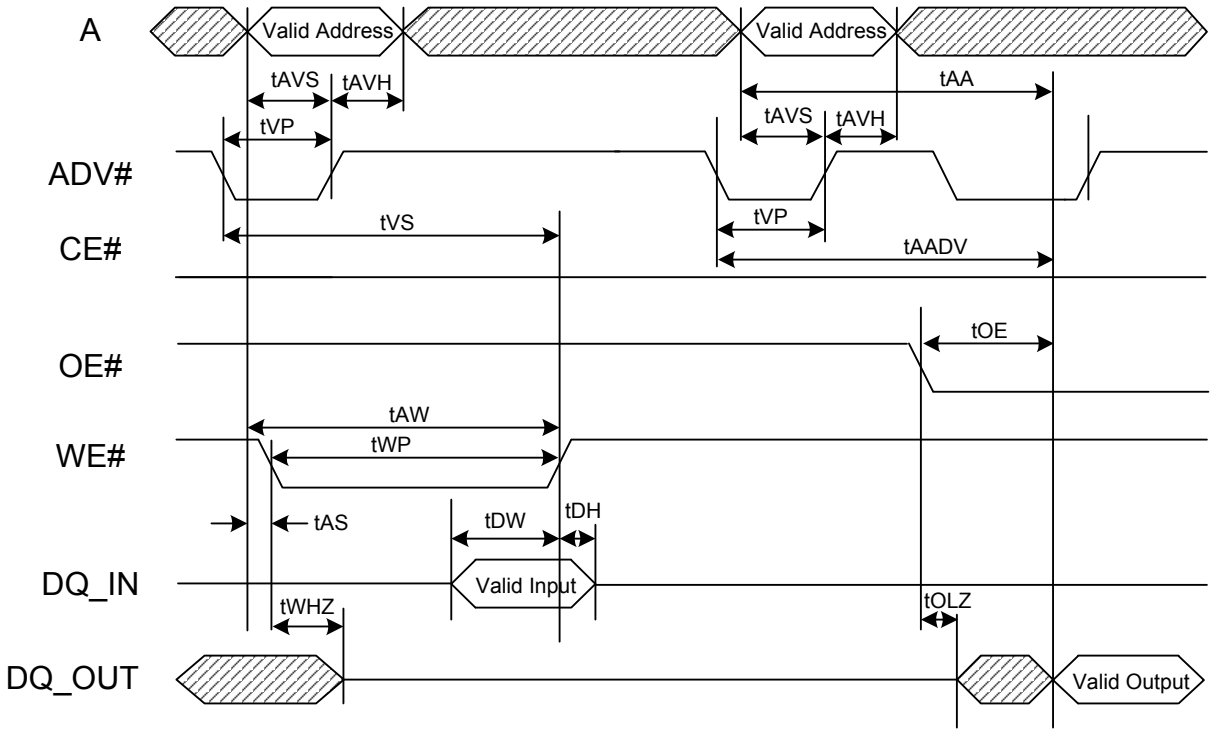


Figure 9. Non Multiplexing Asynchronous Pseudo CRAM Mode Write to Read Timing Parameters



Address Data Multiplexing Asynchronous Mode

Table 9. Address Data Multiplexing Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
	Interface Bandwidth	–	50	MBps
t_{AA}	Address to Data Valid	–	30	ns
t_{EA}	Chip Enable Access Time	–	30	ns
t_{AADV}	ADV# to Data Valid Access Time	–	30	ns
t_{AVS}	Address Valid to ADV# HIGH	5	–	ns
t_{AVH}	ADV# HIGH to Address Hold	2	–	ns
t_{CVS}	CE# LOW Setup Time to ADV# HIGH	5	–	ns
t_{VPH}	ADV# HIGH Time	15	–	ns
t_{VP}	ADV# Pulse Width LOW	7.5	–	ns
t_{AVDOE}	ADV# HIGH to OE# LOW	0	–	ns
t_{OE}	OE# LOW to Data Valid	–	22.5	ns
t_{OLZ}	OE# LOW to Low Z	3	–	ns
t_{OHZ}	OE# HIGH to High Z	–	22.5	ns
t_{LZ}	CE# LOW to Low Z	3	–	ns
t_{HZ}	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
t_{CW}	CE# LOW to Write End	30	–	ns
t_{AW}	Address Valid to Write End	30	–	ns
t_{AVDWE}	ADV# HIGH to Write Start	0	–	ns
t_{WP}	WE# Pulse Width	22	–	ns
t_{AVS}	Address Valid to ADV# HIGH	5	–	ns
t_{AVH}	ADV# HIGH to Address Hold	2	–	ns
t_{CVS}	CE# LOW Setup Time to ADV# HIGH	5	–	ns
t_{VPH}	ADV# HIGH Time	15	–	ns
t_{VP}	ADV# Pulse Width LOW	7.5	–	ns
t_{VS}	ADV# LOW to End of Write	30	–	ns
t_{DS}	Data Setup to Write End	18	–	ns
t_{DH}	Data Hold from Write End	0	–	ns

Figure 10. Address Data Multiplexing Asynchronous Single Read Timing Parameters

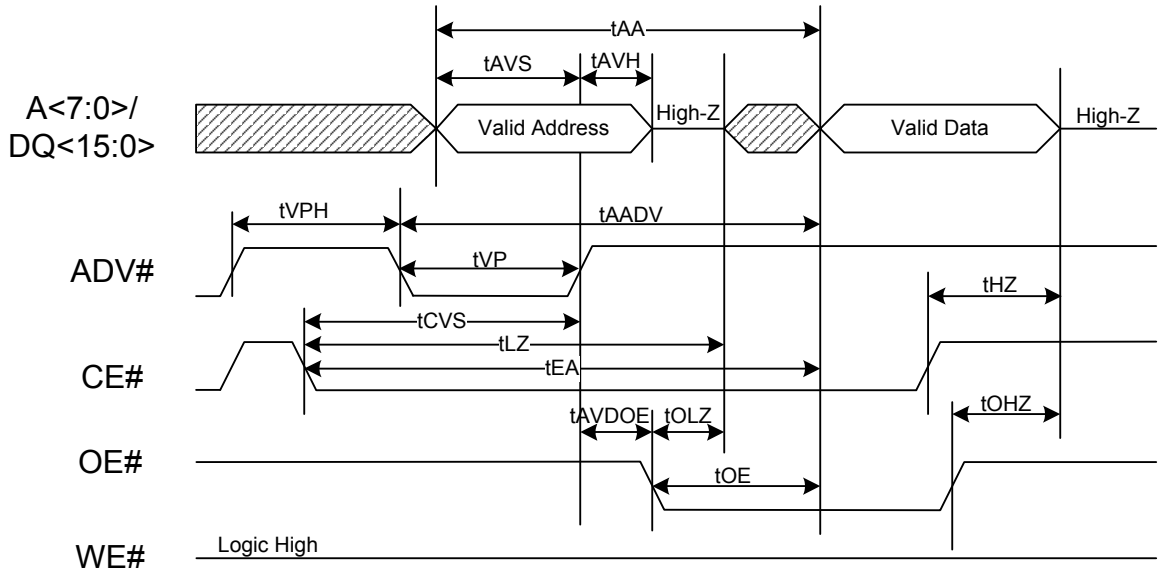
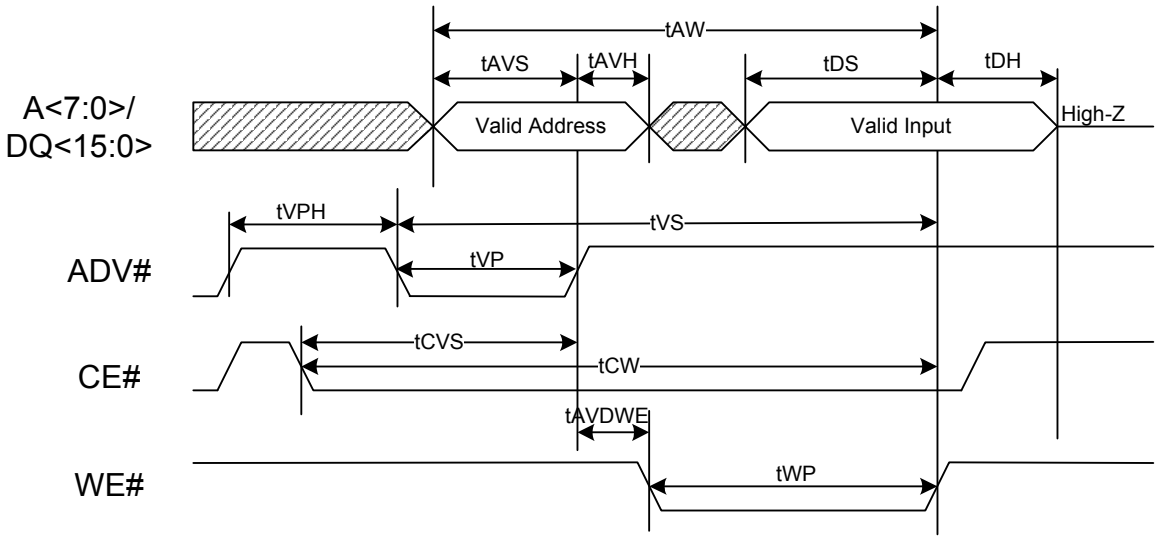


Figure 11. Address Data Multiplexing Asynchronous Single Write Timing Parameters

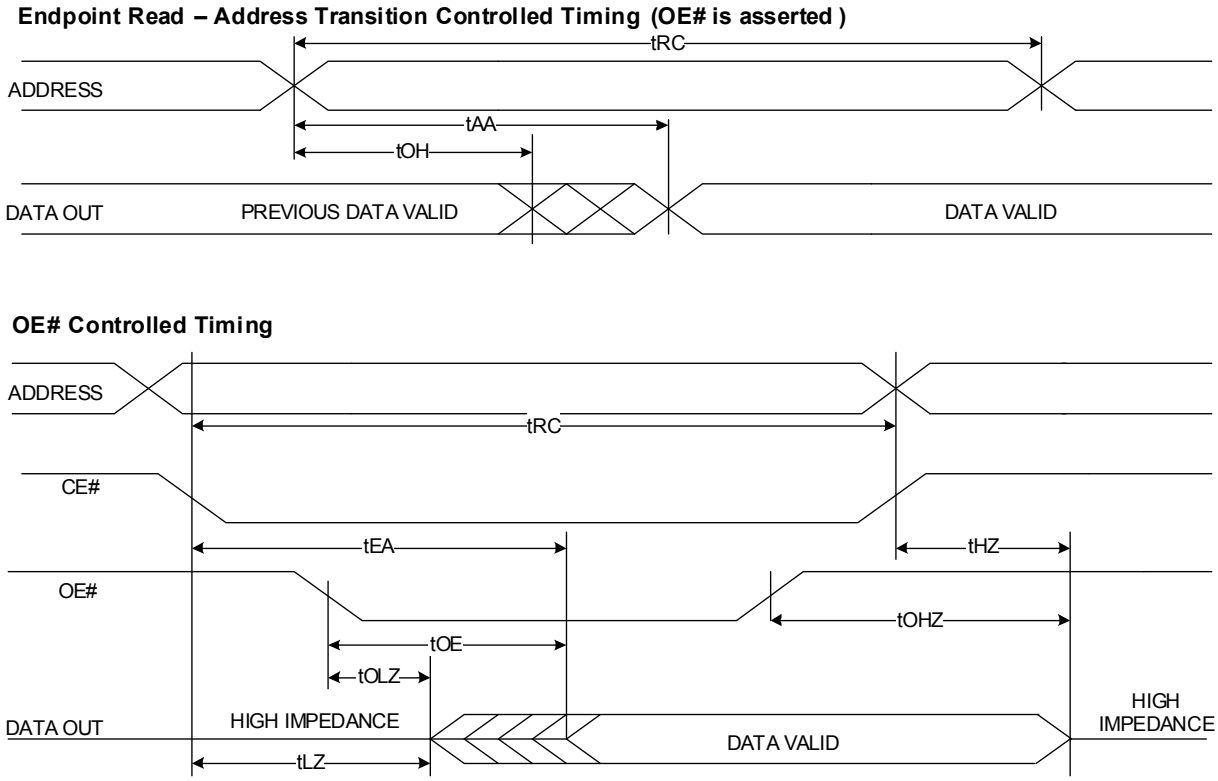


Asynchronous SRAM Mode Timing Parameters

Table 10. Asynchronous SRAM Mode Timing Parameters

Parameter	Description	Min	Max	Unit
	Interface Bandwidth (MBps)	–	66.7	MBps
Read Timing Parameters				
t_{RC}	Read Cycle Time	30	–	ns
t_{AA}	Address to Data Valid	–	30	ns
t_{OH}	Data Output Hold from Address Change	3	–	ns
t_{EA}	Chip Enable to Data Valid	–	30	ns
t_{OE}	OE# LOW to Data Valid	–	22.5	ns
t_{OLZ}	OE# LOW to Low Z	3	–	ns
t_{OHZ}	OE# HIGH to High Z	0	22.5	ns
t_{LZ}	CE# LOW to Low Z	3	–	ns
t_{HZ}	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
t_{WC}	Write Cycle Time	30	–	ns
t_{CW}	CE# LOW to Write End	30	–	ns
t_{AW}	Address Valid to WE# End	30	–	ns
t_{AS}	Address Setup to WE# or CE# Start	0	–	ns
t_{AH}	Address Hold Time from WE# or CE# End for PCRAM to SRAM Changes (Astoria is default in PCRAM mode after RESET. This timing is the requirement for the first time to access the P-Port Interface Configuration Register to change the Astoria to PSRAM mode)	2	–	ns
	Address Hold Time from WE# or CE# End for PSRAM Mode	0	–	
t_{WP}	WE# Pulse Width	22	–	ns
t_{WPH}	WE# HIGH Time	10	–	ns
t_{CPH}	CE# HIGH Time	10	–	ns
t_{DS}	Data Setup to Write End	18	–	ns
t_{DH}	Data Hold from Write End	0	–	ns
t_{WHZ}	Write to DQ High Z Output	–	22.5	ns
t_{OW}	End of Write to Low Z Output	3	–	ns
t_{DPW}	DRQ# Pulse Width	110	–	ns

Figure 12. Non Multiplexing Asynchronous SRAM Read Timing Parameters [10]

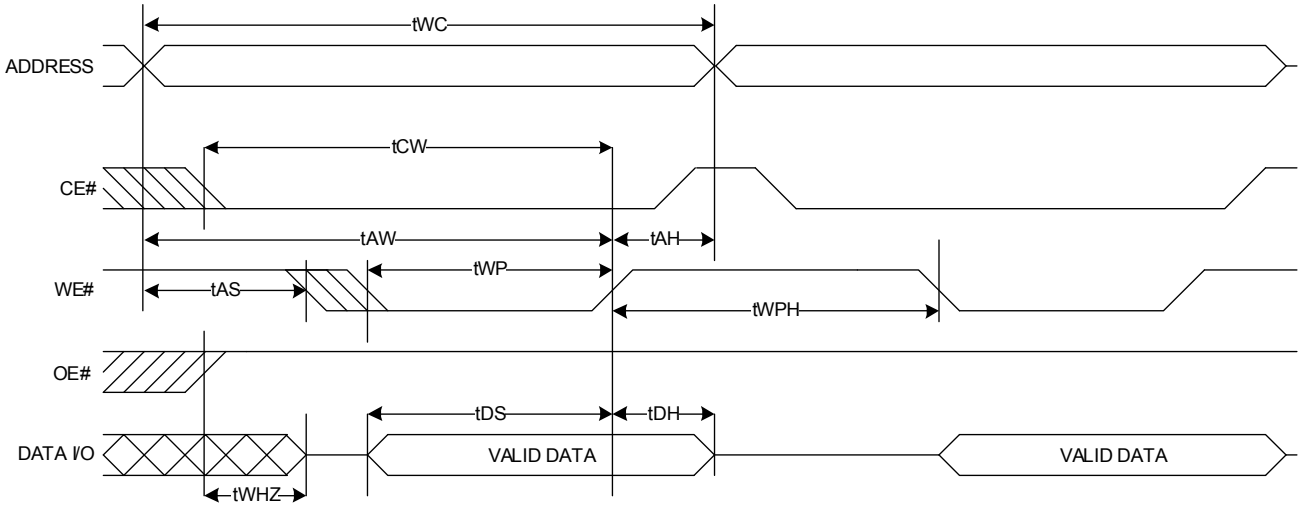


Note

10. Errata: When Arroyo is configured to use SRAM for P-port interface, OE should be asserted simultaneously with CE. If this is not possible, OE should be asserted prior to CE. Otherwise, data can be dropped when external processor reads the Arroyo through SRAM interface. For more information, see the "Errata" on page 50 and "Errata" on page 51.

Figure 13. Non Multiplexing Asynchronous SRAM Write Timing (WE# and CE# Controlled)

Write Cycle 1 WE# Controlled, OE# High During Write



Write Cycle 2 CE# Controlled, OE# High During Write

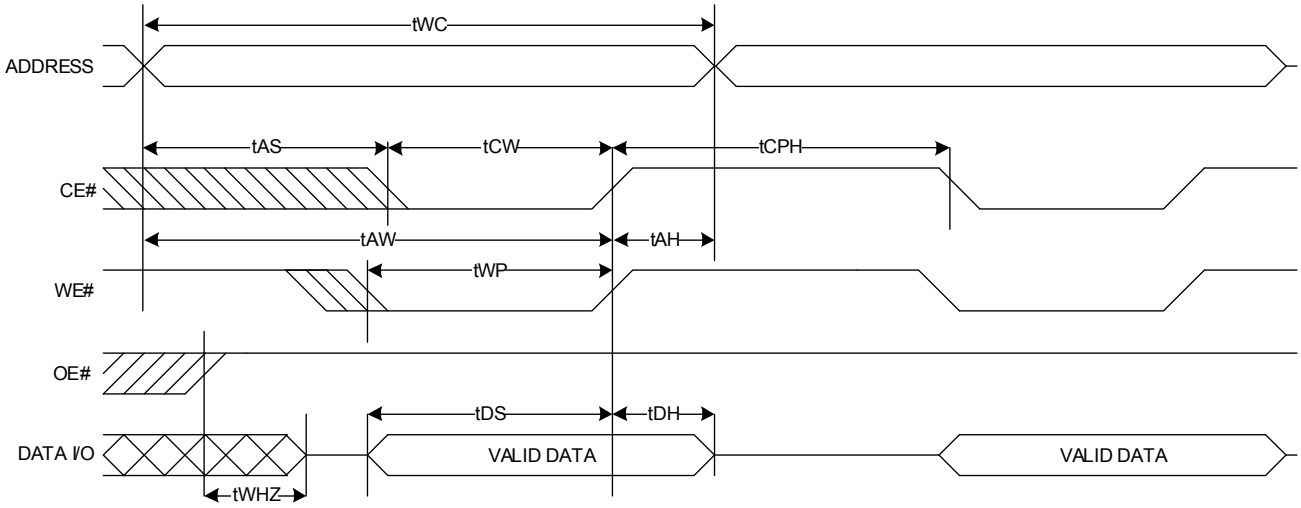
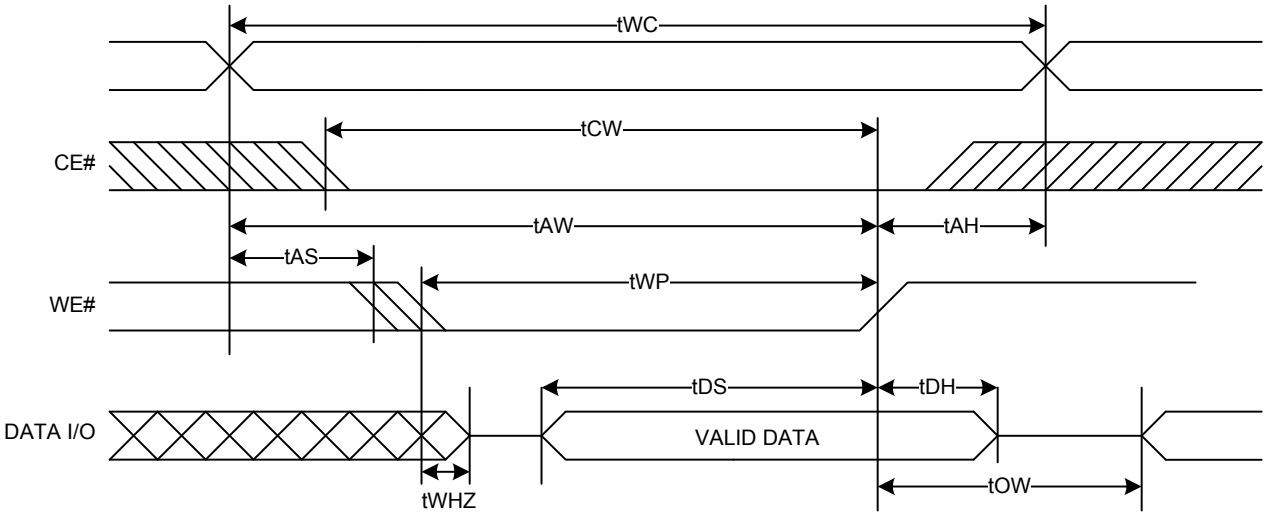


Figure 14. Non Multiplexing Asynchronous SRAM Write Timing (WE# Controlled, OE# LOW)

Write Cycle 3 WE# Controlled. OE# Low



Pseudo NAND (PNAND) Mode

Table 11. PNAND Mode Parameters

Parameter	Description		Min	Max	Unit
t_{ADL}	Address to Data Loading Time	Non LNA Mode Register Write	100	–	ns
		Non LNA Mode EP Write	100	–	ns
		LNA Mode	450	–	ns
t_{ALH}	ALE Hold Time		5	–	ns
t_{ALS}	ALE Setup Time		15	–	ns
t_{AR}	ALE to RE# Delay		10	–	ns
t_{BERS}	Block Erase Time		MCU/S-Port NAND dependent		
t_{CEA}	CE# Access Time		–	35	ns
t_{CH}	CE# Hold Time		5	–	ns
t_{CHZ}	CE# HIGH to O/P HI-Z		–	40	ns
t_{CLH}	CLE Hold Time		5	–	ns
t_{CLR}	CLE to RE# Time		10	–	ns
t_{CLS}	CLE Setup Time		15	–	ns
t_{CS}	CE# Setup Time		20	–	ns
t_{DH}	Data Hold Time		5	–	ns
t_{DS}	Data Setup Time		15	–	ns
t_{OH}	Data Output Hold Time		15	–	ns

Table 11. PNAND Mode Parameters (continued)

Parameter	Description	Min	Max	Unit
t_{PROG}	Program Time for LNA Mode	Depends on MCU/S-Port/NAND		ns
	Program Time for Register Write in Non LNA Mode	130	–	ns
	Program Time for EP Write in Non LNA Mode	130	–	ns
t_R	Busy Duration during Non LNA Register Read using Page Read	130	–	ns
	Busy Duration during Non LNA EP Read using Page Read	130	–	ns
	Busy Duration during LNA Page Read (SBD/SLD)	Depends on MCU/S-Port/NAND		ns
t_{RC}	Read Cycle Time (VFBGA Package)	30	–	ns
	Read Cycle Time (WLCSP Package)	33	–	
t_{REA}	RE# for Register Access Time	–	30	ns
	RE# for EP Access Time	–	30	ns
t_{REH}	RE# HIGH Hold Time	10	–	ns
t_{RHW}	RE# HIGH to WE LOW	40	–	ns
t_{RHZ}	RE# HIGH to Output HI-Z	–	40	ns
t_{RP}	RE# Pulse Width	15	–	ns
t_{RR}	Ready to RE LOW	20	–	ns
t_{RST}	Device Reset Time	Depends on MCU/S-Port/NAND		ns
t_{WB}	WE# HIGH to Busy	–	100	ns
t_{WC}	Write Cycle Time (VFBGA Package)	30	–	ns
	Write Cycle Time (WLCSP Package)	33	–	
t_{WH}	WE# HIGH Hold Time	10	–	ns
t_{WHR}	WE# HIGH to RE LOW in Non LNA Mode	30	–	ns
	WE# HIGH to RE LOW in LNA Mode	450	–	ns
t_{WP}	WE# Pulse Width	15	–	ns

Figure 15. PNAND Mode Command Latch Cycle

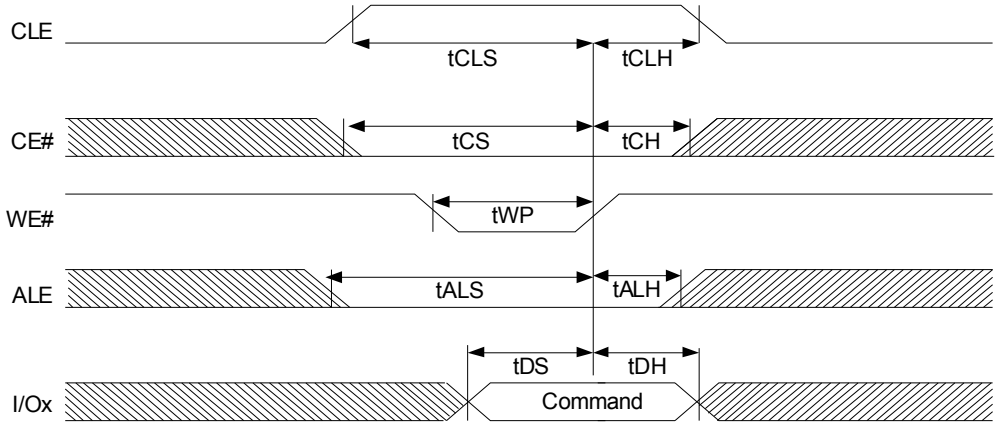


Figure 16. PNAND Mode Address Latch Cycle

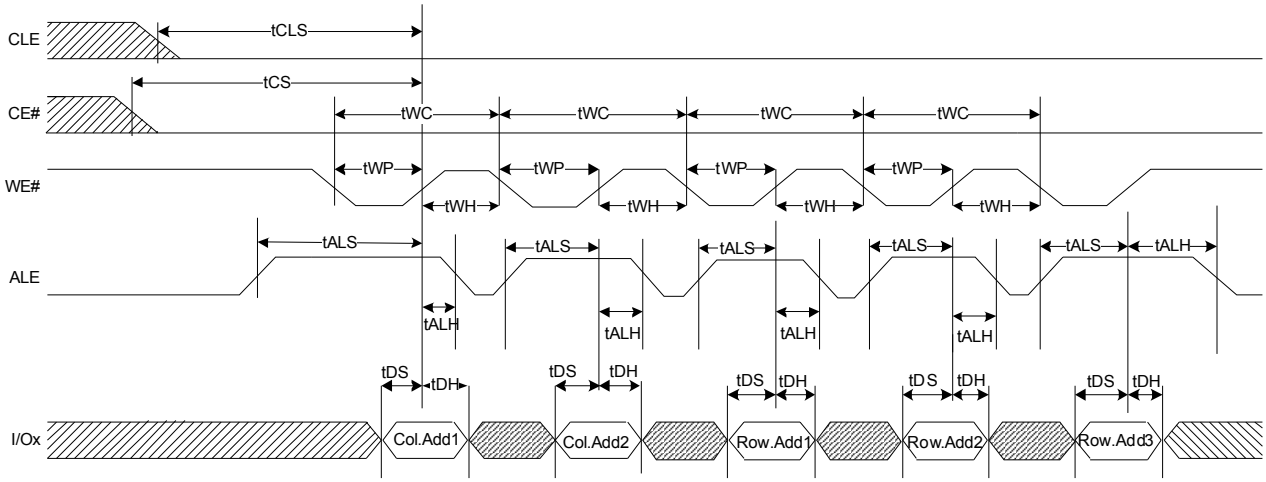


Figure 17. PNAND Mode Input Data Latch Cycle

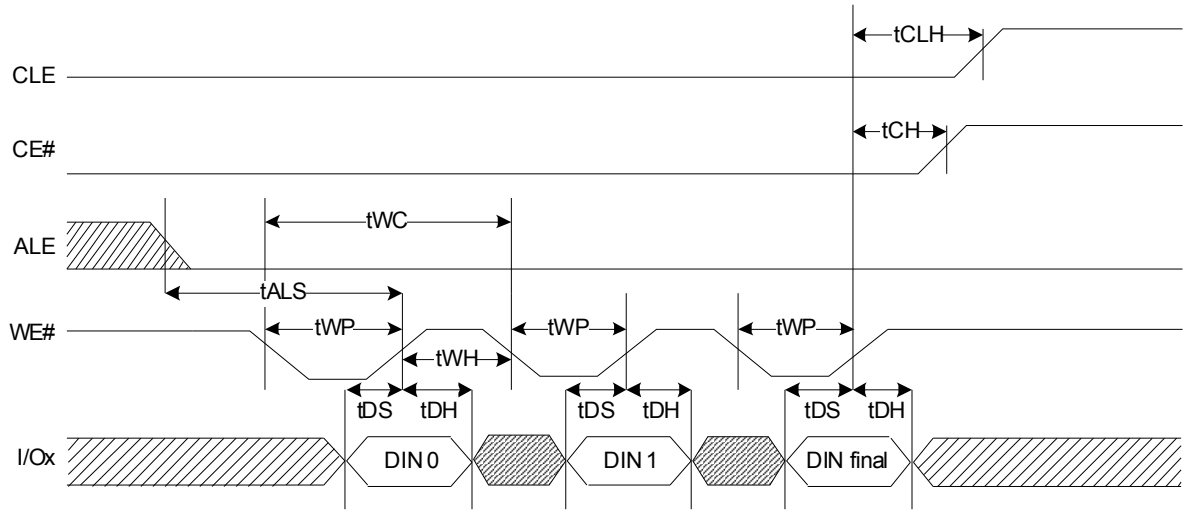


Figure 18. PNAND Mode Serial Access Cycle After Read

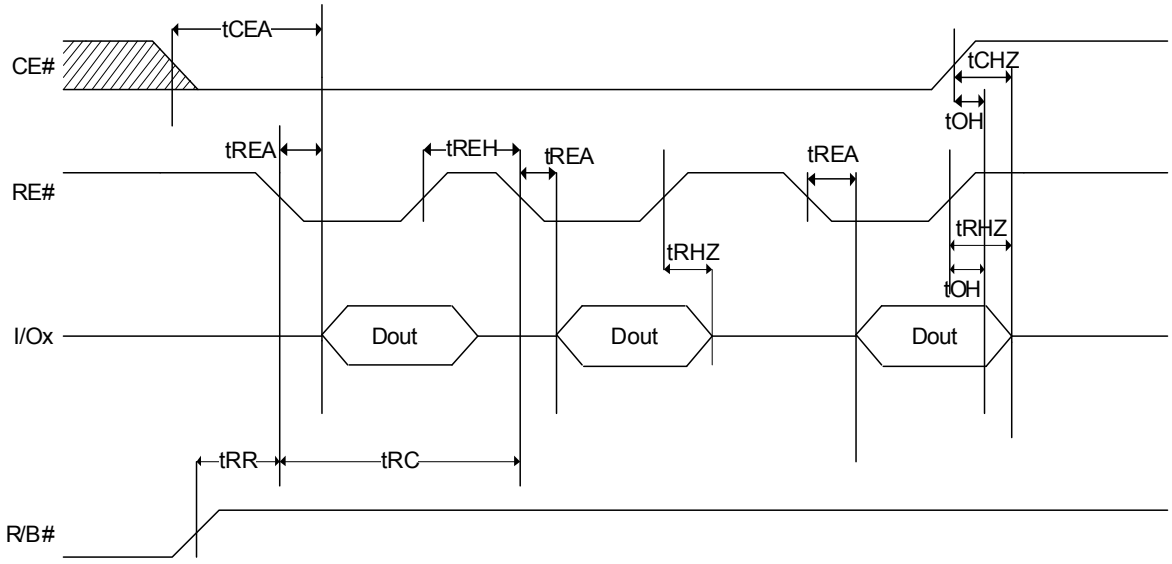


Figure 19. PNAND Mode Status Read Cycle

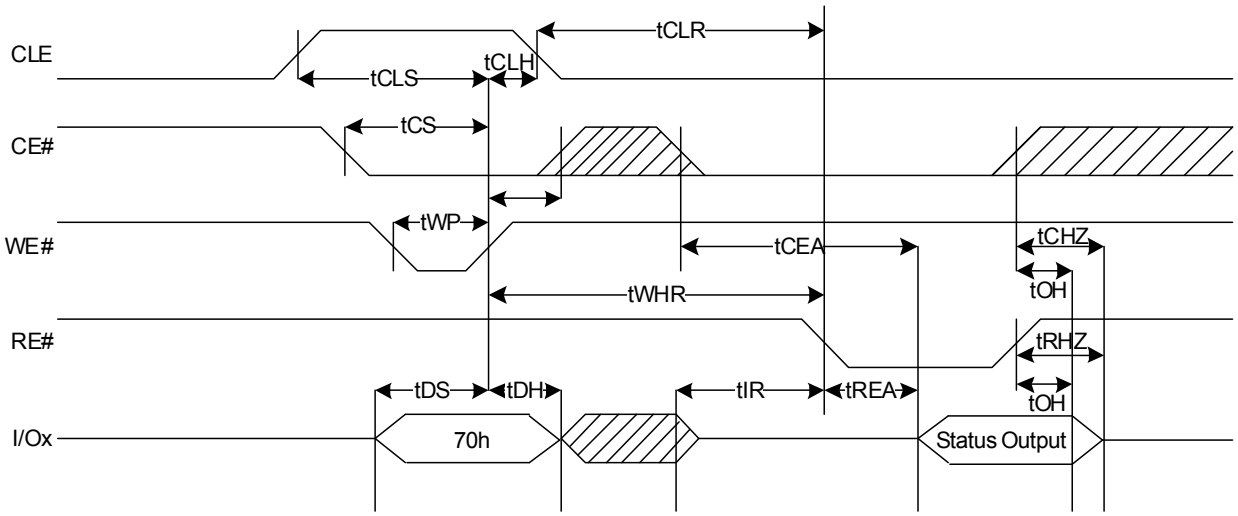


Figure 20. PNAND LBD Read Operation

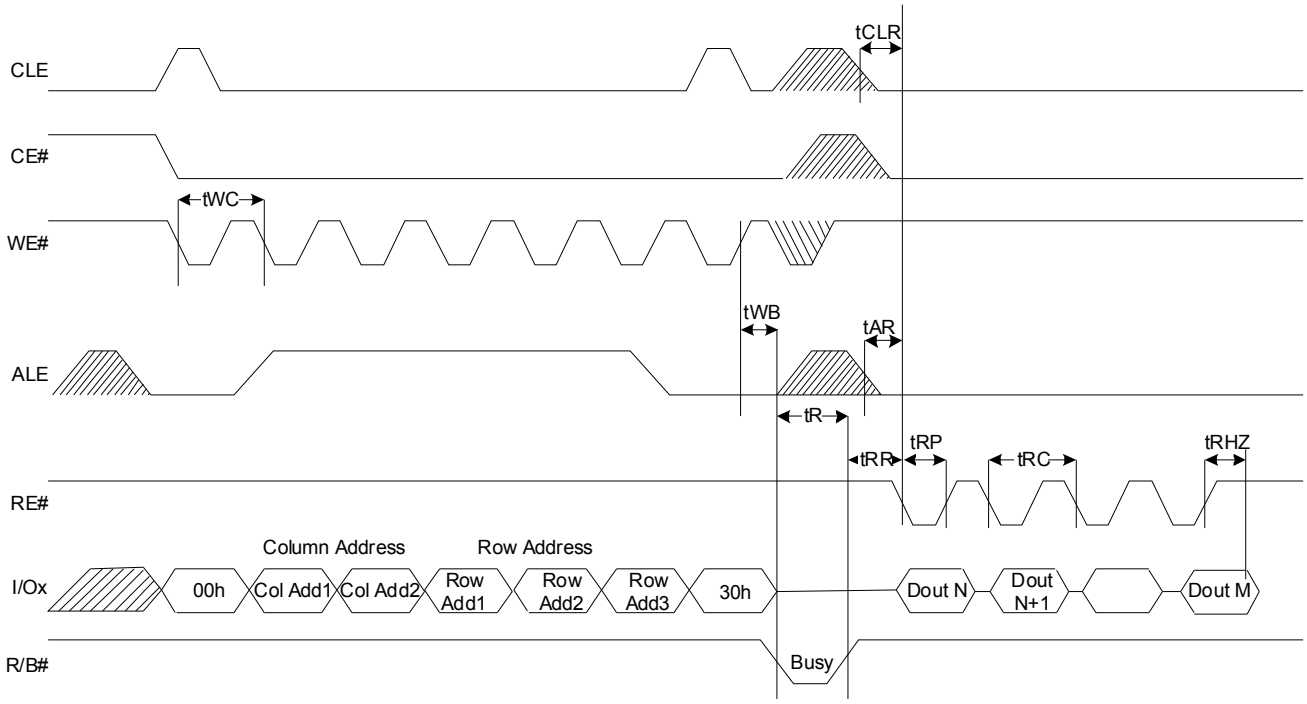
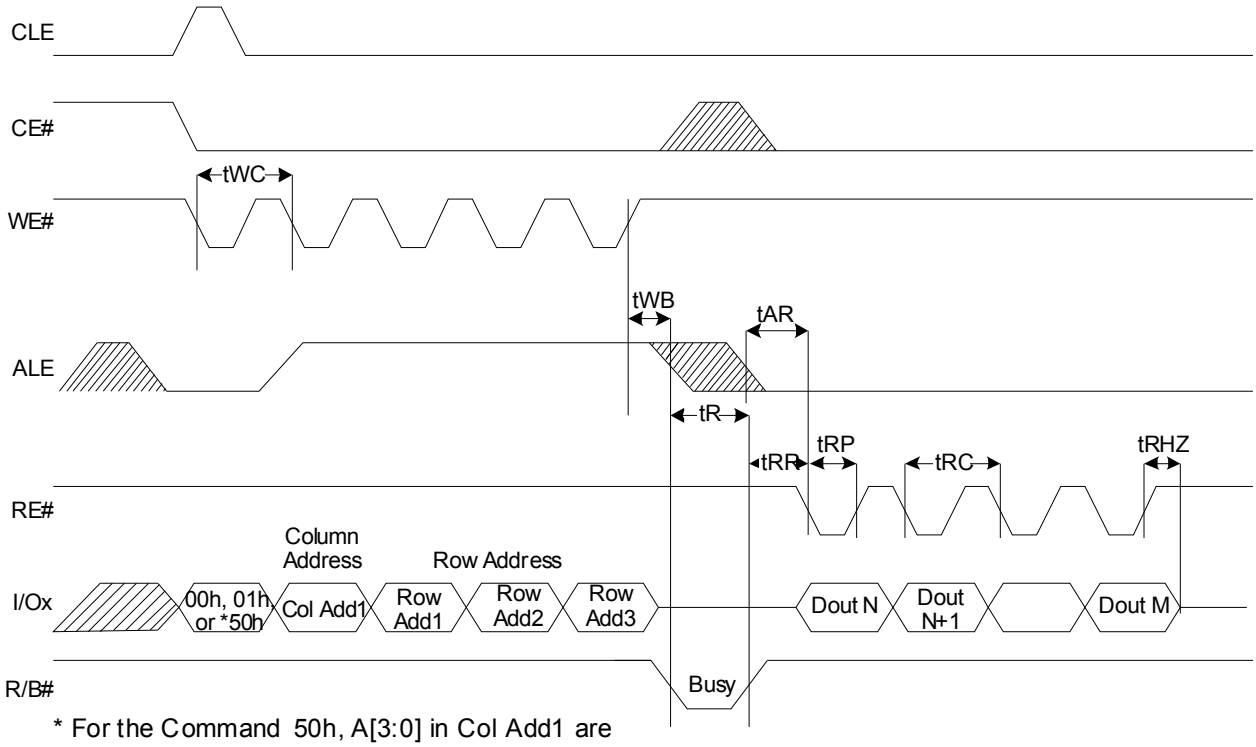


Figure 21. PNAND SBD Read Operation



* For the Command 50h, A[3:0] in Col Add1 are valid address and A [7:4] are Don't care

Figure 22. PNAND Mode LBD Random Data Operation (CASDO)

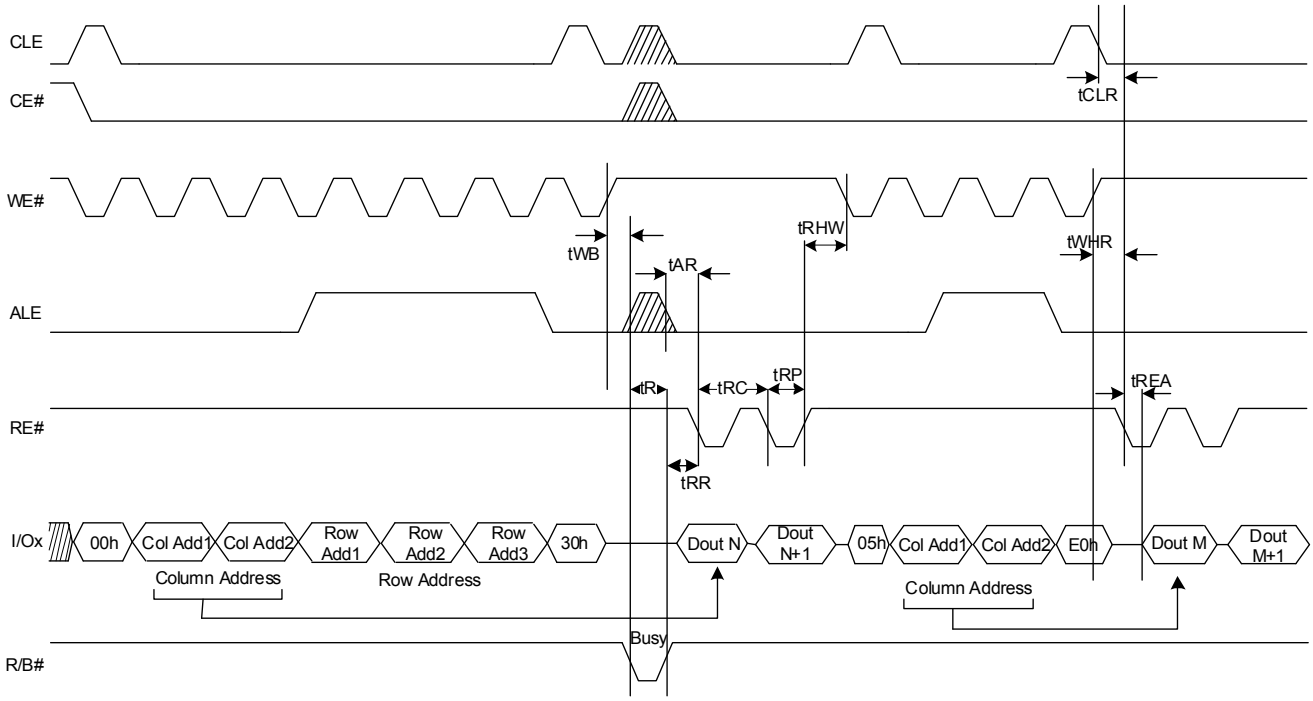
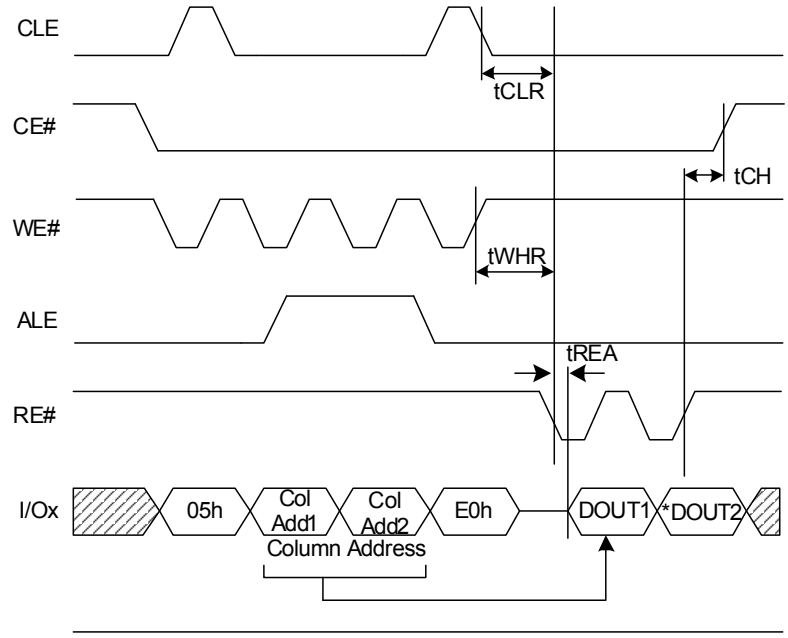


Figure 23. PNAND Mode Register Read Using CASDO in 8-Bit Mode



* This timing diagram shows the 8-bit register read. For 16-bit register read, DOUT2 is not available

Figure 24. PNAND Mode LBD Read Operation (With CE# Don't Care)

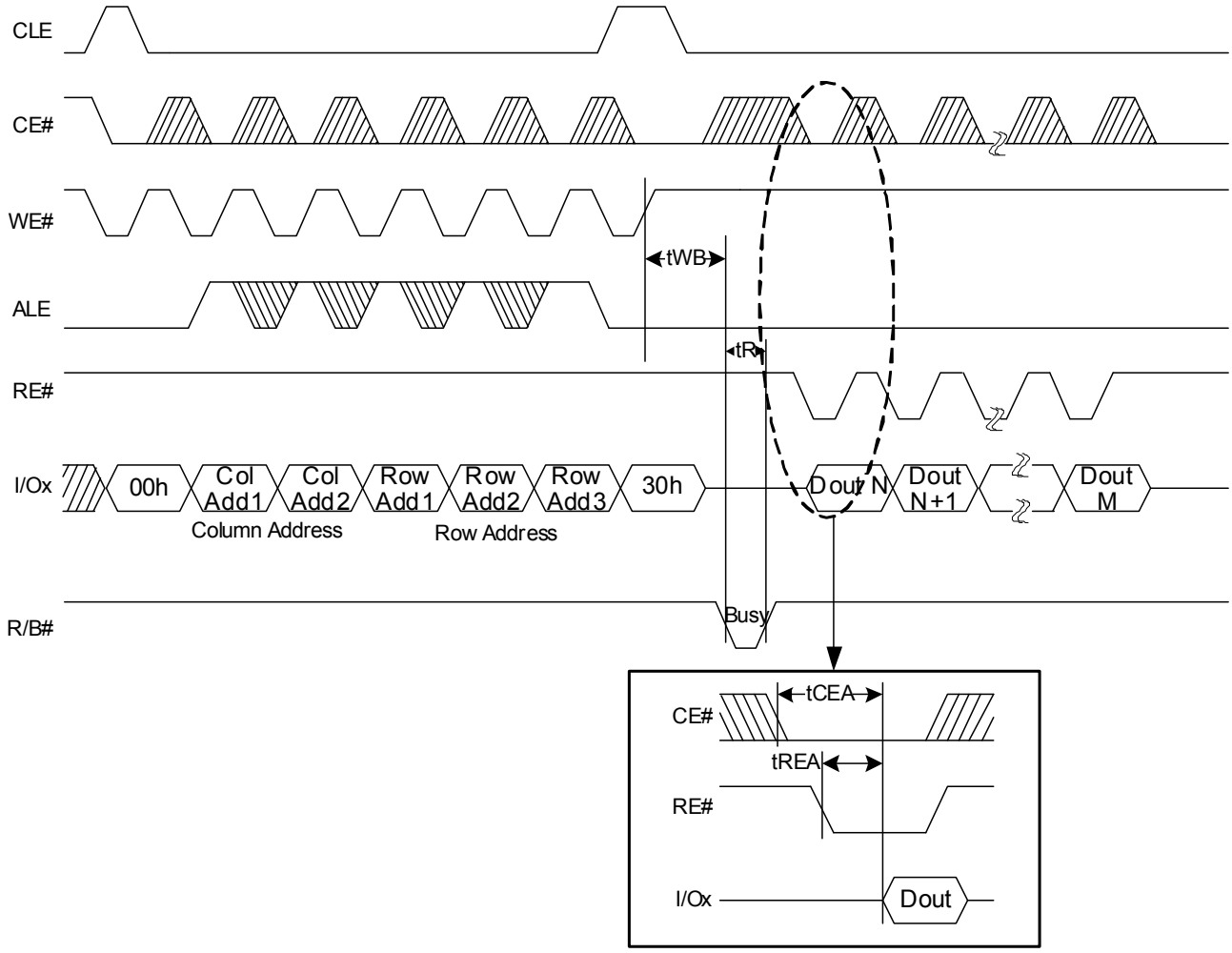


Figure 25. PNAND Mode SBD Read Operation (With CE# Don't Care)

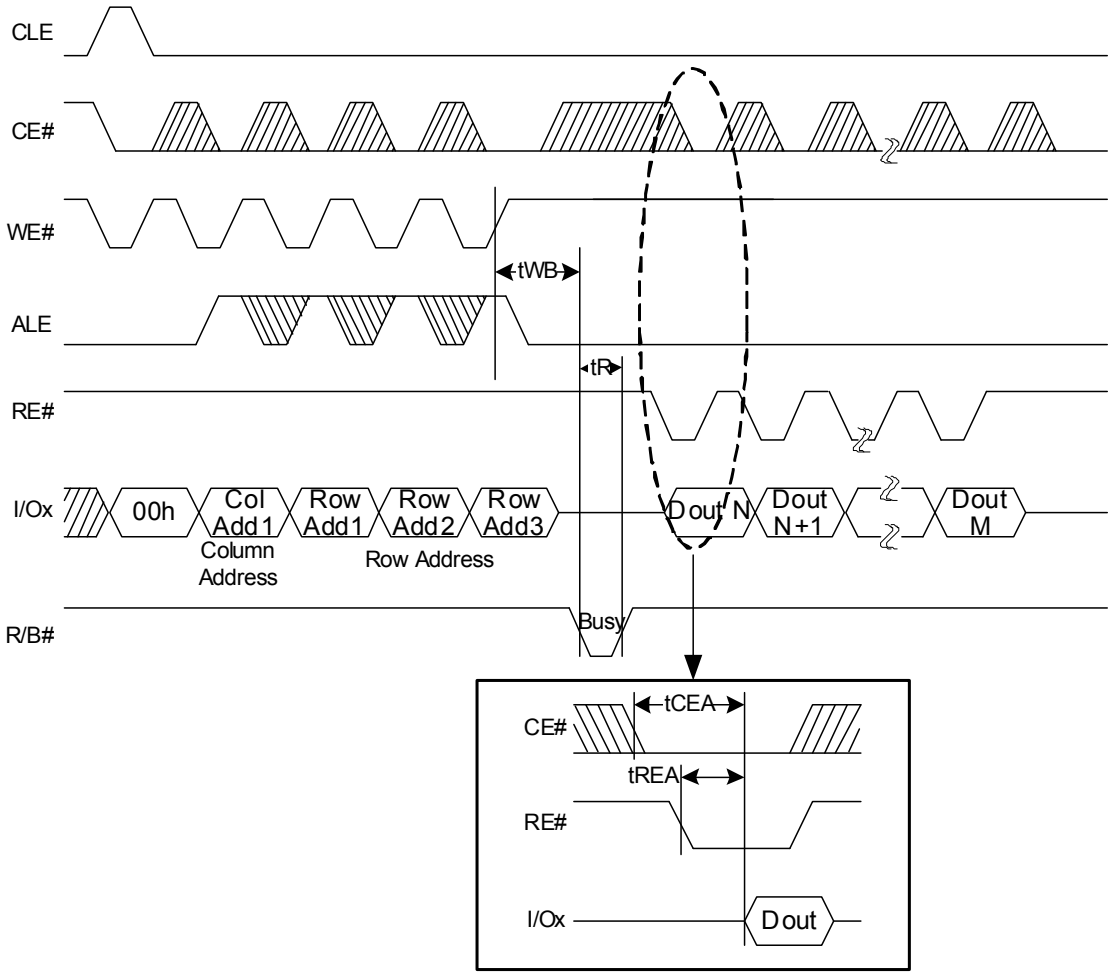
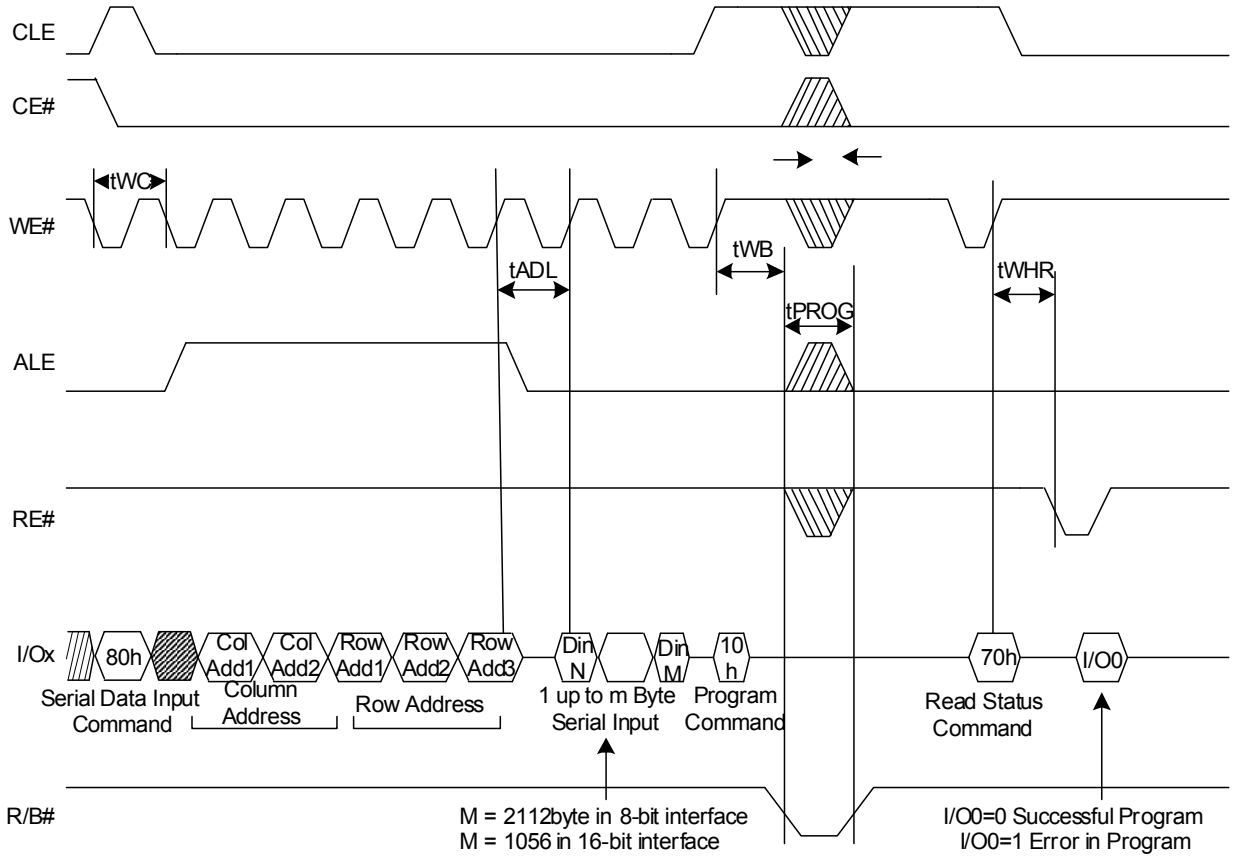


Figure 26. PNAND Mode LBD Page Program Operation



Note: tADL is the time from WE rising edge of final address cycle to the WE rising edge of first data cycle

Figure 27. PNAND Mode SBD Page Program Operation

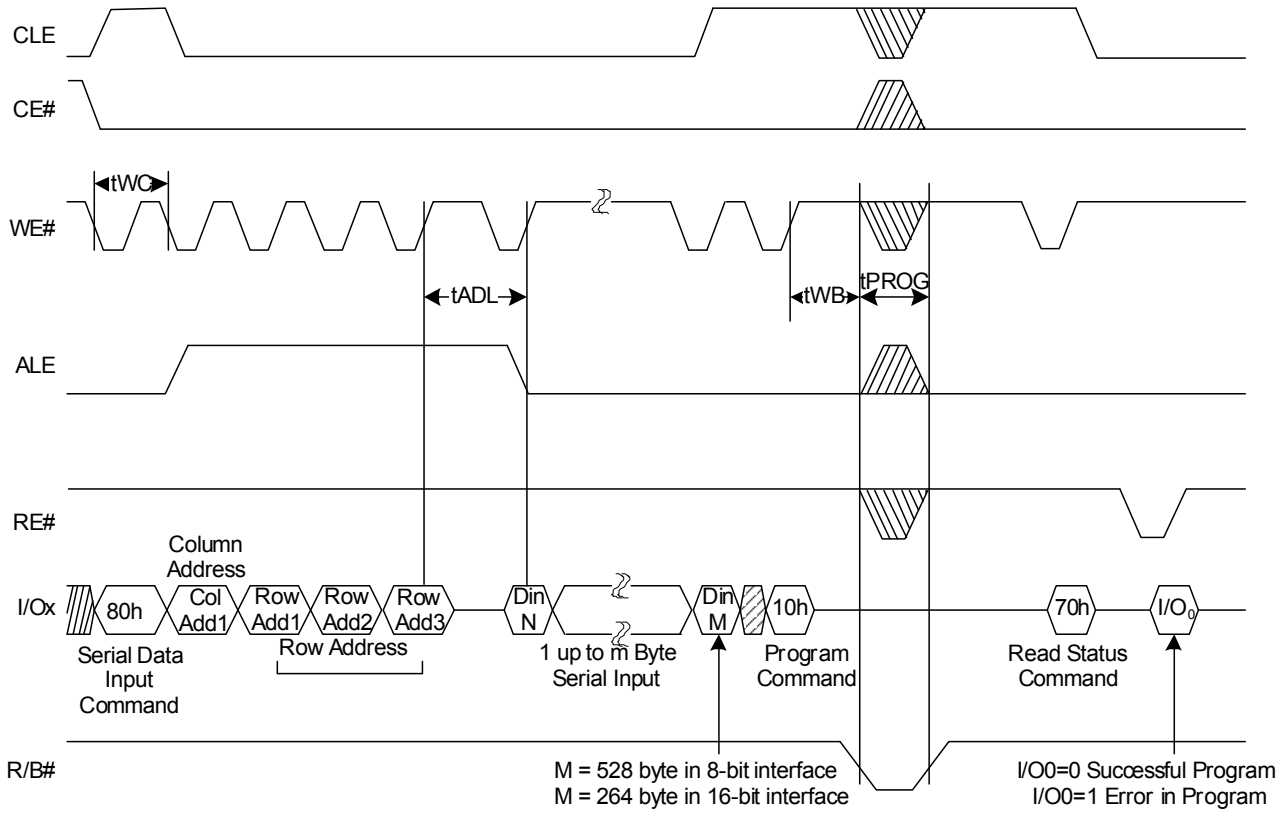
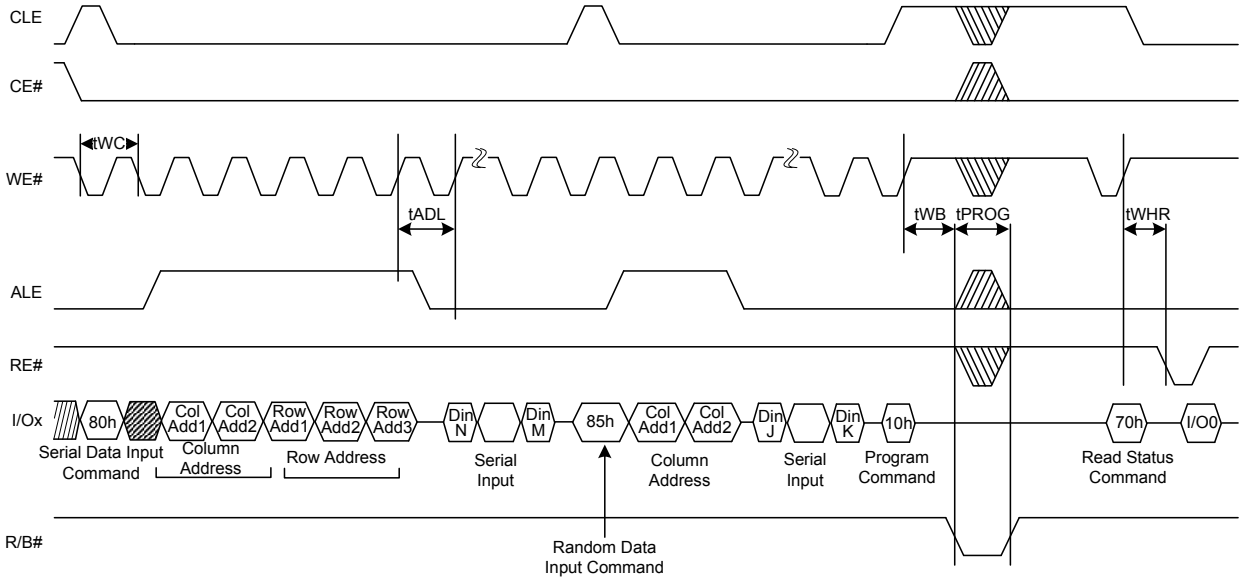
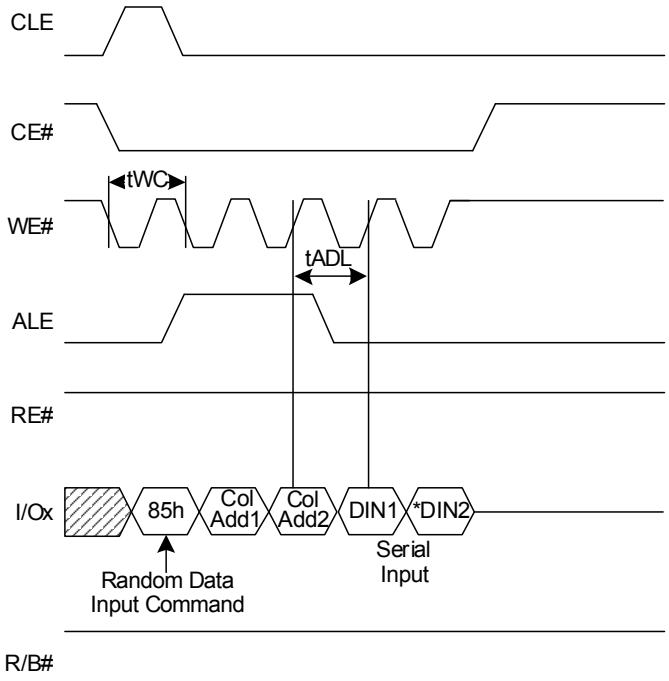


Figure 28. PNAND Mode LBD Page Program Operation with Random Data Input (CASDI)



*Random Programming (CASDI) to endpoint is only supported during logical NAND emulation (LNA mode) of LBD device. Partial page programming is not supported

Figure 29. PNAND Mode Register Write Using CASDI in 8-Bit Mode



* This timing diagram shows the 8-bit register write. For 16-bit register write, DIN2 should not be available

Figure 30. PNAND Mode LBD Page Program Operation (With CE# Don't Care)

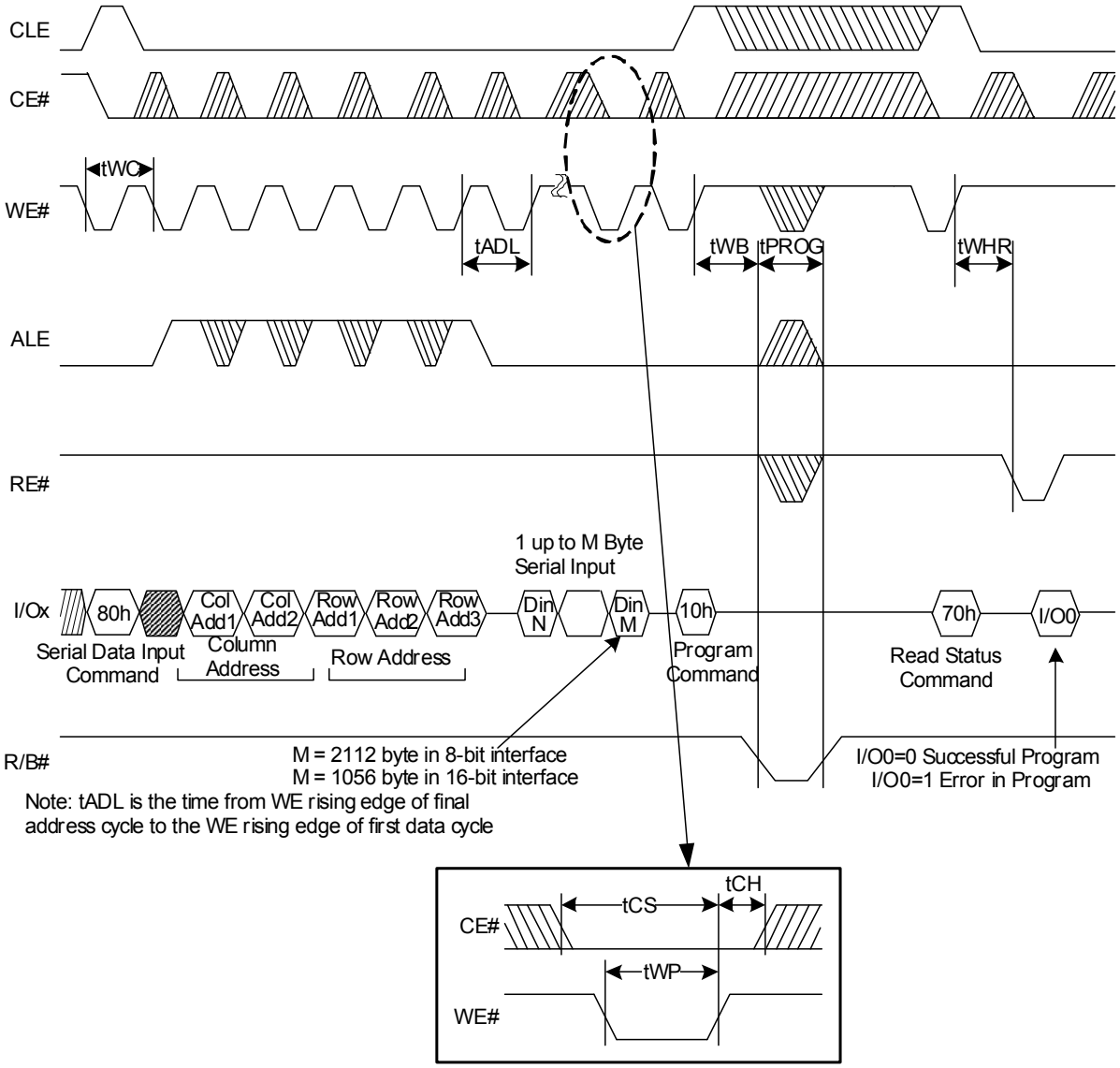


Figure 31. PNAND Mode SBD Page Program Operation (With CE# Don't Care)

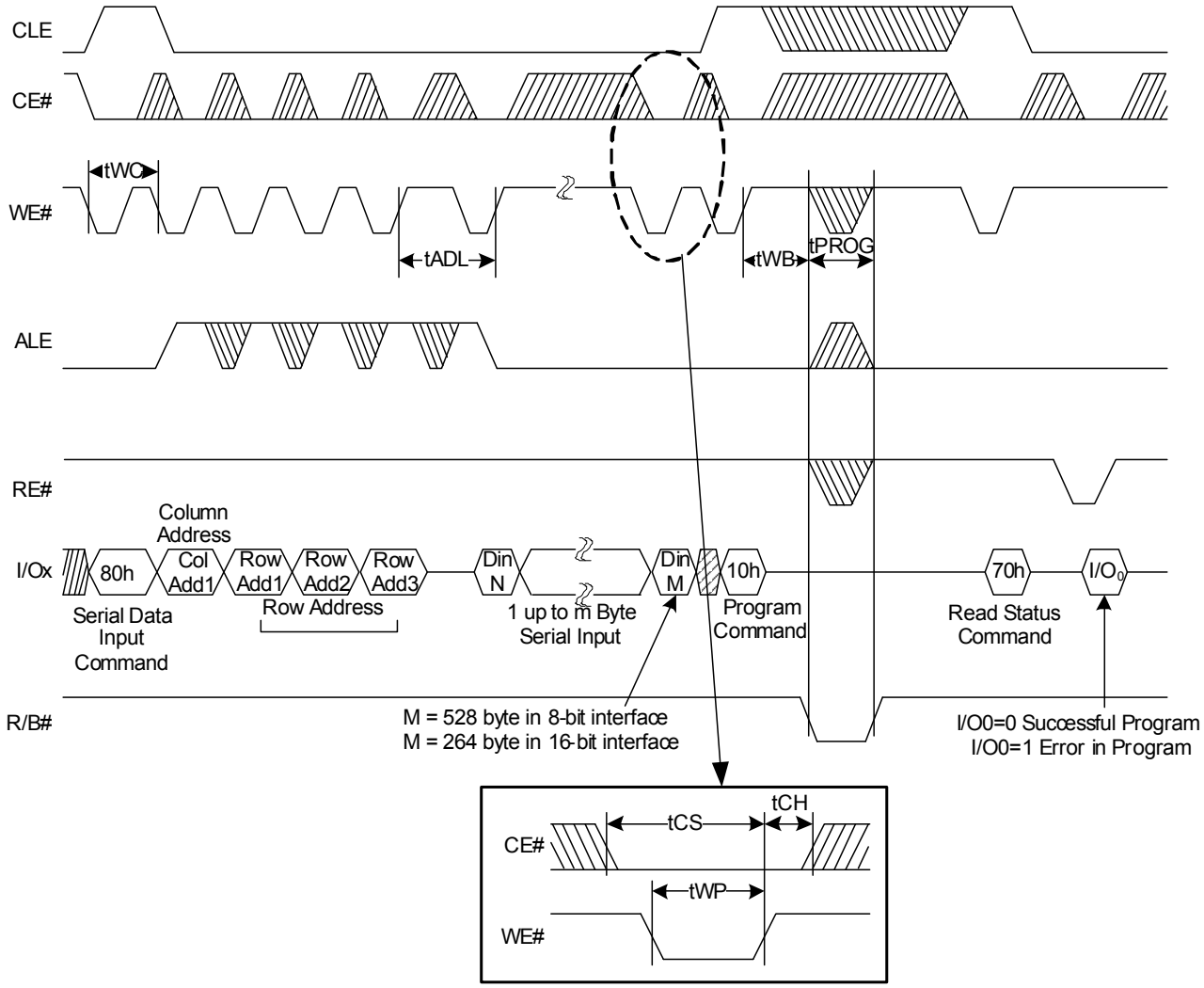


Figure 32. PNAND Mode Block Erase Operation

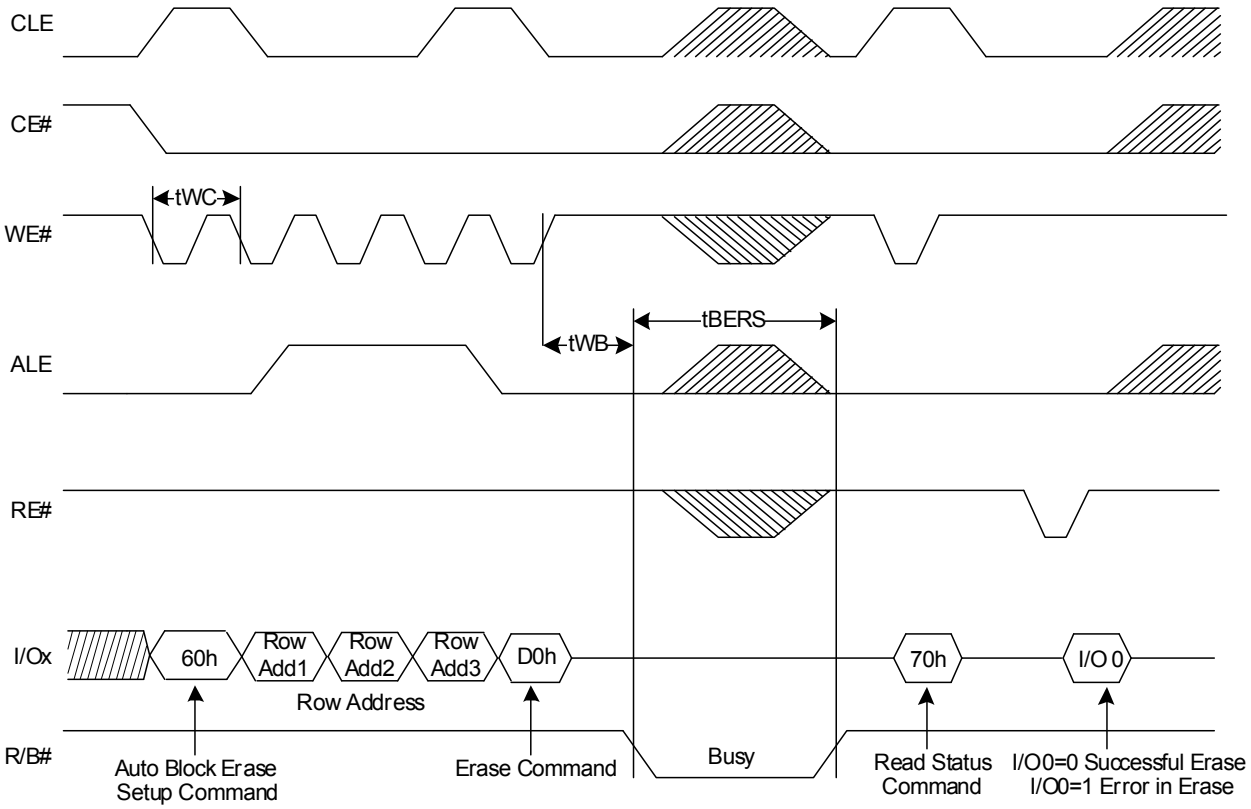
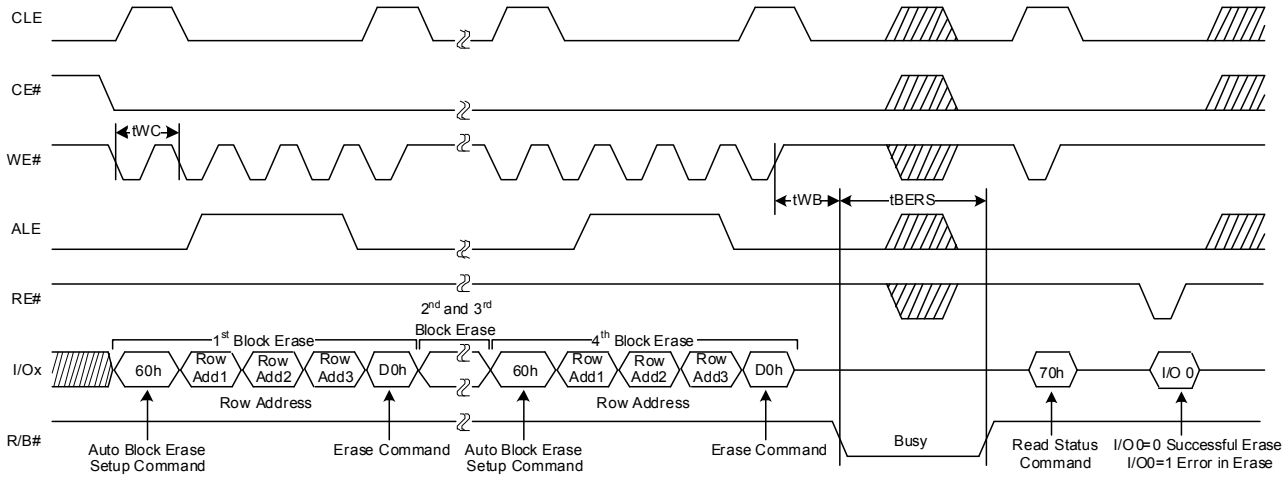
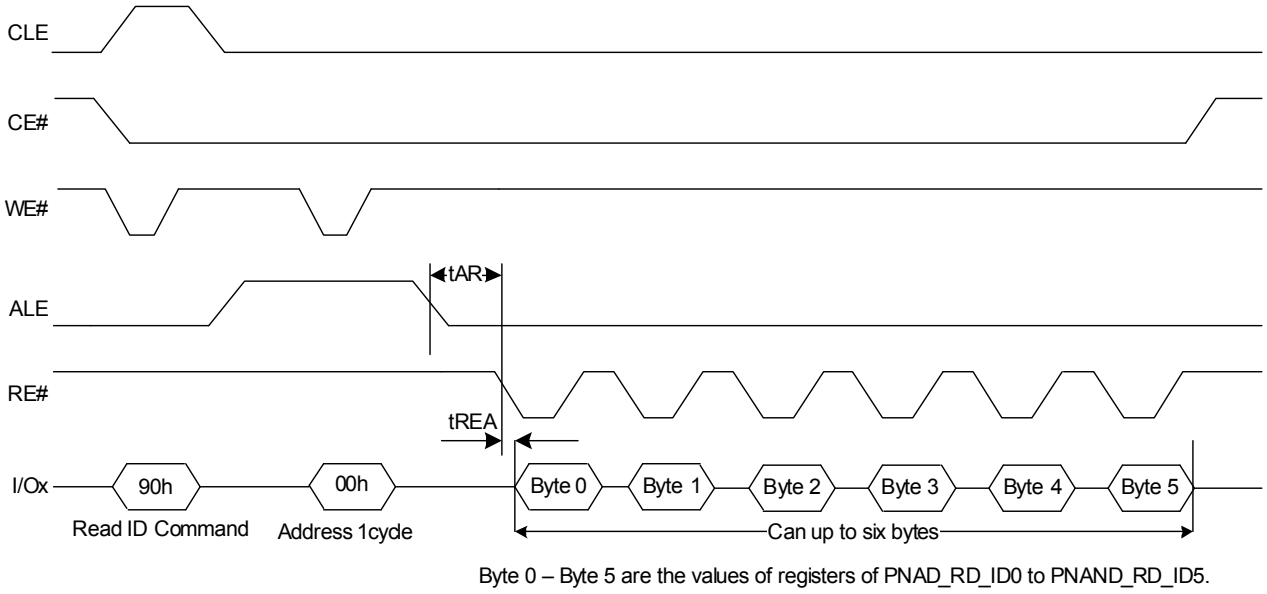


Figure 33. PNAND Mode Multi-Blocks (up to 4) Erase



Note: The multi-block erase can support up to 4 blocks erase

Figure 34. PNAND Mode Read ID Operation



Byte 0 – Byte 5 are the values of registers of PNAD_RD_ID0 to PNAND_RD_ID5.

Figure 35. PNAND Mode Read ID2 Operation

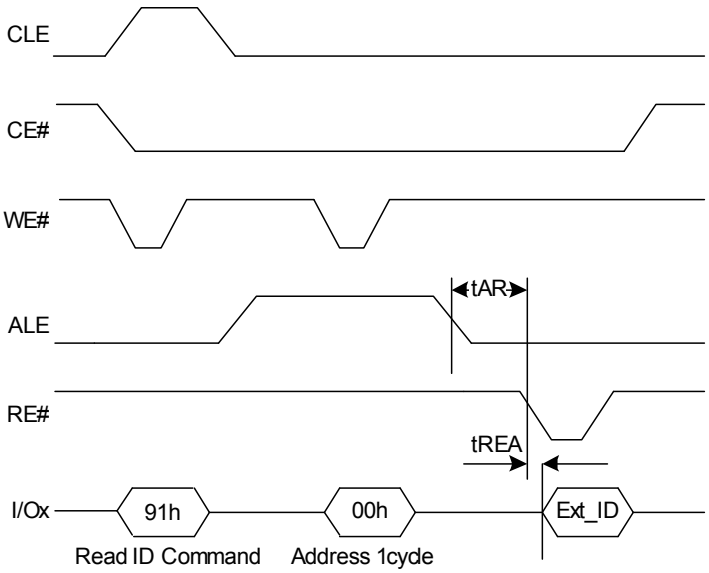


Figure 36. PNAND Mode Reset Operation

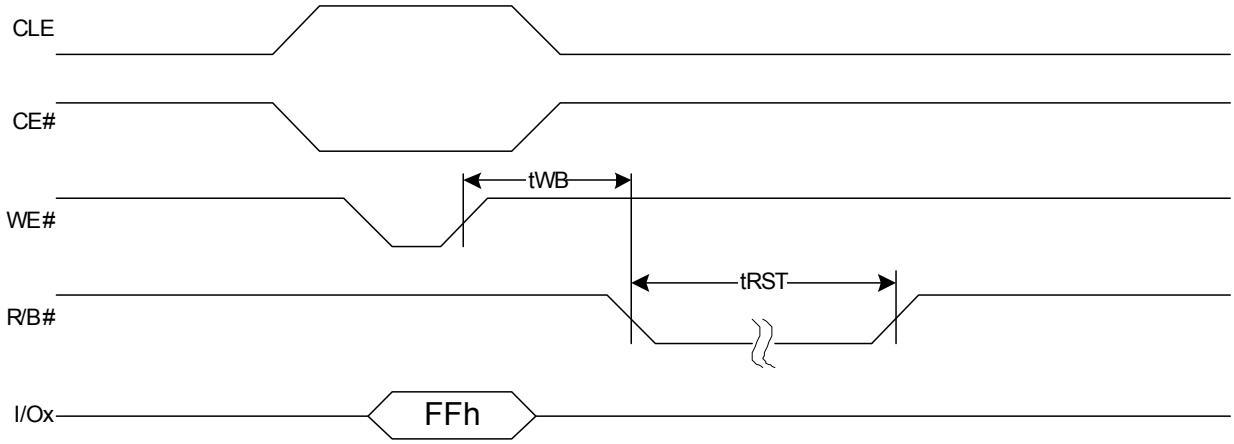
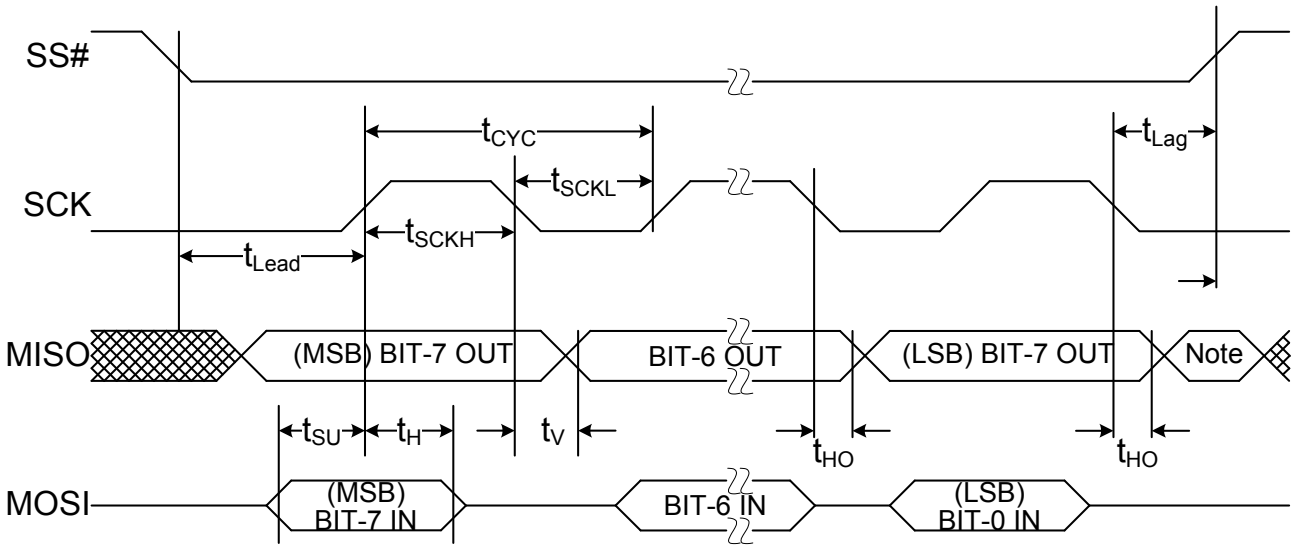


Table 12. SPI Mode Parameters

Parameter	Description	Min	Max	Units
f_{OP}	Operating frequency	0	26	MHz
t_{CYC}	Cycle time	38.5	–	ns
t_{Lead}	Enable lead time	19.23	–	ns
t_{Lag}	Enable lag time	19.23	–	ns
t_{SCKH}	Clock high time	17.33	–	ns
t_{SCKL}	Clock low time	17.33	–	ns
t_{SU}	Data setup time (inputs)	–	7	ns
t_{H}	Data hold time (inputs)	–	7	ns
t_{V}	Data valid time, after enable edge	–	18	ns
t_{HO}	Data hold time, after enable edge	0	–	ns

Figure 37. SPI Timing Diagram



Note: Not defined but normal MSB of character just received

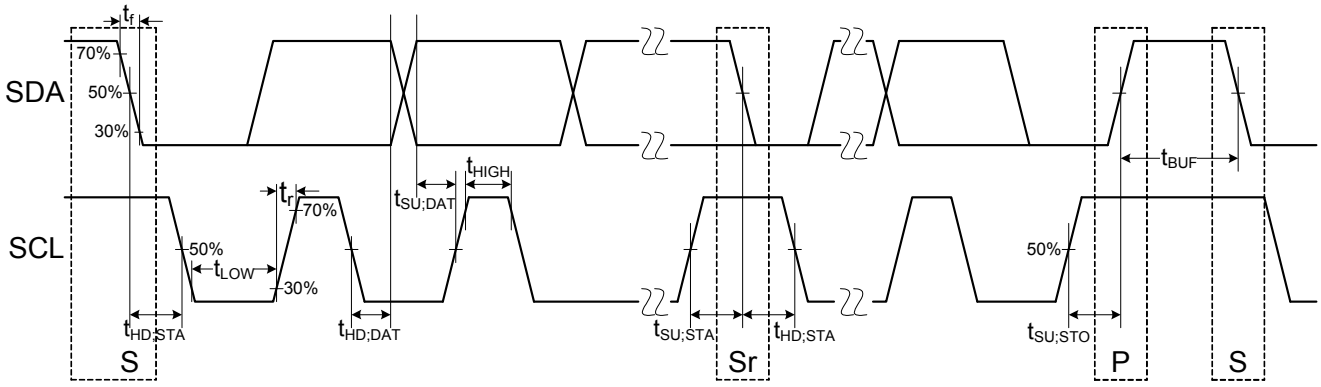
Table 13. PI2C Interface Standard Mode Parameters

Parameter	Description	Min	Max	Units
F	Operating Frequency	0	82	kHz
t_{BUF}	Bus Free Time (between stop and start conditions)	4.7	–	µs
$t_{HD:STA}$	Hold Time After (Repeated) Start Condition. After this period the first clock is generated	4.0	–	µs
$t_{SU:STA}$	Repeated Start Condition Setup Time	4.7	–	µs
$t_{SU:STO}$	Stop Condition Setup Time	4.0	–	µs
$t_{HD:DAT}$	Data Hold Time	0	–	ns
$t_{SU:DAT}$	Data Setup Time	250	–	ns
$t_{TIMEOUT}$	Detect Clock Low Timeout	NA		ms
t_{LOW}	Clock Low Period	4.7	–	µs
t_{HIGH}	Clock High Period	4.0	–	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time (slave device)	NA		ms
t_r	Rise Time	–	1000	ns
t_f	Fall Time	–	300	ns

Table 14. PI2C Interface Fast Mode Parameters

Parameter	Description	Min	Max	Units
F	Operating Frequency	0	312	kHz
t_{BUF}	Bus Free Time (between stop and start condition)	1.3	–	µs
$t_{HD:STA}$	Hold Time after (Repeated) Start Condition. After this period the first clock is generated	0.6	–	µs
$t_{SU:STA}$	Repeated Start Condition Setup Time	0.6	–	µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6	–	µs
$t_{HD:DAT}$	Data Hold Time	0	0.9	ns
$t_{SU:DAT}$	Data Setup Time	100	–	ns
$t_{TIMEOUT}$	Detect Clock Low Timeout	NA		ms
t_{LOW}	Clock Low Period	1.3	–	µs
t_{HIGH}	Clock High Period	0.6	–	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time (slave device)	NA		ms
t_r	Rise Time	–	300	ns
t_f	Fall Time	–	300	ns

Figure 38. PI2C Timing Diagram



Other P-Port Timings

DRQ# Min Pulse Width (t_{DPW}): The minimum duration that DRQ# is deasserted following a DRQ acknowledgement (clear of DMAVAL) is 110 ns in Async mode or five P-Port clock (CLK) cycles in Sync mode.

Same Register Write-to-Read Holdoff (t_{WRHO}): A read of a particular register must wait for a holdoff period following a write operation to that same register address to ensure that valid updated data is read. In Async mode, this holdoff time is 150 ns. In Sync mode, this holdoff time is seven P-Port clock (CLK) cycles.

Register Update-to-Read Holdoff (t_{URHO}): Same status registers are updated as side effect from accesses to other registers. For example, clearing the DMAVAL field automatically clears the associated endpoint buffer bit within the DRQ status register. A holdoff time must elapse from the first register access before the update is reflected in a subsequent read operation. This holdoff time is identical to the t_{WRHO}.

S Port Interface AC Timing Parameters

SD/MMC/MMC+ Timing Parameters

For all conditions, SD/MMC data is driven and sampled on the rising edge of SD_CLK. Note that CE-ATA electrical and timing parameters are equivalent to MMC.

Figure 39. SD/MMC+ Timing Waveform — All Modes

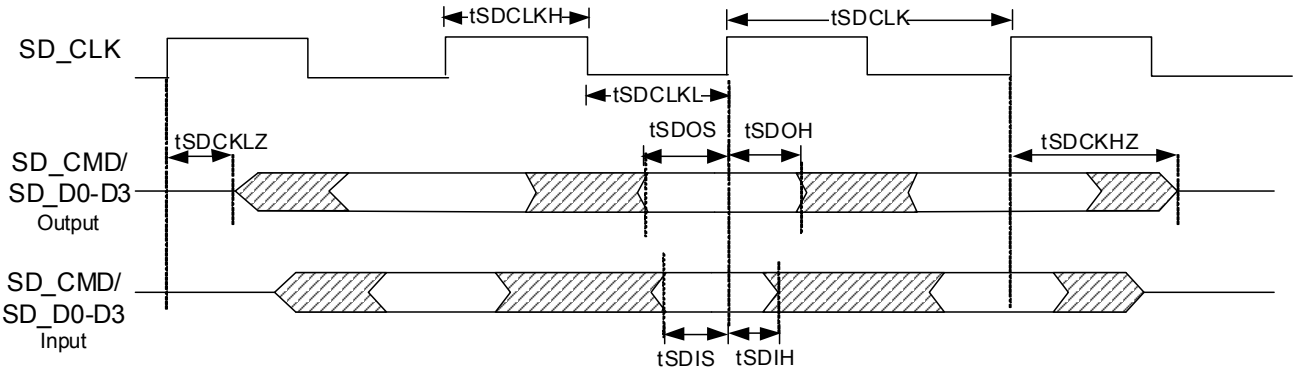


Table 15. Common Timing Parameters for SD/MMC+ – During Identification Mode

Parameter	Description	Min	Max	Units
SDFREQ	SD_CLK Interface Clock Frequency	0	400	kHz
t_{SDCLK}	Clock Period	2.5	–	µs
t_{SDCLKH}	Clock High Time	1.0	–	µs
t_{SDCLKL}	Clock Low Time	1.0	–	µs

Table 16. Common Timing Parameters for SD/MMC+ – During Data Transfer Mode

Parameter	Description	Min	Max	Units
SDFREQ	SD_CLK Interface Clock Frequency	5	48	MHz
t_{SDCLK}	Clock Period	20.8	200	ns
$t_{SDCLKOD}$	Clock Duty Cycle	40	60	%
t_{SCLKR}	Clock Rise Time	–	3	ns
t_{SCLKF}	Clock Fall Time	–	3	ns

Table 17. Timing Parameters for SD – All Modes

Parameter	Description	Min	Max	Units
t_{SDIS}	Input Setup Time	4	–	ns
t_{SDIH}	Input Hold Time	2.5	–	ns
t_{SDOS}	Output Setup Time	7	–	ns
t_{SDOH}	Output Hold Time	6	–	ns
t_{SDCKHZ}	Clock to Data High Z	–	18	ns
t_{SDCKLZ}	Clock to Data Low Z	3	–	ns

Table 18. Timing Parameters for MMC+ – All Modes

Parameter	Description	Min	Max	Units
t_{SDIS}	Input Setup Time	4	–	ns
t_{SDIH}	Input Hold Time	4	–	ns
t_{SDOS}	Output Setup Time	6	–	ns
t_{SDOH}	Output Hold Time	6	–	ns
t_{SDCKHZ}	Clock to Data High Z	–	18	ns
t_{SDCKLZ}	Clock to Data Low Z	3	–	ns

Reset and Standby Timing Parameters

The Arroyo reset mechanism is described in this section. The standby mode is also described.

Sleep Time (t_{SLP}): The maximum time from deassertion of WAKEUP to when Arroyo enters low power state (sleep mode) is 1 ms.

Wakeup Time (t_{WU}): The minimum time from assertion of WAKEUP pin (or initial power on with WAKEUP HIGH) to when any register operation is conducted is 1 ms if an external clock is present, or 5 ms if a crystal is used. The CY_AN_MEM_PWR_MAGT_STAT.WAKEUP field can only be polled after wakeup time following reset deassertion or WAKEUP assertion.

Minimum RESET# pulse width (t_{RPW}): 5 ms when a crystal is used as clock or 1 ms when an external clock is used.

Minimum WAKEUP pulse width (t_{WPW}): 5 ms.

Minimum HIGH on RESET# and WAKEUP (t_{RH}, t_{WH}): The WAKEUP and RESET# pins must be held HIGH for a minimum of 5 ms.

Reset Recovery Time (t_{RR}): A minimum 1 ms reset recovery time must be allowed before Arroyo registers can be accessed for read or write.

Figure 40. Reset and Standby Timing Diagram

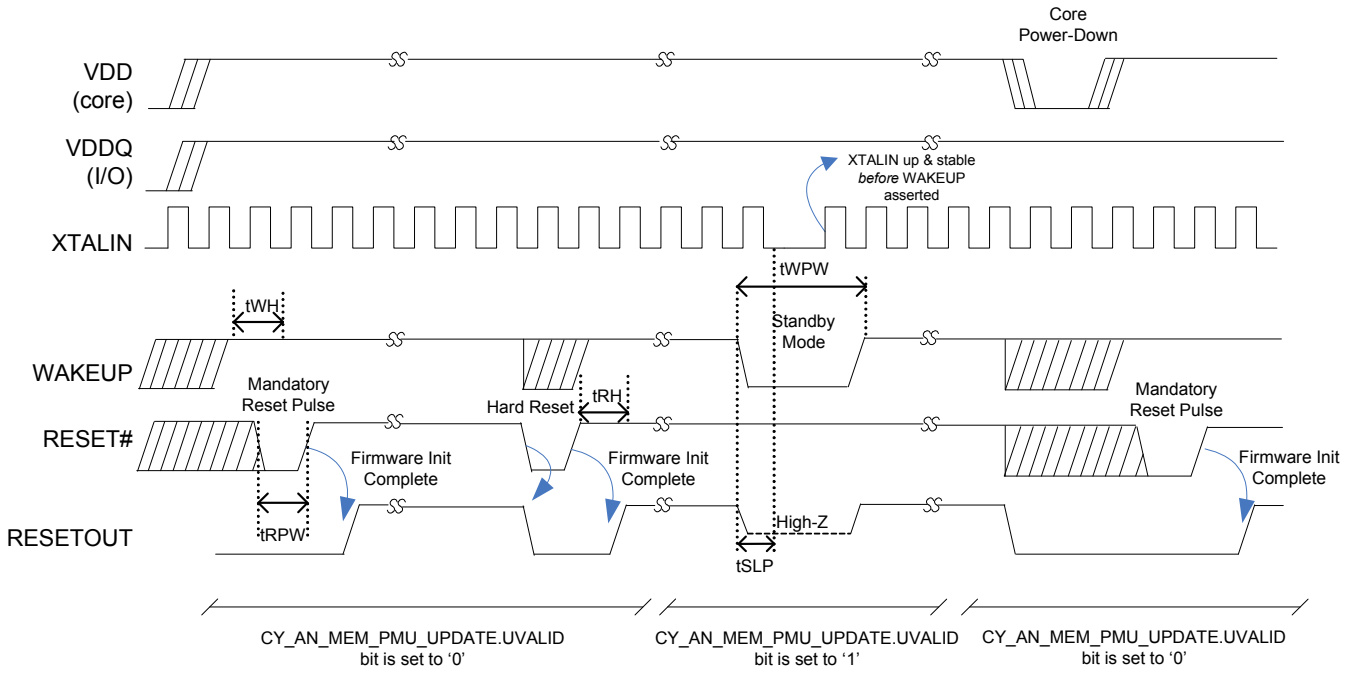
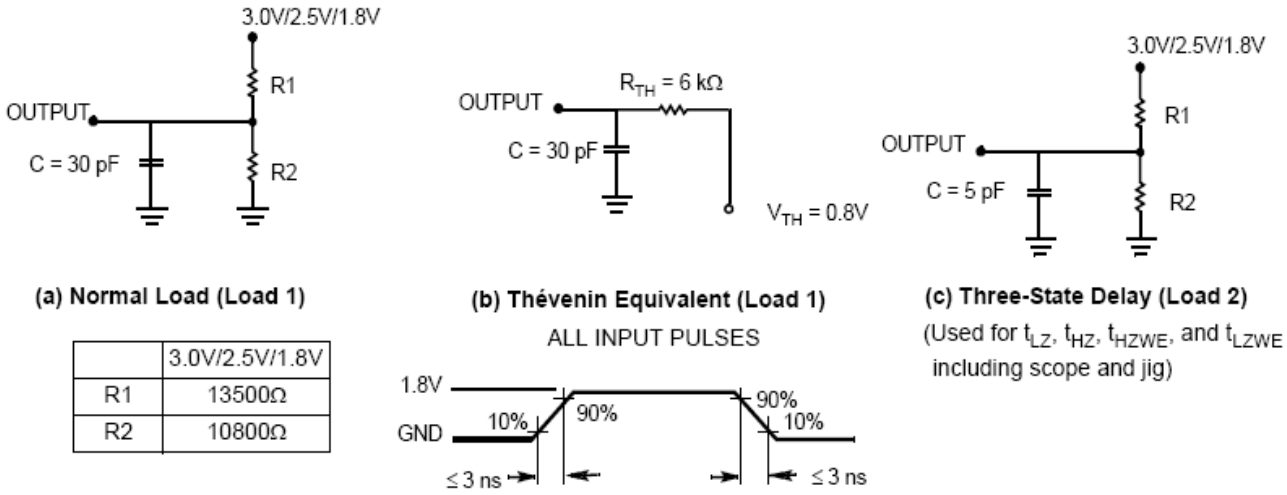


Table 19. Reset and Standby Timing Parameters

Parameter	Description	Conditions	Min	Max	Units
t_{SLP}	Sleep Time		–	1	ms
t_{WU}	Wakeup Time from Standby Mode	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
t_{WH}	WAKEUP High Time		5	–	ms
t_{WPW}	WAKEUP Pulse Width		5	–	ms
t_{RH}	RESET# High Time		5	–	ms
t_{RPW}	RESET# Pulse Width	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
t_{RP}	RESET# Recovery Time		1	–	ms

Figure 41. AC Test Loads and Waveforms (Except SD and MMC, SD and MMC are comply with the SD/MMC specification)



(a) Normal Load (Load 1)

	3.0V/2.5V/1.8V
R1	13500Ω
R2	10800Ω

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 2)

(Used for t_{LZ}, t_{HZ}, t_{HZWE}, and t_{LZWE} including scope and jig)

ALL INPUT PULSES

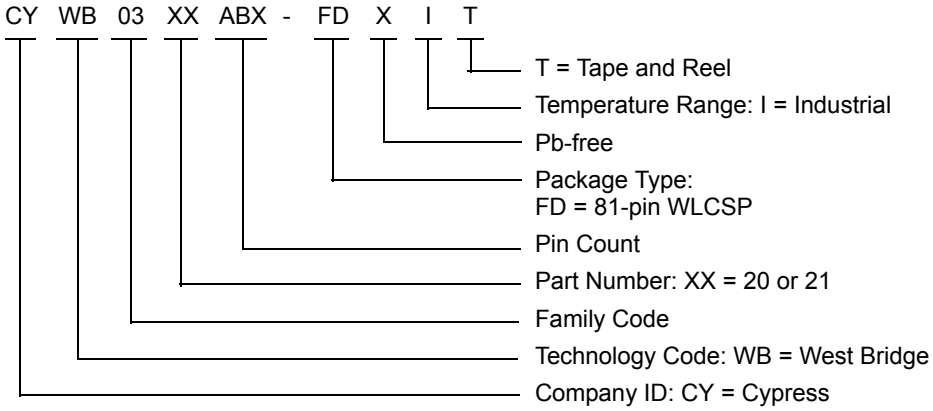
Ordering Information

For ordering information, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 20. Device Ordering Information

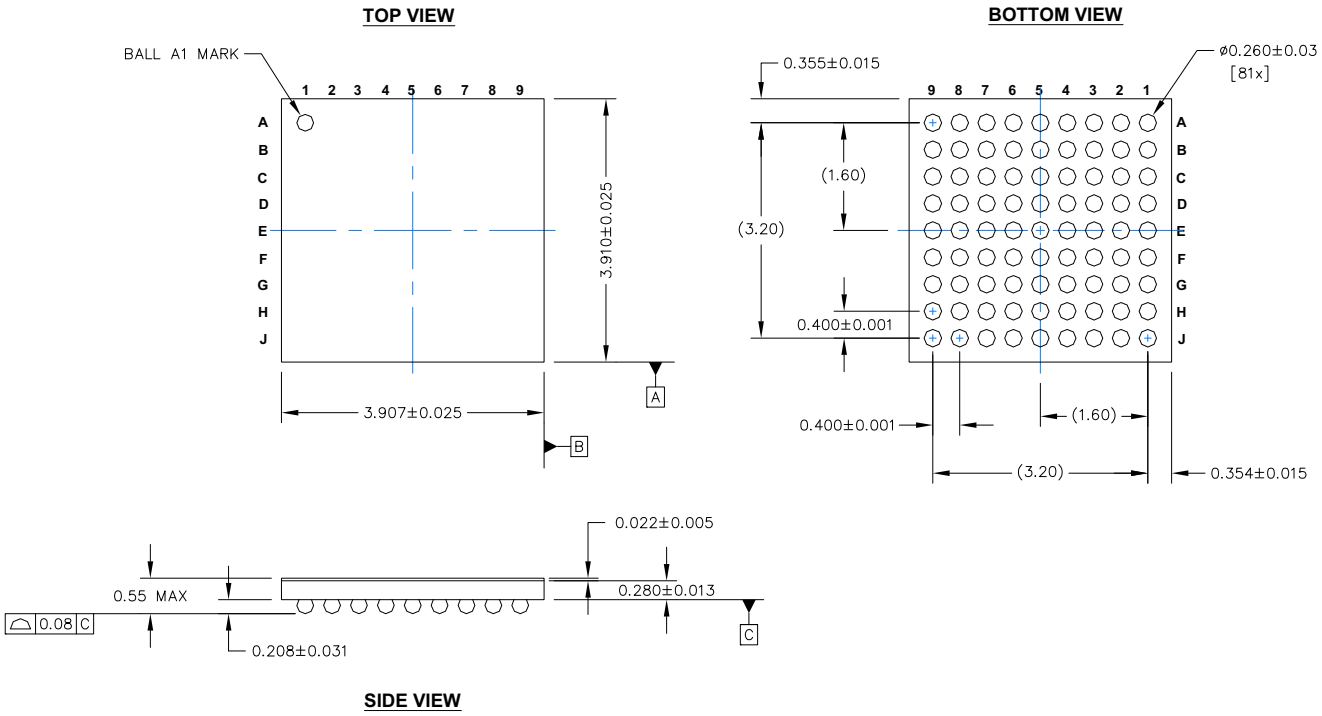
Ordering Code	Package Type	Clock Input Frequencies (MHz)	Status
CYWB0320ABX-FDXIT	81-pin WLCSP (Pb-free)	26	Production Release
CYWB0321ABX-FDXIT	81-pin WLCSP (Pb-free)	19.2, 26	Sample

Ordering Code Definitions



Package Diagram

Figure 42. Astoria 81-pin WLCSP (3.91 × 3.91 × 0.55 mm) FN81B Package Outline, 001-45618



NOTES:

1. ALL DIMENSION ARE IN MM
2. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web
3. JEDEC – Publication 95; Design Guide 4.18

001-45618 *C

Acronyms

Acronym	Description
CE	Chip Enable
ESD	Electrostatic Discharge
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
OE	Output Enable
RE	Read Enable
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
WE	Write Enable
WLCSP	Wafer Level Chip Scale Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
mA	milliampere
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
µW	microwatt
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
ppm	parts per million
pF	picofarad
V	volt
W	watt

Errata

This section describes the errata for West Bridge Arroyo USB and Mass Storage Peripheral Controller, CYWB0320ABX-FDXI. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Package Type	Operating Range
CYWB0320ABX-FDXI	81-pin WLCSP	Industrial

Arroyo Qualification Status

Product Status: In Production

Arroyo Errata Summary

The following table defines the errata applicability to available Arroyo family devices. An “X” indicates that the erratum pertains to the selected device.

Items	CYWB0320ABX-FDXI	Revision	Fix Status
1. P-Port SRAM mode fails if OE and CE are not asserted simultaneously.	[X]	A	–

1. P-Port SRAM mode fails if OE and CE are not asserted simultaneously

■ Problem Definition

When Arroyo is configured to use SRAM for P-port interface, OE should be asserted simultaneously with CE. If this is not possible, OE should be asserted prior to CE.

■ Parameters Affected

Data can be dropped when external processor reads the Arroyo through SRAM interface.

■ Trigger Condition(S)

When Arroyo P-port is configured in SRAM mode and if OE and CE don’t happen at the same time.

■ Scope of Impact

NIL

■ Workaround

The workaround available at this time include asserting OE and CE at the same time and asserting OE prior to CE.

■ Fix Status

NIL.

Errata

This section describes the errata for West Bridge Arroyo USB and Mass Storage Peripheral Controller, CYWB0321ABX-FDXI. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Package Type	Operating Range
CYWB0321ABX-FDXI	81-pin WLCSP	Industrial

Arroyo Qualification Status

Product Status: In Production

Arroyo Errata Summary

The following table defines the errata applicability to available Arroyo family devices. An “X” indicates that the erratum pertains to the selected device.

Items	CYWB0321ABX-FDXI	Revision	Fix Status
1. P-Port PSPI mode fails U-Port to P-Port transfer after wake up from STANDBY mode.	[X]	A	Fixed in SDK in version 1.0 or later

1. P-Port PSPI mode fails U-Port to P-Port transfer after wake up from STANDBY mode

■ Problem Definition

When Arroyo is configured to use SPI for Processor-Port (P-Port) interface, transfers from U-Port to P-Port may intermittently fail after wakeup from STANDBY mode.

■ Parameters Affected

Intermittent failure in U-Port to P-Port transfer after wakeup from STANDBY.

■ Trigger Condition(S)

The condition occurs when Arroyo is configured for PSPI mode and wakes up from STANDBY mode.

■ Scope of Impact

When Arroyo is configured to use SPI for Processor-Port (P-Port) interface, transfers from U-Port to P-Port may intermittently fail after wakeup from STANDBY mode.

■ Workaround

SDK version 1.0 or later provides the software workaround for this issue. The workaround requires using version 1.0 or later of the SDK for the system software development.

The workaround fixes the intermittent failure as described in Problem Definition. However, the workaround cause wakeup time (from STANDBY mode) to increase. This duration increase depends upon the system configuration as listed in the following table:

Arroyo System Configuration	Additional Wakeup Time (from STANDBY mode)
Using external crystal	5 ms
Using external oscillator	1 ms
Firmware image is loaded from EEPROM (through I2C™)	> 250 ms depending on the firmware image size and the I^2C frequency

This errata only affects Arroyo when the P-Port is configured for SPI mode.

■ Fix Status

Fixed in SDK version 1.0 or later.

Document History Page

Document Title: CYWB0320ABX-FDXI/CYWB0321ABX-FDXI, West Bridge®: Arroyo USB and Mass Storage Peripheral Controller Document Number: 001-57458				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2846580	SHIN / AESA	01/12/2010	New data sheet.
*A	2902575	STVC	03/31/2010	Updated Pin Assignments (Updated Table 4). Updated AC Timing Parameters (Added PCRAM Non Multiplexing Asynchronous Mode subsection). Changed status from Advance to Final. Updated links in Sales, Solutions, and Legal Information.
*B	3207801	ANOP	03/28/2011	Updated Pin Assignments (In Table 4, changed R/B# from 'I' to 'O' in the 'I/O' column corresponding to 'PNAND', changed 'A7 or SDA' to 'A6 or SDA' in the 'Pin Description' column corresponding to Ball H1, changed 'A6 or SCL' to 'A5 or SCL' in the 'Pin Description' column corresponding to Ball F2, changed SD_CLK from 'I/O' to 'O' in the 'I/O' column corresponding to 'S-Port Interface'.).
*C	3499405	RSKV	01/17/2012	Updated title to read as "CYWB0320ABX-FDXI/CYWB0321ABX-FDXI, West Bridge®: Arroyo USB and Mass Storage Peripheral Controller". Updated Features. Updated Functional Overview (Updated the subsection Processor Interface (P-Port) (description), updated the subsection Clocking (description, updated Table 1 and added Table 2). Updated Pin Assignments (Updated Table 4 and added Table 5, updated caption of Figure 3 and added Figure 4). Updated AC Timing Parameters (Added Table 12 and Figure 37). Added Ordering Information. Replaced Arroyo-II with Arroyo across the document. Updated to new template.
*D	3539329	RSKV	03/01/2012	Removed the tag "Company Confidential" from the header. Revised package diagram spec. Moving to external web.
*E	3878676	RSKV	01/21/2013	No technical updates. Completing Sunset Review.
*F	3978102	RSKV	04/22/2013	Added Acronyms and Units of Measure. Added Errata. Added Errata.
*G	4072903	RSKV	07/22/2013	Added Errata footnotes (Note 1, 2, 10). Updated Pin Assignments: Added Note 1 and referred the same note in "SRAM Interface" column in Table 4. Added Note 2 and referred the same note in "SPI" column in Table 5. Updated AC Timing Parameters: Updated P Port Interface: Updated Asynchronous SRAM Mode Timing Parameters: Added Note 10 and referred the same note in Figure 12. Updated to new template.

Document History Page (continued)

Document Title: CYWB0320ABX-FDXI/CYWB0321ABX-FDXI, West Bridge®: Arroyo USB and Mass Storage Peripheral Controller Document Number: 001-57458				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	4583918	GAYA	12/01/2014	Updated Features: Replaced “Supports I^2C Boot and Processor Boot” with “Supports USB Boot, I^2C Boot and Processor Boot”. Updated Ordering Information: Updated part numbers. Included a column “Status” and added details in that column. Completing Sunset Review.

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