Bluetooth Module Datasheet

CZW-3021-01

Model:CZW-3021-01 Hardware Version: V2.0 Release Date: 2018.05.11

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1 summary

CZW-3021-01 is a Bluetooth module designed by ShenZhen Cheng Zhi Wei Technology Co.,Ltd. using Qualcomm Bluetooth chip qcc3021 $_{\circ}$

CZW-3021-01 is a Bluetooth, audio and programmable application processor. It includes high-performance, analog, and digital audio codecs, Class-AB speaker driver, advanced power management, Li-ion battery charger, light-emitting diode (LED) drivers, and flexible interfaces including inter₁ integrated circuit sound (I² S), inter-integrated circuit interface (I² C), universal asynchronous receiver transmitter (UART), and programmable input/output (PIO)_o

CZW-3021-01 package is compatible with czw01 series pins, easy replacement and upgrade

| Model Name | CZW-3021-01 |
|-------------------------------|-----------------------|
| Package | 40 Pin Module |
| Dimension | 13mm x 28.5mm x 2.4mm |
| Chipset | QCC3021 |
| Bluetooth Version | Bluetooth 5.1 |
| Power Class | Class2 |
| Transmission Distance | ≥10M |
| Voltage | 2.8~4.2V |
| Temperature | -10∼+70℃ |
| Storage Temperature | -40∼+85℃ |
| Frequency Range | 2402~2480MHz |
| Maximum RF Transmit Power | 9dBm |
| | |
| π/4 DQPSK Receive Sensitivity | -91dBm |
| 8DPSK Receive Sensitivity | -85dBm |

2 General specifications

3 Key Features

3.1 Device description

- ★ High-performance programmable Bluetooth® stereo audio SoC
- ★ Fully qualified single-chip dual-mode Bluetooth v5.0 system
- ★ Tri-core processor architecture with low power for extended battery life

3.2 Features

- ★ Qualified to Bluetooth® v5.0 specification
- ★ 120 MHz Qualcomm® Kalimba[™] audio DSP
- ★ 32 MHz Developer Processor for applications
- ★ Firmware Processor for system
- ★ Flexible QSPI flash programmable platform
- ★ Advanced audio algorithms
- ★ High-performance 24- bit stereo audio interface
- ★ Digital and analog microphone interfaces
- ★ Flexible PIO controller and LED pins with PWM support
- ★ 1-mic Qualcomm[®] cVc[™] speaker noise reduction and echo cancellation technology
- ★ SBC and AAC audio codecs support
- ★ Serial interfaces: UART, Bit Serializer (I² C/SPI), USB 2.0
- ★ Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

3.3 Audio subsystem

★ 32- bit Kalimba audio digital signal processor (DSP) core with flexible clocking from 2 MHz to 120 MHz to allow

optimization and trade-off performance vs. power consumption

- ★ DSP runs from ROM
- ★ 80 KB program random access memory (RAM)
- ★ 256 KB data RAM
- ★ 5 Mb ROM

3.4 Application subsystem

- ★ Dual core application subsystem 32 MHz operation
- ★ 32- bit Firmware Processor:
- ★ 32- bit Developer Processor:
- ★ Both cores execute code from external flash memory using QSPI clocked at 32 MHz
- ★ On-chip caches per core allow for optimized performance and power consumption Bluetooth subsystem

3.5 Bluetooth subsystem

- ★ Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy (Production parts)
- ★ Single ended antenna connection with on-chip balun and Tx/Rx switch
- ★ Bluetooth, Bluetooth low energy, and mixed topologies supported
- ★ Class 1 support

3.6 Li-ion battery charger

★ Integrated battery charger supporting internal mode (up to 200 mA) and external mode (up to 1.8 A)

- ★ Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V
- ★ Thermal monitoring and management are implementable in application software
- ★ Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V

3.7 Power management

- ★ Integrated power management unit (PMU) to minimize external components
- ★ QCC3021 QFN runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)
- ★ Auto-switching between battery and USB (or other) charging source
- ★ Power islands employed to optimize power consumption for variety of use-cases
- ★ Dual switch-mode power supply (SMPS)

3.8 Audio engine and digital audio interfaces

- ★ 24-bit I² S interface with 1 input and 3 output channels
- ★ Programmable audio master clock (MCLK)
- ★ Sony/Philips digital interface (SPDIF): 2, configurable as input or output
- ★ Stereo analog Class-AB headphone outputs
- ★ Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs
- ★ 1 microphone bias (single bias shared by the two channels)
- ★ Digital microphone inputs with capability to interface up to 6 digital microphones
- ★ Both analog-to-digital converter (ADC)s and digital-to₇ analog converter (DAC)s support sample rates of 8, 16, 32, 44.1, 48, 96 kHz. DACs also support 192 kHz

3.9 Peripherals and physical interfaces

★ A UART interface

★ 2 x Bit Serializers (programmable serial peripheral interface (SPI) and I² C hardware accelerator)

- ★ 1 x USB interface
- ★ QSPI NOR flash interface

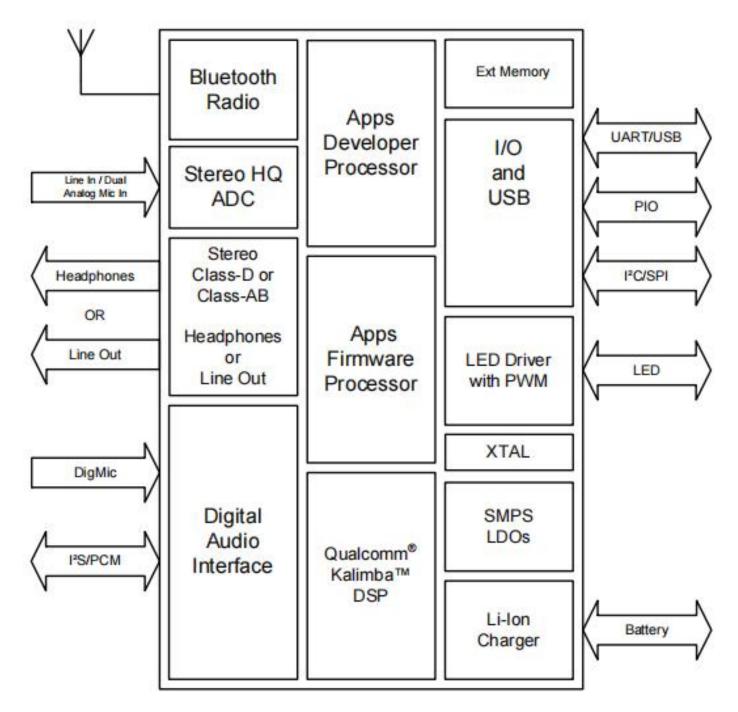
★ Up to 17 PIO and 4 open drain/digital input LED pads with

pulse width modulation (PWM)

4 Applications

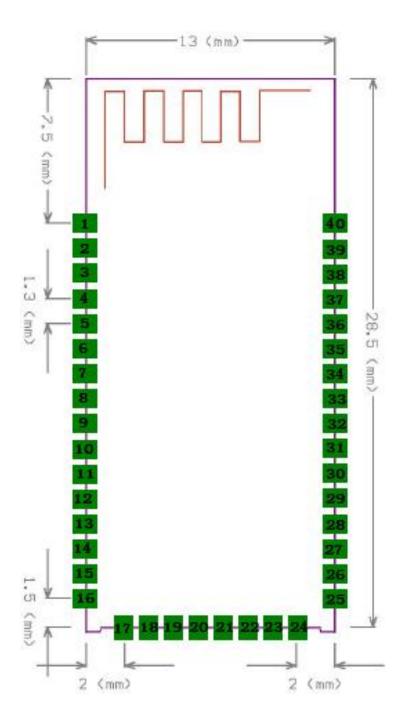
★ Wireless speakers

5 Block Diagram

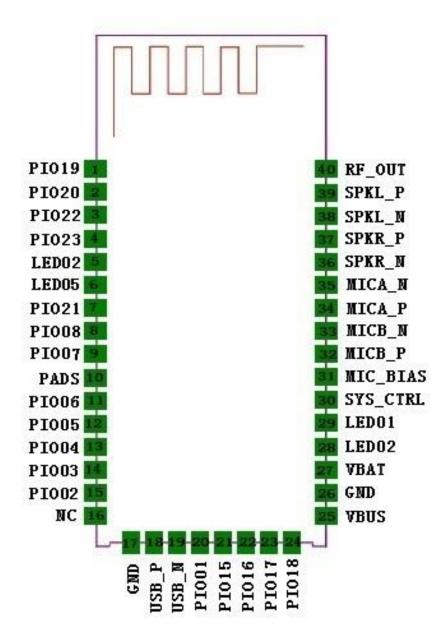


6 Module Package Information

6.1 Pinout Diagram and package dimensions



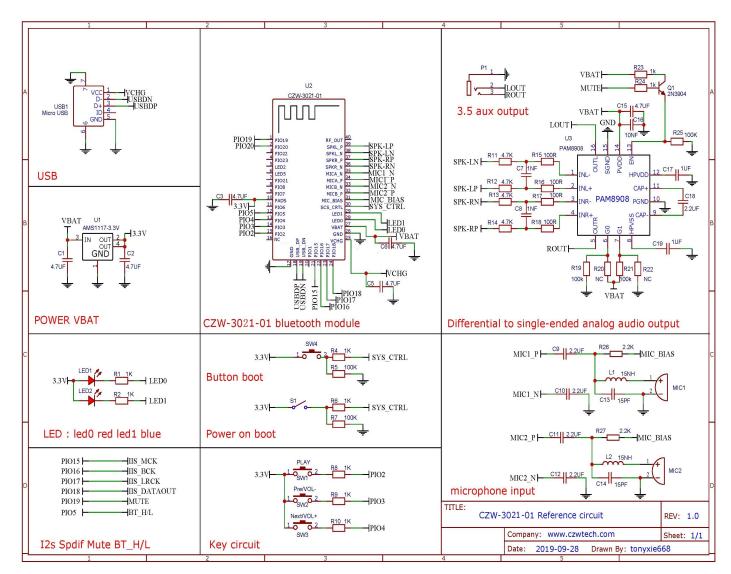
6.2 Module Pin descriptions



7 Pin Function Description

| Pin# | Pin Name | Pin type | Description | |
|--|--|---|--|--|
| | | Digital: Bidirectional with programmable | Programmable I/O line 19. | |
| 1 | PIO[19] | strength internal pull- up/pull-down | Alternative function: PCM DIN[0] | |
| | | Digital: Bidirectional with programmable | Programmable I/O line 20. | |
| 2 | PIO[20] | strength internal pull- up/pull-down | Alternative function: PCM_DOUT[1] | |
| 3 | PIO[22] | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Programmable I/O line 22. | |
| 4 | PIO[23] | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Programmable I/O line 23. | |
| 5 | LED[2] | Analog or digital input/ open drain output. | General-purpose analog/digital input or open drain LED output. | |
| 6 | LED[5] | Analog or digital input/ open drain output. | General-purpose analog/digital input or open drain LED output. | |
| _ | | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Programmable I/O line 21. | |
| 7 | PIO[21] | | Alternative function: PCM DOUT[2] | |
| | | Digital: Bidirectional with programmable | Programmable I/O line 8. | |
| 8 | PIO[8] | strength internal pull- up/pull-down | Alternative function: TBR_CLK | |
| _ | | Digital: Bidirectional with programmable | Programmable I/O line 7. | |
| 9 | PIO[7] | strength internal pull- up/pull-down | Alternative function: TBR_MISO[0] | |
| 10 | PADS | Supply | 1.8 V/3.3 V PIO supply. | |
| | PIO[6] | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Programmable I/O line 6. | |
| 11 | | | Alternative function: TBR_MOSI[0] | |
| | 12Digital: Bidirectional with programmable strength internal pull- up/pull-down | | Programmable I/O line 5. | |
| 12 | | | Alternative function: TBR_MISO[1] | |
| 4.2 | | Digital: Bidirectional with programmable | Programmable I/O line 4. | |
| 13 | PIO[4] | strength internal pull- up/pull-down | Alternative function: TBR_MOSI[1] | |
| | 010[3] | Digital: Bidirectional with programmable | Programmable I/O line 3. | |
| 14 | PIO[3] | strength internal pull- up/pull-down | Alternative function: TBR_MISO[2] | |
| 45 | PIO[2] | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Programmable I/O line 2. | |
| 15 | | | Alternative function: TBR_MISO[3] | |
| 16 | NC | NC | NC | |
| 17 | GND | Ground | Ground | |
| 18 | USB_DP | Digital | USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection | |
| 19 | USB DN | Digital | USB Full Speed device D- I/O. IEC-61000-4-2 (device level) | |
| | 555_51 | | ESD Protection | |
| 20 | PIO[1] | Digital: Bidirectional with programmable strength internal pull- up/pull-down | Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot. | |
| Digital: Ridirectional with programmable | | Digital: Bidirectional with programmable | Alternative function: Programmable I/O line 1 | |
| 21 | PIO[15] | strength internal pull- up/pull-down | Programmable I/O line 15. | |
| | | Digital: Bidirectional with programmable | Alternative function: MCLK_OUT | |
| 22 | PIO[16] | strength internal pull- up/pull-down | Programmable I/O line 16. | |
| | | | Alternative function: PCM_CLK | |

| Pin# | Pin Name | Pin type | Description | |
|----------|----------|---|--|--|
| | | Digital: Bidirectional with programmable | Programmable I/O line 17. | |
| 23 | PIO[17] | strength internal pull- up/pull-down | Alternative function: PCM SYNC | |
| | | Digital: Bidirectional with programmable | Programmable I/O line 18. | |
| 24 | PIO[18] | strength internal pull- up/pull-down | Alternative function: PCM_DOUT[0] | |
| 24 | VBUS | Supply | Charger input to Bypass regulator. | |
| 26 | GND | Ground | Ground | |
| 27 | VBAT | Supply | Battery voltage input. | |
| 28 | LED[0] | Analog or digital input/ open drain output. | General-purpose analog/digital input or open drain LED output. | |
| 29 | LED[1] | Analog or digital input/ open drain output. | General-purpose analog/digital input or open drain LED output. | |
| 30 | SYS_CTRL | Digital input | Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull. Additional function: PIO[0] input only | |
| 31 | MIC_BIAS | VDD_AUDIO_1V8 | Mic bias output. | |
| 32 | MIC2_P | VDD_AUDIO_1V8 | Microphone differential 2 input, positive. Alternative function: Differential audio line input right, positive | |
| 33 | MIC2_N | VDD_AUDIO_1V8 | Microphone differential 2 input, negative. Alternative function: Differential audio line input right, negative | |
| 34 | MIC1_P | VDD_AUDIO_1V8 | Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive | |
| 35 | MIC1_N | VDD_AUDIO_1V8 | Microphone differential 1 input, positive. Alternative function: Differential audio line input left, positive | |
| | | | Headphone/speaker differential right output, negative. | |
| 36 | SPKR N | VDD AUDIO HP SPKR | Alternative function: Differential right line output, negative | |
| | | | Headphone/speaker differential right output, positive. | |
| 37 | SPKR_P | VDD_AUDIO_HP_ SPKR | Alternative function: Differential right line output, positive | |
| 38 | SPKL_N | VDD_AUDIO_HP_ SPKL | Headphone/speaker differential left output, negative. Alternative function: Differential left line output, negative | |
| | | | Headphone/speaker differential left output, positive. Alternative function: Differential left line output, positive | |
| 39 40 | SPKL_P | | Bluetooth transmit/receive. | |
| 40 | RF_OUT | VDD_BT_RADIO | | |



8 Reference application circuit

Notice: for reference only, please design the circuit according to the actual application

9 Electrical Characteristics

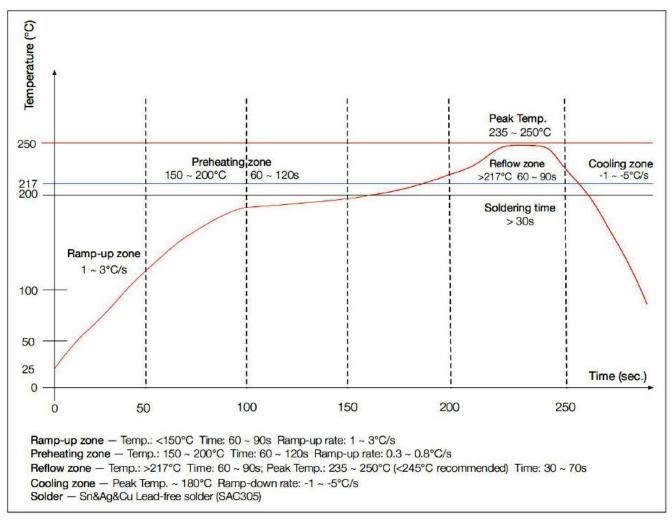
9.1 Absolute Maximum Ratings

| Rating | Minimum | Maximum |
|---------------------|---------------|---------|
| Storage temperature | - 40 ℃ | +85℃ |

9.2 Recommended Operating Conditions

| Operating Condition | Minimum | Maximum |
|-----------------------------|--------------|---------|
| Operating temperature range | -40 ℃ | +85℃ |
| Supply voltage: VBAT | +2.8V | +4.3V |

10 Recommended reflow temperature profile



The module Must go through 100 $^\circ\!\!\mathbb{C}$ baking for at least 12 hours before SMT AND IR reflow process!

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