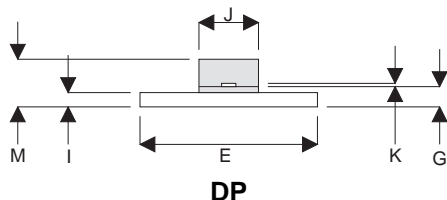
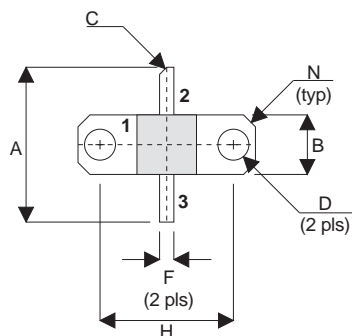


MECHANICAL DATA



PIN 1 SOURCE PIN 2 DRAIN  
PIN 3 GATE

DIM	mm	Tol.	Inches	Tol.
A	16.51	0.25	0.650	0.010
B	6.35	0.13	0.250	0.005
C	45°	5°	45°	5°
D	3.30	0.13	0.130	0.005
E	18.92	0.08	0.745	0.003
F	1.52	0.13	0.060	0.005
G	2.16	0.13	0.085	0.005
H	14.22	0.08	0.560	0.003
I	1.52	0.13	0.060	0.005
J	6.35	0.13	0.250	0.005
K	0.13	0.03	0.005	0.001
M	5.08	0.51	0.200	0.020
N	1.27 x 45°	0.13	0.050 x 45°	0.005

**GOLD METALLISED  
MULTI-PURPOSE SILICON  
DMOS RF FET  
10W – 12.5V – 500MHz  
SINGLE ENDED**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{rss}$
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS  
from 1 MHz to 500 MHz

ABSOLUTE MAXIMUM RATINGS ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	50W
$BV_{DSS}$	Drain – Source Breakdown Voltage	40V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	10A
$T_{stg}$	Storage Temperature	$-65$ to $150^{\circ}C$
$T_j$	Maximum Operating Junction Temperature	$200^{\circ}C$

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
B <sub>V</sub> DSS Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0      I <sub>D</sub> = 100mA	40			V
I <sub>D</sub> DSS Zero Gate Voltage Drain Current	V <sub>DS</sub> = 12.5V      V <sub>GS</sub> = 0			1	mA
I <sub>G</sub> DSS Gate Leakage Current	V <sub>GS</sub> = 20V      V <sub>DS</sub> = 0			1	μA
V <sub>GS(th)</sub> Gate Threshold Voltage*	I <sub>D</sub> = 10mA      V <sub>DS</sub> = V <sub>GS</sub>	1		7	V
g <sub>fs</sub> Forward Transconductance*	V <sub>DS</sub> = 10V      I <sub>D</sub> = 1A	0.8			S
G <sub>PS</sub> Common Source Power Gain	P <sub>O</sub> = 10W	10			dB
η Drain Efficiency	V <sub>DS</sub> = 12.5V      I <sub>DQ</sub> = 0.2A	50			%
VSWR Load Mismatch Tolerance	f = 500MHz	20:1			—
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 0      V <sub>GS</sub> = -5V      f = 1MHz			60	pF
C <sub>oss</sub> Output Capacitance	V <sub>DS</sub> = 12.5V      V <sub>GS</sub> = 0      f = 1MHz			40	pF
C <sub>rss</sub> Reverse Transfer Capacitance	V <sub>DS</sub> = 12.5V      V <sub>GS</sub> = 0      f = 1MHz			4	pF

\* Pulse Test:    Pulse Duration = 300 μs , Duty Cycle ≤ 2%

## HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.**

## THERMAL DATA

R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 3.5°C / W
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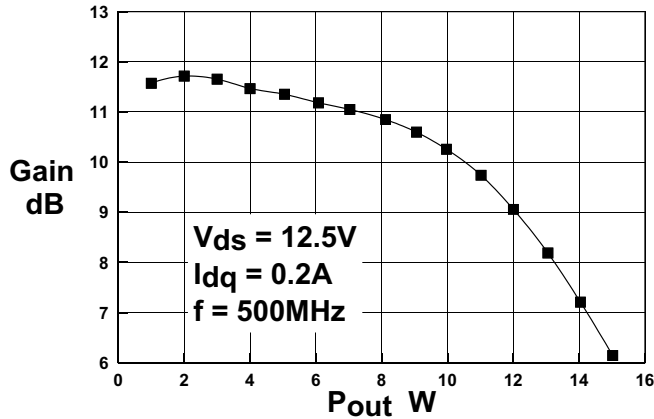


Figure 1- Gain vs. Power Output

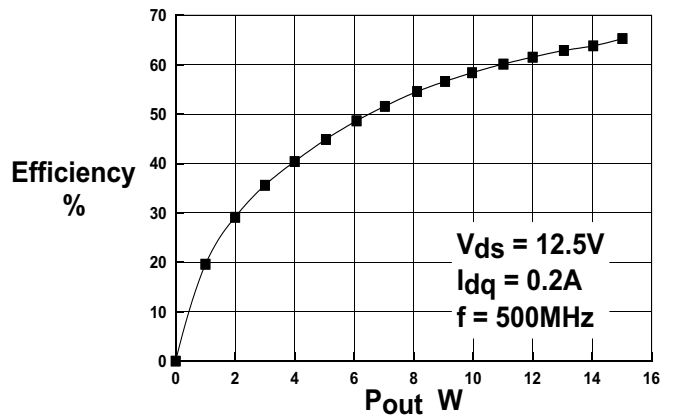


Figure 2 - Efficiency vs. Power Output

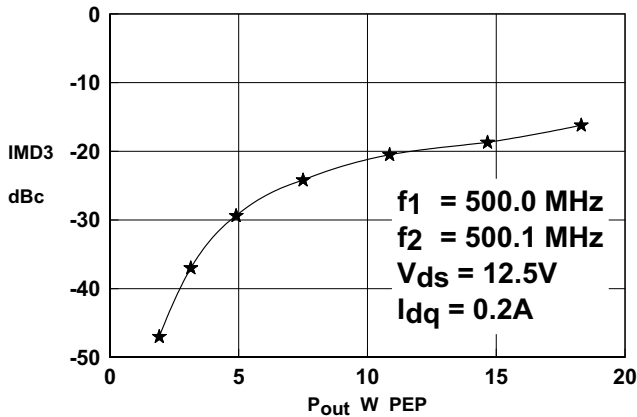


Figure 3 - IMD vs. Power Output

OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z <sub>S</sub> Ω	Z <sub>L</sub> Ω
500MHz	2.7 + j2.7	3.5 - j0.9

Typical S Parameters

! V<sub>DS</sub> = 12.5V, I<sub>DQ</sub> = 1A  
 # MHZ S M A R 50

Freq MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
100	0.92	-157	9.33	90	0.018	18	0.72	-174
200	0.92	-162	8.12	81	0.022	24	0.75	-175
300	0.91	-167	6.90	71	0.026	29	0.78	-176
400	0.91	-172	5.69	62	0.03	35	0.80	-177
500	0.91	-177	4.48	52	0.034	41	0.83	-178
600	0.90	178	3.26	43	0.038	47	0.85	-179
700	0.90	173	2.05	33	0.042	52	0.88	-180
800	0.89	168	0.83	24	0.046	58	0.90	179
900	0.90	162	0.70	17	0.054	55	0.91	174
1000	0.90	160	0.58	16	0.061	55	0.91	174

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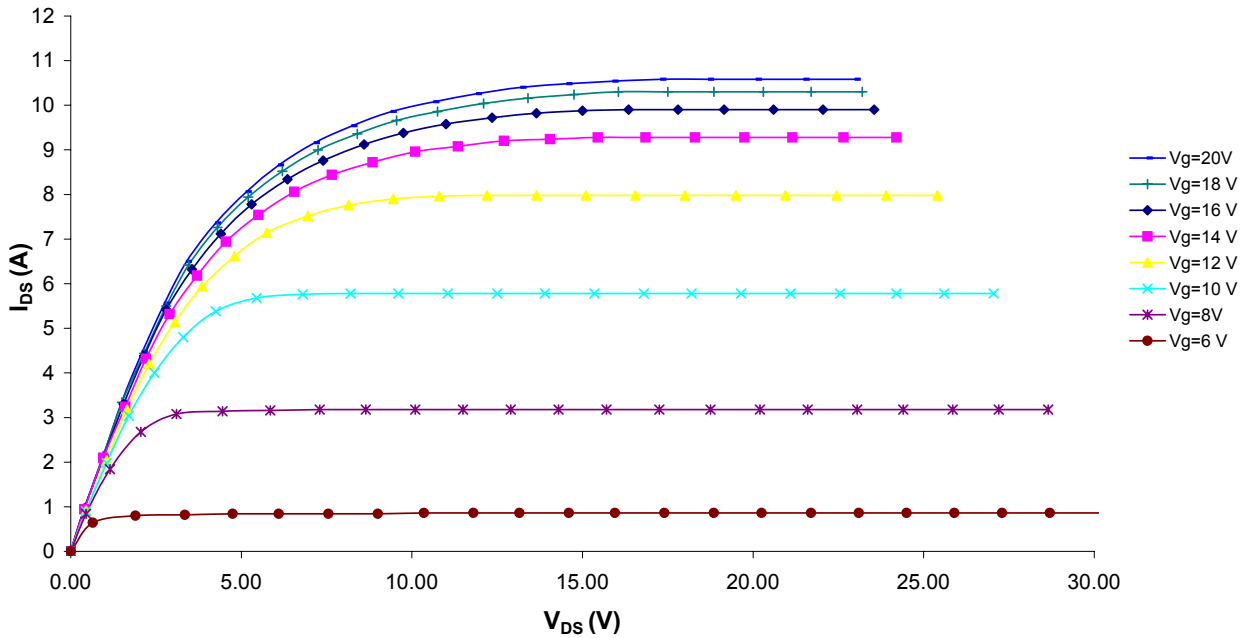


Figure 4 – Typical IV Characteristics.

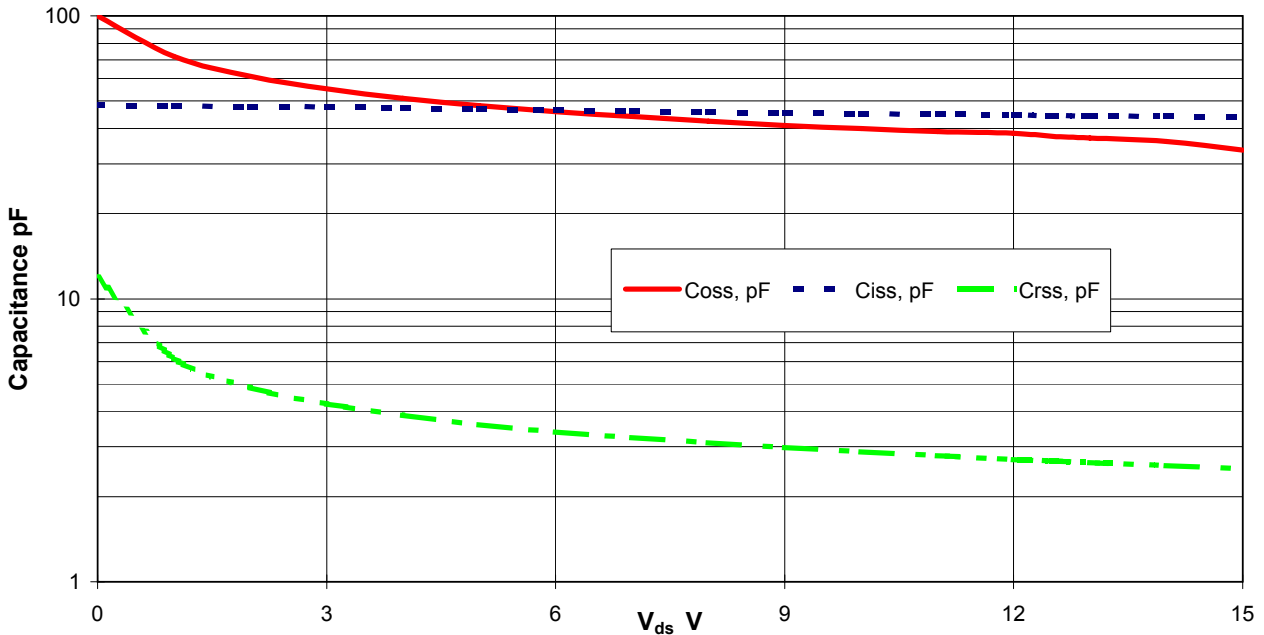
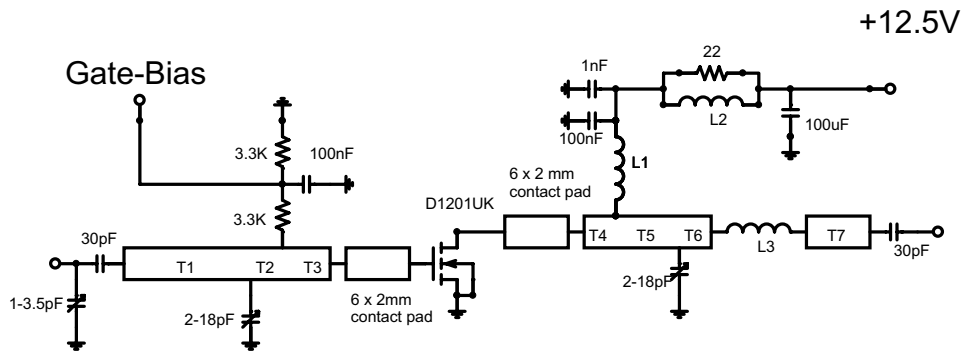


Figure 5 – Typical CV Characteristics.

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Substrate 0.8mm PTFE/glass, Er=2.5

All microstrip lines W=2.2mm

T1 32mm

T2 4mm

T3 5mm

T4 3mm

T5 9mm

T6 7.5mm

T7 13mm

L1 6 turns 0.5mm dia enamelled copper wire, 3mm i.d.

L2 1.5 turns 0.5mm enamelled copper wire on Siemens B62152A7 2 hole ferrite core

L3 1/16" dia wire hairpin loop 15mm long

## D1201UK 500MHz Test Fixture