

SILICON POWER TRANSISTOR 2SD2164

NPN SILICON EPITAXIAL TRANSISTOR FOR LOW-FREQUENCY POWER AMPLIFIERS AND LOW-SPEED SWITCHING

The 2SD2164 is a single power transistor developed especially for high h_{FE} . This transistor is ideal for simplifying drive circuits and reducing power dissipation because its h_{FE} is as high as that of Darlington transistors, but it is a single transistor.

In addition, this transistor features a small resin insulated package, thus contributing to high-density mounting and mounting cost reduction.

FEATURES

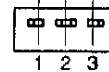
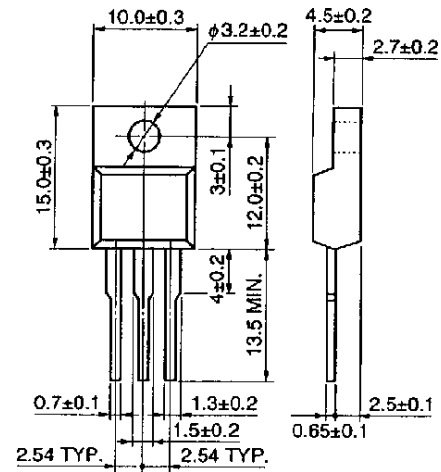
- High h_{FE} and low $V_{CE(sat)}$:
 $h_{FE} \cong 1,300$ TYP. ($V_{CE} = 5.0$ V, $I_C = 0.5$ A)
 $V_{CE(sat)} \cong 0.3$ V TYP. ($I_C = 2.0$ A, $I_B = 20$ mA)
- Full mold package that does not require an insulating board or insulation bushing

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	60	V
Collector to emitter voltage	V_{CEO}	60	V
Emitter to base voltage	V_{EBO}	7.0	V
Collector current (DC)	$I_{C(DC)}$	3.0	A
Collector current (pulse)	$I_{C(pulse)}$	5.0 ^{Note}	A
Base current (DC)	$I_{B(DC)}$	0.5	A
Total power dissipation	$P_T (T_C = 25^\circ\text{C})$	20	W
Total power dissipation	$P_T (T_A = 25^\circ\text{C})$	2.0	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note $PW \leq 300 \mu\text{s}$, duty cycle $\leq 10\%$

PACKAGE DRAWING (UNIT: mm)



Electrode Connection

1. Base
2. Collector
3. Emitter

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

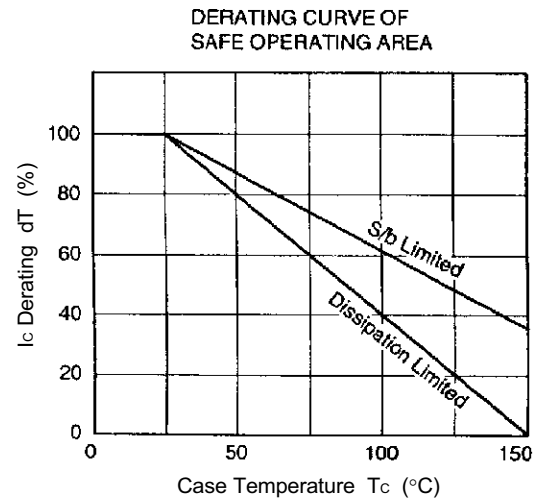
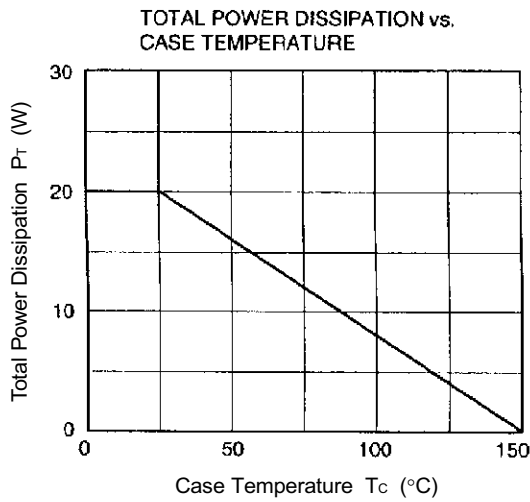
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	I _{CBO}	V _{CB} = 60 V, I _E = 0 A			10	μA
Emitter cutoff current	I _{EBO}	V _{EB} = 7.0 V, I _C = 0 A			10	μA
DC current gain	h _{FE1}	V _{CE} = 5.0 V, I _C = 0.5 A ^{Note}	800	1,300	3,200	
DC current gain	h _{FE2}	V _{CE} = 5.0 V, I _C = 3.0 A ^{Note}	500	1,000		
Collector saturation voltage	V _{CE(sat)}	I _C = 2.0 A, I _B = 20 mA ^{Note}		0.3	0.5	V
Base saturation voltage	V _{BE(sat)}	I _C = 2.0 A, I _B = 20 mA ^{Note}			1.2	V
Gain bandwidth product	f _T	V _{CE} = 5.0 V, I _C = 0.1 A		110		MHz
Collector capacitance	C _{ob}	V _{CB} = 10 V, I _E = 0 A, f = 1.0 MHz		50		pF

Note Pulse test PW ≤ 350 μs, duty cycle ≤ 2%

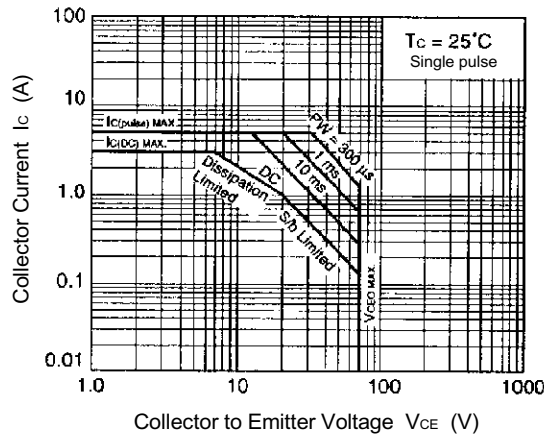
h_{FE1} CLASSIFICATION

Marking	M	L	K
h _{FE1}	800 to 1,600	1,000 to 2,000	1,600 to 3,200

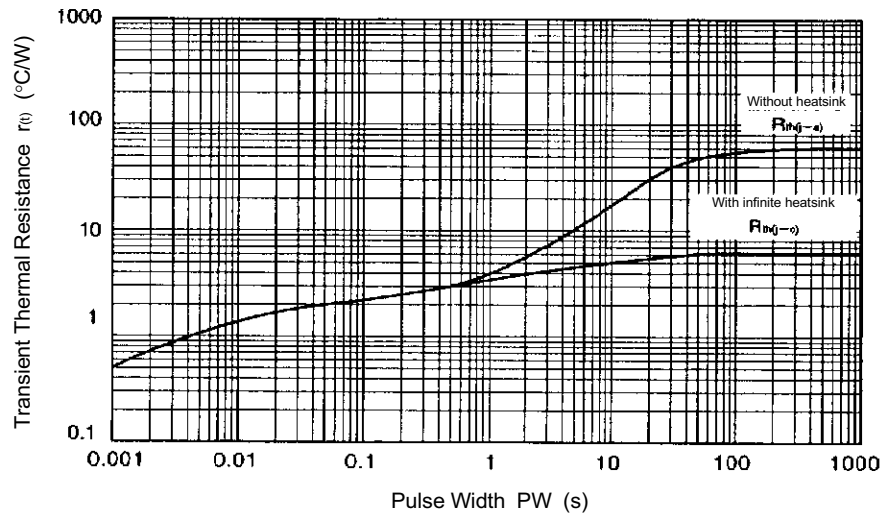
TYPICAL CHARACTERISTICS (T_A = 25°C)

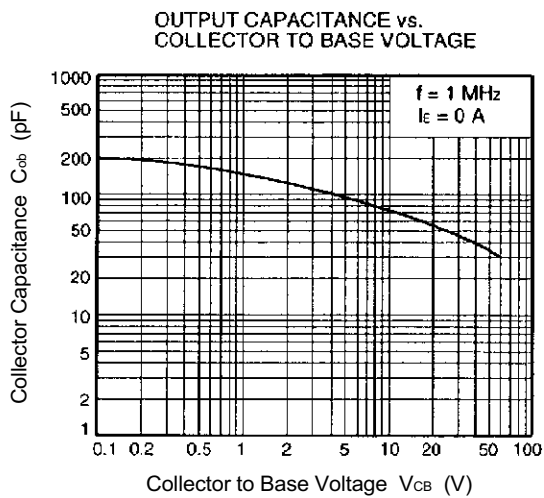
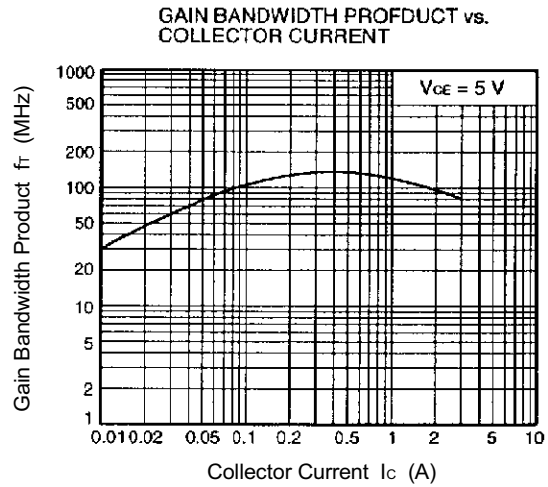
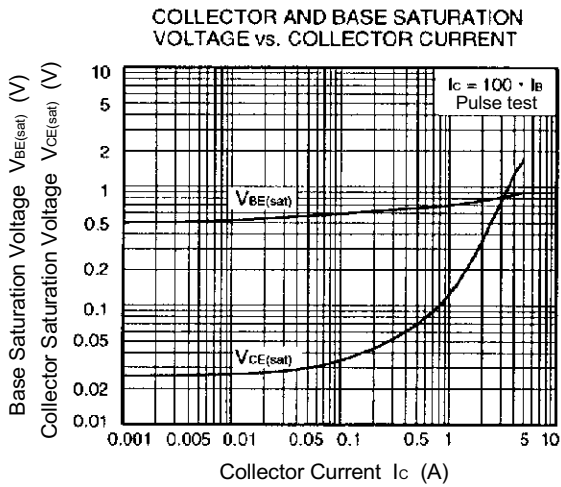
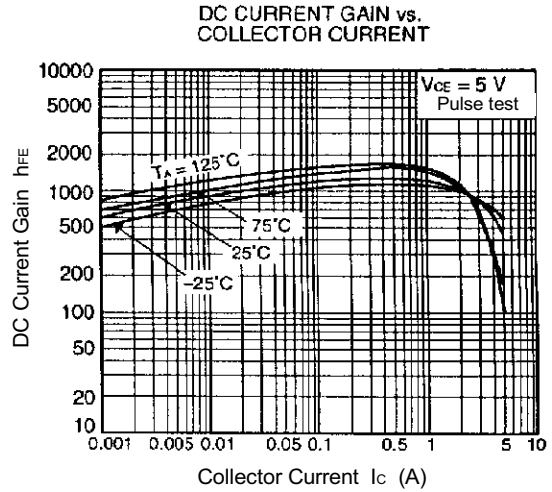
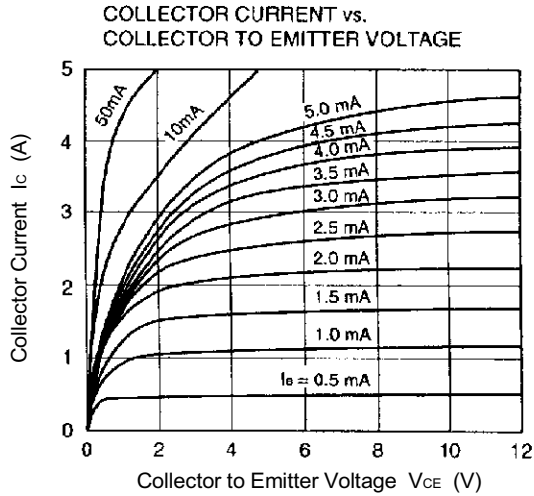


FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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