

Silicon NPN Power Transistors

2SD1710

DESCRIPTION

- With TO-3PML package
- High voltage;high speed
- High reliability.

APPLICATIONS

- Ultrahigh-definition CRT display
- Horizontal deflection output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

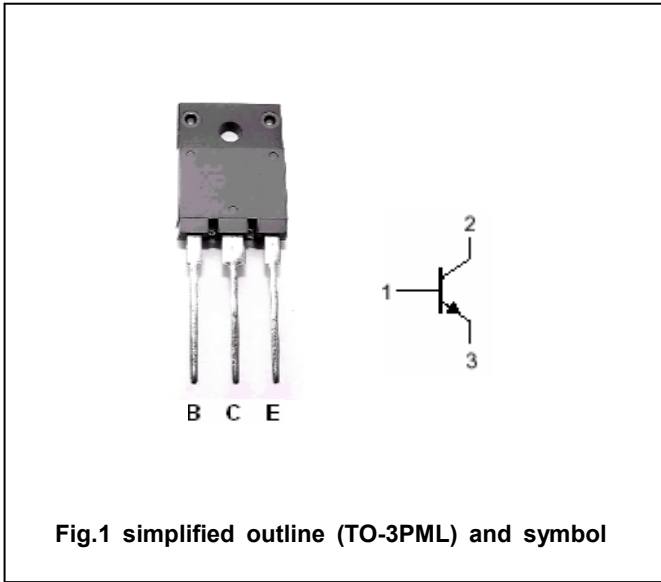


Fig.1 simplified outline (TO-3PML) and symbol

Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	1500	V
V _{CEO}	Collector-emitter voltage	Open base	800	V
V _{EBO}	Emitter-base voltage	Open collector	6	V
I _C	Collector current		5	A
P _C	Collector power dissipation	T _C =25°C	50	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

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 $T_j=25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	$I_C=100\text{mA}; I_B=0$	800			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=4\text{A}; I_B=0.8\text{ A}$			5.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=4\text{A}; I_B=0.8\text{ A}$			1.5	V
I_{EBO}	Emitter cut-off current	$V_{EB}=4\text{V}; I_C=0$			0.1	mA
I_{CBO}	Collector cut-off current	$V_{CB}=800\text{V}; I_E=0$			10	μA
I_{CES}	Collector cut-off current	$V_{CE}=1500\text{V}; R_{BE}=0$			1.0	mA
h_{FE}	DC current gain	$I_C=0.5\text{ A}; V_{CE}=5\text{V}$	10		40	

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PACKAGE OUTLINE

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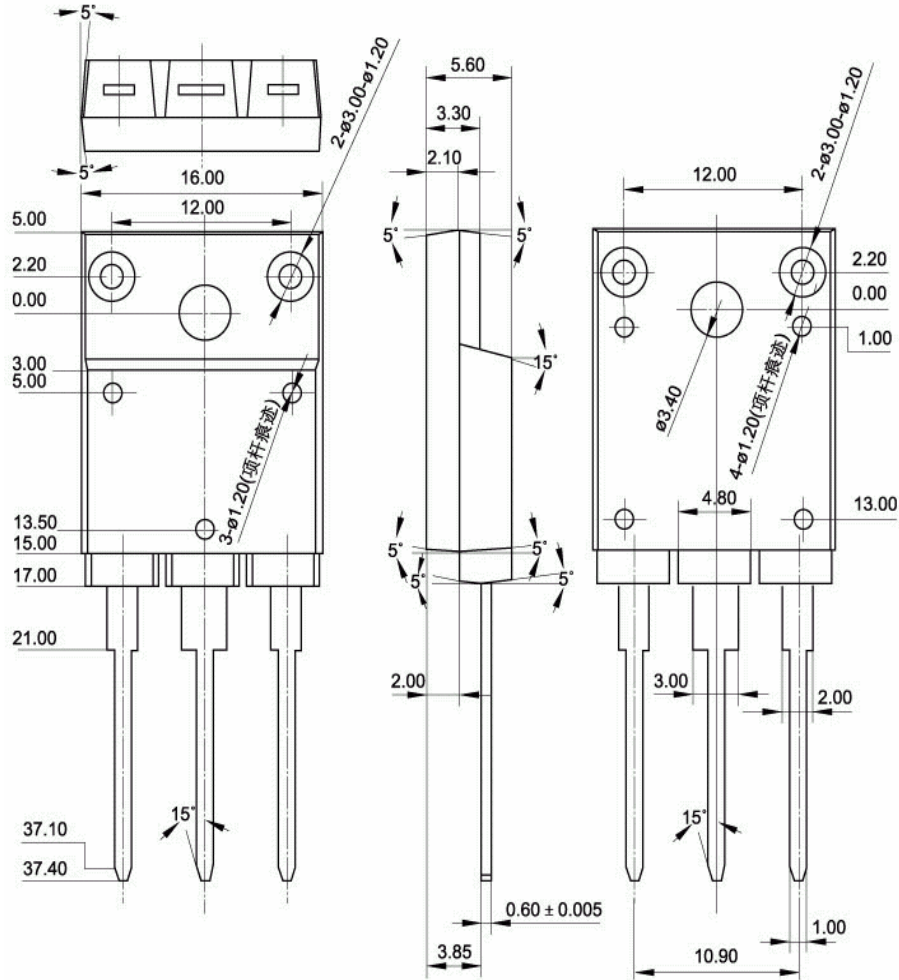


Fig.2 Outline dimensions