27F64
64K (8K x 8) CHMOS FLASH MEMORY

- **Quick-Erase™ Algorithm**
  - **Two Second Typical Array Electrical Erasure**
- **High Performance Speeds**
  - **150 ns Maximum Access Time**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current for Power-Down Savings**
- **Quick-Pulse Programming™ Algorithm**
  - **One Second Typical Chip Program**
- **On-Board Program/Erase**
  - **New Modes Simplify In-Module Firmware Upgrades**
- **2764A and 27C64 JEDEC Pinout**
  - **28 Pin Cerdip Package**
    (See Packaging Spec., Order # 231369)
- **EPROM Based ETOX™ Process**
  - **3 Year CHMOS* EPROM Manufacturing Base**
  - **Improved Latch-Up Immunity through EPI Processing**

The Intel 27F64 ETOX™ (EPROM tunnel oxide) flash memory is a 64K bit non-volatile memory organized as 8192 bytes of 8 bits. The 27F64 electrically erases all bits in parallel, making it ideal for EPROM applications where U.V. erasure is impractical or time consuming. Electrical erasure allows manufacturers to efficiently implement code changes for testing and end-of-line final configuration.

To decrease the cost of servicing and updating program code, the 27F64 offers new programming and erase modes called On-Board modes. These modes simplify in-circuit programming and erasure by maintaining V_{CC} at 5V, and $\overline{CE}$ and $\overline{OE}$ at standard logic levels. Devices socketed or soldered to circuit boards can be erased and programmed via an edge connector to a PROM programmer, or via the board tester already available. The Quick-Erase™ algorithm and On-Board features give system designers innovative capabilities. Compared to byte-alterable E^2PROM, these features address industry's need for a cost-effective code update solution.

Intel's new ETOX flash memory process combines the programming mechanism of EPROM with the erase mechanism of E^2PROM to produce dense electrically erasable memories with the reliability and manufacturability of today's EPROM technology.

Intel's unique Epitaxial (EPI) processing provides excellent latch-up immunity. Prevention of latch-up is specified for stress up to 100 mA from $-1V$ to $V_{CC} + 1V$ on address and data pins. All high voltage pins are protected from overshoot up to 14V.

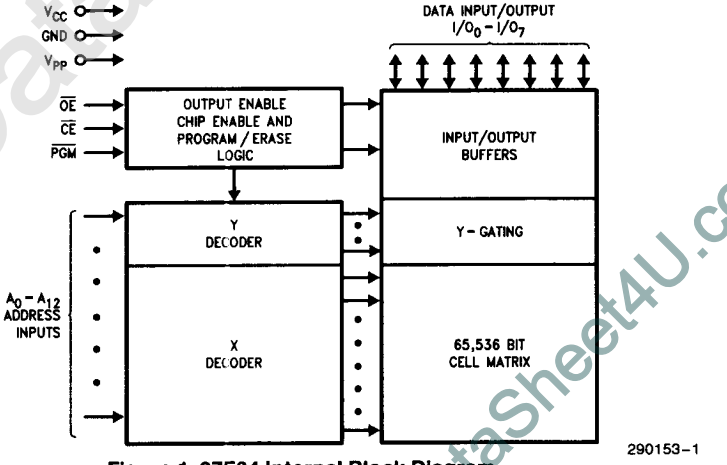

Figure 1. 27F64 Internal Block Diagram

*CHMOS is a patented process of Intel Corporation.

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Order Number: 290153-004

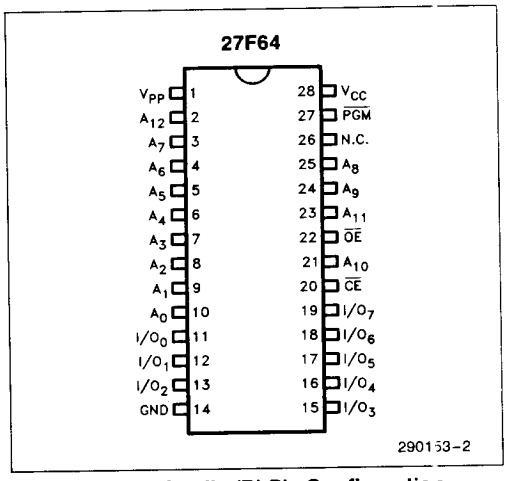


Figure 2. Cerdip (D) Pin Configuration

Pin Names

A_0–A_{12}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program
V_{PP}	Program/Erase Power
V_{CC}	Device Power
GND	Ground
N.C.	No Internal Connection

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{12}	I	**ADDRESS BUS** inputs the memory addresses, and selects the 8 bits in the 256 row by 256 column array.
I/O_0–I/O_7	I/O	**DATA BUS** inputs data during memory program cycles; outputs data during memory read cycles. The data bus is active high and floats to tri-state OFF when the chip is deselected or the outputs disabled.
$\overline{CE}$	I	**CHIP ENABLE** activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	I	**OUTPUT ENABLE** when active low gates the device's output through the data buffers during a read cycle. $\overline{OE}$ driven to a third logic level V_H 11.5V–13.0V, selects the conventional chip erase mode.
$\overline{PGM}$	I	**PROGRAM** controls the program and erase pulse-width in the conventional modes by being driven low. $\overline{PGM}$ driven to a third logic level V_H (11.5V–13.0V) gates entry into the On-Board program verify, erase, and erase verify modes*. In the On-Board erase mode, $\overline{CE}$ controls the erase pulse width.
V_{PP}		**PROGRAM/ERASE POWER SUPPLY** (12.75V ±0.25V) for programming and erasing the device. V_{PP} also supplies the Flash memory cell margin voltage during the On-Board program verify and erase verify modes. In these modes, V_{PP} must switch to 6.25V ±0.25V and 3.25V ±0.25V, respectively.
V_{CC}		**DEVICE POWER** for most operations (5V ±5%). V_{CC} also supplies the memory cell's margin voltage during the conventional program verify and erase verify modes. In these modes, V_{CC} must switch to 6.25V ±0.25V and 3.25V ±0.25V, respectively.
GND		**GROUND:** Reference for the device's circuitry.
N.C.		**NO INTERNAL CONNECTION** to this device. Pin may be driven or left floating.

NOTE:
*For complete discussion and explanation of the On-Board modes, refer to the On-Board device operation section.

PRINCIPLES OF OPERATION

The 27F64 features two distinct modes of operation—conventional EPROM and On-Board. Both follow the same program and erase algorithms although the implementations differ. Due to specified V_{CC} levels, the conventional modes tend to be more suited to programming and erasure in a PROM programmer, than to in-circuit code alteration. Intel offers the new program and erase methodology (On-Board modes) in consideration of the new trends in system design and manufacturing.

In all cases, the 27F64 flash memory performs the read and standby functions exactly like Intel's 2764A and 27C64 EPROMs.

The following sections discuss the read mode and then the specifics of the two program/erase methodologies. Discussion of conventional modes precedes that of On-Board modes.

READ MODE

The 27F64 is functionally equivalent to the 2764A or 27C64 in the read mode, and can replace either in existing designs. The 27F64 has two read control pins, both of which must be logically active to obtain data at the outputs. Chip Enable ($\overline{CE}$) controls device selection and activates internal circuitry. Output Enable ($\overline{OE}$) controls the selected device's I/O buffers and gates data onto the output pins. The address access time (t_{ACC}) specifies the maximum delay time from stable address inputs to valid data out, with $\overline{CE}$ and $\overline{OE}$ active low. The chip enable access time (t_{CE}) specifies the maximum delay from $\overline{CE}$ active low to valid data, assuming stable addresses and $\overline{OE}$ driven low. Valid data becomes available on the outputs a maximum of t_{OE} after $\overline{OE}$ transitions high to low. The t_{OE} specification assumes stable chip selection and addresses for $t = t_{ACC} - t_{OE}$ or $t_{CE} - t_{OE}$. (See Figure 3. Read Operation A.C. Waveforms for graphical explanation.)

STANDBY MODE

With $\overline{CE}$ at a logic high (V_{IH}), the standby mode disables most of the 27F64's circuitry and substantially reduces the device's power consumption to 100 μA (with CMOS inputs). The outputs assume a high impedance state, independent of the $\overline{OE}$ input.

Table 2. Conventional Mode Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Program/Erase Inhibit	X	X	X	X	X	V_{CC}(4)	5.0V	
Program	V_{IL}	V_{IH}	V_{IL}	X	X	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	12.75V	6.25V	D_{OUT}
Quick-Erase	V_{IL}	V_H(2)	V_{IL}	X	X	12.75V	3.25V	High Z
Erase Verify	V_{IL}	V_{IL}	V_{IH}	X	X	12.75V	3.25V	D_{OUT}
inteligent ID™ Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}(3)	V_{CC}	5.0V	89H
inteligent ID™ Device	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}(3)	V_{CC}	5.0V	03H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $11.5V \leq V_H \leq 13.0V$.
3. $A_1 - A_8$, $A_{10} - A_{12} = V_{IL}$.
4. With $V_{PP} \leq V_{CC}$, the 27F64 inhibits all erase and program functions.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C(1)
During Program/Erase ..... 25°C ±15°C
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with Respect to Ground ..... −2.0V to +7V(2)
Voltage on Pin A_9, $\overline{PGM}$, or $\overline{OE}$ with Respect to Ground −2.0V to +13.5V(2, 3)
V_{PP} Supply Voltage with Respect to Ground During Programming/Erase ..... −2.0V to +14V(2, 3)
V_{CC} Supply Voltage with Respect to Ground ..... −2.0V to +7.0V(2)
Program/Erase Cycles 100
Output Short Circuit Current ..... 100 mA(4)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2V for periods less than 20 ns.
3. Maximum D.C. Voltage on A_9, $\overline{PGM}$, $\overline{OE}$, or V_{PP} is 13V. $\overline{OE}$, $\overline{PGM}$ or A_9 may overshoot to 13.5V for periods less than 20 ns. V_{PP} may overshoot to 14V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

Table 3a. Read Operation

D.C. CHARACTERISTICS TTL/NMOS Compatible

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current		20, 30	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA(1, 4)
I_{PP1}	V_{PP} Read Current		100	μA	$V_{PP} = V_{CC}$(2)
V_{IL}	Input Low Voltage	−0.5	0.8	V	$V_{PP} = V_{CC}$
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	$V_{PP} = V_{CC}$(3)
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA, $V_{CC} = V_{CC}$ min
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min

NOTES:
1. Maximum active read power is the sum of I_{CC} active + I_{PP}. The maximum current value is with the outputs unloaded.
2. V_{PP} may be equal to V_{CC}, or one diode drop below V_{CC}.
3. If driven higher than V_{CC} + 0.5V during programming, the data input transistors will forward bias and pull down the bus driver.
4. 20 mA for STD versions; 30 mA for -150, -170, and -200 ns versions.

Table 3b. Read Operation (Continued)

D.C. CHARACTERISTICS CMOS Compatible

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	μA	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current		±10	μA	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current		100	μA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{CC} \pm 0.2V$(7)
I_{CC1}	V_{CC} Active Read Current		20, 30	mA	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$, f = 5 MHz, I_{OUT} = 0 mA(1, 5, 6)
I_{PP1}	V_{PP} Read Current		100	μA	$V_{PP} = V_{CC}$(2)
V_{IL}	Input Low Voltage	−0.5	0.8	V	$V_{PP} = V_{CC}$(3)
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	$V_{PP} = V_{CC}$(3, 5)
V_{OL}	Output Low Voltage		0.40	V	I_{OL} = 1.6 mA, $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.1 mA, $V_{CC} = V_{CC}$ min
V_{OH2}		V_{CC} − 0.4		V	I_{OH} = −100 μA, (4) $V_{CC} = V_{CC}$ min

NOTES:
1. Maximum active read power is the sum of I_{CC} active + I_{PP}. The maximum current value is with the outputs unloaded.
2. V_{PP} may be equal to V_{CC}, or one diode drop below V_{CC}.
3. To maintain CMOS leakage current specifications, do not drive the data inputs above V_{CC} or below ground.
4. V_{OH2} specifies the minimum high output voltage with 100 μA of bus leakage.
5. If driven higher than V_{CC} + 0.5V during programming, the data input transistor's will forward bias and pull down the bus driver.
6. 20 mA for STD versions; 30 mA for -150, -170 and -200 ns versions.
7. Signal driving $\overline{CE}$ is assumed to be in the CMOS logic "1" steady state.

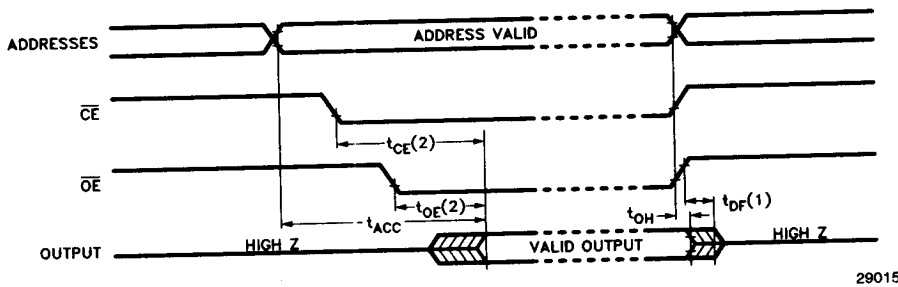
READ OPERATION

Table 4. Read Operation

A.C. CHARACTERISTICS 27F64(1) $0 \le T_A \le 70°C$

Versions		V_{CC} ±5%	D27F64-150V05		D27F64-170V05		D27F64-200V05		D27F64-250V05		Unit
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		170		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay			150		170		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay			65		70		75		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			35		35		55		60	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OH} = 2.0V and V_{OL} = 0.8V.
2. Guaranteed and sampled.



NOTES:
1. This parameter is only sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

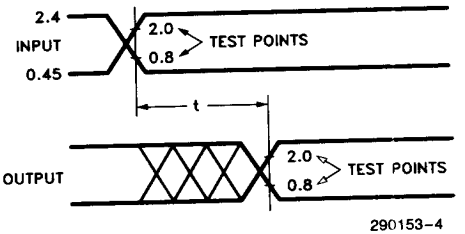
Figure 3. A.C. Waveforms 27F64

CAPACITANCE(1) $T_A = 25°C, f = 1.0$ MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0V$

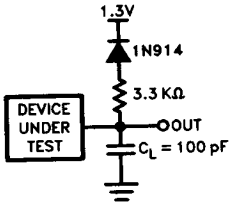
NOTE:
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".
Rise/Fall Time ≤ 10 ns

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

CONVENTIONAL OPERATION

PROGRAM MODE

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

In the conventional program mode, the 27F64 operates like the P2764A and the 27C64 EPROMs. The Quick-Pulse Programming algorithm enables one second programming of the entire flash array. (See Figure 8. Quick Pulse Programming Algorithm.)

Erasure removes charge from the flash memory memory cells leaving the array in the logic high state (0FFH). Programming injects charge onto the floating gate, changing selected cell data to the low state. Data bytes can include both unaltered erased state and programmed state bits.

The method by which you enter the 27F64 into the programming mode is as follows: raise V_{CC} to 6.25V, raise V_{PP} to 12.75V, lower $\overline{CE}$ to V_{IL}, and select the desired address. While applying eight bits of data in parallel to the device's inputs, toggle $\overline{PGM}$ low to program the byte. (See Figure 4. Conventional Programming/Verify Waveforms.)

PROGRAM VERIFY MODE

Setting V_{PP} to 12.75V, V_{CC} to 6.25V, $\overline{PGM}$ to V_{IH}, $\overline{CE}$ and $\overline{OE}$ to V_{IL}, places the device in the program verify mode. V_{CC} provides an elevated reference level which guarantees a minimum of ten years' data retention in the normal read mode.

The Quick-Pulse Programming algorithm (Figure 8) requires a final array verify after the completion of byte programming. The system should verify the entire array with V_{CC} and V_{PP} at 6V.

QUICK-ERASE™ MODE

The Quick-Erase mode of the 27F64 eliminates the requirement of U.V. light for device erasure. Electrical erasure removes charge from all bits of the array in parallel, via Fowler-Nordheim tunneling.[1] The Quick-Erase algorithm controls the electrical erasure and verification sequence. (See Figure 9. Quick-Erase algorithm.)

Enter the device into the Quick-Erase mode by lowering V_{CC} to 3.25V, raising V_{PP} and $\overline{OE}$ to 12.75V, and setting $\overline{CE}$ to V_{IL}. Toggling $\overline{PGM}$ low controls the erase pulse width. (See Figure 5. Conventional Quick-Erase/Verify Waveforms.)

ERASE VERIFY MODE

After returning $\overline{PGM}$ to a logic "1" level in the Quick-Erase mode, change $\overline{OE}$ from a high voltage level (12.75V) to V_{IL} to select the erase verify mode. Sequentially verify each address in the array for valid erased data (0FFH). V_{CC} at 3.25V provides the erased reference level for the flash memory cell. Verification at this level guarantees ten years of data integrity for normal read mode operation.

Once all bytes in the array verify, the algorithm returns the device to the read mode, and performs a final erase verify at V_{CC} = 5V.

PROGRAM AND ERASE INHIBIT MODE

With V_{PP} and V_{CC} at 5V, the 27F64 effectively bars spurious programming and erasure of the flash memory array. Other ways to control the program or erase modes include maintaining $\overline{PGM}$ or $\overline{CE}$ at a V_{IH} logic level.

inteligent Identifier™ MODE

The inteligent Identifier mode outputs the manufacturer code (89H) and device code (03H). Programming equipment automatically matches a device with its proper algorithms.

With $\overline{PGM}$ at V_{IH}, $\overline{CE}$ and $\overline{OE}$ active low, and A_1 through A_{12} at V_{IL}, raising A_9 to a high voltage level (11.5V–13V) activates the inteligent Identifier mode. Byte 0 (A_0 = V_{IL}) represents the manufacturer's code, and byte 1 (A_0 = V_{IH}) represents the device identifier.

REFERENCE

1. R. Williams, *Phys. Rev.*, Vol. 140, p. 569, 1965.

Table 5. Conventional Programming/Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Leakage Current (All Inputs)		±1.0	µA	$V_{IN} = V_{CC}$ or GND(7)
V_{IL}	Input Low Level (All Inputs)	−0.5	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5$ mA
I_{CC2}	V_{CC} Programming Current		30	mA	$\overline{CE} = V_{IL}$(3, 6)
I_{PP2}	V_{PP} Programming Current		30	mA	$\overline{CE} = V_{IL}$(3, 6)
V_H	High Voltage Detect Level	11.5	13.0	V	(Notes 4, 5)
V_{PP2}	V_{PP} Program/Verify Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)
V_{CC2}	V_{CC} Program/Verify Supply	6.0	6.5	V	$\overline{CE} = V_{IL}$(6)

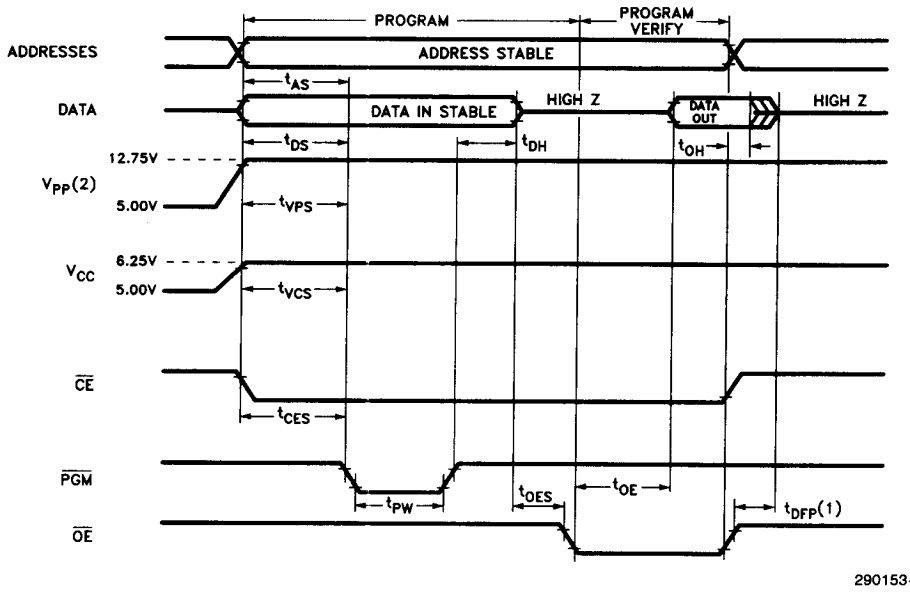
A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits				Test Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	
t_{PW}	Program Pulse Width	95	100	105	µs	Quick-Pulse™
t_{OE}	$\overline{OE}$ to Output Delay			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 27F64 before V_{PP} and removed from the device after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with the outputs unloaded during verfication.
4. V_H is the third logic level. The range of V_H encompasses the traditional 11.5V–12.5V, as well as the Quick-Pulse Programming V_{PP} range 12.5V–13.0V.
5. Forcing V_H on pin A9 and the proper levels on the control pins puts the device into the int$_e$ligent Identifier mode.
6. This specification applies to both programming and verification. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
7. During program verify, the output leakage current $I_{LO} = \pm 10$ µA maximum. $V_{OUT} = V_{CC}$ or GND.



NOTES:
1. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
2. When programming the 27F64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 4. Conventional Programming/Program Verify Waveforms

Table 6. Conventional Quick-Erase™/Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	µA	$V_{IN} = V_{CC}$ or GND(7)
V_{IL}	Input Low Voltage	-0.5	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.5$	V	(Note 1)
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	$I_{OH} = -400$ µA at V_{OH} (min)
I_{CC3}	V_{CC} Erase Current		10	mA	$\overline{CE} = V_{IL}$(5, 6)
I_{PP3}	V_{PP} Erase/Verify Current		10	mA	$\overline{CE} = V_{IL}$
V_{CC3}	V_{CC} Erase/Verify Supply	3.0	3.50	V	$\overline{CE} = V_{IL}$(6)
V_{PP3}	V_{PP} Erase/Verify Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)

A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{VPS}	V_{PP} Setup Time	2		µs	(Note 2)
t_{VCS}	V_{CC} Setup Time	2		µs	(Note 2)
t_{CES}	$\overline{CE}$ Setup Time	2		µs	
t_{EW}	Erase Pulse Width	1	1855	ms	(Note 3)
t_{OES}	$\overline{OE}$ Setup Time	2		µs	
t_{PO}	$\overline{OE}$ to V_{IH} from $\overline{PGM}$ Hi	1		µs	
t_{ACC}	Address to Output Delay	2		µs	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay	2		µs	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		ns	
t_{DFE}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 4)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. V_{CC} must be applied to the 27F64 before V_{PP} and removed from the device after V_{PP}.
3. Erase pulse width varies with pulse number. (See Quick-Erase Algorithm.)
4. This parameter is only sampled and not 100% tested.
5. The maximum current value is with the outputs unloaded during verification.
6. This specification applies to both erasure and verification. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
7. During erase verify, the output leakage current $I_{LO} = \pm 10$ µA maximum. $V_{OUT} = V_{CC}$ or GND.

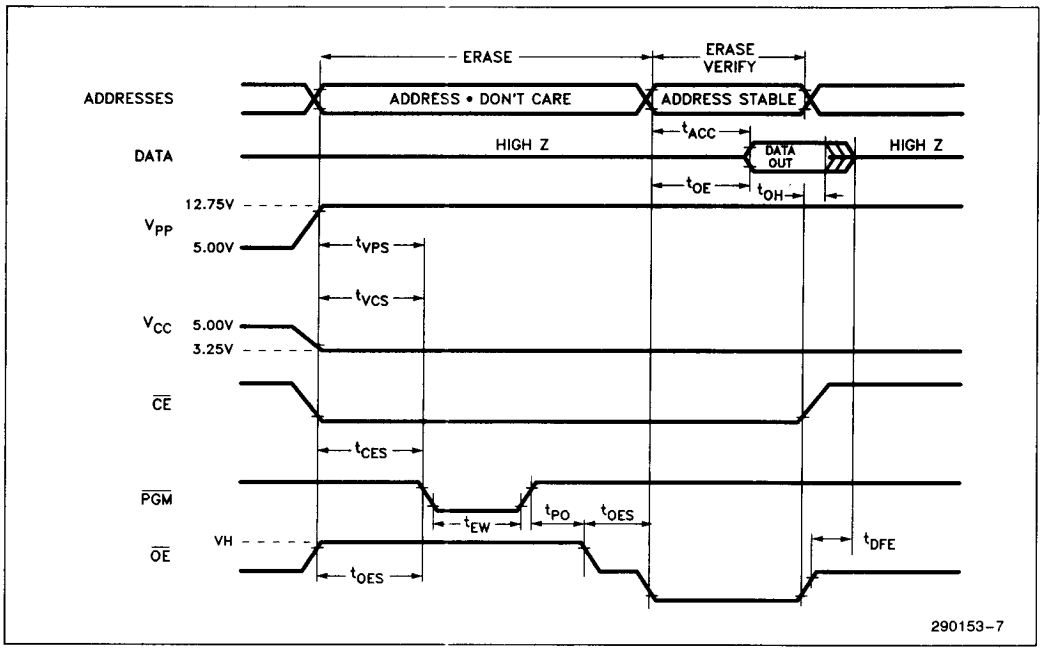


Figure 5. Conventional Quick-Erase™/Verify Waveforms

ON-BOARD OPERATION

Board level designers and manufacturers prefer to delay EPROM programming until the last possible moment. Benefits include the ability to change code between testing and end-of-line configuration, inventory control, and reduced costs. Efficient algorithms, such as Intel's Quick-Pulse Programming algorithm, enable EPROM programming to take place during the board assembly process, or afterwards with the EPROM in-circuit.

Intel's 27F64 flash memory simplifies in-module programming* by offering designers the On-Board modes. These modes transfer the non-TTL voltages to pins generally unused in EPROM-based system design: $\overline{PGM}$ and V_{PP}. V_{CC} maintains 5.0V throughout all operations. Internal circuitry derives the erase and program reference levels from V_{PP} instead of from V_{CC}. Since systems rarely connect $\overline{PGM}$ to a common bus with other types of memory, the On-Board modes select certain features with $\overline{PGM}$ at V_H rather than $\overline{OE}$ at V_H. A similar argument holds for specifying a new int$_e$ligent Identifier mode that maintains A_9 at TTL logic levels.

Differences in mode implementation have been highlighted in Table 7 for your convenience.

*A few issues arise from programming EPROMs on-board. EPROMs should be programmed and verified at an elevated V_{CC} to insure proper cell margins and long term data retention. PROM programmers can accommodate this V_{CC} voltage easily; however, other logic devices populating the board might not operate predictably. One solution to this problem involves running separate V_{CC} traces to the edge connector. The 3.25V V_{CC} level needed for the conventional Quick-Erase algorithm poses similar problems. Specifying A_9 at a V_H level to read the int$_e$ligent Identifier, and $\overline{OE}$ at V_H to erase, forces the board designer to add extra buffering and isolation circuitry.

Table 7. On-Board Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Program/Erase Inhibit	X	X	X	X	X	V_{CC}(4)	5.0V	
Program	V_{IL}	V_{IH}	V_{IL}	X	X	12.75V	5.0V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_H(2)	X	X	6.25V	5.0V	D_{OUT}
Quick-Erase	V_{IL}(5)	V_{IH}	V_H	X	X	12.75V	5.0V	High Z
Erase Verify	V_{IL}	V_{IL}	V_H	X	X	3.25V	5.0V	D_{OUT}
Int$_e$ligent ID™ Manufacturer	V_{IL}	V_{IL}	V_{IL}	V_{IL}(3)	V_{IL}(3)	V_{CC}	5.0V	89H
Int$_e$ligent ID™ Device	V_{IL}	V_{IL}	V_{IL}	V_{IL}(3)	V_{IH}(3)	V_{CC}	5.0V	03H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $11.5 \leq V_H \leq 13.0V$.
3. A_1–$A_{12} = V_{IL}$.
4. With $V_{PP} \leq V_{CC}$ the 27F64 inhibits all erase and program functions.
5. $\overline{CE}$ controls the erase pulse width.

SIMILARITIES TO CONVENTIONAL MODES

The On-Board read, output disable, standby, and program/erase inhibit modes all operate identically to the conventional equivalent modes. See appropriate conventional mode sections for descriptions and details.

PROGRAM MODE

With the exception of V_{CC} specified at 5V, the On-Board program mode functions exactly like its standard EPROM counterpart. Programming with V_{CC} at 5V eliminates the need for dual V_{CC} power buses for in-circuit programming. Users of On-Board programming still enjoy all the benefits attributed to Intel's Quick-Pulse Programming algorithm. (See Figure 8. Quick-Pulse Programming Algorithm, and Figure 6. On-Board Programming/Verify Waveforms.)

PROGRAM VERIFY MODE

After completing each program pulse ($\overline{PGM}$ transition from logic 0 to 1), lower V_{PP} to 6.25V, raise $\overline{PGM}$ to V_H level (11.5V–13.0V), and set $\overline{OE}$ to V_{IL} to enter the program verify mode. Invalid data indicates the need for another program pulse; lower $\overline{PGM}$ from V_H to V_{IH} prior to raising V_{PP} to 12.75V. Valid data indicates completion of the programming loop.

The Quick-Pulse Programming algorithm (Figure 8) requires a final array verify after completion of byte programming. The system should verify the entire array with V_{PP} at 6V, and $\overline{PGM}$ at V_H.

QUICK-ERASE™ MODE

To select the Quick-Erase mode, set $\overline{CE}$ and $\overline{OE}$ to V_{IH}, V_{CC} to 5.0V, V_{PP} to 12.75V, and $\overline{PGM}$ to V_H (11.5V–13.0V). Toggle $\overline{CE}$ low for the predetermined erase pulse width. Note that $\overline{CE}$ controls the erase time in the On-Board mode, not $\overline{PGM}$. (See Figure 7. On-Board Erase/Verify Waveforms and Figure 9. Quick-Erase Algorithm.)

ERASE VERIFY MODE

To transition from Quick-Erase to erase verify mode, raise $\overline{CE}$ to V_{IH} for 1 μs, then lower V_{PP} below 2V, and $\overline{CE}$ to V_{IL} for 2 μs. Raise V_{PP} to the 3.25V erase verify level, place the address to be verified on the bus, and gate the data from the device outputs by lowering $\overline{OE}$ to V_{IL}. Continue checking through the array until an address does not verify, and then raise $\overline{CE}$ to V_{IH} to set up for the next erase pulse.

inteligent Identifier™ MODE

Board programmers can read the On-Board inteligent Identifier™ by setting V_{CC} and V_{PP} to 5.0V, A_1–A_{12} to V_{IL}, and $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ to V_{IL}. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer's code (89H) and byte 1 ($A_0 = V_{IH}$) represents the device identifier (03H).

Table 8. On-Board Program/Program Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$ (Notes 1, 2)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{CC4}	V_{CC} Program/Verify Current		30	mA	$\overline{CE} = V_{IL}$(4, 5, 6)
I_{PP4}	V_{PP} Program/Verify Current		30	mA	$\overline{CE} = V_{IL}$(4, 5, 6)
V_{CC4}	V_{CC} Program/Verify Supply	4.50	5.50	V	$\overline{CE} = V_{IL}$(5, 6)
V_{PP4}	V_{PP} Program Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(6)
V_{PPV4}	V_{PP} Verify Supply	6.0	6.5	V	$\overline{CE} = V_{IL}$(6)

A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{AS}	Address Setup Time	2		µs	
t_{DS}	Data Setup Time	2		µs	
t_{VPS}	V_{PP} Setup Time	2		µs	
t_{CES}	$\overline{CE}$ Setup Time	2		µs	
t_{PW}	Program Pulse Width	95	105	µs	
t_{DH}	Data Hold Time	2		µs	
t_{VPH}	V_{PP} Hold Time from $\overline{PGM} = V_{IH}$	0		µs	
t_{MS}	Margin Setup Time	0		µs	
t_{OES}	$\overline{OE}$ Setup Time	2		µs	
t_{OE}	$\overline{OE}$ to Output Delay		150	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0			
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 3)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 27F64 before V_{PP} and removed from the device after V_{PP}.
2. See Conventional and On-Board Read Operation D.C. Characteristics tables for I_{LI}, I_{LO}, V_{IL}, V_{IH}, V_{OL} and V_{OH} values.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.
4. The maximum current value is with the outputs unloaded during verification.
5. This specification applies to both programming and verification.
6. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.

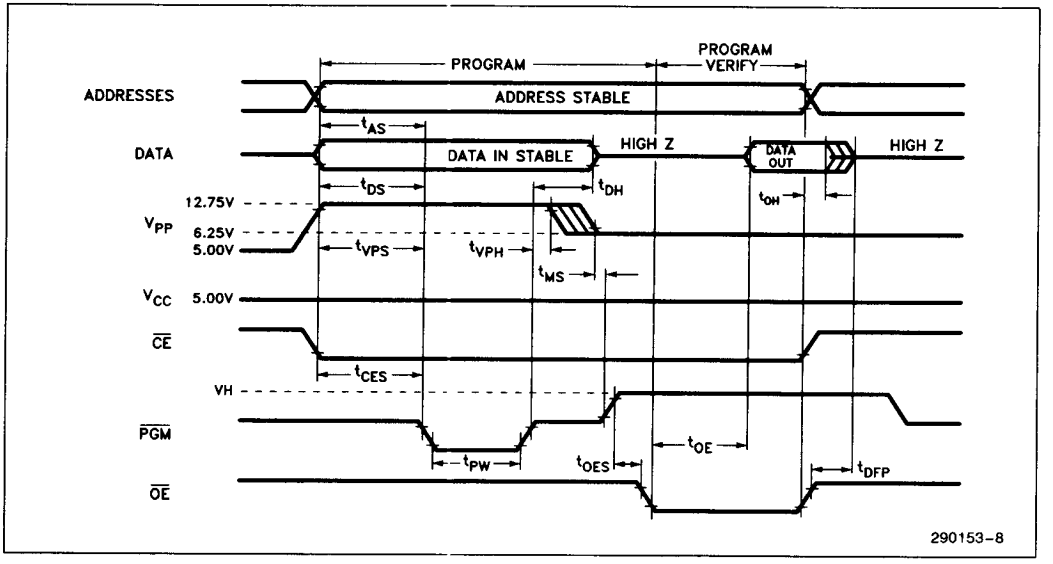


Figure 6. On-Board Programming/Verify Waveforms

Table 9. On-Board Quick-Erase™/Erase Verify Operation

D.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$ (Notes 1, 2)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{CC5}	V_{CC} Erase Current		10	mA	$\overline{CE} = V_{IL}$(5, 7)
I_{CCV5}	V_{CC} Erase/Verify Current		30	mA	$\overline{CE} = V_{IL}$(5, 7)
I_{PP5}	V_{PP} Erase/Verify Current		10	mA	$\overline{CE} = V_{IL}$(5, 6, 7)
V_{CC5}	V_{CC} Erase/Verify Supply	4.50	5.50	V	$\overline{CE} = V_{IL}$(6, 7)
V_{PP5}	V_{PP} Erase Supply	12.5	13.0	V	$\overline{CE} = V_{IL}$(7)
V_{PPV5}	V_{PP} Verify Supply	3.0	3.50	V	$\overline{CE} = V_{IL}$(7)

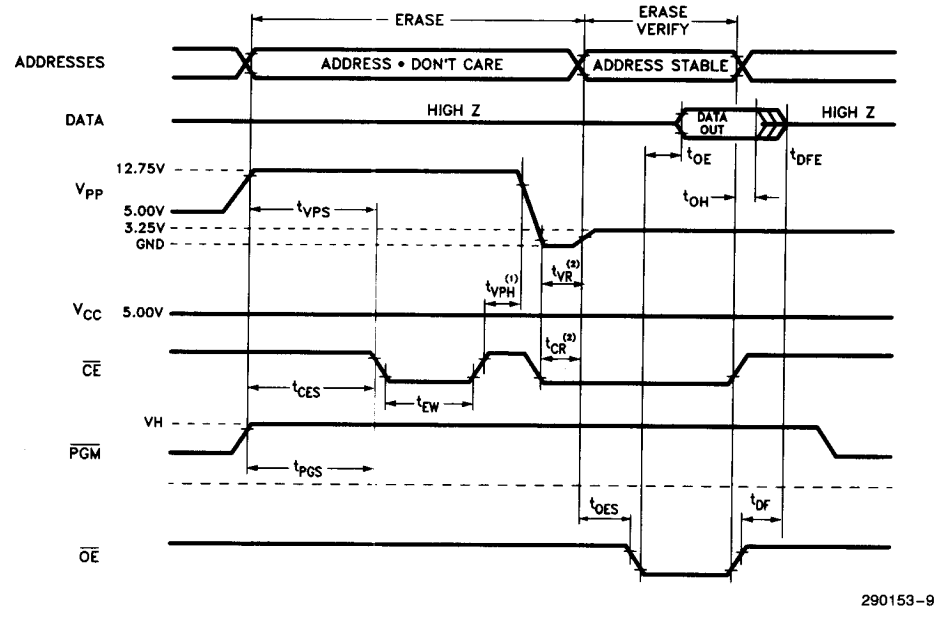
A.C. CHARACTERISTICS $T_A = 25°C \pm 15°C$

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{VPS}	V_{PP} Setup Time	2		µs	
t_{CES}	$\overline{CE}$ Setup Time	2		µs	
t_{PGS}	$\overline{PGM}$ Setup Time	2		µs	
t_{EW}	Erase Pulse Width	1	1855	ms	(Notes 3, 8)
t_{VPH}	V_{PP} Hold Time from $\overline{CE} = V_{IH}$	1		µs	
t_{VR}	V_{PP} Recovery Time	2		µs	
t_{CR}	$\overline{CE}$ Recovery Time	2		µs	
t_{OES}	$\overline{OE}$ Setup Time	2		µs	
t_{OE}	$\overline{OE}$ to Output Delay	150		ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0			
t_{DFE}	$\overline{OE}$ High to Output Float Delay	0	130	ns	(Note 4)

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) . . . . . 10 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

NOTES:
1. V_{CC} must be applied to the 27F64 before V_{PP} and removed from the device after V_{PP}.
2. See conventional and On-Board Read Operation D.C. Characteristics for I_{LI}, I_{LO}, V_{IL}, V_{IH}, V_{OL} and V_{OH} values.
3. Erase pulse width varies with pulse number. (See Quick-Erase algorithm.)
4. This parameter is only sampled and not 100% tested.
5. The maximum current value is with the outputs unloaded during verification.
6. This specification applies to both programming and verification.
7. See timing waveforms for $\overline{PGM}$ and $\overline{OE}$ test conditions.
8. $\overline{CE}$ controls the erase pulse width in the On-Board Quick-Erase mode.



NOTES:
1. Raise $\overline{CE}$ to complete the erase pulse prior to lowering V_{PP}.
2. V_{PP} and $\overline{CE}$ must be at V_{IL} at the same time, for a period of 2 μs. V_{PP} must be lowered to V_{IL} prior to lowering $\overline{CE}$ to V_{IL}.

Figure 7. On-Board Quick-Erase™/Verify Waveforms

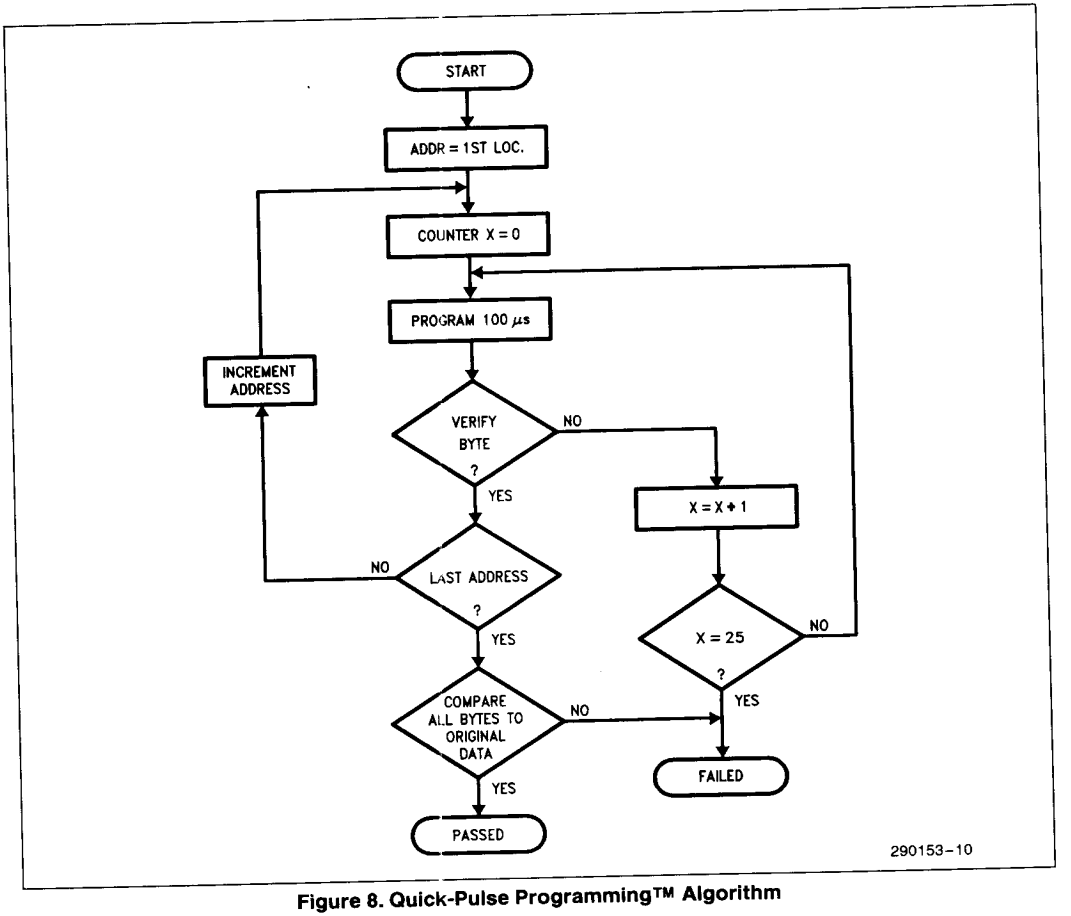
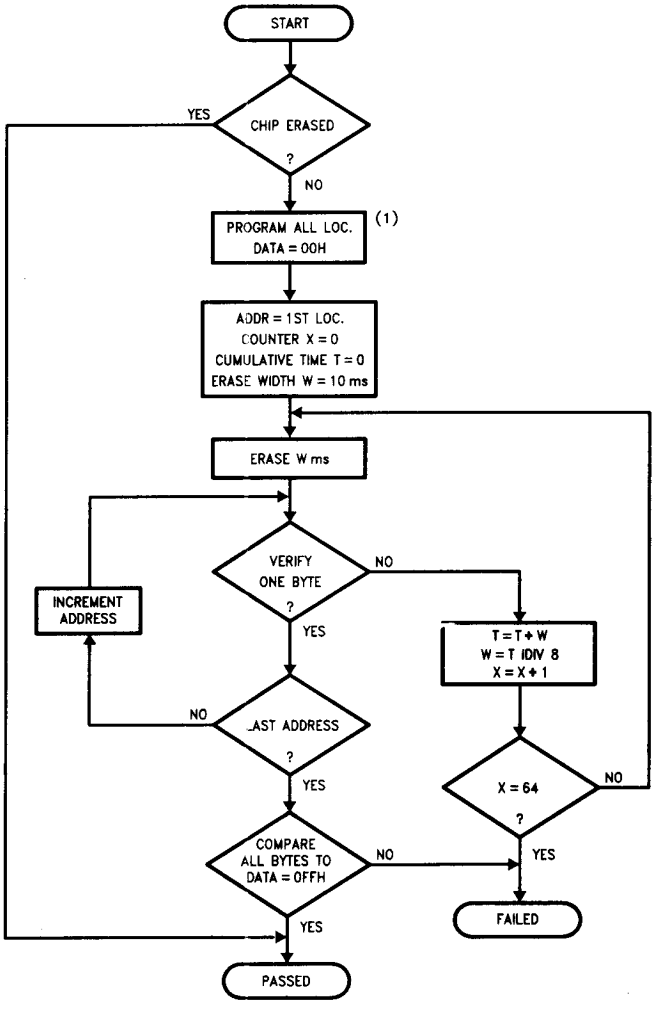


Figure 8. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING™ CHARACTERISTICS

The Quick-Pulse Programming algorithm specifies a higher V_{PP} voltage than the int$_e$ligent Programming™ algorithm to provide greater programming energy. This energy leads to faster device programming. A higher reference level checks cell margin and eliminates the time consuming over-program pulses. After entering the program mode, toggle $\overline{PGM}$ low for 100 μs, and immediately follow with a byte verification. The algorithm allows up to twenty-five program pulses per byte, although most bytes verify on the first or second pulse. When all bytes have been programmed, set V_{PP} or V_{CC} to its 6.0V final verify mode voltage. Compare all bytes to the original data to confirm proper programming. See Figure 8 for the Quick-Pulse Programming algorithm.

NOTE:
Use the program verify mode for this final verify. Choice of supply (V_{PP} or V_{CC}) depends on implementation. Use of the conventional program verify mode requires setting V_{CC} equal to 6.0V ±0.25V for final verify, use of the On-Board program verify mode requires setting V_{PP}.



NOTE:
1. Program the array using Quick-Pulse Programming™ algorithm.

Figure 9. Quick-Erase™ Algorithm

QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm enables efficient removal of charge from all bits in the array simultaneously. The algorithm erases the device for the minimum amount of time necessary to simulate U.V. erasure, by employing a closed-loop flow similar to Quick-Pulse Programming. Although the algorithm allows a maximum erase time of 10 seconds, erasure usually occurs within 1–2 seconds. This is three orders of magnitude faster than typical U.V. erase times.

Prior to erasing a device, you should check its present status. If it passes the erase verify test, go directly to code programming. Flash memories leave

the factory in the erased state for your convenience. You must begin the Quick-Erase algorithm by equalizing the amount of charge stored on each cell by Quick-Pulse Programming the array to 00H. This provides for a uniform and reliable erasure of the array. Erase execution then continues with an initial erase pulse of 10 ms. Erase verification (data = FFH) starts at address 00H and continues through the array until the end, or until a byte reads data other than 0FFH. With each erase pulse, an increasing number of bytes will verify to the erased state. To improve efficiency, store the last byte verified in a register. After the next erase pulse, you can resume verification at that address rather than at the beginning of the array.

Upon finding a byte that does not verify, calculate the next erase pulse width (W) as follows:

a) add the current erase pulse-width (W) to the cumulative erase time (T)—
$$T = T + W;$$
b) integer divide the new cumulative erase time (T) by 8—
$$W = T \text{ IDIV8};$$
c) increment the pulse counter (X) by 1—
$$X = X + 1.$$

Note that step b, which produces the next erase pulse width (W), should be an integer divide-by-8, with the remainder truncated. This division can be easily accomplished by 3 subsequent register shifts right. A total of sixty-four erase pulses are allowed, which corresponds to approximately 10 seconds of cumulative erase time.

Once all bytes in the array verify, the algorithm returns the device to the read mode, and performs a final erase verify at V_{CC} = 5V.

SYSTEM DESIGN CONSIDERATIONS

Two Line Output Control

Flash memories are often used in larger memory arrays. Intel provides two read control inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder output should enable $\overline{CE}$, while the system's read signal controls all flash memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low-power standby condition.

Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of Chip Enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and GND, and between V_{PP} and GND (V_{PP} specifically in On-Board programming applications).

Place the high frequency, low inherent inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Use of On-Board programming features requires the printed circuit board designer to pay extra attention to the V_{PP} power supply trace. Flash memories program via hot electron injection onto the floating gate. The V_{PP} pin supplies the memory cell currents for programming. Use similar trace widths and layout consideration as given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

See the application note AP-74, High Speed Memory System Design Using 2147H, for more details on decoupling and power bus layout considerations (gridding), etc.

Power Up/Down Sequencing

Upon powering up the 27F64, V_{CC} must reach its steady state value before raising V_{PP} to the 12.75V level. In addition, upon power down, V_{PP} must be at ground before lowering V_{CC}. Failure to follow either of the above sequences could inadvertently place the 27F64 into the Quick-Erase or Program mode.

Additional Information	Order Number
AP-314 "The 27F64 Flash Memory—Your Solution for On-Board Programming"	292043
ER-19 "The Intel 27F64 Flash Memory"	294003
ER-20 "ETOX™ Flash Memory Technology"	294005
RR-60 "ETOX™ Flash Memory Reliability Data Summary"	293002