NEC
ELECTRON DEVICE

DATA SHEET

MOS INTEGRATED CIRCUIT

μPD35H74

2 592-BIT CCD LINEAR IMAGE SENSOR

The μPD35H74 is a 2 592-bit linear image sensor consisting of charge coupled devices (CCDs), which convert light to voltage. This product is made up of a 2 592-bit photosensor array, charge transfer register with a pair of 1 296-bit CCDs. The photosensor has a 11 μm pitch.

FEATURES

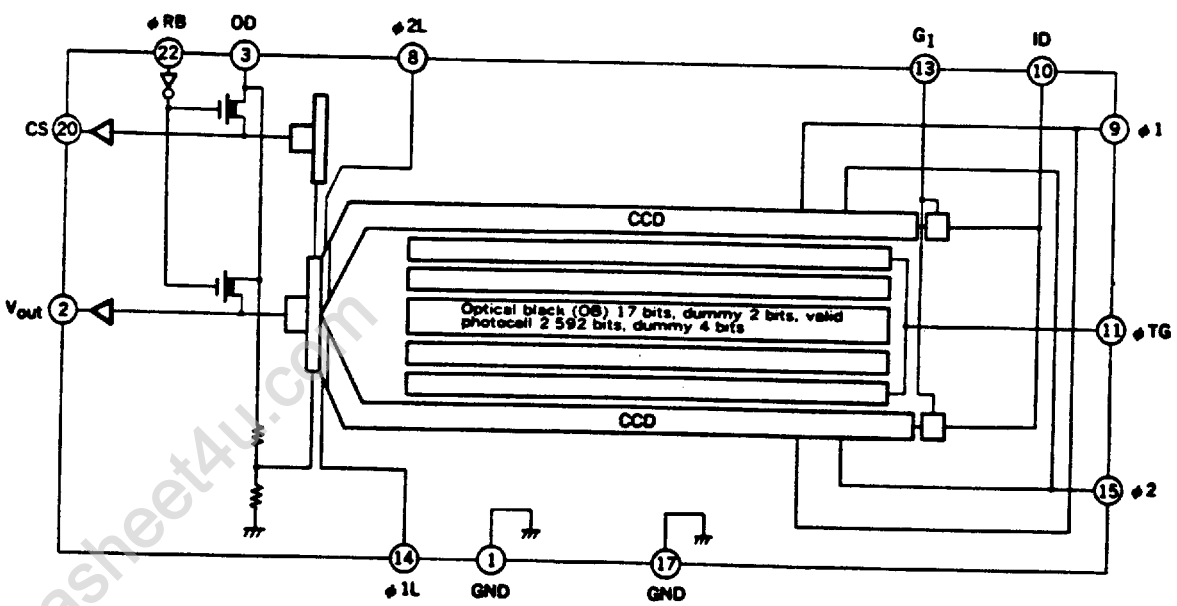
- High response sensitivity: Providing a response ten times better than the existing equivalent NEC product (μPD3574D) to the light from a white fluorescent lamp
- Peak response wavelength: 550 nm green
- Reads the shorter side of a A4-size sheet at a resolution of 12 dot/mm
- Driven by a 12 V single power supply
- All signal clock input: drive by CMOS 5 V

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD35H74D	22-pin ceramic DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

BLOCK DIAGRAM



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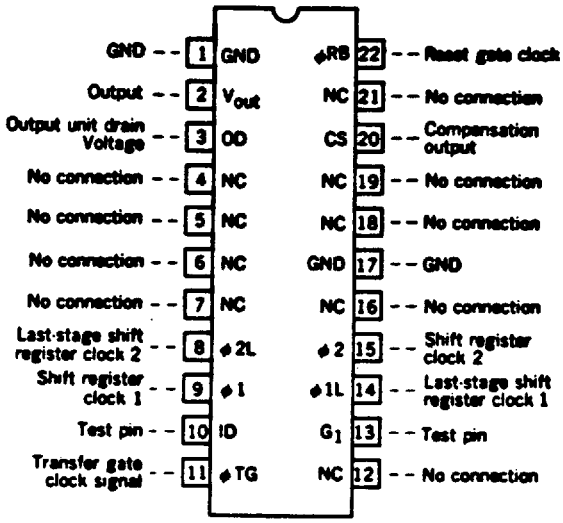
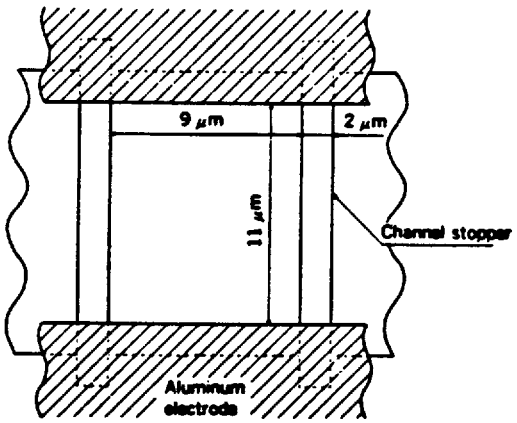
PIN CONNECTION DIAGRAM (Top View)



PHOTOELEMENT STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Output unit drain voltage	V_{OD}	−0.3 to +15	V
Test pin ID voltage	V_{ID}	−0.3 to +15	V
Shift register clock signal voltage	$V_{\phi 1}$	−0.3 to +15	V
	$V_{\phi 2}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi RB}$	−0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −25 to +60 °C)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output unit drain voltage	V_{OD}	11.4	12.0	12.6	V
Test pin G_1 voltage	G_1		0		V
Test pin ID voltage	V_{ID}	11.4	12.0	12.6	V
Shift register clock φ1, φ1L signal high level	$V_{\phi 1H}$	4.5 (V_{OD}−3)	5.0 (V_{OD})	5.5 (V_{OD}+0.6)	V
Shift register clock φ1, φ1L signal low level	$V_{\phi 1L}$	−0.3 (−0.3)	0 (0)	0.5 (0.8)	V
Shift register clock φ2, φ2L signal high level	$V_{\phi 2H}$	4.5 (V_{OD}−3)	5.0 (V_{OD})	5.5 (V_{OD}+0.6)	V
Shift register clock φ2, φ2L signal low level	$V_{\phi 2L}$	−0.3 (−0.3)	0 (0)	0.5 (0.8)	V
Reset signal RBH high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset signal RBL low level	$V_{\phi RBL}$	−0.3	0	0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5 (V_{OD}−3)	$V_{\phi 1H}$	$V_{\phi 1H}$	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3 (−0.3)	0 (0)	0.5 (0.8)	V
Data rate	$f_{\phi R}$	0.2	1	10	MHz

Remark: ( ) is the case of input signal clock 12 V.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{OD} = 12.0 V, $f_{\phi 1}$ = 0.5 MHz, data rate = 1 MHz, storage time = 10 ms, light source: 3 200 K Halogen-lamp + C500 (Cut-filter of infrared light), Input signal clock = 5 V_{p-p})

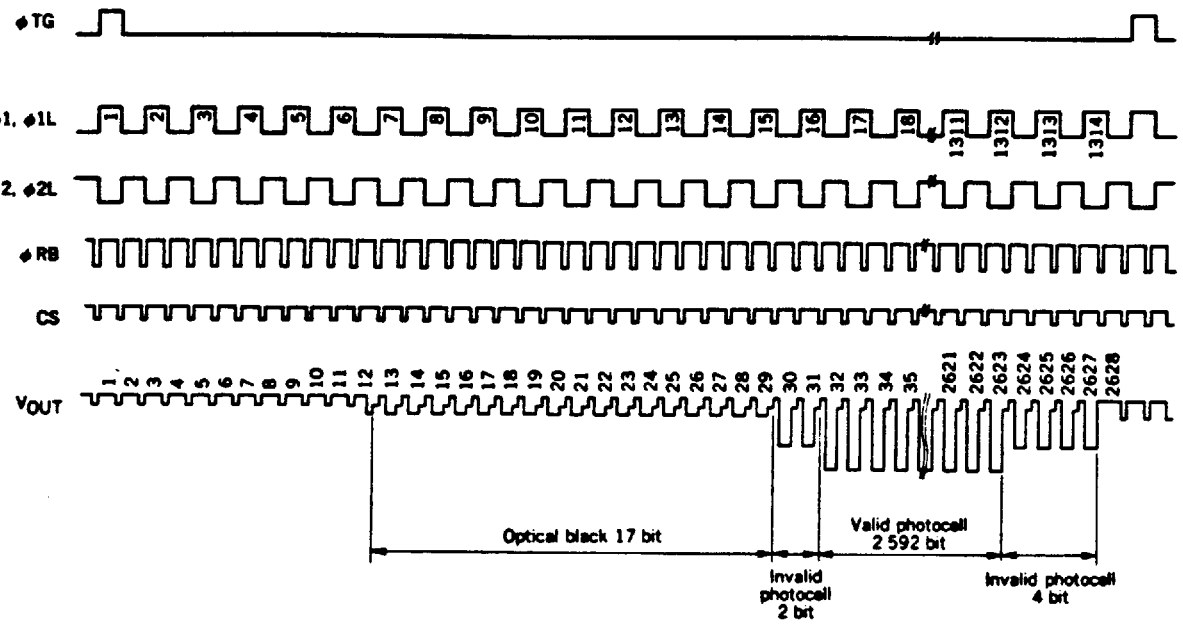
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Saturation voltage	V_{sat}	1.5	2.0		V	
Saturation exposure	SE		0.28		L_{XS}	white fluorescent lamp
Photo response non-uniformity	PRNU		±2	±8	%	V_{out} = 500 mV
Average dark signal	ADS		0.1	5	mV	light shielding
Dark signal non-uniformity	DSNU	−5	0.5	+5	mV	light shielding
Power consumption	P_W		80	150	mW	
Output impedance	Z_O		0.5	1	kΩ	
Response	R_F	4.9	7.0	9.1	V/L_{XS}	white fluorescent lamp
	R_W		21.0			W lamp
Response peak wavelength			550		nm	
Image lag	IL		2	5	%	V_{out} = 500 mV
Offset level	V_{OS}	5.0	7.0	9.0	V	
Input capacity of shift register clock pin	$C_{\phi 1}$		700		pF	
	$C_{\phi 2}$		700			
Reset pin input capacity	$C_{\phi RB}$		5		pF	
Input capacity of transfer gate signal pin	$C_{\phi TG}$		100		pF	
Output rise delay time	t_d		20		ns	
Register in-balance	RI			3	%	V_{out} = 500 mV
Transfer efficiency	TTE	92			%	V_{out} = 500 mV, $f_{\phi R}$ = 10 MHz
Dynamic range	DR		4000		times	V_{sat}/DSNU
Reset field-through noise	RFSN	−300	−100	200	mV	
AC-voltage of compensation output	V_{CSOF}	5.0	7.0	9.0	V	
AC-voltage of off-set level to compensation output	$\lvert V_{OS}-V_{CSOF}\rvert$			300	mV	

Remark:

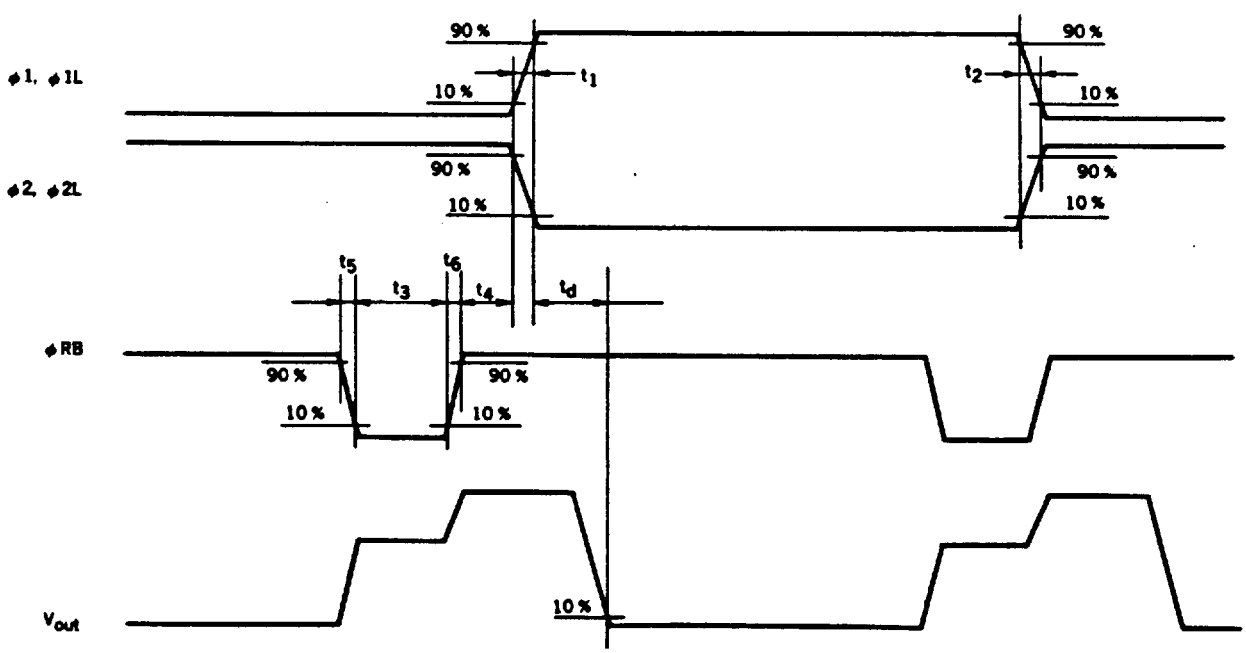
RFSN is changed by V_{OD}. The change ration: $\frac{\Delta RFSN}{\Delta V_{OD}} \fallingdotseq \frac{90\ mV}{0.6\ V}$

Therefore within recommended operating condition (V_{OD} = 12 V±0.6 V), RFSN's dispersion has −390 mV to +290 mV.

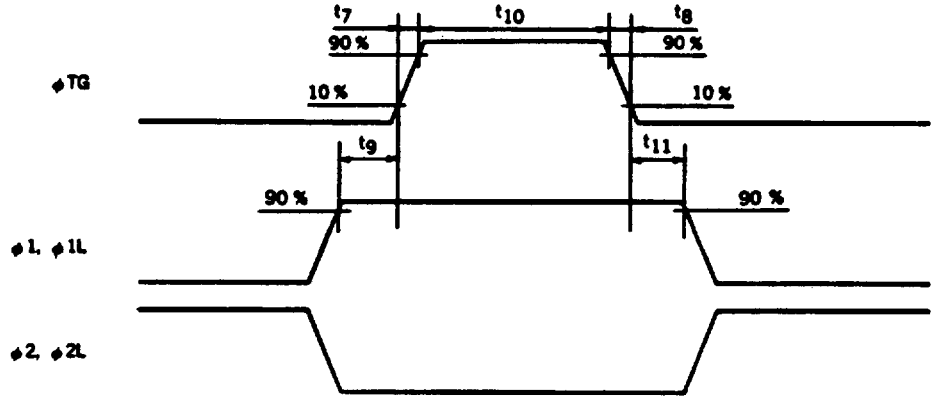
TIMING CHART



Timing chart for $\phi 1$, $\phi 1L$, $\phi 2$, $\phi 2L$, ϕRB, V_{out}



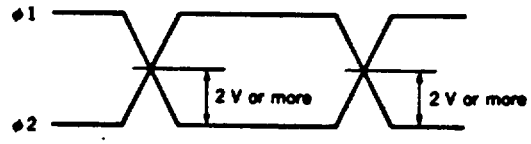
Timing chart for φTG, φ1, φ1L, φ2, φ2L



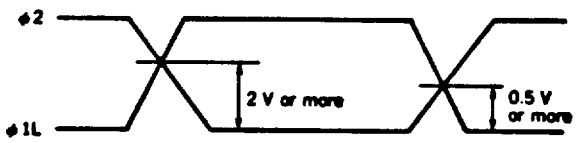
(Unit: ns)

ITEM	MIN.	TYP.	MAX.
t_1, t_2	0	50	150
t_3	20	100	(500)
t_4	20	100	(500)
t_5, t_6	0	50	50
t_7, t_8	0	50	100
t_9, t_{11}	0	100	(500)
t_{10}	500	1000	(5000)

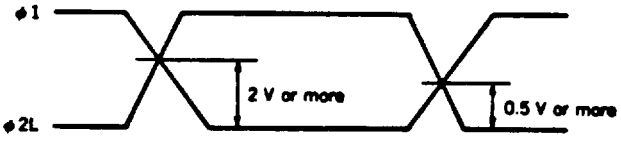
Cross points φ1, φ2



Cross points φ1L, φ2



Cross points φ1, φ2L



Remark: Please adjust input-resistance of terminal φ1, φ2, φ1L, φ2L about cross points between (φ1, φ2), (φ1L, φ2), (φ1, φ2L).

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DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}

   The point at which the response linearity is lost.

2. Saturation exposure: SE

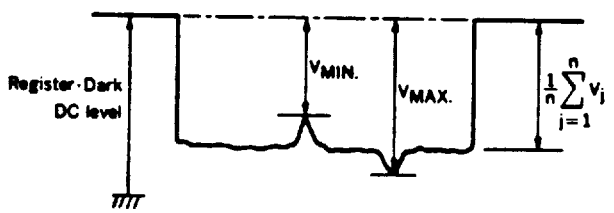
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs

3. Photo response non-uniformity: PRNU

   Expressed by the following expressing with the peak/bottom ratio to the average output voltage of all the valid bits.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

   n : Number of valid bits
   V_j : Output voltage of each bit



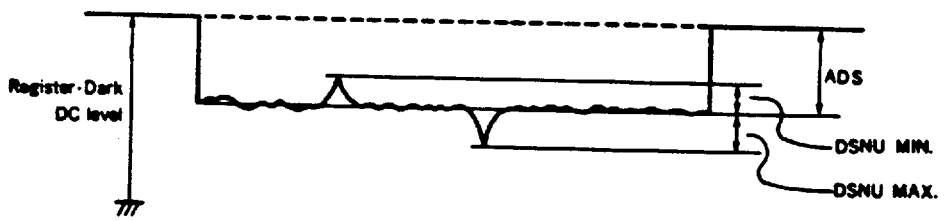
4. Average dark signal: ADS

   Output average voltage in light shielding

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark signal non-uniformity: DSNU

   The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Z_O

   Output pin impedance when viewed externally

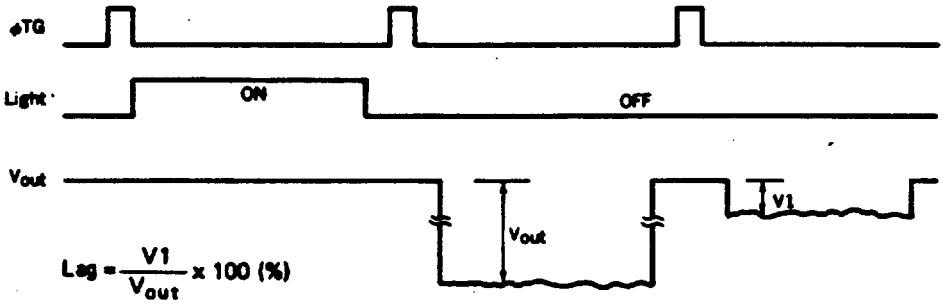
7. Response: R

   Output voltage divided by exposure (lx·s).

   Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of one line.



$$Lag = \frac{V1}{V_{out}} \times 100\ (\%)$$

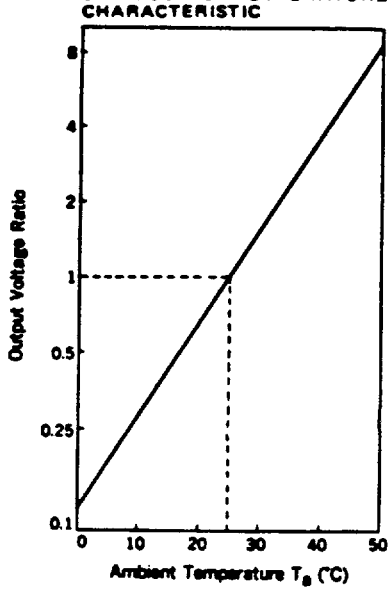
9. Register Imbalance: RI

The rate between the average output voltage which is the difference between the output voltage from Odd and Even bits, and the average output voltage of all the valid bits.

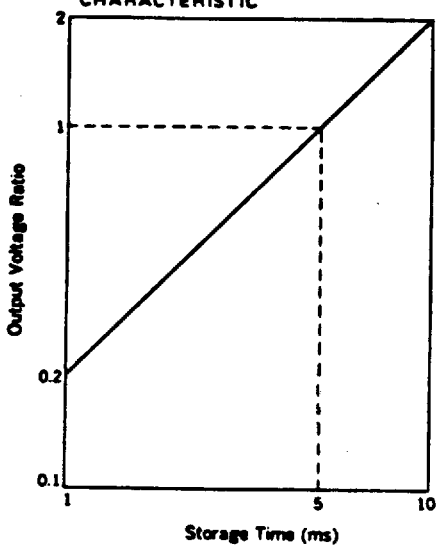
$$RI = \frac{\frac{1}{n}\sum_{j=1}^{n} |V_j - V_{j+1}|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100\ (\%)$$

STANDARD CHARACTERISTIC CURVES (T_a = 25 °C)

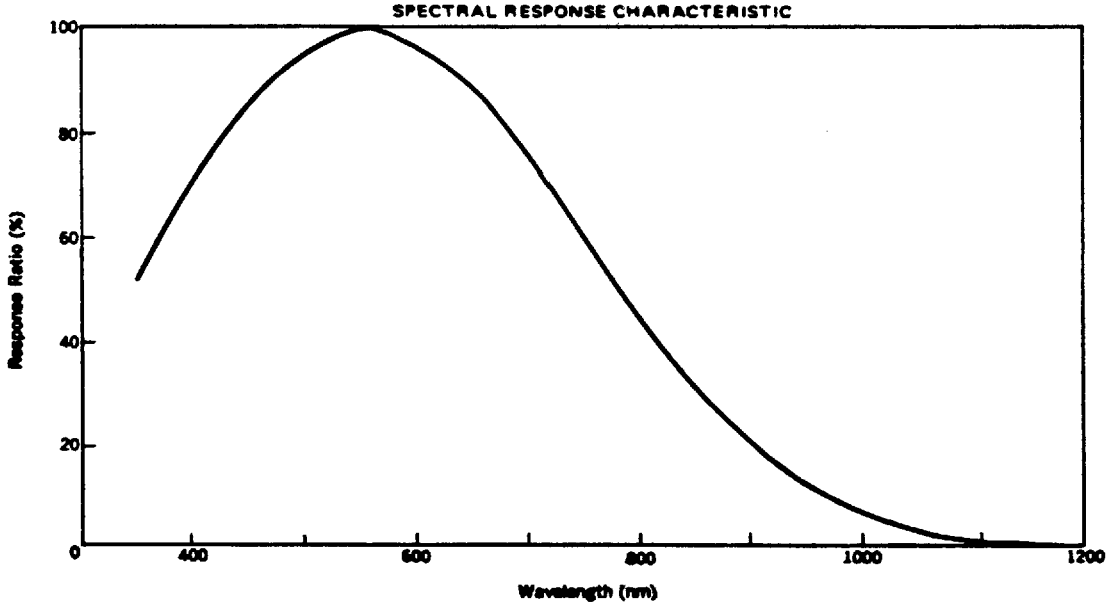
DARK OUTPUT TEMPERATURE CHARACTERISTIC



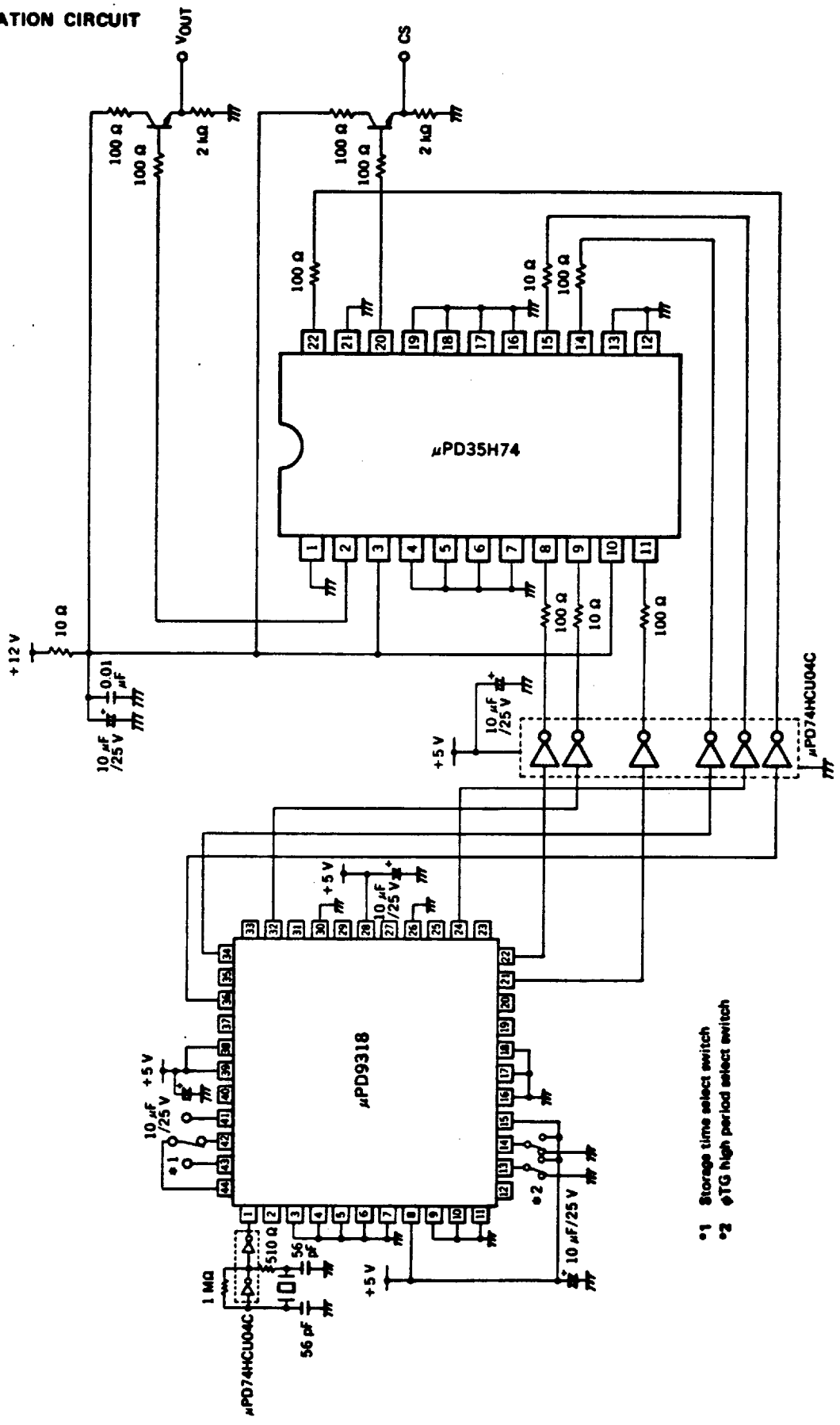
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC



SPECTRAL RESPONSE CHARACTERISTIC

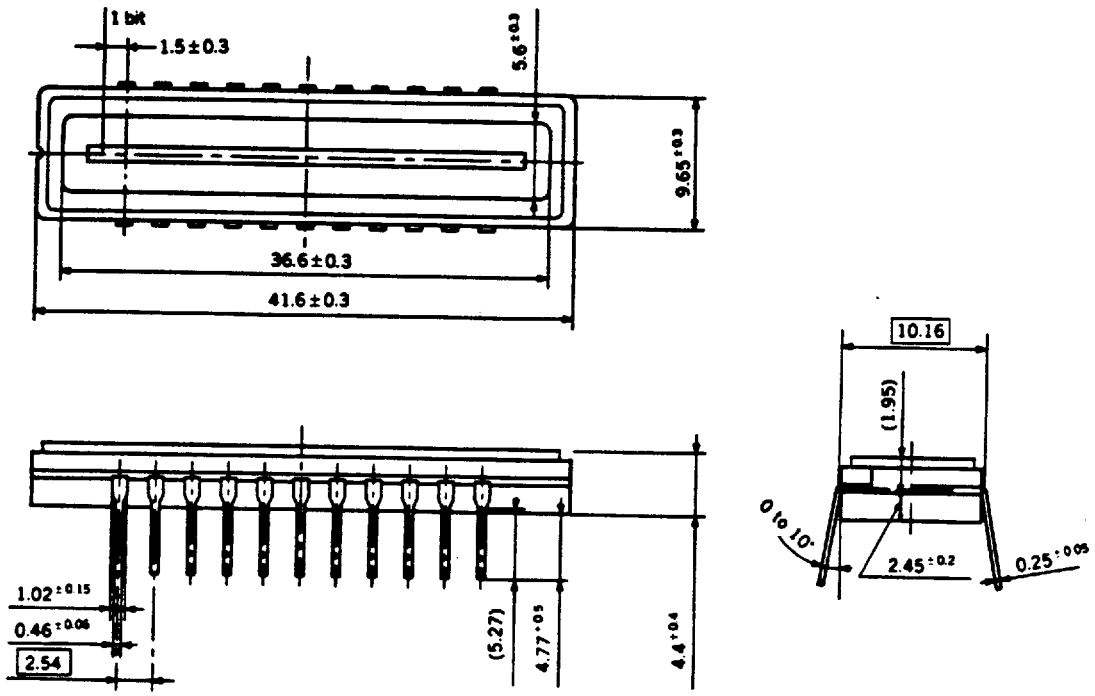


APPLICATION CIRCUIT



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS (Unit: mm)



Name	Dimensions	Refractive index
Glass cap	39.5 × 9.0 × 0.7	1.5