

T-33-29

0.5-Ampere N-P-N Darlington Power Transistors

h_{FE} Min. — 10,000
 1.33 Watt power dissipation at $T_A = 25^\circ$

Features:

- Operates from IC without predriver

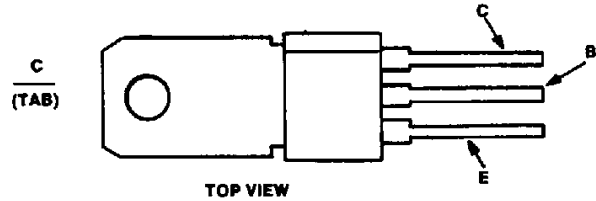
Application:

- Solenoid Driver
- Lamp Driver
- Relay Substitute
- Switching Regulator

The D40C-series silicon n-p-n Darlington power transistors are designed for use in general-purpose amplifier and medium-speed switching circuits. The high gain of these devices makes it possible for them to be driven directly from integrated circuits. The monolithic base-to-emitter resistors have been deleted from the structure to enhance the gain characteristics. These devices feature minimum gains of 10,000.

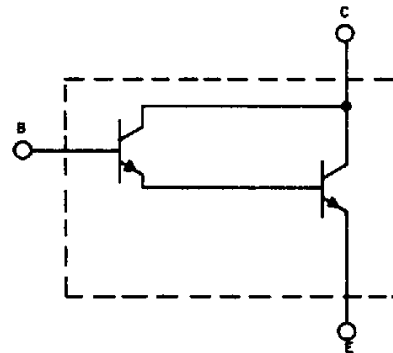
These devices are supplied in the JEDEC TO-202AB plastic package.

TERMINAL DESIGNATIONS



92CS-4322

JEDEC TO-202AB



92CS-43150

Schematic diagram for all types.

POWER TRANSISTORS

MAXIMUM RATINGS ($T_A = 25^\circ C$) (unless otherwise specified)

RATING	SYMBOL	D40C1	D40C4	D40C7	UNITS
Collector-Emitter Voltage	V_{CEO}	30	40	50	Volts
Collector-Emitter Voltage	V_{CES}	30	40	50	Volts
Emitter Base Voltage	V_{EBO}	13	13	13	Volts
Collector Current — Continuous	I_C	0.5	0.5	0.5	A
Collector Current — Peak ⁽¹⁾	I_{CM}	1.0	1.0	1.0	A
Base Current — Continuous	I_B	0.1	0.1	0.1	A
Total Power Dissipation: @ $T_A = 25^\circ C$ @ $T_C = 25^\circ C$	P_D	1.33 6.25	1.33 6.25	1.33 6.25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	$^\circ C/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	20	20	$^\circ C/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	260	260	260	$^\circ C$

(1) Pulse Test: Pulse Width = 300ms. Duty Cycle \leq 2%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ C$) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
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OFF CHARACTERISTICS⁽¹⁾

T-33-29

Collector-Emitter Voltage ($I_C = 10mA$)	D40C1	V _{CEO}	30	—	—	Volts
	D40C4		40	—	—	
	D40C7		50	—	—	
Collector Cut-off Current ($V_{CE} = \text{Rated } V_{CE}$)	($T_C = 25^\circ C$)	I _{CES}	—	—	0.5	μA
	($T_C = 150^\circ C$)	I _{CBO}	—	—	20	
Emitter Cutoff Current ($V_{EB} = 13V$)		I _{EBO}	—	—	0.1	μA

SECOND BREAKDOWN

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 2
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ON CHARACTERISTICS⁽¹⁾

DC Current Gain ($I_C = 200mA, V_{CE} = 5V$)	h_{FE}	10K	—	60K	
Collector-Emitter Saturation Voltage ($I_C = 500mA, I_B = 0.5mA$)	V _{CE(sat)}	—	—	1.5	V
Base-Emitter Saturation Voltage ($I_C = 500mA, I_B = 0.5mA$)	V _{BE(sat)}	—	—	2.0	Volts

DYNAMIC CHARACTERISTICS

Collector Capacitance ($V_{CB} = 10V, f = 1MHz$)	C _{CBO}	—	—	220	pF
Current Gain - Bandwidth Product ($I_C = 20mA, V_{CE} = 5V$)	f _T	—	75	—	MHz

SWITCHING CHARACTERISTICS

Resistive Load					
Delay Time + Rise Time	$I_C = 1A, I_{B1} = I_{B2} = 1mA$ $V_{CC} = 30V, t_p = 25 \mu sec$	t _d + t _r	—	100	ns
Storage Time		t _s	—	350	
Fall Time		t _f	—	800	

(1) Pulse Test: PW \leq 300ms Duty Cycle \leq 2%.

HARRIS SEMICOND SECTOR

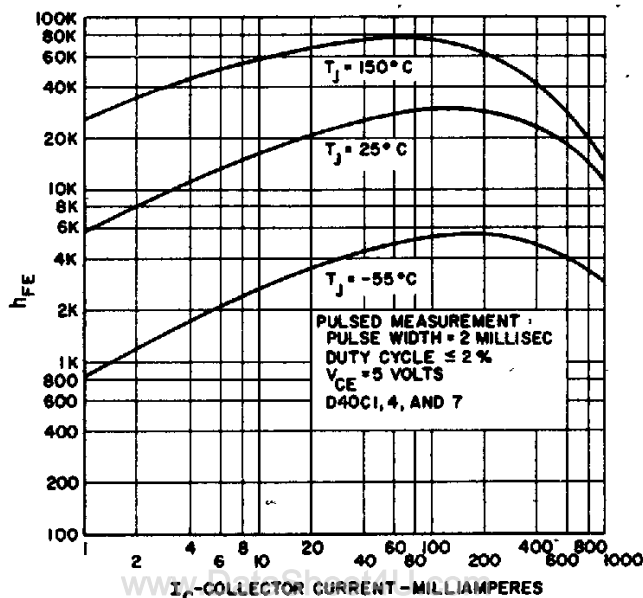


FIG 1. TYPICAL h_{FE} vs. I_C

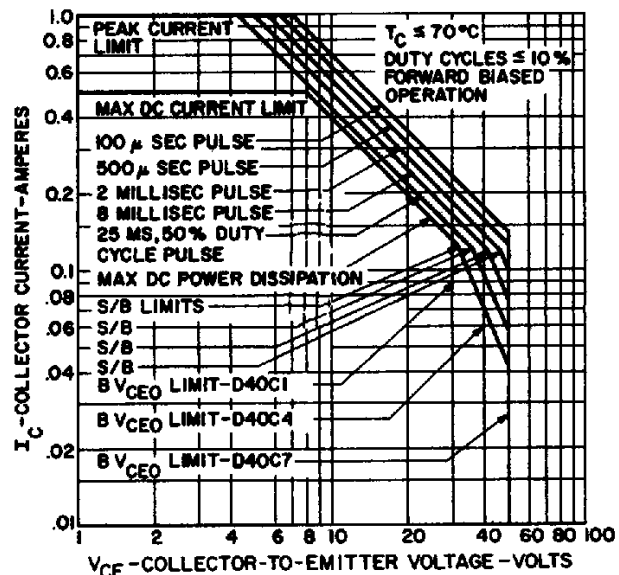


FIG. 2 SAFE REGION OF OPERATION

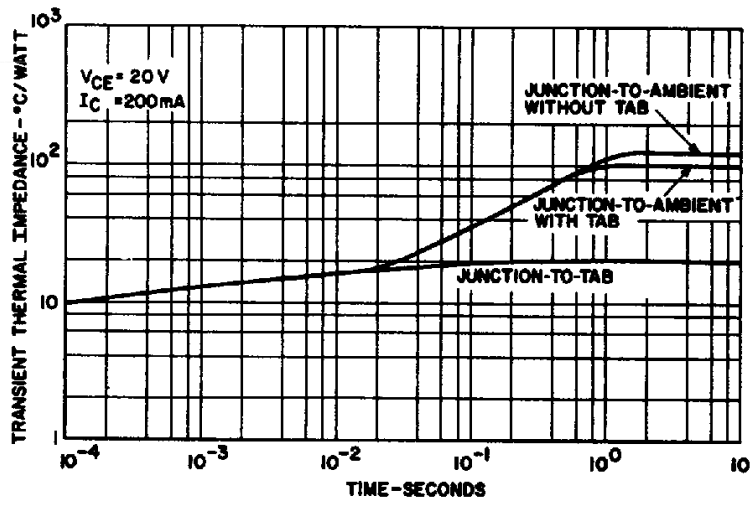


FIG. 3 MAXIMUM TRANSIENT THERMAL IMPEDANCE

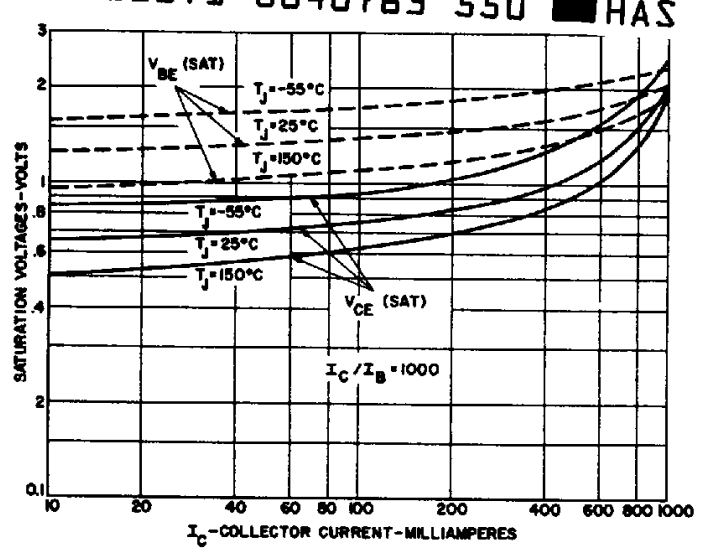


FIG. 4 TYPICAL SATURATION VOLTAGES

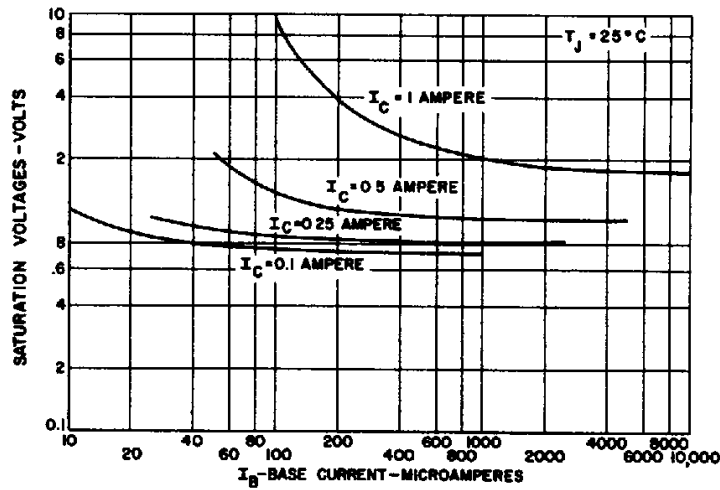


FIG. 5 TYPICAL SATURATION VOLTAGES

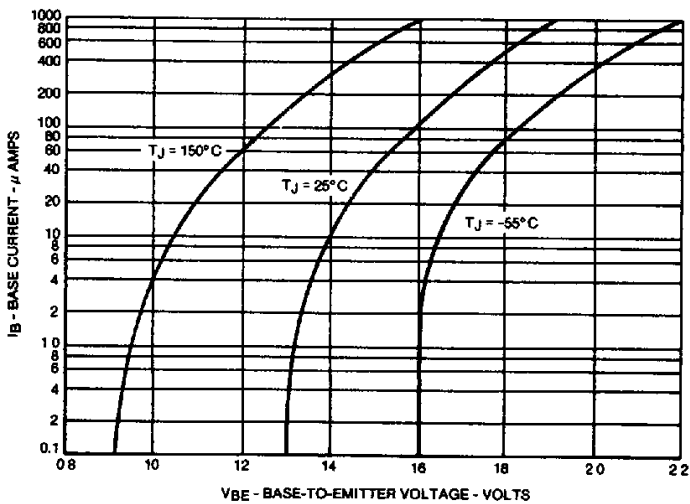


FIG. 6 TYPICAL INPUT CHARACTERISTICS

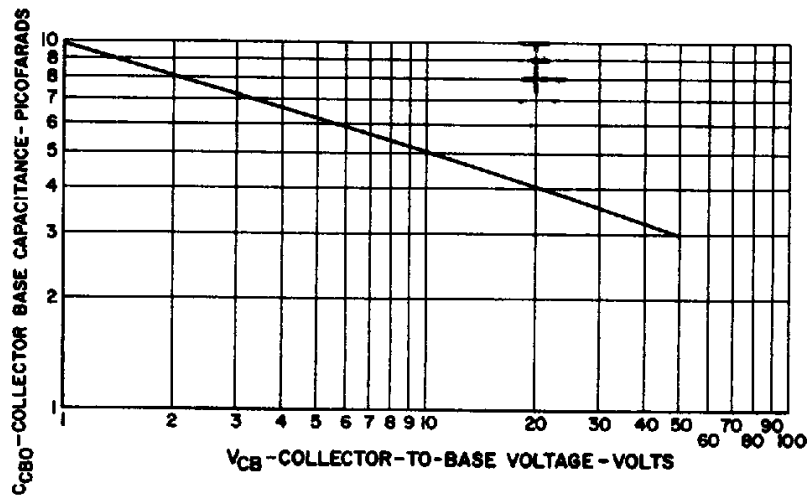


FIG. 7 TYPICAL C_{CB0} vs. VOLTAGE