NEC
NEC Electronics Inc.

μPD41416
16,384 x 4-BIT
DYNAMIC NMOS RAM

Revision 2

Description

The μPD41416 is a 16,384-word by 4-bit dynamic N-channel MOS RAM designed to operate from a single +5 V power supply. The negative voltage substrate bias is internally generated; its operation is both automatic and transparent. The μPD41416 utilizes a double-polylayer, N-channel, silicon gate process which provides high storage cell density, high performance, and high reliability.

The μPD41416 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0-A_6 during the refresh period of 2 milliseconds.

Multiplexed address inputs permit the μPD41416 to be packaged in a standard 18-pin dual-in-line package for high system bit density.

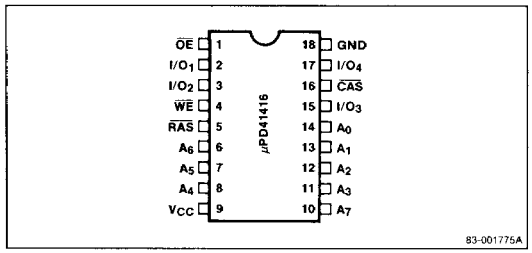
Features

- 16,384-word × 4-bit organization
- Single +5 V power supply ±10%
- Standard 18-pin plastic package
- $\overline{CAS}$, $\overline{OE}$ or early write mode to control D_{OUT} buffer impedance
- Low power dissipation,
  —Active (t_{RC} = min): 303 mW
  —Standby: 28 mW
- Read, write, read-write, read-modify-write. $\overline{RAS}$-only refresh, hidden refresh, and page mode capabilities
- 128 refresh cycles during 2 ms period

Performance Ranges

Device	t_{RAC}	t_{CAC}	t_{OEA}
μPD41416-12	120 ns	60 ns	30 ns
μPD41416-15	150 ns	75 ns	40 ns
μPD41416-20	200 ns	100 ns	50 ns

Pin Configuration

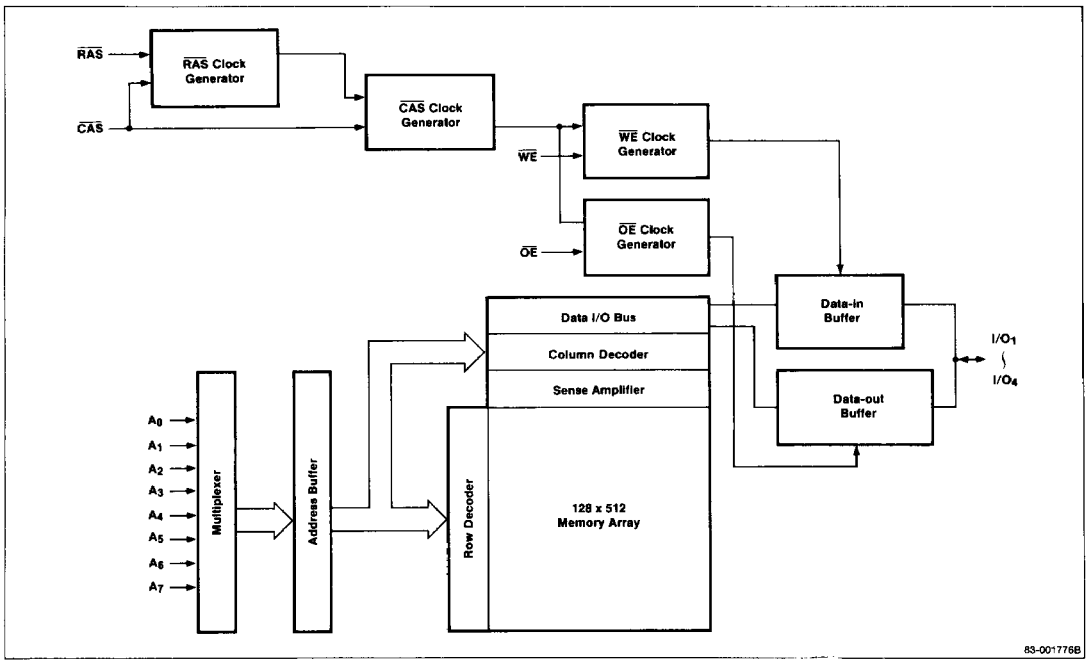


Pin Identification

No.	Symbol	Function
1	$\overline{OE}$	Output enable
2-3, 15, 17	I/O_1-I/O_4	Data input / output
4	$\overline{WE}$	Write enable
5	$\overline{RAS}$	Row address strobe
6-8, 10-14	A_0-A_7	Address inputs: A_0-A_5 = Column address inputs A_0-A_6 = Refresh address A_0-A_7 = Row address inputs
9	V_{CC}	+5 V power supply
16	$\overline{CAS}$	Column address strobe
18	GND	Ground

5

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 V to +7.0 V
Storage temperature, T_{STG}	−55°C to 125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\ V \pm 10\%$; $f = 1.0\ MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance, address inputs	C_{I1}			5	pF	
Input capacitance, strobe inputs	C_{I2}			8	pF	
Input / output capacitance, data ports	$C_{I/O}$			7	pF	

DC Characteristics

$T_A = 0°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage, high	V_{CC}	4.5	5.0	5.5	V	
Supply voltage, low	GND	0	0	0	V	
Standby supply current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = High impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	$0\ V \leq V_{IN} \leq V_{CC}$, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, $0\ V \leq V_{OUT} \leq +5.5\ V$
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2\ mA$
Output voltage, high	V_{OH}	2.4			V	$I_{OUT} = -2\ mA$
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input voltage, high	V_{IH}	2.4		5.5	V	

AC Characteristics (Notes 2, 3, 4)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41416-12 Min	Limits μPD41416-12 Max	Limits μPD41416-15 Min	Limits μPD41416-15 Max	Limits μPD41416-20 Min	Limits μPD41416-20 Max	Unit	Test Conditions
Operating supply current, average	I_{CC1}		55		50		45	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min. (Note 5)
Operating supply current, refresh mode, average	I_{CC3}		45		40		35	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min. (Note 5)
Operating supply current, page mode operation, average	I_{CC4}		45		40		35	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min. (Note 5)
Random read or write cycle time	t_{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t_{RWC}	300		355		445		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		180		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	(Notes 7, 9)
Output turn-off delay from $\overline{CAS}$	t_{OFF}	0	30	0	40	0	50	ns	(Note 10)
Transition time, rise and fall	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}		90		100		120	ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	30	100	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		30		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	50		60		70		ns	
$\overline{RAS}$ precharge, $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		20		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		30		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	35		45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		155		ns	
Write command pulse width	t_{WP}	35		45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)

5

AC Characteristics (Notes 2, 3, 4) (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41416-12 Min	Limits μPD41416-12 Max	Limits μPD41416-15 Min	Limits μPD41416-15 Max	Limits μPD41416-20 Min	Limits μPD41416-20 Max	Unit	Test Conditions
Data-in hold time	t_{DH}	35		45		55		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		155		ns	
Refresh period	t_{REF}		2		2		2	ms	
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	95		120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	155		195		255		ns	
Access time from $\overline{OE}$	t_{OEA}	30		40		50		ns	
Data delay time	t_{OED}	30		40		50		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	0	50	ns	(Note 10)

Notes:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the outputs open.

(6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0°C$ to $70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

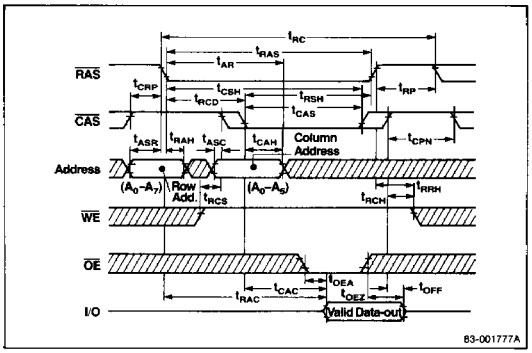
(12) t_{CRP} requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

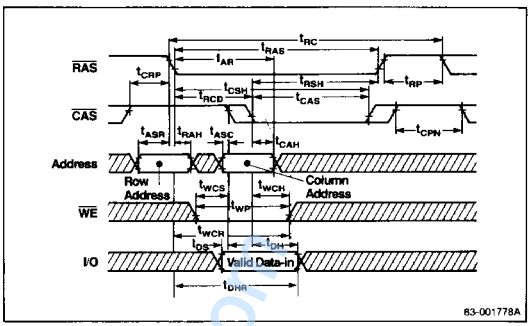
(14) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

Timing Waveforms

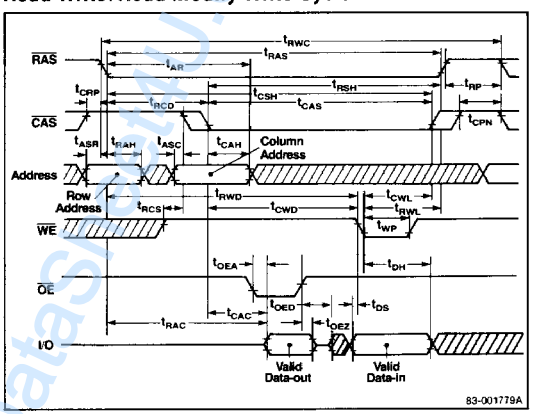
Read Cycle



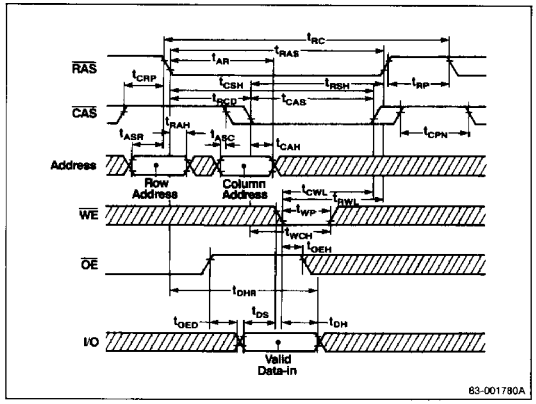
Write Cycle (Early Write)



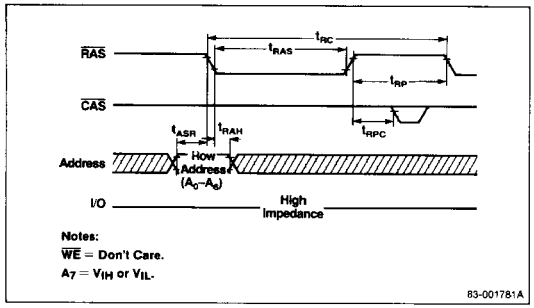
Read-Write/Read-Modify-Write Cycle



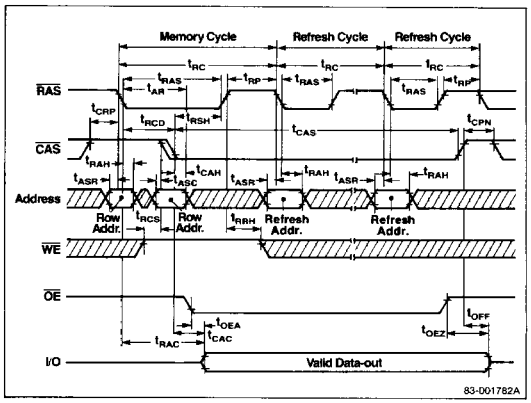
OE-Controlled Write Cycle



"RAS-Only" Refresh Cycle



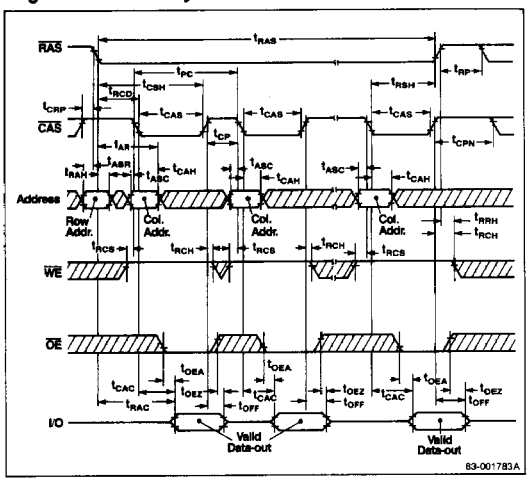
Hidden Refresh Cycle



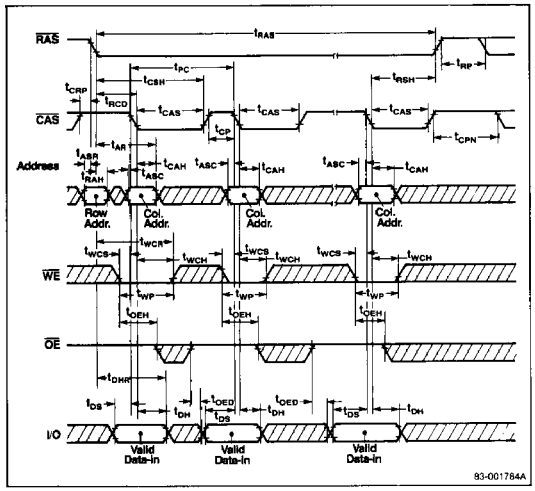
5

Timing Waveforms (cont)

Page Mode Read Cycle



Page Mode Write Cycle (Early Write)



Page Mode Read-Write/Read-Modify-Write Cycle