

www.DataSheet4U.com

### Description

The μPD4364 is a high-speed, 8192-word by 8-bit static RAM. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4364 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V (-xxL and -xxLL versions).

The μPD4364 is packaged in standard and slim 28-pin plastic DIP, as well as plastic miniflat packages that are plug-in compatible with 2764-type EPROMs.

### Features

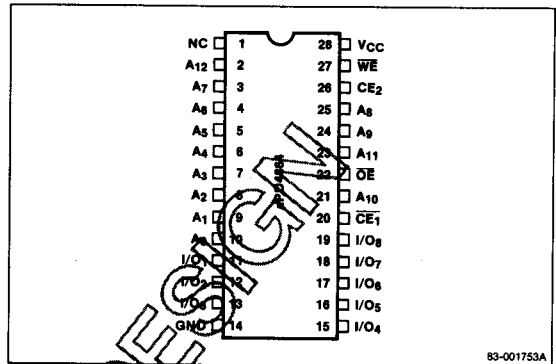
- Single +5-volt power supply
- Fully static operation—no clock or refreshing required
- TTL-compatible—all inputs and outputs
- Common I/O using three-state outputs
- One output enable and two chip enable pins for easy application
- Data retention voltage: 2 V min for -xxL and -xxLL versions
- Plug-in compatible with 2764-type EPROMs
- Standard 28-pin plastic DIP
- 28-pin 300 mil plastic slim DIP
- 28-pin plastic miniflat package

### Pin Identification

| Name                               | Function                       |
|------------------------------------|--------------------------------|
| A <sub>0</sub> -A <sub>12</sub>    | Address input                  |
| I/O <sub>1</sub> -I/O <sub>8</sub> | Data input/output              |
| CE <sub>1</sub>                    | Chip enable input, active low  |
| CE <sub>2</sub>                    | Chip enable input, active high |
| OE                                 | Output enable input            |
| WE                                 | Write enable input             |
| GND                                | Ground                         |
| V <sub>CC</sub>                    | +5-volt power supply           |
| NC                                 | No connection                  |

### Pin Configuration

#### 28-Pin Plastic DIP or Miniflat



### Ordering Information

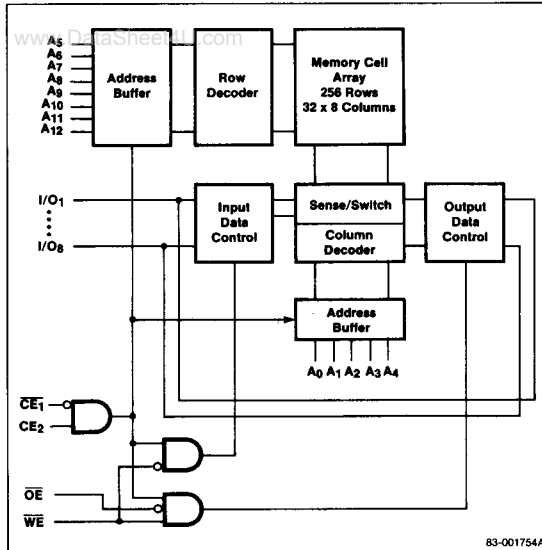
| Part Number<br>(Notes 2, 3) | Standby<br>Current (max) | Access<br>Time (max) | Package         |
|-----------------------------|--------------------------|----------------------|-----------------|
| μPD4364C-xx                 | 2 mA                     | (Notes 1,4)          | 28-pin DIP      |
| C-xxL                       | 100 μA                   |                      |                 |
| C-xxLL                      | 50 μA                    |                      |                 |
| CX-xx                       | 2 mA                     | (Notes 1,5)          | 28-pin slim DIP |
| CX-xxL                      | 100 μA                   |                      |                 |
| μPD4364G-xx                 | 2 mA                     | (Notes 1,4)          | 28-pin miniflat |
| G-xxL                       | 100 μA                   |                      |                 |
| G-xxLL                      | 50 μA                    |                      |                 |

#### Notes:

- (1) The symbol "xx" in the part number denotes access time.
 

| xx | Access Time (max) |
|----|-------------------|
| 10 | 100 ns            |
| 12 | 120 ns            |
| 15 | 150 ns            |
| 20 | 200 ns            |
- (2) The symbol C, CX, or G in the part number denotes a 28-pin plastic package.  
 C = 600-mil DIP  
 CX = 300-mil slim DIP  
 G = Miniflat
- (3) Part number example: μPD4364CX-12L denotes a 300-mil DIP package, 120-ns maximum access time, and 100-μA maximum standby current.
- (4) Contact your NEC sales representative for availability of a -10LL version.
- (5) A 200-ns access time is not available in the CX package.

**Block Diagram**



**Absolute Maximum Ratings**

|                                    |                            |
|------------------------------------|----------------------------|
| Supply voltage, $V_{CC}$ (Note 1)  | -0.5 to 7.0 V              |
| Input voltage, $V_{IN}$ (Note 1)   | -0.5 V to $V_{CC} + 0.5$ V |
| Output voltage, $V_{OUT}$ (Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Operating temperature, $T_{OPR}$   | 0 to 70°C                  |
| Storage temperature, $T_{STG}$     | -55 to 125°C               |
| Power dissipation, $P_D$           | 1.0 W                      |

**Notes:**

(1) -3.0 V min (pulse width of 50 ns max)

**Comment:** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended DC Operating Conditions.

**Capacitance**

$T_A = 25^\circ\text{C}$ ;  $f = 1.0$  MHz

| Parameter                | Symbol    | Limits |     |     | Unit | Test Conditions |
|--------------------------|-----------|--------|-----|-----|------|-----------------|
|                          |           | Min    | Typ | Max |      |                 |
| Input capacitance        | $C_i$     |        | (1) |     | pF   | $V_i = 0$ V     |
| Input/output capacitance | $C_{i/O}$ |        | 8   |     | pF   | $V_{i/O} = 0$ V |

**Notes:**

- (1) Maximum input capacitance  
 CX package: 5 pF  
 C or G package, 100-ns version: 5 pF  
 C or G package, except 100-ns version: 6 pF

**Recommended DC Operating Conditions**

$T_A = 0$  to  $+70^\circ\text{C}$

| Parameter           | Symbol   | Limits |     |                | Unit |
|---------------------|----------|--------|-----|----------------|------|
|                     |          | Min    | Typ | Max            |      |
| Supply voltage      | $V_{CC}$ | 4.5    | 5.0 | 5.5            | V    |
| Input voltage, low  | $V_{IL}$ | -0.3   |     | 0.8            | V    |
| (Note 1)            |          |        |     |                |      |
| Input voltage, high | $V_{IH}$ | 2.2    |     | $V_{CC} + 0.5$ | V    |

**Notes:**

(1) -3.0 V min (pulse width 50 ns max)

**DC Characteristics**

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = 5$  V  $\pm 10\%$

| Parameter                | Symbol     | Limits     |     |     | Unit          | Test Conditions  |
|--------------------------|------------|------------|-----|-----|---------------|--|
|                          |            | Min        | Typ | Max |               |  |
| Input leakage current    | $I_{LI}$   |            | 1   |     | $\mu\text{A}$ | $V_{I/O} = 0$ V to $V_{CC}$  |
| Output leakage current   | $I_{LO}$   |            | 1   |     | $\mu\text{A}$ | $V_{I/O} = 0$ V to $V_{CC}$<br>$CE_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$                                      |
| Operating supply current | $I_{CCA1}$ |            | (1) |     | mA            | $CE_1 = V_{IL}$ ,<br>$CE_2 = V_{IH}$ ,<br>$I_{I/O} = 0$ ,<br>Min cycle   |
|                          |            | $I_{CCA2}$ | 5   | 10  | mA            | $CE_1 = V_{IL}$ ,<br>$CE_2 = V_{IH}$ ,<br>$I_{I/O} = 0$ ,<br>DC current  |
|                          |            | $I_{CCA3}$ | 3   | 5   | mA            | $CE_1 \leq 0.2$ V,<br>$CE_2 \geq V_{CC} - 0.2$ V,<br>$V_{IL} \leq 0.2$ V,<br>$V_{IH} \geq V_{CC} - 0.2$ V,<br>$f = 1$ MHz, $I_{I/O} = 0$ |
| Standby supply current   | $I_{SB}$   |            | (2) |     | mA            | $CE_1 \geq V_{IH}$ or $CE_2 = V_{IL}$  |
|                          |            | $I_{SB1}$  | (3) |     | mA            | $CE_1 \geq V_{CC} - 0.2$ V<br>$CE_2 \geq V_{CC} - 0.2$ V   |
|                          |            | $I_{SB2}$  | (3) |     | mA            | $CE_2 \leq 0.2$ V  |
| Output voltage, low      | $V_{OL}$   |            | 0.4 |     | V             | $I_{OL} = 2.1$ mA  |
| Output voltage, high     | $V_{OH}$   |            | 2.4 |     | V             | $I_{OH} = -1.0$ mA   |

**Notes:**

- (1) μPD4364-10/10L: 45 mA max  
 μPD4364-12/12L/12LL: 40 mA max  
 μPD4364-15/15L/15LL: 40 mA max  
 μPD4364-20/20L/20LL: 35 mA max
- (2) μPD4364-xx: 5 mA max  
 μPD4364-xxL: 3 mA max  
 μPD4364-xxLL: 3 mA max
- (3) μPD4364-xx: 2 mA max  
 μPD4364-xxL: 100 μA max  
 μPD4364-xxLL: 50 μA max

## AC Characteristics

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = 5 V ±10%

www.DataSheet4U.com

| Parameter   | Symbol           | Limits             |     |                         |     |                         |     |                         |     | Unit |
|---|------------------|--------------------|-----|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|
|   |                  | μPD4364<br>-10/10L |     | μPD4364<br>-12/12L/12LL |     | μPD4364<br>-15/15L/15LL |     | μPD4364<br>-20/20L/20LL |     |      |
|   |                  | Min                | Max | Min                     | Max | Min                     | Max | Min                     | Max |      |
| <b>Read Cycle</b>                                     |                  |                    |     |                         |     |                         |     |                         |     |      |
| Read cycle time                                       | t <sub>RC</sub>  | 100                |     | 120                     |     | 150                     |     | 200                     |     | ns   |
| Address access time                                   | t <sub>AA</sub>  |                    | 100 |                         | 120 |                         | 150 |                         | 200 | ns   |
| $\overline{CE}_1$ access time                         | t <sub>CO1</sub> |                    | 100 |                         | 120 |                         | 150 |                         | 200 | ns   |
| CE <sub>2</sub> access time                           | t <sub>CO2</sub> |                    | 100 |                         | 120 |                         | 150 |                         | 200 | ns   |
| Output enable to output valid                         | t <sub>OE</sub>  |                    | 50  |                         | 60  |                         | 70  |                         | 100 | ns   |
| Output hold from address change                       | t <sub>OH</sub>  | 10                 |     | 10                      |     | 15                      |     | 15                      |     | ns   |
| Chip enable ( $\overline{CE}_1$ ) to output in low-Z  | t <sub>LZ1</sub> | 10                 |     | 10                      |     | 15                      |     | 15                      |     | ns   |
| Chip enable (CE <sub>2</sub> ) to output in low-Z     | t <sub>LZ2</sub> | 10                 |     | 10                      |     | 15                      |     | 15                      |     | ns   |
| Output enable to output in low-Z                      | t <sub>OLZ</sub> | 5                  |     | 5                       |     | 5                       |     | 5                       |     | ns   |
| Chip enable ( $\overline{CE}_1$ ) to output in high-Z | t <sub>HZ1</sub> |                    | 35  |                         | 40  |                         | 50  |                         | 100 | ns   |
| Chip enable (CE <sub>2</sub> ) to output in high-Z    | t <sub>HZ2</sub> |                    | 35  |                         | 40  |                         | 50  |                         | 100 | ns   |
| Output enable to output in high-Z                     | t <sub>OHZ</sub> |                    | 35  |                         | 40  |                         | 50  |                         | 80  | ns   |
| <b>Write Cycle</b>                                    |                  |                    |     |                         |     |                         |     |                         |     |      |
| Write cycle time                                      | t <sub>WC</sub>  | 100                |     | 120                     |     | 150                     |     | 200                     |     | ns   |
| Chip enable ( $\overline{CE}_1$ ) to end of write     | t <sub>CW1</sub> | 80                 |     | 85                      |     | 100                     |     | 180                     |     | ns   |
| Chip enable (CE <sub>2</sub> ) to end of write        | t <sub>CW2</sub> | 80                 |     | 85                      |     | 100                     |     | 180                     |     | ns   |
| Address valid to end of write                         | t <sub>AW</sub>  | 80                 |     | 85                      |     | 100                     |     | 180                     |     | ns   |
| Address setup time                                    | t <sub>AS</sub>  | 0                  |     | 0                       |     | 0                       |     | 0                       |     | ns   |
| Write pulse width                                     | t <sub>WP</sub>  | 60                 |     | 70                      |     | 90                      |     | 140                     |     | ns   |
| Write recovery time                                   | t <sub>WR</sub>  | 5                  |     | 5                       |     | 5                       |     | 5                       |     | ns   |
| Data valid to end of write                            | t <sub>DW</sub>  | 40                 |     | 50                      |     | 60                      |     | 80                      |     | ns   |
| Data hold time  | t <sub>DH</sub>  | 0                  |     | 0                       |     | 0                       |     | 0                       |     | ns   |
| Write enable to output in high-Z                      | t <sub>WHZ</sub> |                    | 35  |                         | 40  |                         | 50  |                         | 100 | ns   |
| Output active from end of write                       | t <sub>OW</sub>  | 5                  |     | 5                       |     | 10                      |     | 10                      |     | ns   |

### Notes:

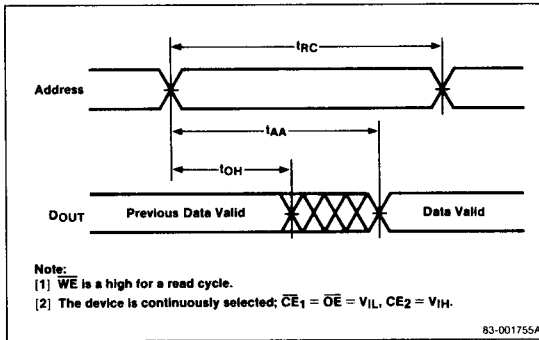
- (1) Input pulse levels: 0.8 to 2.4 V  
 Input pulse rise and fall times: 5 ns  
 Timing reference levels: 1.5 V  
 Output load: 1 TTL gate and C<sub>L</sub> = 100 pF

### Truth Table

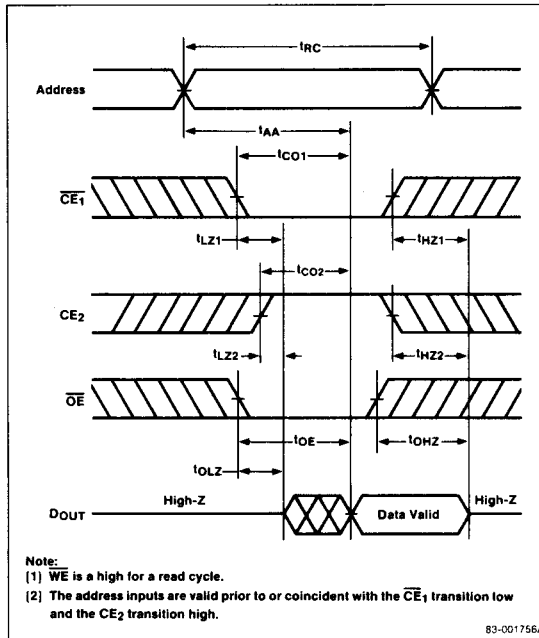
| $\overline{CE}_1$ | CE <sub>2</sub> | $\overline{OE}$ | $\overline{WE}$ | Mode                     | I/O              | I <sub>CC</sub> |
|-------------------|-----------------|-----------------|-----------------|--------------------------|------------------|-----------------|
| H                 | X               | X               | X               | Not selected             | High-Z           | Standby         |
| X                 | L               | X               | X               | Not selected             | High-Z           | Standby         |
| L                 | H               | H               | H               | D <sub>OUT</sub> disable | High-Z           | Active          |
| L                 | H               | L               | H               | Read                     | D <sub>OUT</sub> | Active          |
| L                 | H               | X               | L               | Write                    | D <sub>IN</sub>  | Active          |

Timing Waveforms

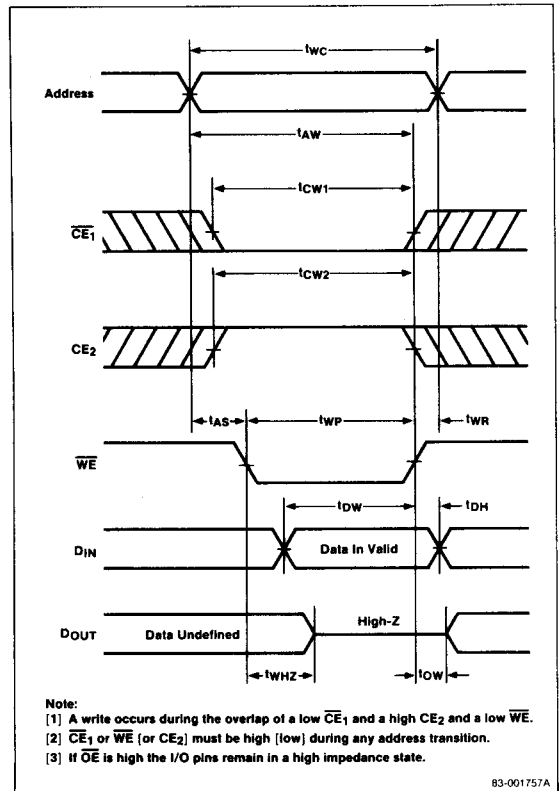
Read Cycle No. 1 (Address Access)



Read Cycle No. 2 (Chip Enable Access)

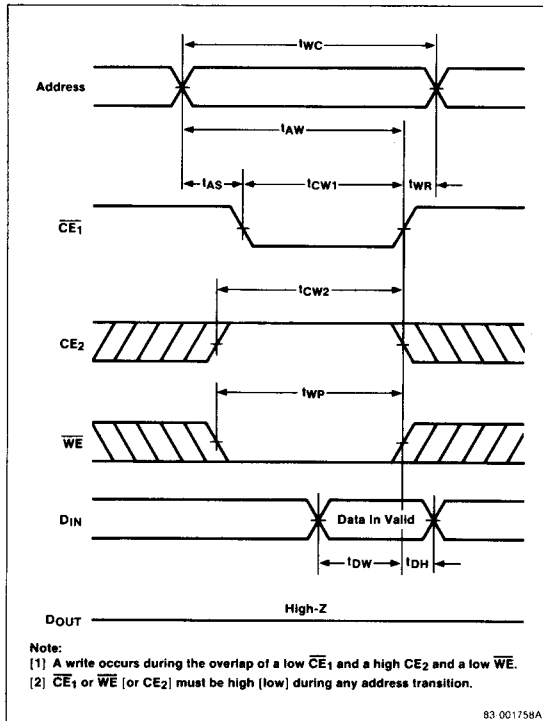


Write Cycle No. 1 ( $\overline{WE}$  Controlled)

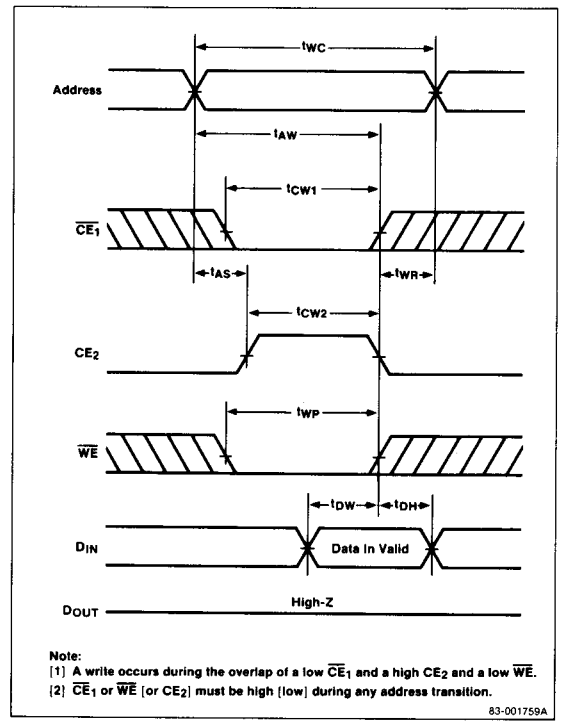


## Timing Waveforms (cont)

### Write Cycle No. 2 ( $\overline{CE}_1$ Controlled)



### Write Cycle No. 3 ( $\overline{CE}_2$ Controlled)



**Low V<sub>CC</sub> Data Retention Characteristics**

T<sub>A</sub> = 0 to +70°C

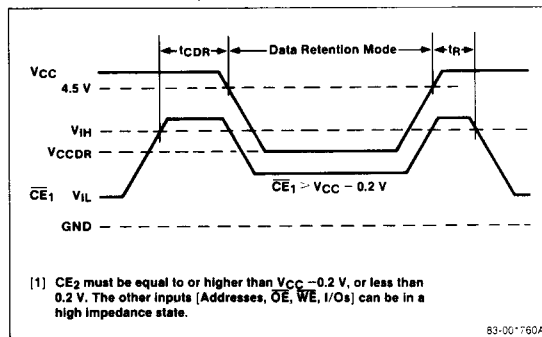
www.DataSheet4U.com

| Parameter                            | Symbol             | Limits |                 |     | Unit | Test Conditions  |
|--------------------------------------|--------------------|--------|-----------------|-----|------|--|
|                                      |                    | Min    | Typ             | Max |      |  |
| Data retention supply voltage        | V <sub>CCDR1</sub> | 2.0    | 5.5             |     | V    | $\overline{CE}_1 \geq V_{CC} - 0.2 V$<br>$CE_2 \geq V_{CC} - 0.2 V$                            |
|                                      | V <sub>CCDR2</sub> | 2.0    | 5.5             |     | V    | $CE_2 \leq 0.2 V$  |
| Data retention supply current        | I <sub>CCDR1</sub> |        | 1 (2)           |     | μA   | V <sub>CC</sub> = 3.0 V<br>$\overline{CE}_1 \geq V_{CC} - 0.2 V$<br>$CE_2 \geq V_{CC} - 0.2 V$ |
|                                      | I <sub>CCDR2</sub> |        | 1 (2)           |     | μA   | V <sub>CC</sub> = 3.0 V<br>$CE_2 \leq 0.2 V$   |
| Chip deselect to data retention time | t <sub>CDR</sub>   | 0      |                 |     | ns   |  |
| Operation recovery time              | t <sub>R</sub>     |        | t <sub>RC</sub> |     | ns   | Note 3   |

**Notes:**

- (1) This table is applicable to μPD4364-xxL and -xxLL only.
- (2) μPD4364-xxL: 50 μA max; 15 μA (0 to 40°C)  
μPD4364-xxLL: 20 μA max; 5 μA (0 to 40°C)
- (3) t<sub>RC</sub> is read cycle time.

**Data Retention ( $\overline{CE}_1$  Controlled)**



**Data Retention (CE<sub>2</sub> Controlled)**

