VERY HIGH SPEED
PNP POWER TRANSISTORS
COMPLEMENTARY TO THE D44VM SERIES

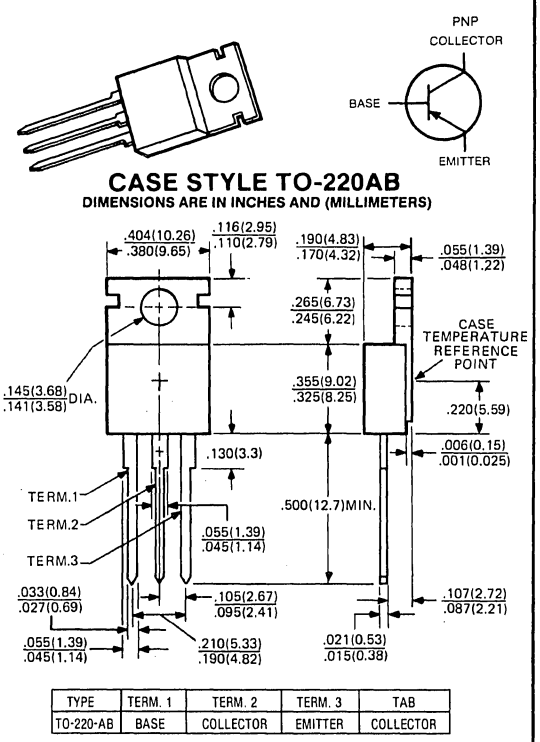
D45VM Series

-30 - -80 VOLTS
-8 AMP, 50 WATTS

The D45VM is an PNP power transistor especially designed for use in switching circuits such as switching regulators, high-frequency inverters/converters and other applications where very fast switching and low-saturation voltages are necessary. This device is characterized with performance information which relates directly to switching, including 100° C maximum limits specified for switching times, saturation voltages, and leakage currents.

Features:

- Very Fast Switching $t_s \leqslant 500$ ns resistive
  $t_f \leqslant 75$ ns
- Very Low $V_{CE(sat)} \leqslant 0.4V$ @ $I_C = 4A$
- High Gain $H_{FE} \geqslant 40$ @ $I_C = 4A$



TYPE	TERM. 1	TERM. 2	TERM. 3	TAB
TO-220-AB	BASE	COLLECTOR	EMITTER	COLLECTOR

maximum ratings ($T_A = 25°C$) (unless otherwise specified)

RATING	SYMBOL	D45VM1	D45VM4	D45VM7	D45VM10	UNIT
Collector-Emitter Voltage	$V_{CEO(sus)}$	-30	-45	-60	-80	V
Collector-Emitter Voltage	V_{CEX}	-30	-45	-60	-80	V
Collector-Emitter Voltage	V_{CEV}	-50	-70	-80	-100	V
Emitter Base Voltage	V_{EBO}			-7		V
Collector Current — Continuous — Peak (1)	I_C I_{CM}			-8 -20		A
Base Current — Continuous — Peak (1)	I_B I_{BM}			-2 -5		A
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25° C	P_D			50 20 0.4		Watts W/° C
Operating and Storage Junction Temperature Range	T_J, T_{STG}			-55 to +150		°C

thermal characteristics

CHARACTERISTICS	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	74	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	235	°C

(1) Pulse measurement condition PW ⩽ 6.0 ms.

electrical characteristics (T_C = 25° C) (unless otherwise specified)

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
off characteristics[1]				
Collector-Emitter Sustaining Voltage[1] (I_C = -100mA, I_B = 0) D45VM1 D45VM4 D45VM7 D45VM10	$V_{CEO(sus)}$	 -30 -45 -60 -80	 — — — —	V
Collector-Emitter Voltage[2] (I_C = 3A, V_{CLAMP} = Rated V_{CEX}, $T_C \leqslant$ 100° C) D45VM1 D45VM4 D45VM7 D45VM10	V_{CEX}	 -30 -45 -60 -80	 — — — —	V
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = -4.0V) (V_{CEV} = Rated Value, $V_{BE(off)}$ = -4.0V, T_C = 100° C)	I_{CEV}	 — —	 -10 -100	μA
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100° C)	I_{CER}	—	-100	μA
Emitter Cutoff Current (V_{EB} = 7V, I_C = 0)	I_{EBO}	—	-10	μA
second breakdown				
Second Breakdown with Base Forward Biased	F_{BSOA}	SEE FIGURE 7		
Second Breakdown with Base Reverse Biased	R_{BSOA}	SEE FIGURE 8		
on characteristics[1]				
DC Current Gain (I_C = -4A, V_{CE} = -1V) (I_C = -6A, V_{CE} = -1V)	h_{FE}	 40 20	 — —	—
Collector-Emitter Saturation Voltage (I_C = -4A, I_B = -0.2A) (I_C = -6A, I_B = -0.3A) (I_C = -8A, I_B = -0.8A, T_C = 100° C)	$V_{CE(sat)}$	 — — —	 -0.4 -0.6 -1.0	V
Base-Emitter Saturation Voltage (I_C = -4A, I_B = -0.2A) (I_C = -4A, I_B = -0.2A, T_C = 100° C)	$V_{BE(sat)}$	 — —	 -1.2 -1.2	V
dynamic characteristics		**Typical**		
Current-Gain — Bandwidth Product (I_C = -0.1A, V_{CE} = -10V, f_{test} = 1 MHz)	f_T	50		MHz
Output Capacitance (V_{CB} = -10V, I_E = 0, f_{test} = 1 MHz)	C_{OB}	70		pF

switching characteristics

			Maximum		
Resistive Load (See Figure 16 for Test Circuit)		T_C	25° C	100° C	
Delay Time	V_{CC} = 30V, I_C = 6A I_{B1} = I_{B2} = 0.6A t_p = 25 μsec	t_d	30	40	nsec
Rise Time		t_r	250	350	nsec
Storage Time		t_s	500	600	nsec
Fall Time		t_f	75	250	nsec
Inductive Load, Clamped (See Figure 15 for Test Circuit)					
Storage Time	$V_{CE(CLAMP)}$ = 30V, I_C = 6A	t_s	500	600	nsec
Fall Time	I_{B1} = I_{B2} = 0.6A, $V_{BE(OFF)}$ = -5V	t_f	70	100	nsec
			Typical		
Storage Time	L = 200 μh	t_s	340	430	nsec
Fall Time		t_f	40	57	nsec

(1) Pulse Duration = 300 μsec, Duty Factor ⩽ 2%.
(2) See Figure 15 for Test Circuit.

TYPICAL DC CHARACTERISTICS

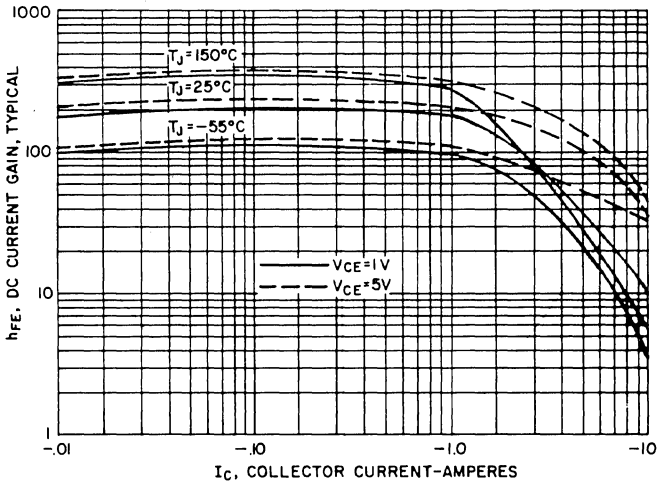


FIGURE 1. DC CURRENT GAIN

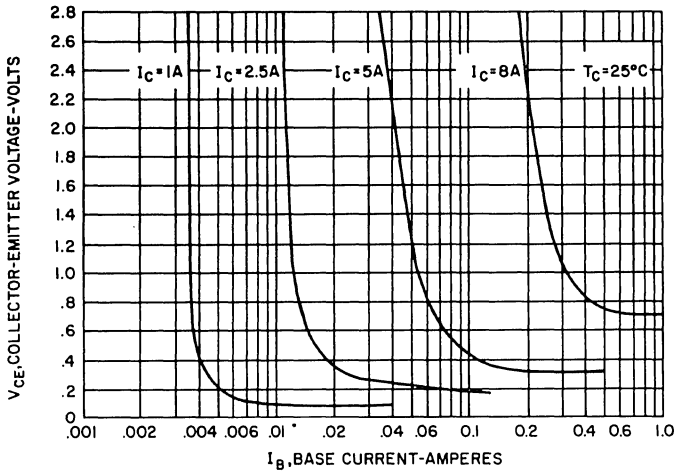


FIGURE 2. COLLECTOR SATURATION REGION

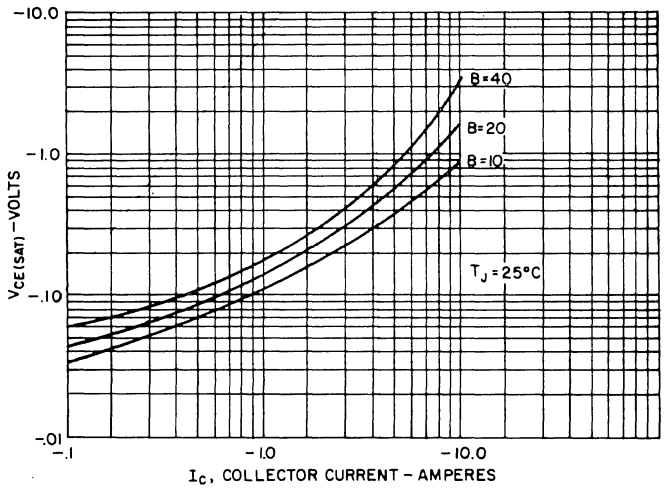


FIGURE 3. $V_{CE(SAT)}$ VS. I_C

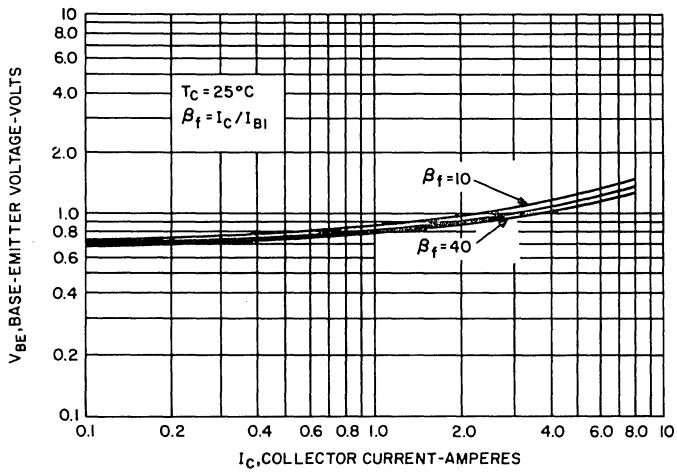


FIGURE 4. $V_{BE(SAT)}$ VS. I_C

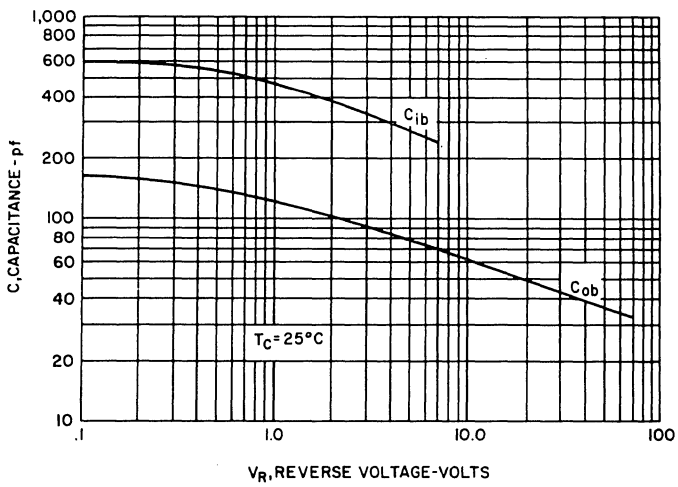


FIGURE 5. CAPACITANCE

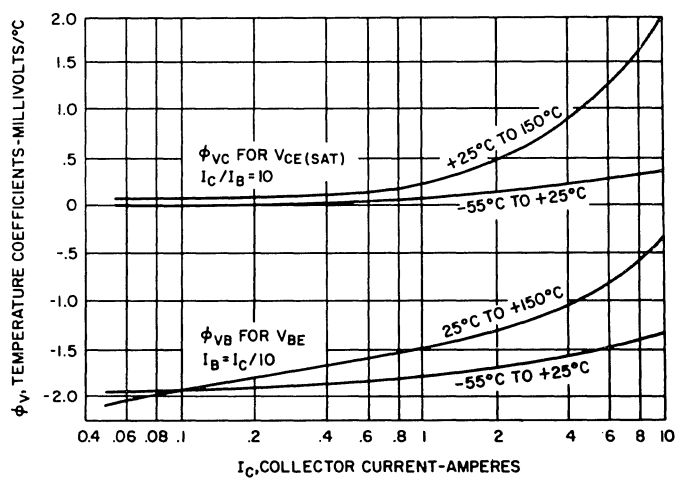


FIGURE 6. SATURATION VOLTAGE TEMPERATURE COEFFICIENTS

SAFE OPERATING AREA

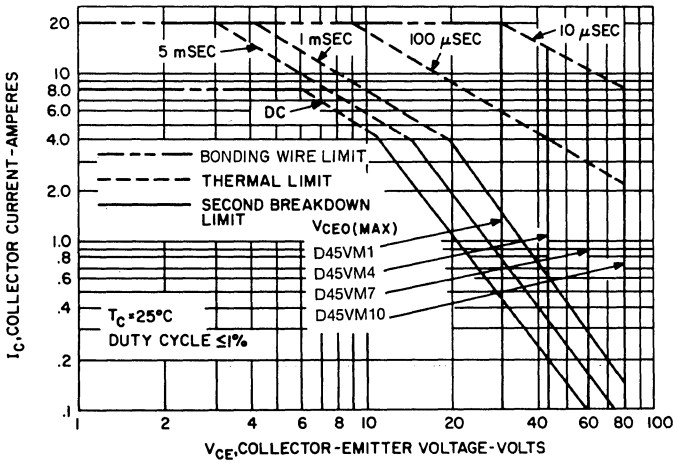


FIGURE 7. FORWARD BIAS SOA

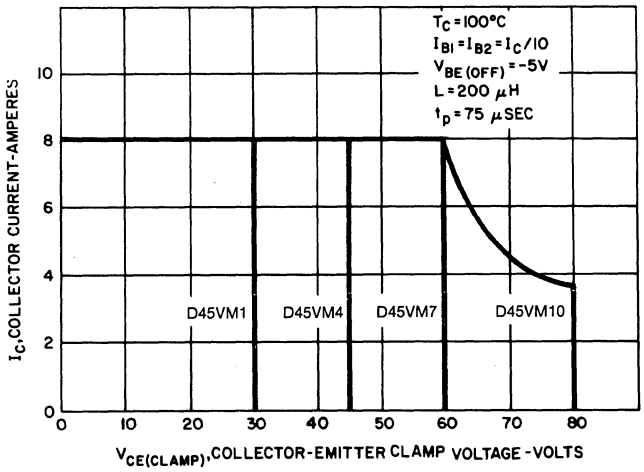


FIGURE 8. CLAMPED REVERSE BIAS SOA

TYPICAL SWITCHING CHARACTERISTICS

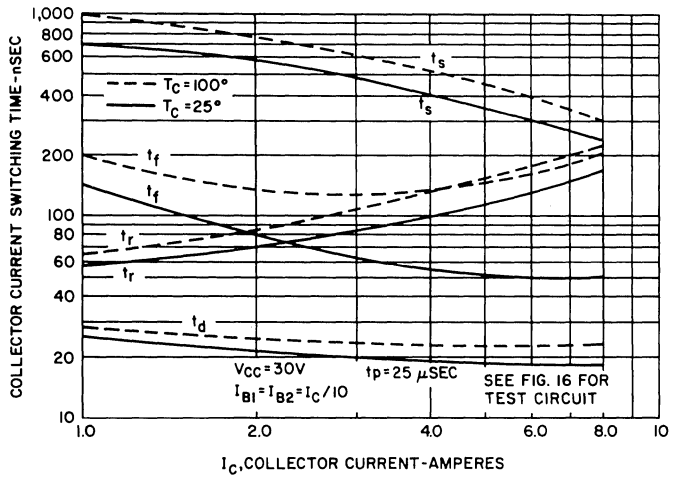


FIGURE 9. RESISTIVE SWITCHING TIME

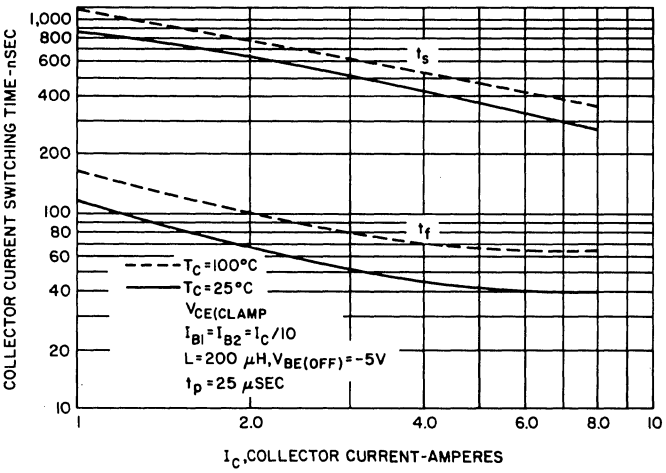


FIGURE 10. CLAMP INDUCTIVE TURN-OFF TIME

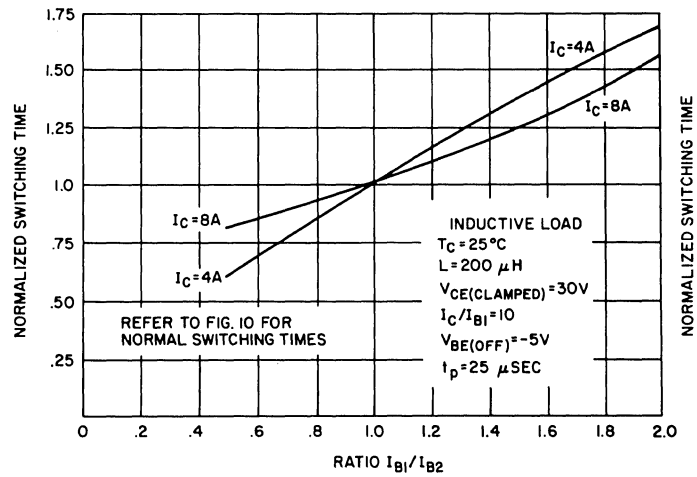


FIGURE 11. STORAGE TIME VARIATION WITH I_{B2}

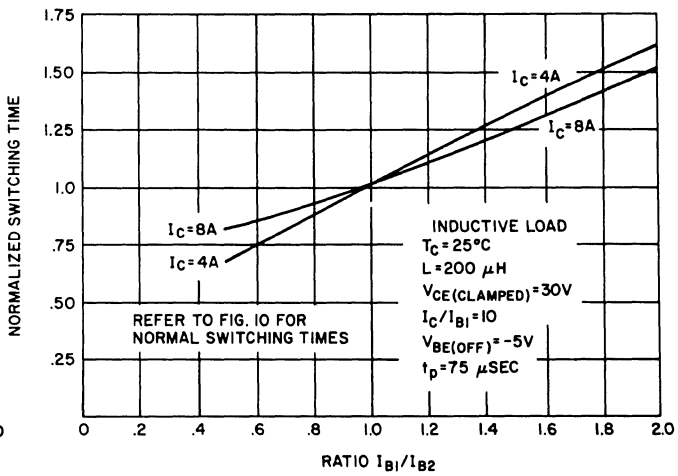


FIGURE 12. FALL TIME VARIATION WITH I_{B2}

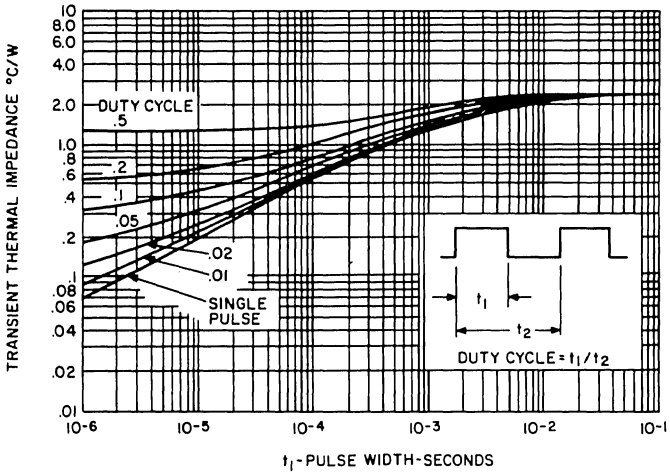


FIGURE 13. TRANSIENT THERMAL RESPONSE

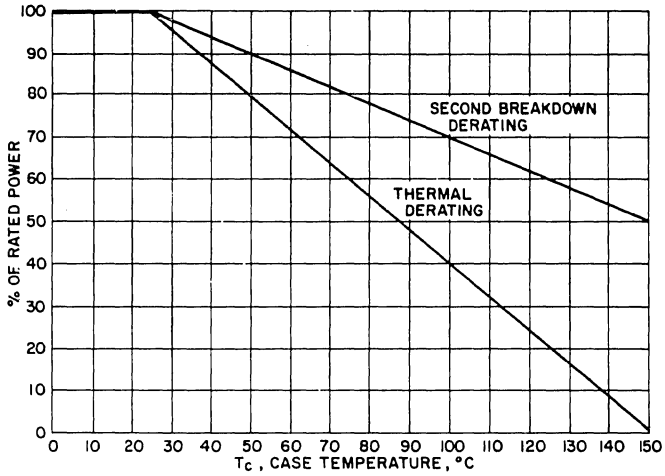


FIGURE 14. POWER DERATING FACTOR

TEST CIRCUITS

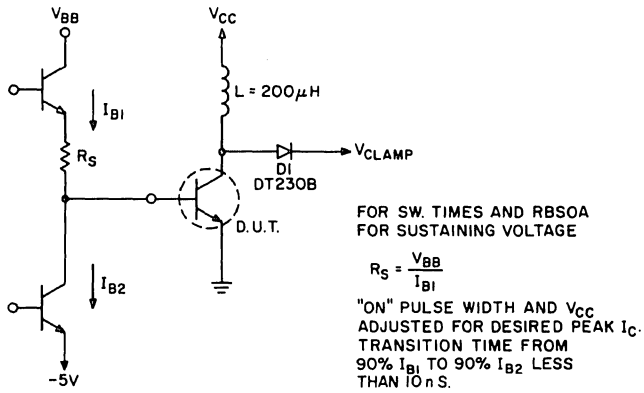


FIGURE 15. INDUCTIVE SWITCHING AND V_{CEX}

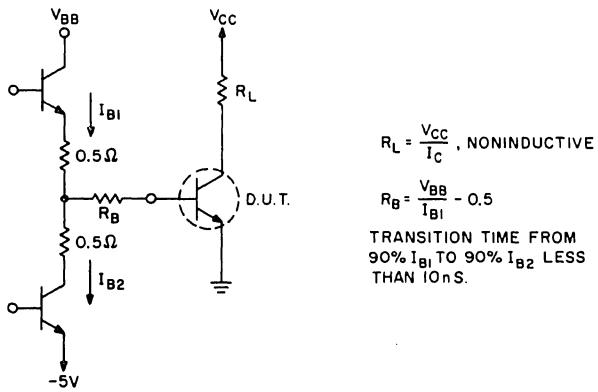


FIGURE 16. RESISTIVE SWITCHING