NEC

MOS INTEGRATED CIRCUIT

μPD4701A

INCREMENTAL ENCODER COUNTER

DESCRIPTION

The μPD4701A is a counter for an X, Y 2-axis incremental encoder. When a two-phase encoder signal is input for the X and Y axes, direction discrimination and computation is performed, and count data is output in 8-bit parallel form. In addition, a 3-contact-point input buffer is incorporated, which is useful for applications which use a pointing device such as a mouse or track-ball. The CPU checks the switch input flag or count flag and reads the 12-bit count data in two operations, one for the lower byte and one for the upper byte. The key input flag is output together with the count data in the upper byte.

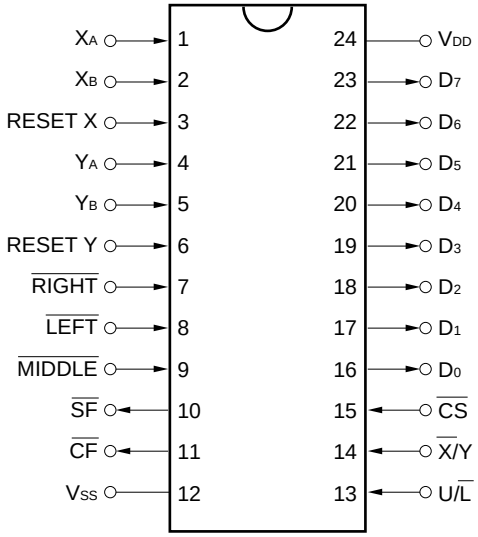
FEATURES

- X, Y 2-axis incremental encoder counter
- Counter input (Schmitt-triggered input)
  X axis: X_A, X_B 2-phase signal
  Y axis: Y_A, Y_B 2-phase signal
  } 4-multiplication count method used
- Counters: 12-bit binary up/down counters (2 sets, X & Y)
  Reset value: 000H
- Count data output: 8-bit parallel latch output × 2 (including key input flag)
- On-chip 3-contact-point key input buffer circuit
- CMOS
- Single +5 V power supply

PIN NAMES

X_A, Y_A : A-phase inputs
X_B, Y_B : B-phase inputs
$\overline{RIGHT}$, $\overline{LEFT}$, $\overline{MIDDLE}$ } Key inputs
$\overline{CS}$: Chip Select
$\overline{X}/Y$: X/Y Counter Select
$U/\overline{L}$: Upper/Lower Byte Select
$D_{0\ to\ 7}$: Data outputs
$\overline{CF}$: Count flag RESET X } Counter reset inputs
$\overline{SF}$: Count flag RESET Y }

PIN CONFIGURATION (Top View)



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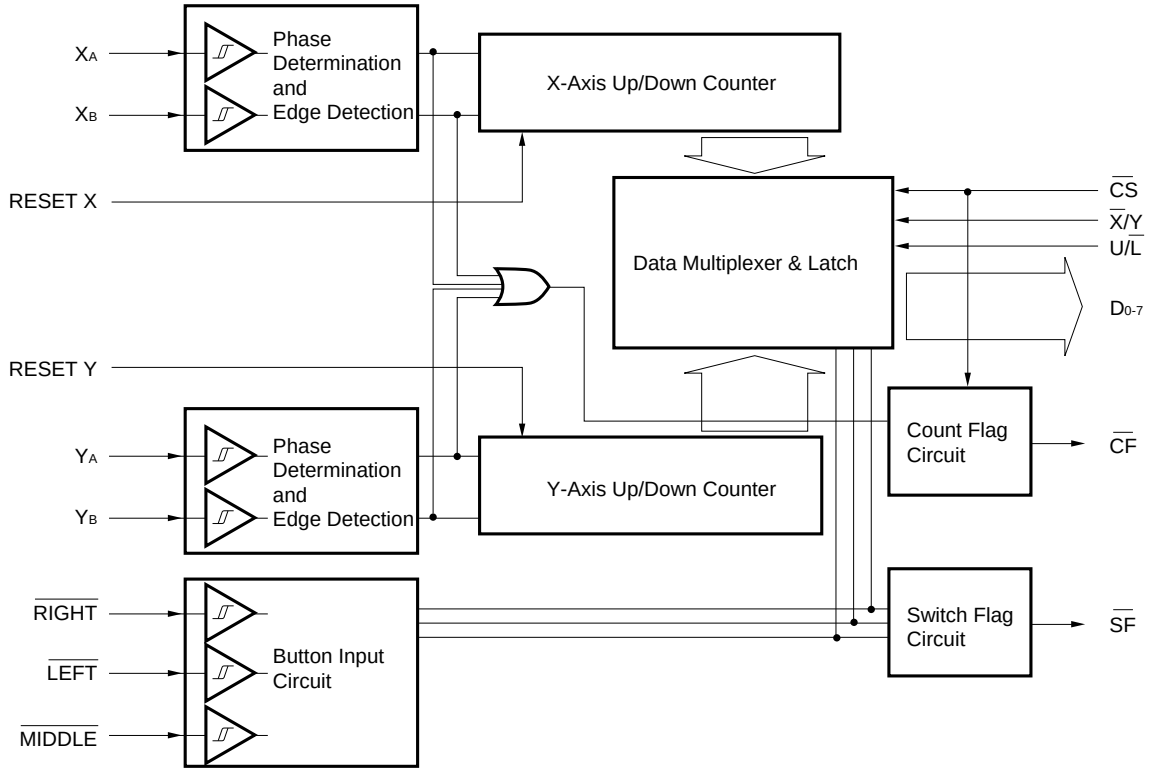
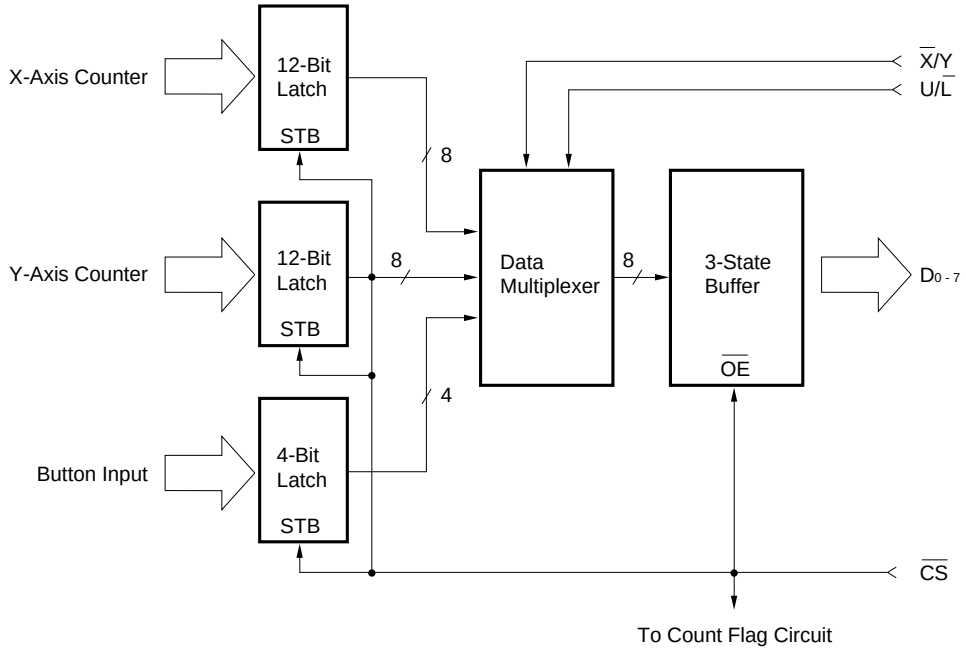
ORDERING INFORMATION

Part Number	Package
μPD4701AC	24-pin plastic DIP (600 mil)
μPD4701AGT	24-pin plastic SOP (375 mil)

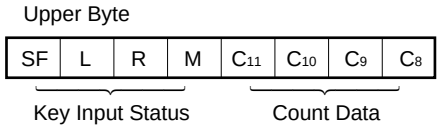
BLOCK DIAGRAM



DATA MULTIPLEXER/LATCH BLOCK



PIN FUNCTIONS

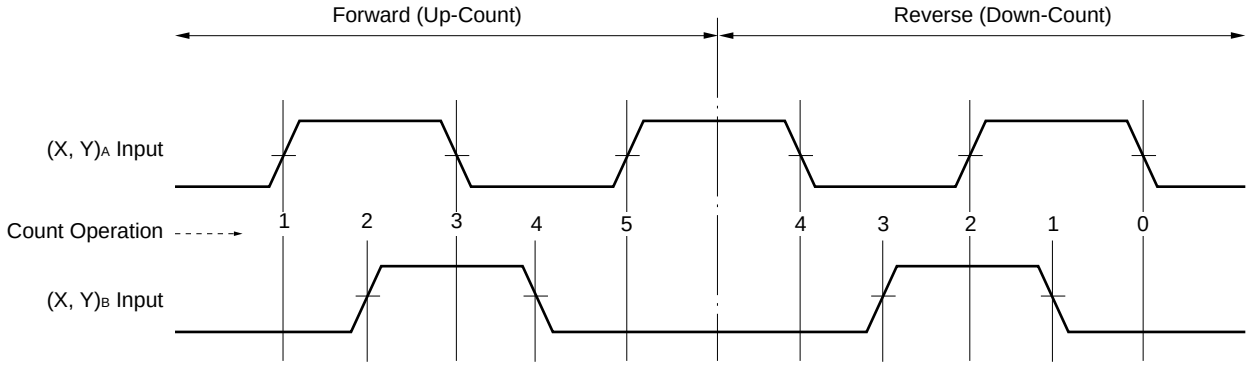
	Pin Name	Input/Output	Function
CPU interface block	$\overline{CS}$	Input	Chip Select input. "L" input activates outputs D0 to 7. "H" input sets outputs D0 to 7 to high impedance. Output data is latched on the fall edge of $\overline{CS}$. "L" must be maintained during a count data read.
	$\overline{X}$/Y	Input	Counter Select input. "L" input selects the X counter, and "H" input selects the Y counter.
	U/$\overline{L}$	Input	Byte Select input. "L" input selects the lower byte and "H" input selects the upper byte, controlling data output.
	RESET X RESET Y	Input	Counter reset inputs. RESET X input resets the X counter, and RESET Y input resets the Y counter. Both are active-"H".
	$D_{0 \text{ to } 7}$	Output (3-state)	Bus for data output to the CPU. Outputs the byte data selected by the $\overline{X}$/Y and U/$\overline{L}$ inputs. The data latched on the fall of $\overline{CS}$ is output.
	$\overline{CF}$	Output	Counter flag output. Set (= "L" output) when the X or Y counter changes while $\overline{CS}$ = "H". Reset (= "H" output) on the fall of $\overline{CS}$. While $\overline{CS}$ = "L", count flag output is disabled and the "H" level is output.
	$\overline{SF}$	Output	Switch flag output. Becomes active (= "L" output) when the $\overline{RIGHT}$, $\overline{LEFT}$ or $\overline{MIDDLE}$ switch input is "L".
Mouse interface block	X_A, X_B	Input (Schmitt input)	X counter 2-phase signal input pins
	Y_A, Y_B	Input (Schmitt input)	Y counter 2-phase signal input pins
	$\overline{RIGHT}$ $\overline{LEFT}$ $\overline{MIDDLE}$	Input (Schmitt input)	Key switch input pins. Key switch input are read as the high-order 4 bits of the X counter and Y counter upper byte as the internal status. 
Power supply block	V_{DD}		+5 V power supply connection pin
	V_{SS}		Ground pin

DESCRIPTION OF OPERATIONS

1. COUNT OPERATION

The μPD4701A executes an up-count and down-count by means of A & B 2-phase signals in the 12-bit up-down counter. An up-count is performed when the A-phase signals (X_A, Y_A) are phase-advanced, and a down-count is performed when the B-phase signals (X_B, Y_B) are phase-advanced. The edge of each signal is a count source. (4-multiplication count method: see Fig. 1.)

Fig. 1 Count Operation Timing Chart



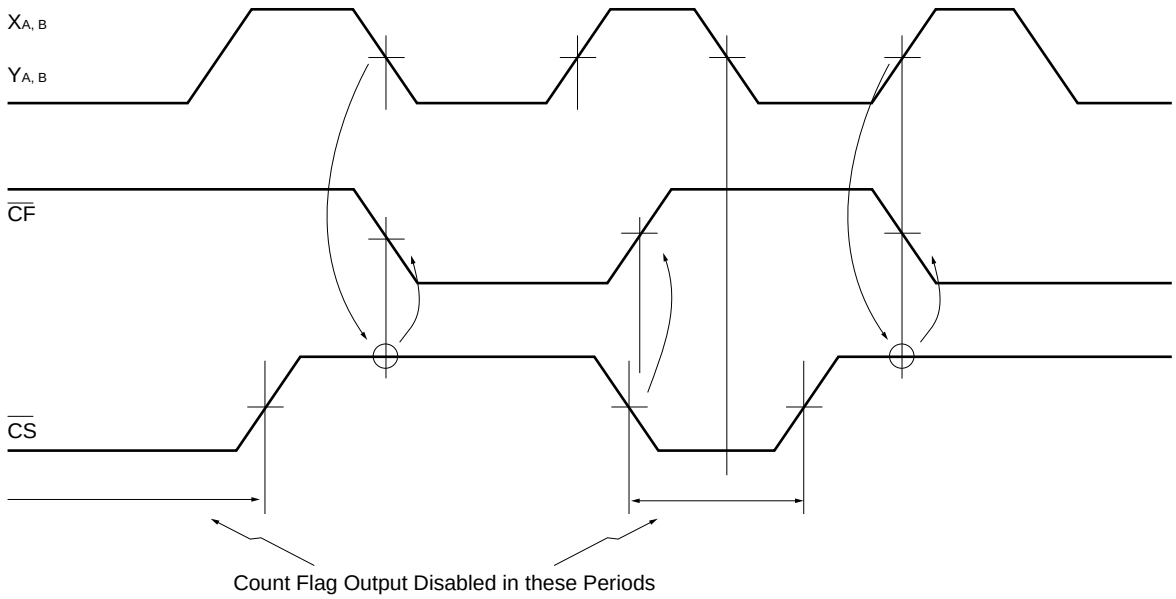
This count operation is executed independently for the X axis (X_A, X_B) and Y axis (Y_A, Y_B). This operation is initialized by reset input (RESET X, RESET Y) only.

In an up-count, the next value after FFFH is 000H, and in a down-count, the next value after 000H is FFFH.

2. OPERATION OF COUNT FLAG, $\overline{CF}$

The count flag, $\overline{CF}$, indicates that a count source (either $X_{A, B}$ or $Y_{A, B}$ edge input) has occurred while the $\overline{CS}$ signal is "H", and is an active-low output. $\overline{CF}$ is reset ($\rightarrow$ "H") by $\overline{CS}$ signal "L" input. While $\overline{CS}$ = "L", count flag output is disabled and the "H" level is output.

Fig. 2 Count Flag Output Timing Chart



3. SWITCH INPUT OPERATION

The μPD4701A can process up to 3 contact points as switch inputs (active-"L" input). Switch input is read as part of the count data upper byte together with the switch flag status as an internal status (see Fig. 3). These are all active-"H" outputs. The switch flag status, SF, is equivalent to the switch flag output, $\overline{SF}$, described below.

Fig. 3 Data Output Format

Bit No.	7	6	5	4	3	2	1	0
Upper Byte	SF	L	R	M	C_{11}	C_{10}	C_9	C_8
Bit No.	7	6	5	4	3	2	1	0
Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

SF : Switch Flag
L : Left Switch
R : Right Switch
M : Middle Switch
C_{11-0} : Count Data (12 bit)

4. OPERATION OF SWITCH FLAG, $\overline{SF}$

The switch flag, $\overline{SF}$, becomes active (active-"L" output) when the $\overline{RIGHT}$, $\overline{LEFT}$ or $\overline{MIDDLE}$ switch input is "L". $\overline{SF}$ can also be read as the switch flag status together with the count data.

5. DATA READ OPERATION

The CPU reads the count data and switch input status by controlling $\overline{CS}$, $\overline{X}$/Y and U/$\overline{L}$. The relation between these is shown in Table 1. (At this time, the data latched on the falling edge of $\overline{CS}$ is output. If $\overline{X}$/Y or U/$\overline{L}$ is switched while $\overline{CS}$ is still "L", the data at the point at which $\overline{CS}$ changes from "H" to "L" is read. When $\overline{CS}$ is set to "H", new data is read into the latch, and the new data is confirmed on the next fall of CS.

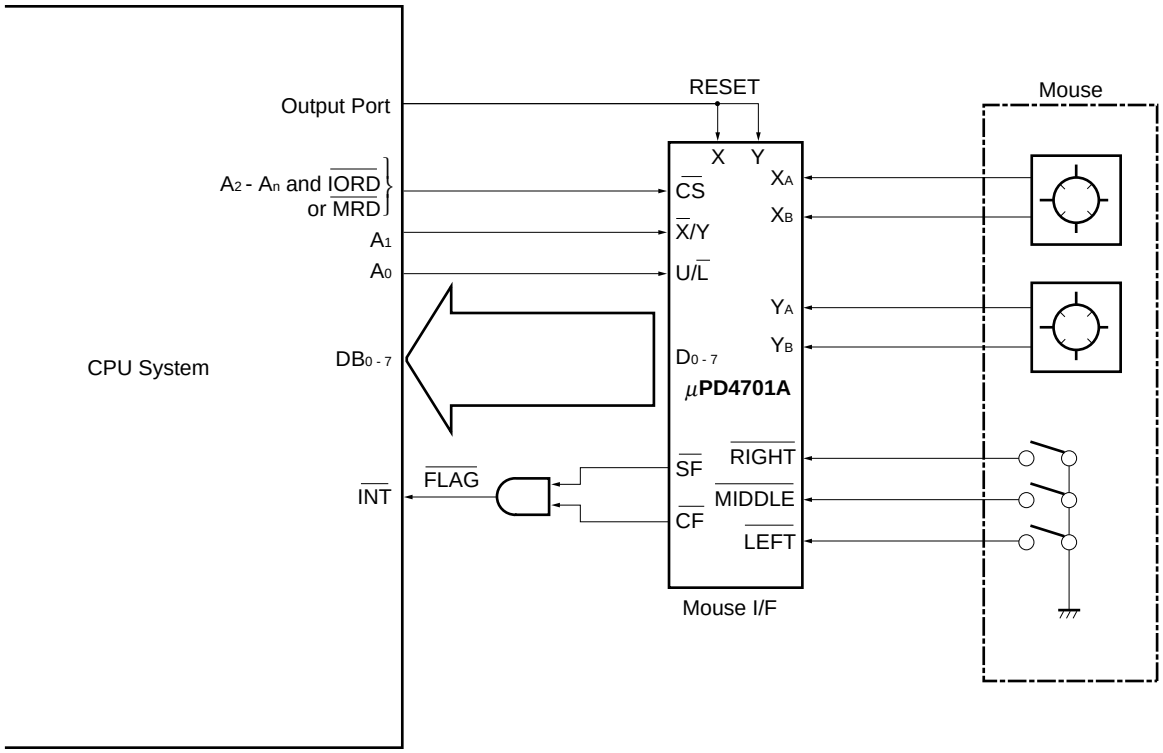
Table 1 Data Output Table

$\overline{CS}$	$\overline{X}$/Y	U/$\overline{L}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	$_XC_7$	$_XC_6$	$_XC_5$	$_XC_4$	$_XC_3$	$_XC_2$	$_XC_1$	$_XC_0$
0	0	1	SF	L	R	M	$_XC_{11}$	$_XC_{10}$	$_XC_9$	$_XC_8$
0	1	0	$_YC_7$	$_YC_6$	$_YC_5$	$_YC_4$	$_YC_3$	$_YC_2$	$_YC_1$	$_YC_0$
0	1	1	SF	L	R	M	$_YC_{11}$	$_YC_{10}$	$_YC_9$	$_YC_8$
1	×	×	FLOATING							

6. CONNECTION TO CPU SYSTEM

An example of connection to a CPU system is shown in Fig. 4.

Fig. 4 Example of Connection to CPU System



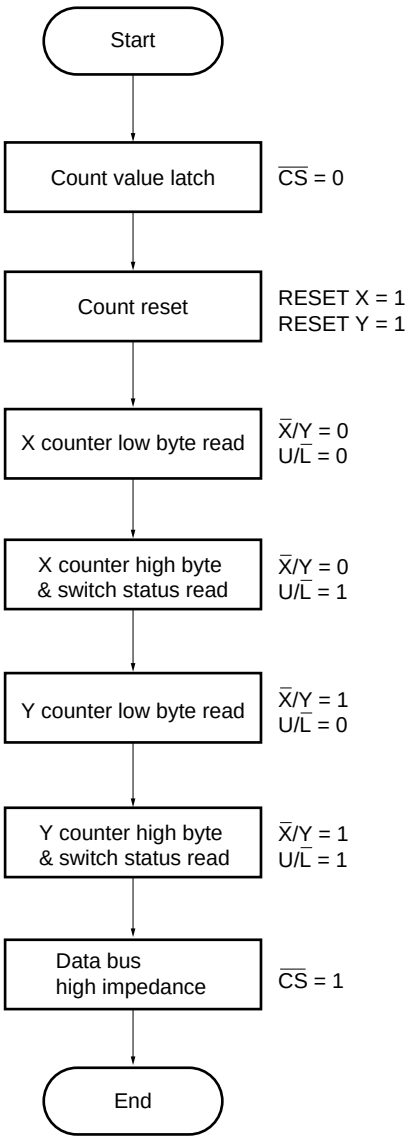
μPD4701A Pin Name	Description
$\overline{X}$/Y	Connected to address line A_1.
U/$\overline{L}$	Connected to address line A_0.
$\overline{CS}$	Connects address lines A_2 to A_n and the signal resulting from decoding $\overline{IORD}$ in the I/O address mode or $\overline{MRD}$ in the memory address mode, or an output port. The low level must be maintained during a count data read.
$D_{0\ to\ 7}$	Connected to the data bus.
$\overline{SF}$, $\overline{CF}$	When these are used as interrupt signals, they are connected to the CPU $\overline{INT}$ pin.
RESET X RESET Y	These are connected to a CPU output port or reset signal.

The above connections enable the CPU to read the X counter, Y counter and switch input status.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

An example of a μPD4701A data read is shown in Fig. 5.

Fig. 5 Example of μPD4701A Data Read



*** $\overline{CS}$ must be kept at "0" during the read.**

7. APPLICATION AREAS

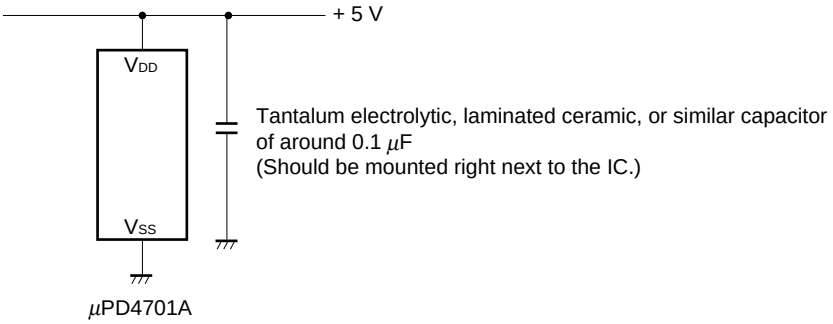
Two-phase incremental signals are used for detection and measurement of a vector quantity (a quantity that has direction and magnitude), and are widely employed in measuring instruments such as micrometers and linear scales, control systems for digital servo motors, X-Y tables, etc., head position control for printers, magnetic disks, etc., robot arm position control, and so on.

The μPD4701A incorporates the direction judgment circuit and count pulse generator required for 2-phase incremental signal processing, up/down counters for counting these pulses, and a data latch to hold the read data, in IC form, enabling an X, Y 2-axis incremental signal processing system to be implemented easily.

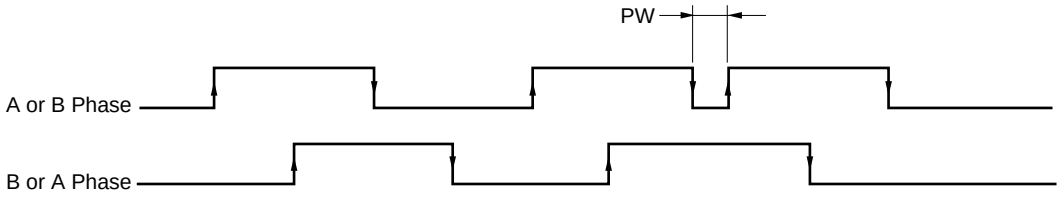
In addition, a 3 switch-input buffer is incorporated, enabling this device to be widely used in man-machine interface and centronics interface application areas.

8. OPERATING PRECAUTIONS

1) As the μPD4701A incorporates two sets of 12-bit counters, large transient currents flow during a count operation. Adecoupling capacitor of around 0.1 μF should therefore be inserted between V_{DD} and V_{SS} of the μPD4701A.



2) If a pulse shorter than the signal phase difference time t_{SAB} (350 ns) is input to the A/B phase inputs (X_A, X_B, Y_A, Y_B) this will result in a miscount. Therefore, if pulses shorter than t_{SAB} are to be input because of encoder bounds, etc., a filter should be attached to the A/B phase inputs.



If PW ≥ t_{SAB} (350 ns), the count value remains the same before and after pulse input. (UP count → DOWN count or DOWN count → UP count is implemented, and therefore the result is equivalent to no change in the count value.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	–0.5 to +7.0	V
Input voltage	V_I	–1.0 to V_{DD} + 1.0	V
Output voltage	V_O	–0.5 to V_{DD} + 0.5	V
Operating temperature	T_{opt}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Permissible loss	P_D	500	mW

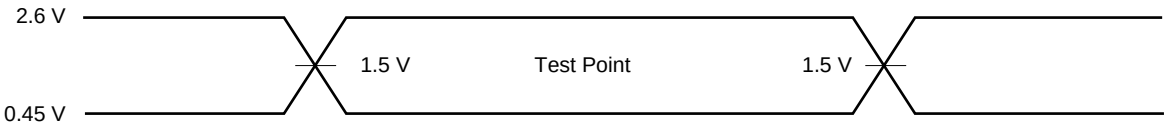
DC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER	SYMBOL	RATING		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Input voltage high	V_{IL}		0.8	V	
Input voltage low	V_{IH}	2.6		V	X_A, X_B, Y_A, Y_B and $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$, $\overline{\text{MIDDLE}}$
	V_{IH}	2.2		V	Other than the above
Output voltage low	V_{OL}		0.45	V	I_{OL} = 12 mA
Output voltage high	V_{OH}	V_{DD} – 0.8		V	I_{OH} = –4 mA
Static consumption current	I_{DD}		50	μA	V_I = V_{DD}, V_{SS}
Input current	I_I	–1.0	1.0	μA	V_I = V_{DD}, V_{SS}
3-state output leak current	I_{OFF}	–10	10	μA	
Dynamic consumption current	$I_{DD\ dyn}$		2	mA	f_{IN} = 500 kHz
Hysteresis voltage	V_H	0.25		V	X_A, X_B, Y_A, Y_B and $\overline{\text{LEFT}}$, $\overline{\text{RIGHT}}$, $\overline{\text{MIDDLE}}$

AC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = +5 V ± 10 %)

PARAMETER		SYMBOL	RATING		UNIT	TEST CONDITIONS
			MIN.	MAX.		
X_A, X_B	Input cycle	t_{CYAB}	2		μs	f_{in} = 500 kHz
Y_A, Y_B	High-level pulse width	t_{PWABH}	900		ns	
	Low-level pulse width	t_{PWABL}	900		ns	
	Signal phase difference time	t_{SAB}	350		ns	
$\overline{R}$, $\overline{L}$	High-level pulse width	t_{PWSWH}	30		μs	Switch OFF
$\overline{M}$	Low-level pulse width	t_{PWSWL}	30		μs	Switch ON
$\overline{SF}$	Setting delay time	t_{DSFL}		50	ns	Switch ON
	Reset delay time	t_{DSFH}		50	ns	Switch OFF
RESET	Pulse width	t_{PWRS}	100		ns	
W, Y	Count enable time	t_{SCTEN}	0		ns	From $RESET_{X, Y}$ ↓
	Count clear time	t_{DCTCL}		100	ns	From $RESET_{X, Y}$ ↑
$\overline{CF}$	Flag setting time	t_{DABCF}		120	ns	From $X_{A, B}$, $Y_{A, B}$
	Flag reset time	t_{DCSCF}		100	ns	From $\overline{CS}$ ↓
	Count setting time	t_{SCT}	0		ns	From $\overline{CF}$ ↓
$\overline{CS}$	$\overline{CF}$ enable time	t_{SCSCF}	140		ns	From $\overline{CF}$ ↓
	$\overline{CF}$ disable time	t_{HABCS}	140		ns	From $X_{A, B}$, $Y_{A, B}$
	Pulse width	t_{PWCS}	200		ns	
$\overline{X}$/Y	Address setup time	t_{SACS}	0		ns	To $\overline{CS}$ ↓
U/$\overline{L}$	Address hold time	t_{HCSAB}	0		ns	From $\overline{CS}$ ↑
$D_{0 to 7}$	Output delay time	t_{DCSD}		150	ns	From $\overline{CS}$ ↓
	Output delay time	t_{DAD}		100	ns	From $\overline{X}$/Y, U/$\overline{L}$
	Floating time	t_{FCSD}		50	ns	From $\overline{CS}$ ↑

AC TEST INPUT WAVEFORM



AC test : The input is driven by 2.6 V for logic “1”, and 0.45 V for logic “0”.
Timing measurement is performed at 1.5 V for both logic “1” and logic “0”.

Fig. 6 Two-Phase Signal & Switch Signal Input Timing

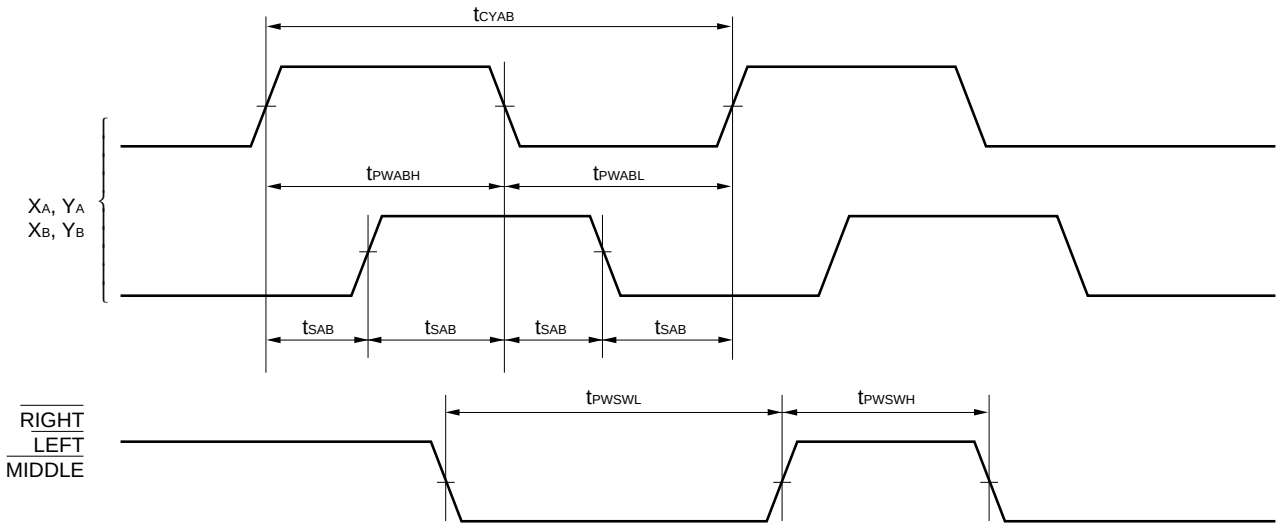


Fig. 7 Count Flag Output Timing

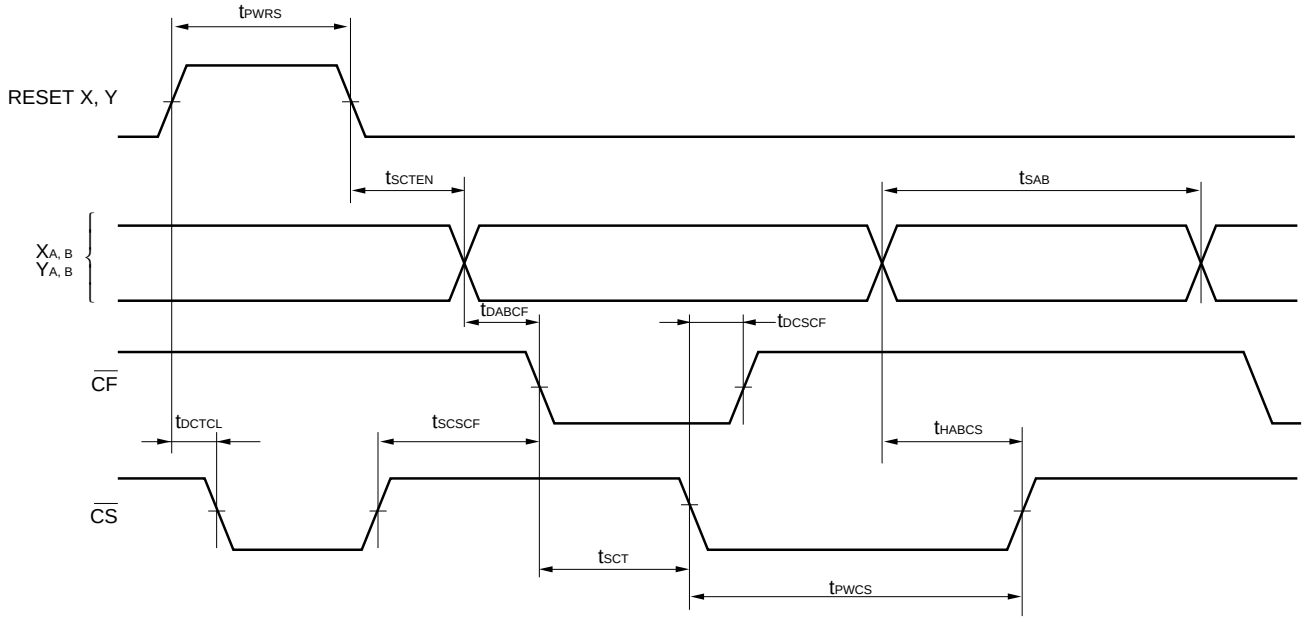


Fig. 8 Data Output Timing

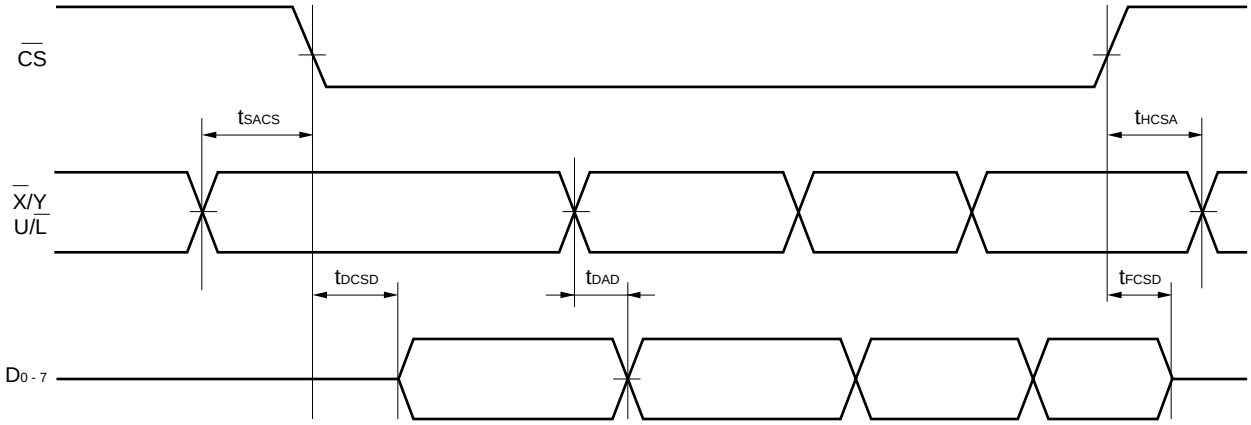
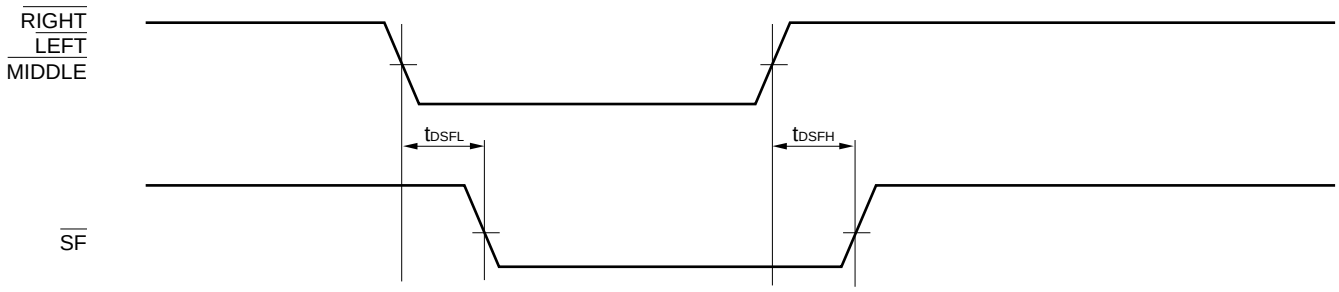


Fig. 9 Switch Flag Signal Output Timing



RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

μPD4701AGT

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: None	IR35-00-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: None	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit*: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

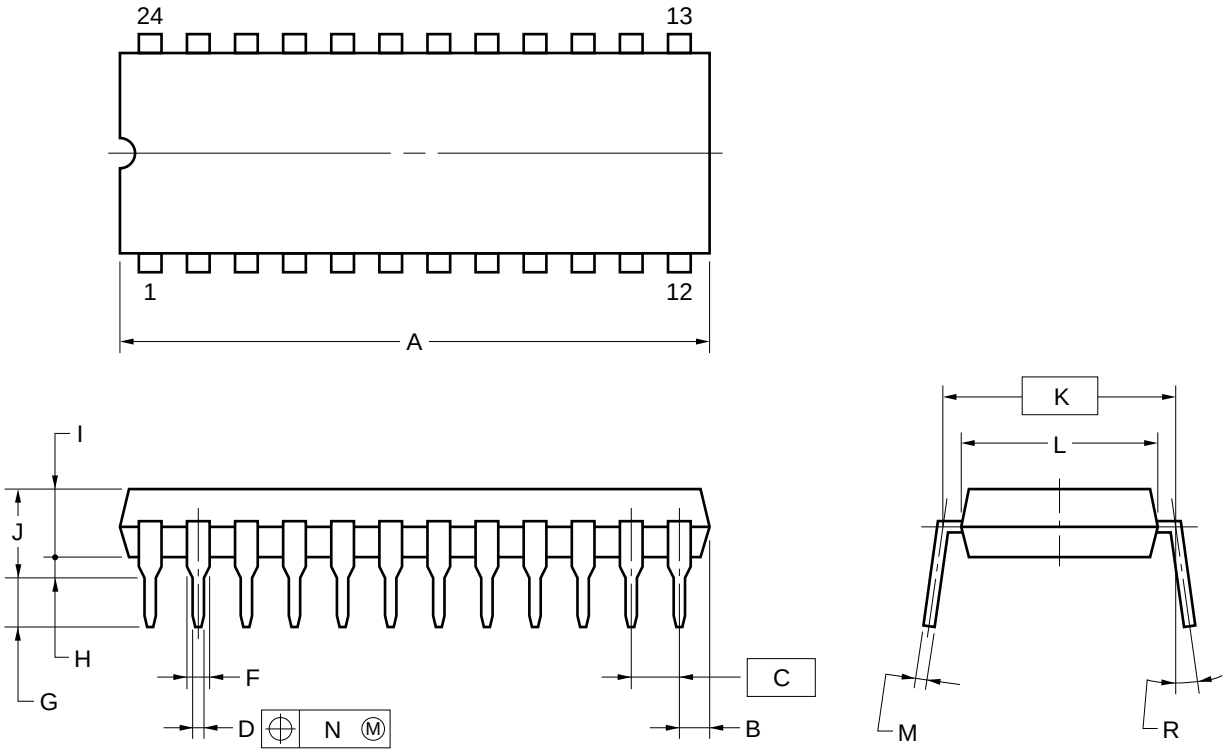
Note Do not apply more than a single process at once, except for "Partial heating method".

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD4701AC

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	

24PIN PLASTIC DIP (600 mil)



NOTES

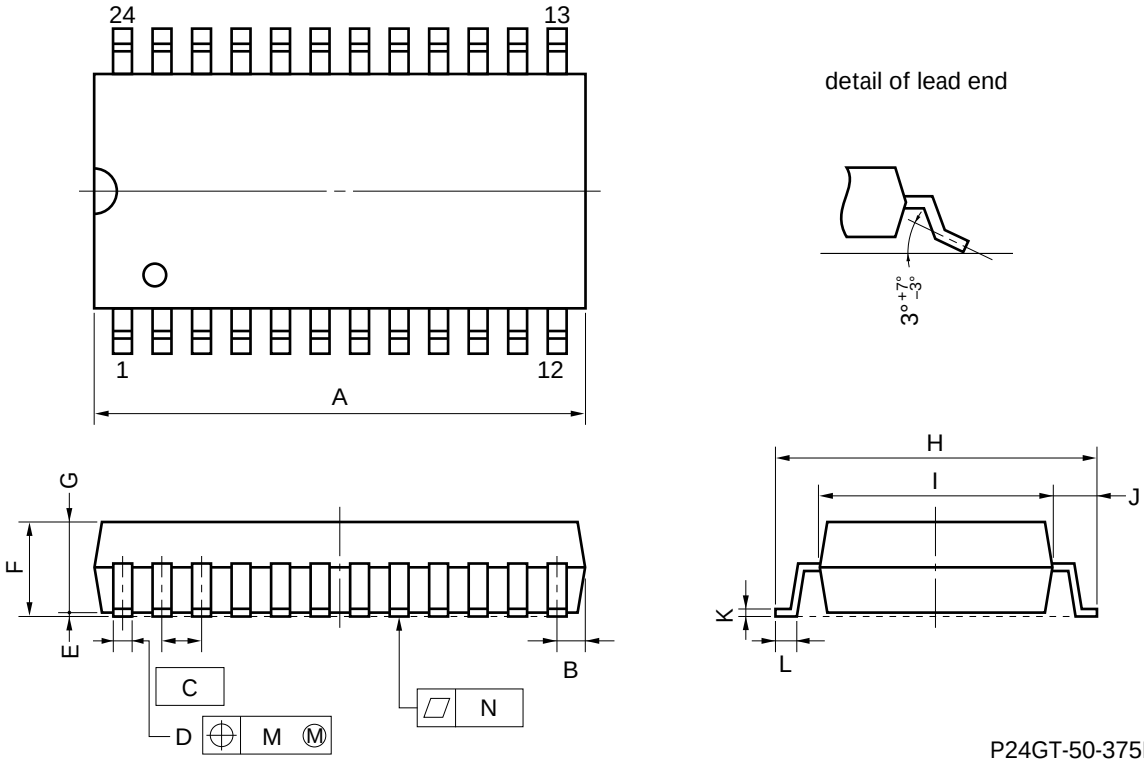
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	33.02 MAX.	1.300 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P24C-100-600-1

24 PIN PLASTIC SOP (375 mil)



P24GT-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.71 MAX.	0.619 MAX.
B	0.87 MAX.	0.035 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.50±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2±0.2	$0.283^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

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Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.

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