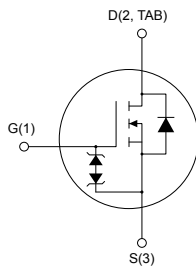


## N-channel 500 V, 2.2 $\Omega$ typ., 3 A SuperMESH™ Power MOSFETs in IPAK and DPAK packages



AM01479V1

### Features

Order codes	$V_{DS}$	$R_{DS(on)}$ max.	$P_{TOT}$	Package
STD4NK50Z-1	500 V	2.7 $\Omega$	45 W	IPAK
STD4NK50ZT4				DPAK

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

### Applications

- Switching applications

### Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

#### Product status link

[STD4NK50Z-1](#)
[STD4NK50ZT4](#)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	500	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	3	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
ESD	Gate-source human body model ( $C = 100\text{ pF}$ , $R = 1.5\text{ k}\Omega$ )	2.8	kV
$T_j$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 3\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		IPAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	100		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb		50	$^\circ\text{C}/\text{W}$

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2oz Cu board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j\text{ max}$ )	3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	120	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, T_C = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$		2.2	2.7	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	310		pF
$C_{oss}$	Output capacitance			49		
$C_{rss}$	Reverse transfer capacitance			10		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to } 400\text{ V}$	-	33		
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 3\text{ A}, V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	12		nC
$Q_{gs}$	Gate-source charge			3		
$Q_{gd}$	Gate-drain charge			7		

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 1.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$		10		ns
$t_r$	Rise time			7		
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	21		ns
$t_f$	Fall time			11		

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	260		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 40\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	935		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	7.2		A

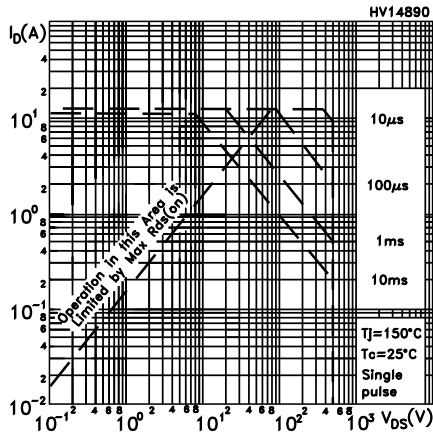
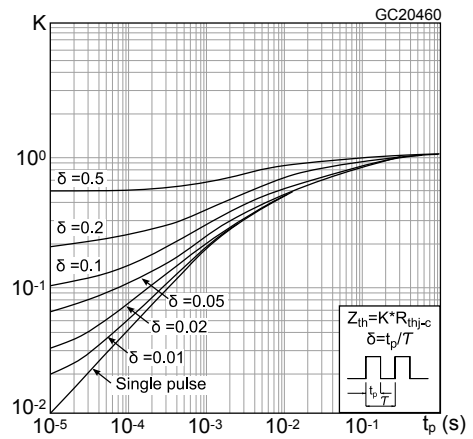
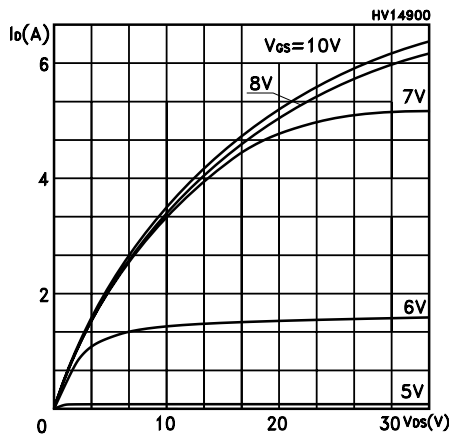
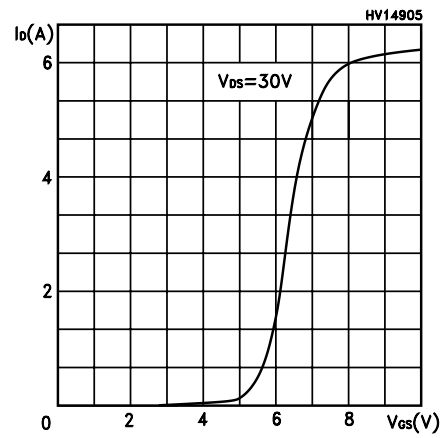
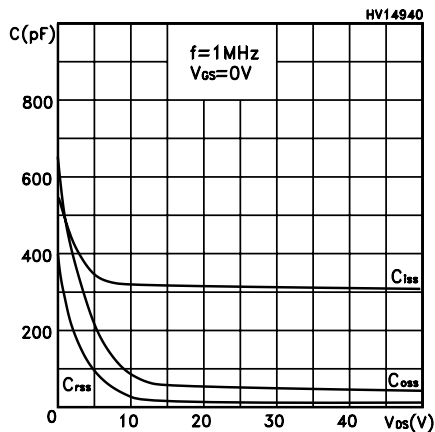
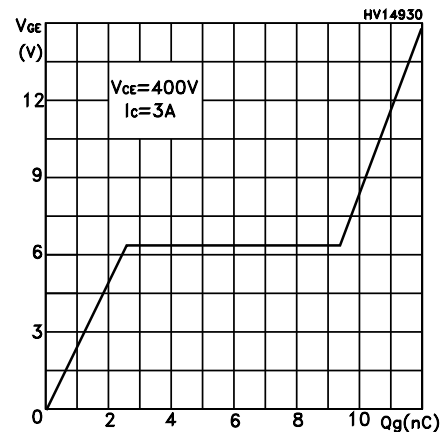
1. Pulse width limited by safe operating area.

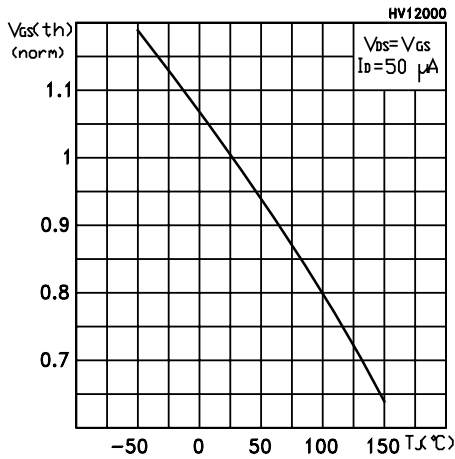
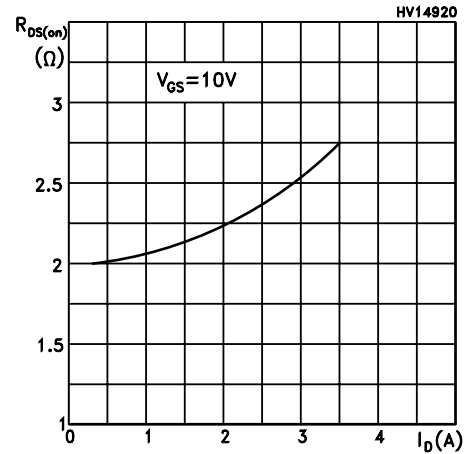
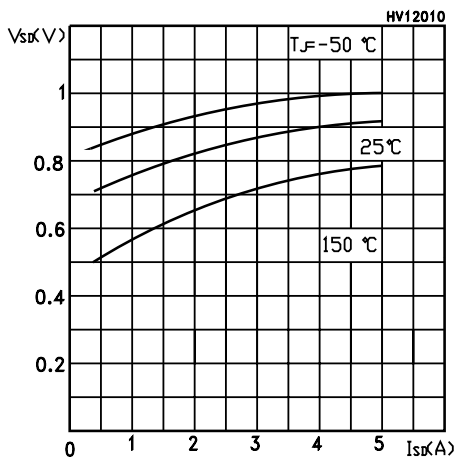
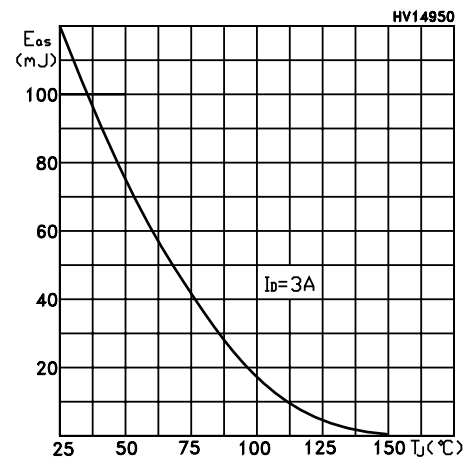
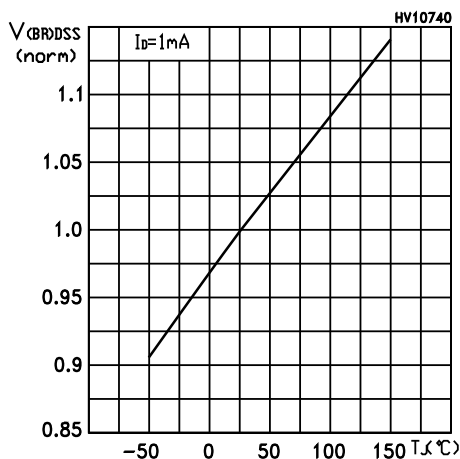
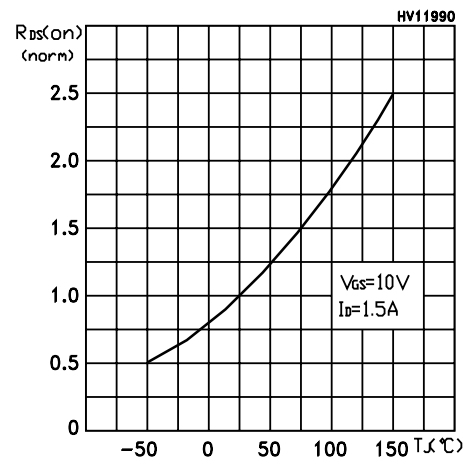
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

**Table 8. Gate-source Zener diode**

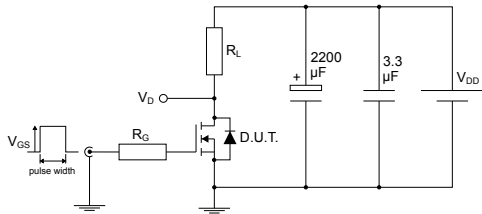
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

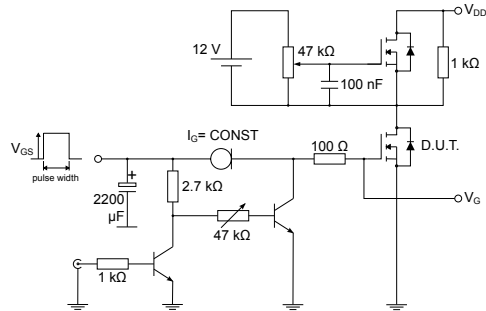
**2.1 Electrical characteristics (curves)**
**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Capacitance variations**

**Figure 6. Gate charge vs gate-source voltage**


**Figure 7. Normalized gate threshold voltage vs temperature**

**Figure 8. Static drain-source on resistance**

**Figure 9. Source-drain diode forward characteristic**

**Figure 10. Maximum avalanche energy vs temperature**

**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 12. Normalized on resistance vs temperature**


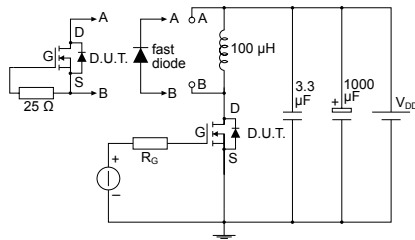
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


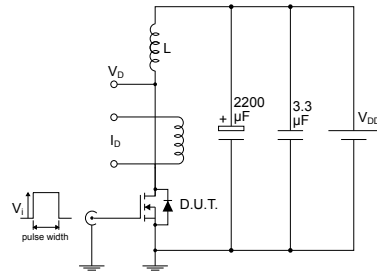
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


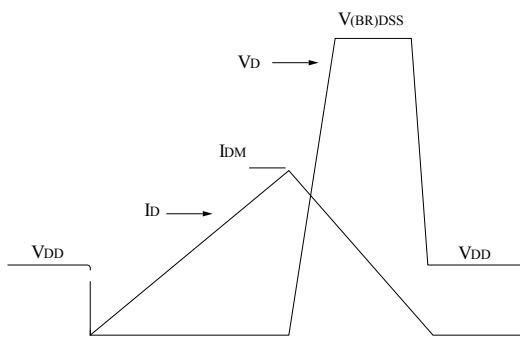
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


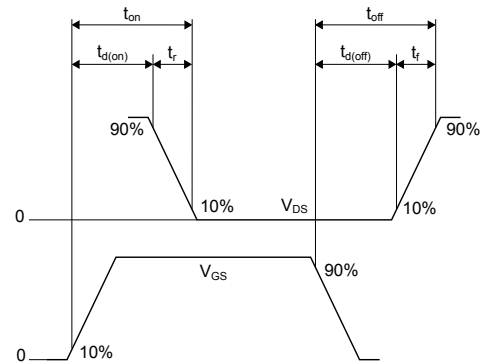
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

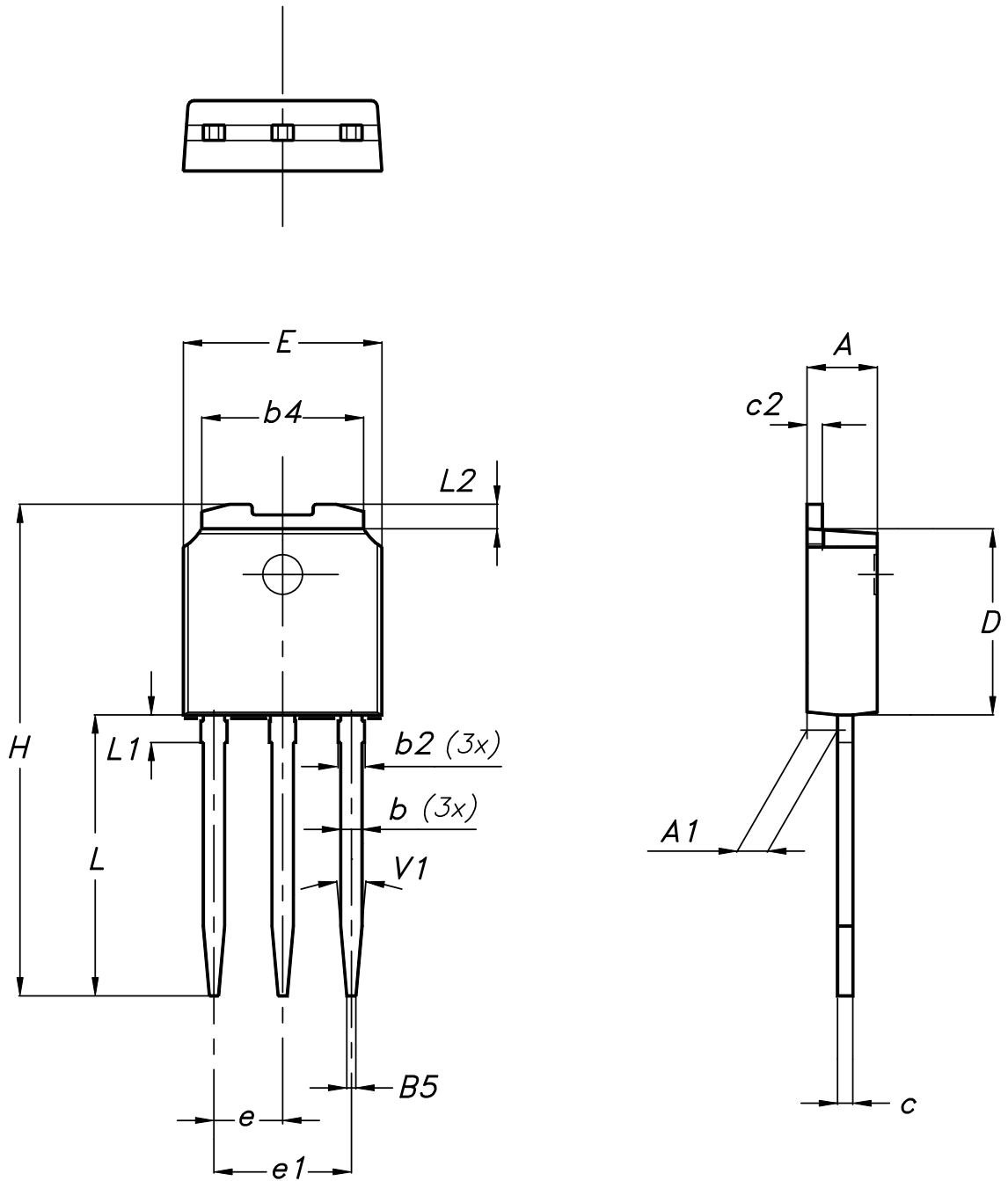
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



### 4.1 IPAk (TO-251) type A package information

Figure 19. IPAk (TO-251) type A package outline



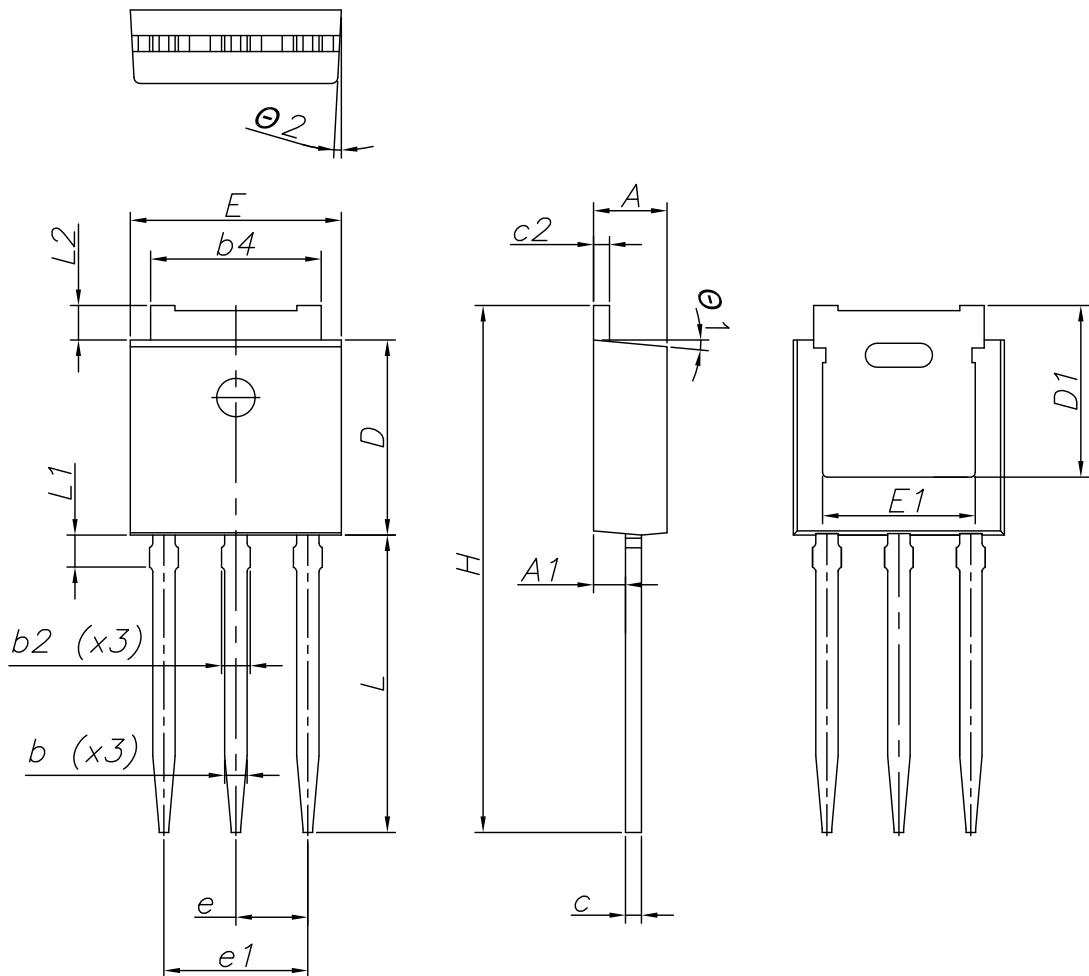
0068771\_IK\_typeA\_rev14

**Table 9. IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

## 4.2 IPAK (TO-251) type C package information

Figure 20. IPAK (TO-251) type C package outline



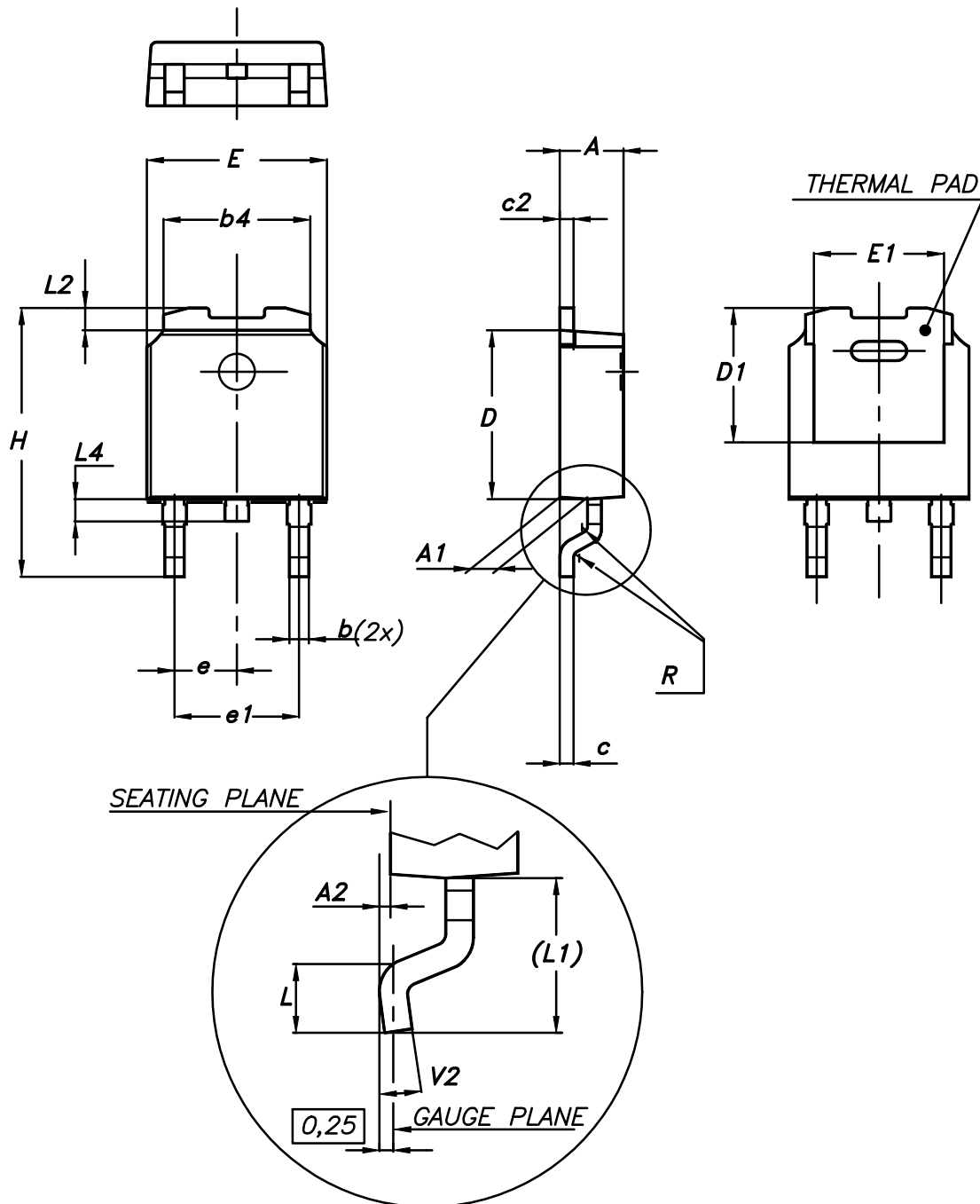
0068771\_IK\_typeC\_rev14

**Table 10. IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

### 4.3 DPAK (TO-252) type A package information

Figure 21. DPAK (TO-252) type A package outline



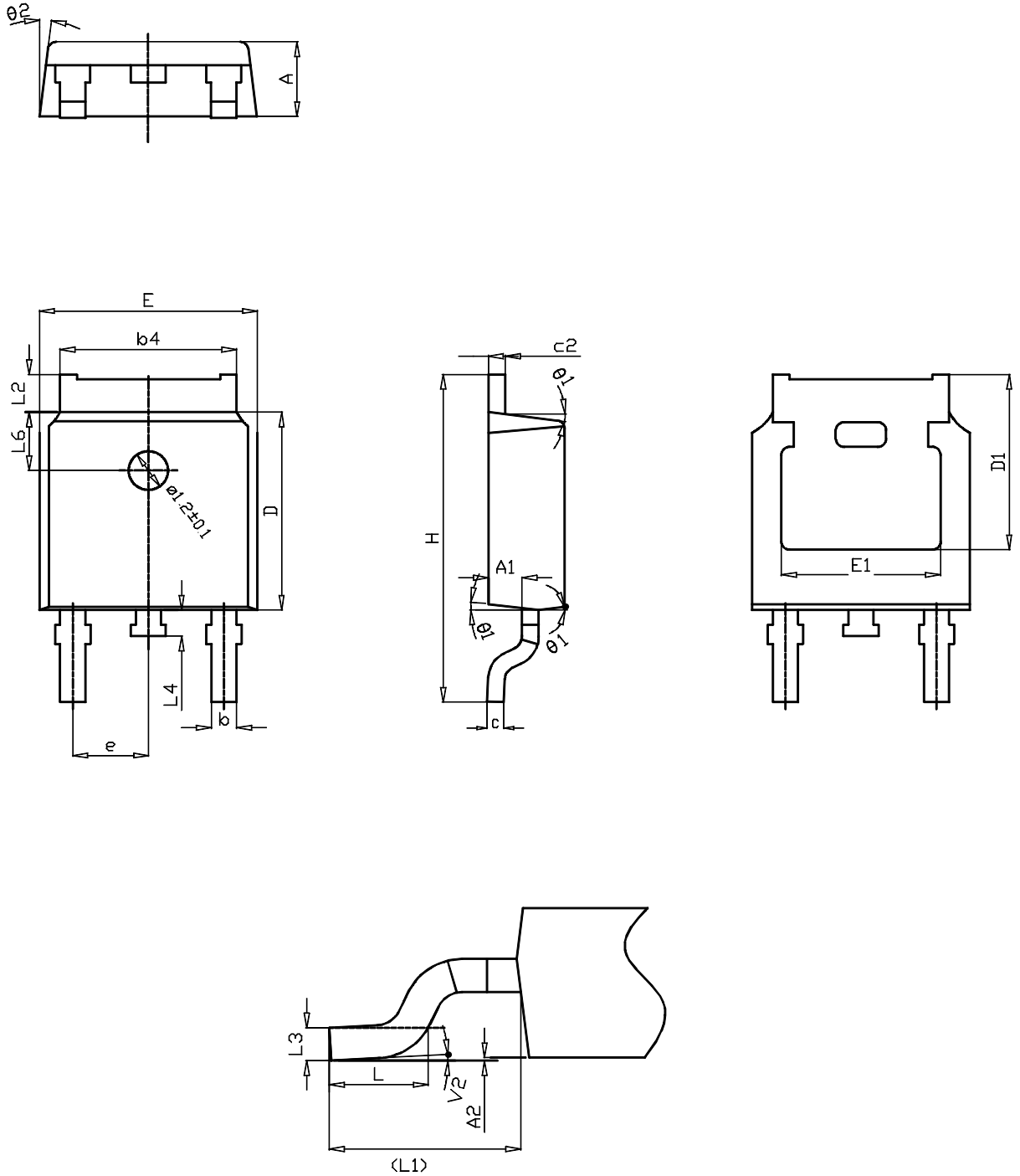
0068772\_A\_25

**Table 11. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

#### 4.4 DPAK (TO-252) type C package information

Figure 22. DPAK (TO-252) type C package outline



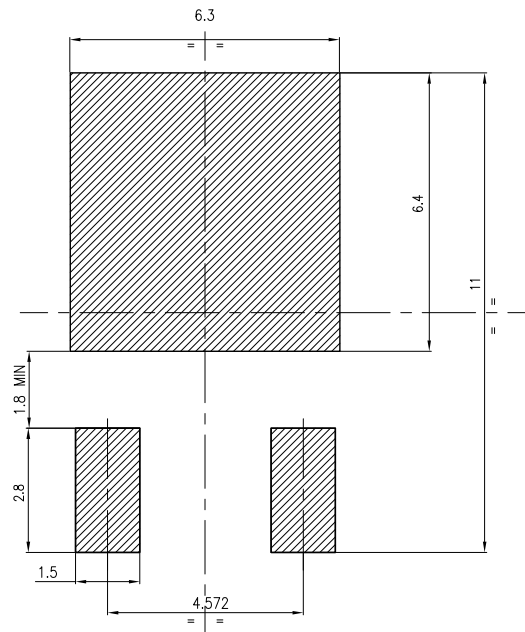
0068772\_C\_25

**Table 12. DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°



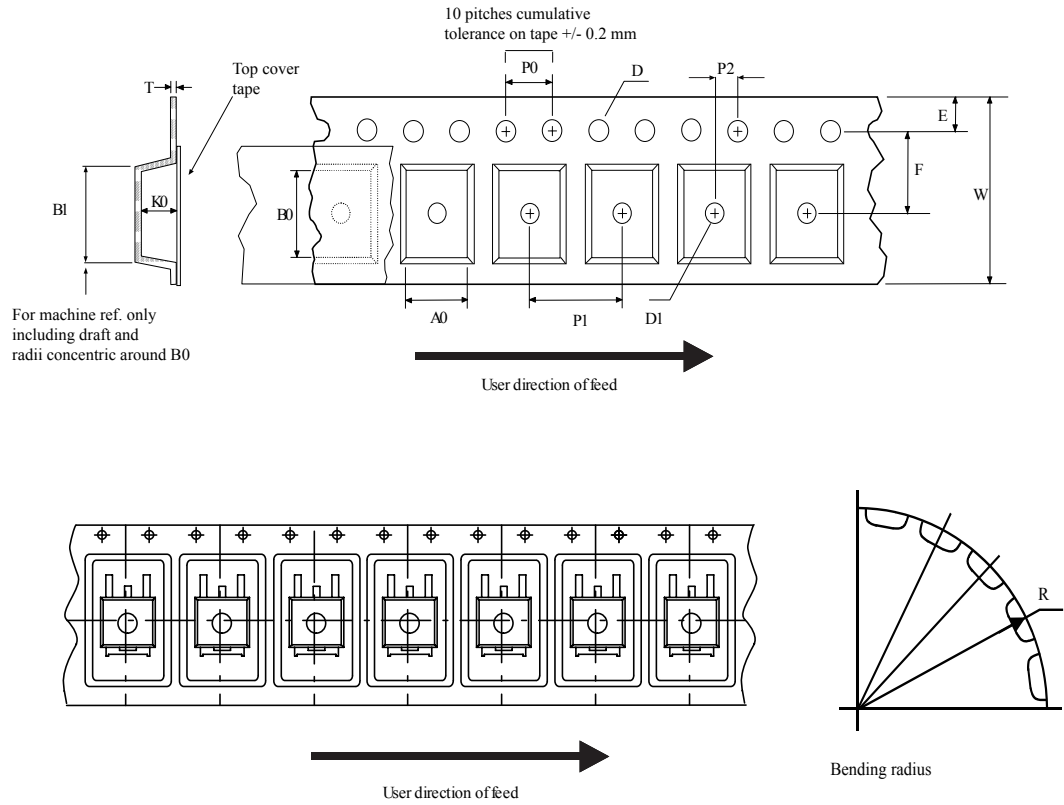
Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



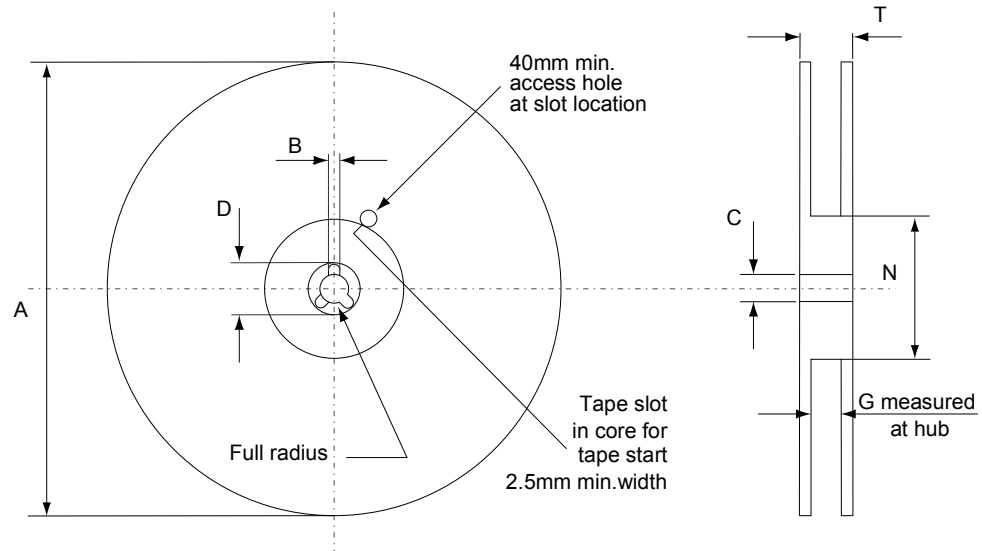
FP\_0068772\_25\_C

## 4.5 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



AM08852v1

**Figure 25. DPAK (TO-252) reel outline**


AM06038v1

**Table 13. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STD4NK50Z-1	D4NK50Z	IPAK	Tube
STD4NK50ZT4		DPAK	Tape and reel

## Revision history

**Table 15. Document revision history**

Date	Version	Changes
09-Dec-2002	2	Updated document.
20-Aug-2018	3	<p>Removed maturity status indication from cover page. The document status is production data.</p> <p>The part numbers STP4NK50Z and STP4NK50FP have been moved to a separate datasheet.</p> <p>Updated <a href="#">Section 1 Electrical ratings</a>, <a href="#">Section 2 Electrical characteristics</a> and <a href="#">Section 4 Package information</a>.</p> <p>Added <a href="#">Section 5 Ordering information</a>.</p> <p>Minor text changes.</p>

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