ALPHA & OMEGA
SEMICONDUCTOR

AOD5T40P

400V,3.9A N-Channel MOSFET

General Description

- Trench Power AlphaMOS-II technology
- Low $R_{DS(ON)}$
- Low Ciss and Crss
- High Current Capability
- RoHS and Halogen Free Compliant

Applications

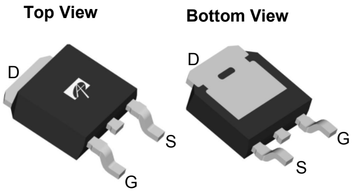
- General Lighting for LED and CCFL
- AC/DC Power supplies for Industrial, Consumer, and Telecom

Product Summary

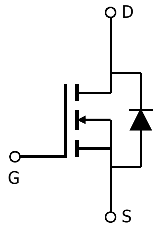
V_{DS} @ $T_{j,max}$	500V
I_{DM}	15A
$R_{DS(ON),max}$	< 1.45Ω
$Q_{g,typ}$	5nC
E_{oss} @ 320V	0.9µJ

100% UIS Tested
100% R_g Tested

TO-252
DPAK



AOD5T40P



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD5T40P	TO-252	Tape & Reel	2500

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	3.9	A
	T_C=100°C		2.5	
Pulsed Drain Current [C]		I_{DM}	15	
Avalanche Current [C] L=1mH		I_{AR}	5	A
Repetitive avalanche energy [C]		E_{AR}	13	mJ
Single pulsed avalanche energy [H]		E_{AS}	108	mJ
MOSFET dv/dt ruggedness		dv/dt	50	V/ns
Peak diode recovery dv/dt			5	
Power Dissipation [B]	T_C=25°C	P_D	52	W
	Derate above 25°C		0.4	W/°C
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		T_L	300	°C

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient [A,D]	$R_{\theta JA}$	45	55	°C/W
Maximum Case-to-sink [A]	$R_{\theta CS}$	-	0.5	°C/W
Maximum Junction-to-Case[D,F]	$R_{\theta JC}$	2	2.4	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C	400			V
		I_D=250µA, V_{GS}=0V, T_J=150°C		500		
BV_{DSS} /∆TJ	Breakdown Voltage Temperature Coefficient	I_D=250µA, V_{GS}=0V		0.39		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=400V, V_{GS}=0V			1	µA
		V_{DS}=320V, T_J=125°C			10	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±30V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=5V, I_D=250µA	3	4.2	5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=1A		1.2	1.45	Ω
g_{FS}	Forward Transconductance	V_{DS}=40V, I_D=1A		1.9		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.8	1	V
I_S	Maximum Body-Diode Continuous Current				3.9	A
I_{SM}	Maximum Body-Diode Pulsed Current [C]				15	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz		273		pF
C_{oss}	Output Capacitance			16		pF
$C_{o(er)}$	Effective output capacitance, energy related [I]	V_{GS}=0V, V_{DS}=0 to 320V, f=1MHz		18		pF
$C_{o(tr)}$	Effective output capacitance, time related [J]			30		pF
C_{rss}	Reverse Transfer Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz		1.5		pF
R_g	Gate resistance	f=1MHz		2.3		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=320V, I_D=3.9A		5	9	nC
Q_{gs}	Gate Source Charge			1.8		nC
Q_{gd}	Gate Drain Charge			1.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=200V, I_D=3.9A, R_G=25Ω		17		ns
t_r	Turn-On Rise Time			14		ns
$t_{D(off)}$	Turn-Off DelayTime			18		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=3.9A,dI/dt=100A/µs,V_{DS}=100V		172		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=3.9A,dI/dt=100A/µs,V_{DS}=100V		1.1		µC

A. The value of R $_{qJA}$ is measured with the device in a still air environment with T_A=25° C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The R $_{\theta JA}$ is the sum of the thermal impedance from junction to case R $_{qJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C.
G.These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
H. L=60mH, I_{AS}=1.9A, V_{DD}=150V, R_G=10Ω, Starting T_J=25° C.
I. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS.}$
J. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS.}$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

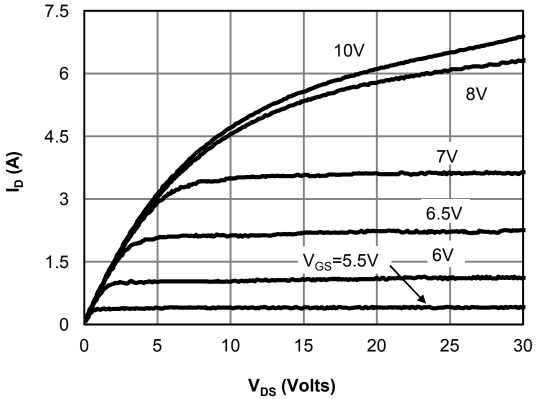


Figure 1: On-Region Characteristics

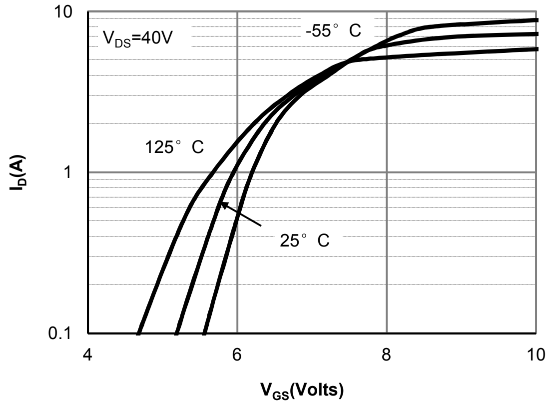


Figure 2: Transfer Characteristics

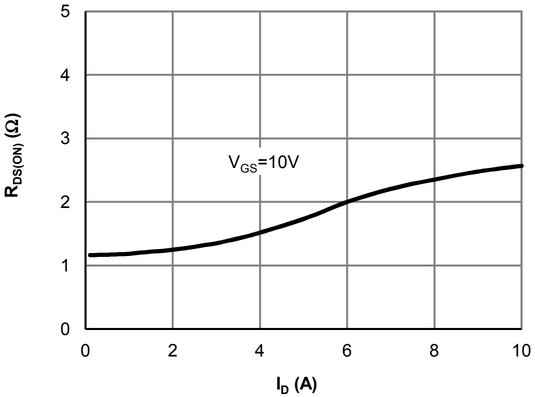


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

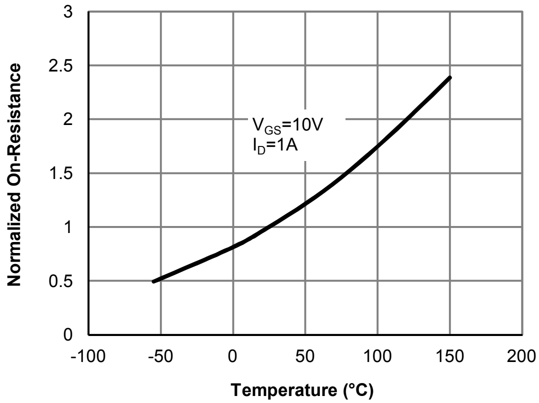


Figure 4: On-Resistance vs. Junction Temperature

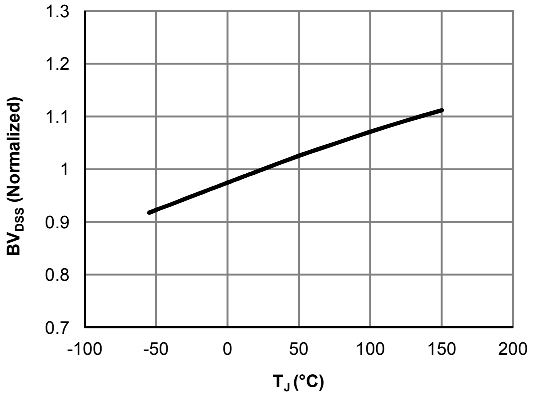


Figure 5: Break Down vs. Junction Temperature

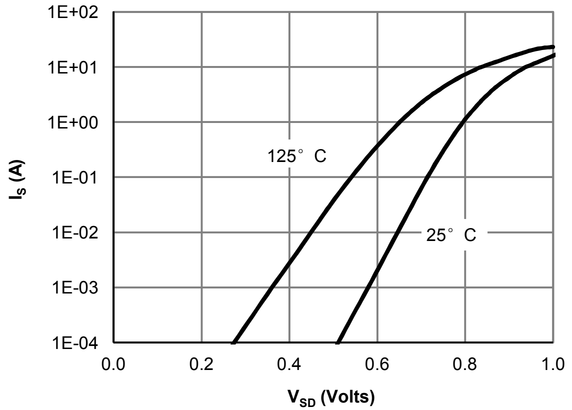


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

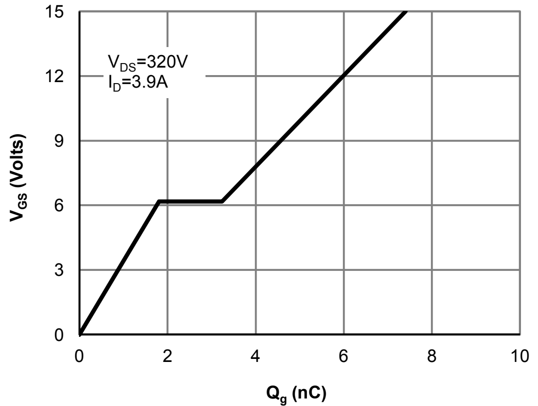


Figure 7: Gate-Charge Characteristics

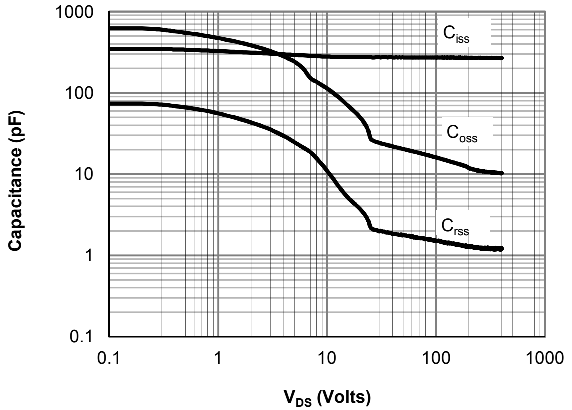


Figure 8: Capacitance Characteristics

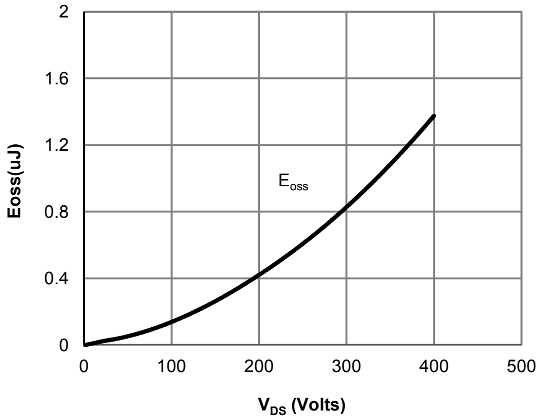


Figure 9: Coss stored Energy

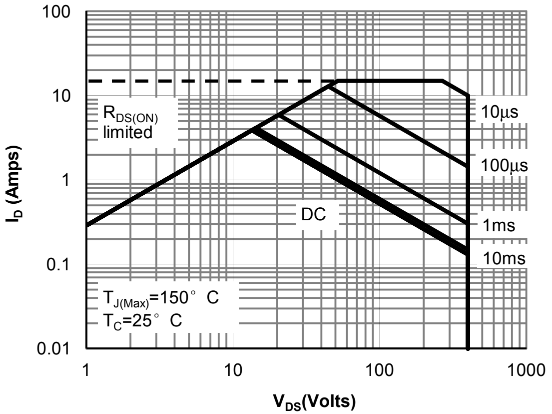


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

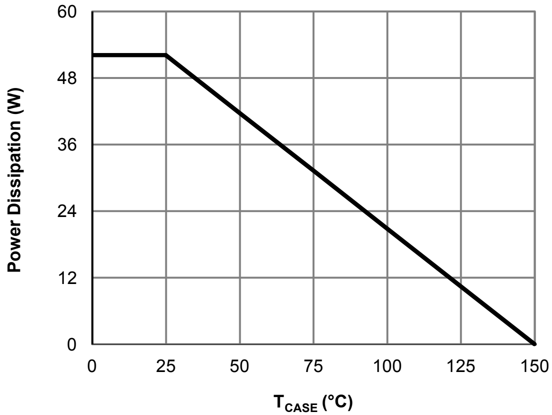


Figure 11: Power De-rating (Note B)

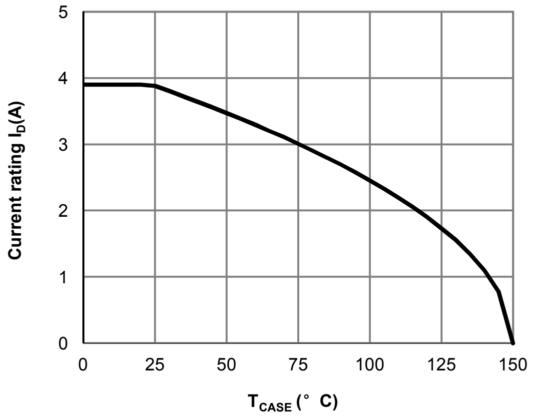


Figure 12: Current De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

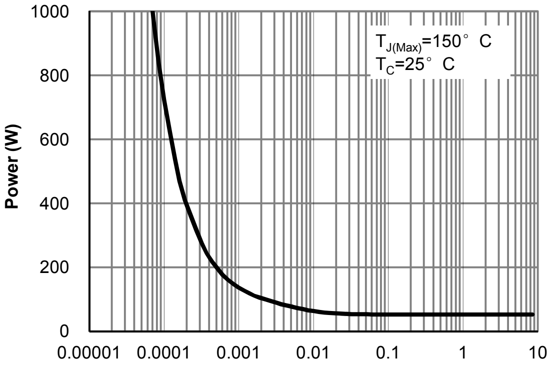


Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)

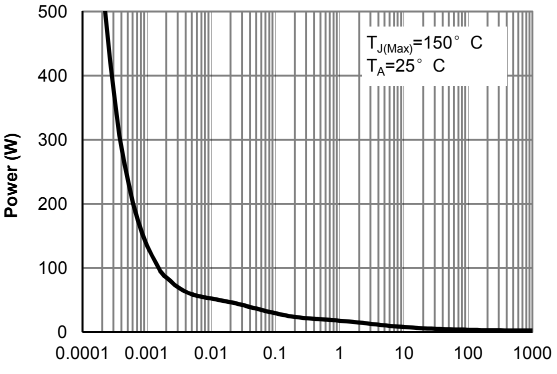


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

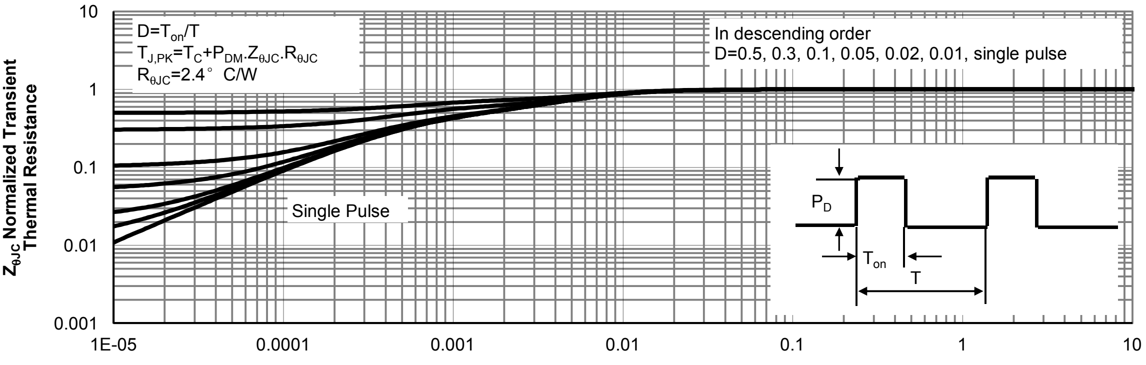


Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)

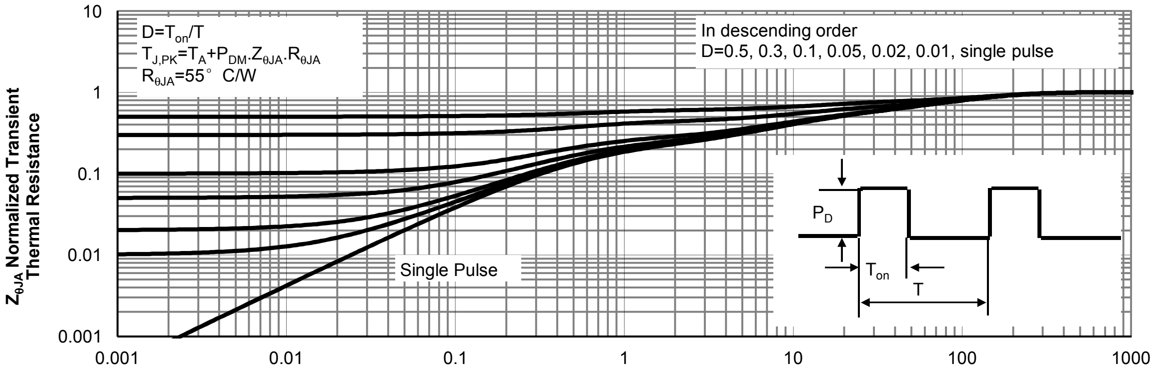
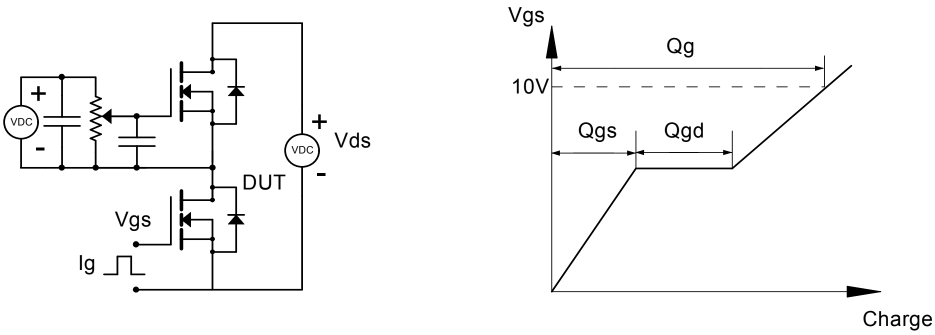
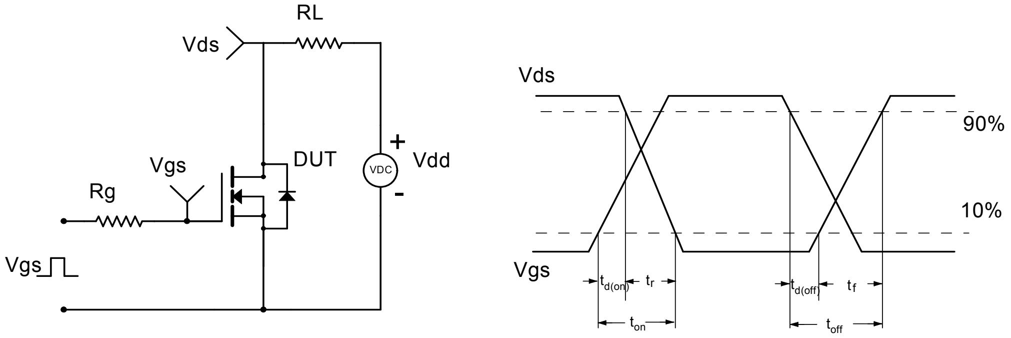


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

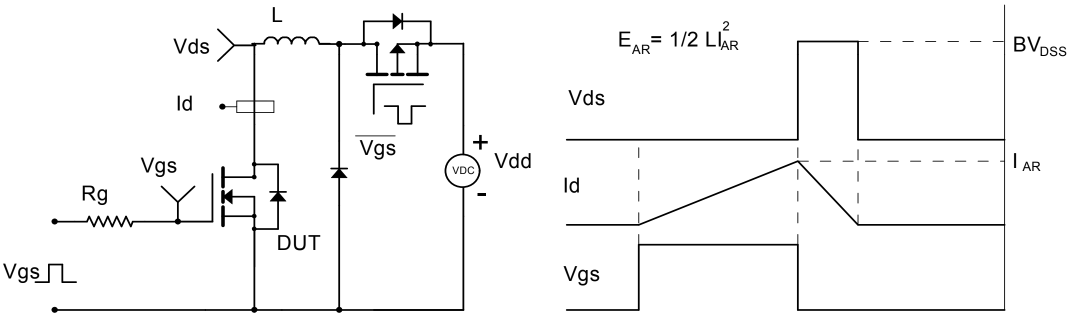
Gate Charge Test Circuit & Waveform



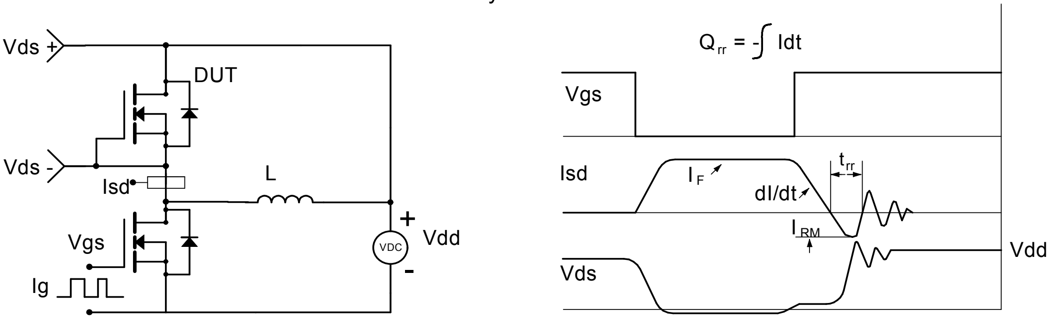
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



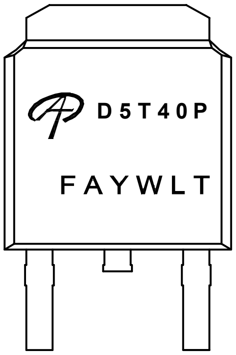
Diode Recovery Test Circuit & Waveforms



ALPHA & OMEGA
SEMICONDUCTOR

Document No.	PD-02166
Version	B
Title	AOD5T40P Marking Description

TO252(DPAK) PACKAGE MARKING DESCRIPTION



Green product

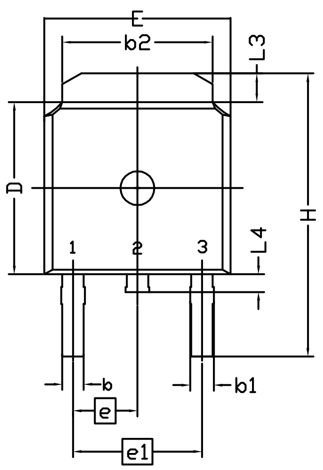
NOTE:
LOGO - AOS Logo
D5T40P - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

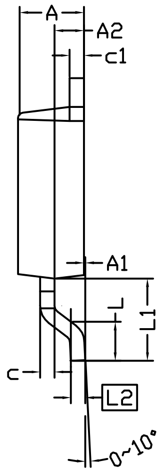
PART NO.	DESCRIPTION	CODE
AOD5T40P	Green product	D5T40P

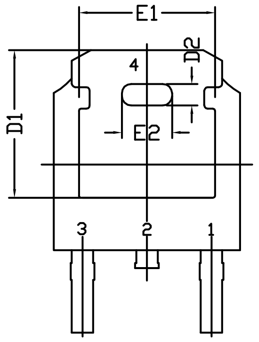
ALPHA & OMEGA
SEMICONDUCTOR, LTD.

Document No.	PO-00009
Version	S

TO252(DPAK) PACKAGE OUTLINE

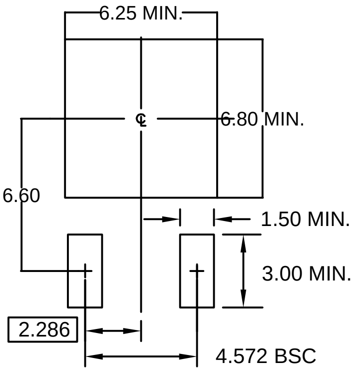






SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	-----	0.127	0.000	-----	0.005
A2	0.889	1.041	1.143	0.035	0.041	0.045
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.762	0.840	1.143	0.030	0.033	0.045
b2	4.953	5.340	5.461	0.195	0.210	0.215
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.610	0.018	0.020	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
D2	0.662	0.762	0.862	0.026	0.030	0.034
E	6.350	6.604	6.731	0.250	0.260	0.265
E1	4.318	4.826	4.901	0.170	0.190	0.193
E2	1.678	1.778	1.878	0.066	0.070	0.074
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.414	0.370	0.395	0.410
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.635	-----	1.016	0.025	-----	0.040

RECOMMENDED LAND PATTERN



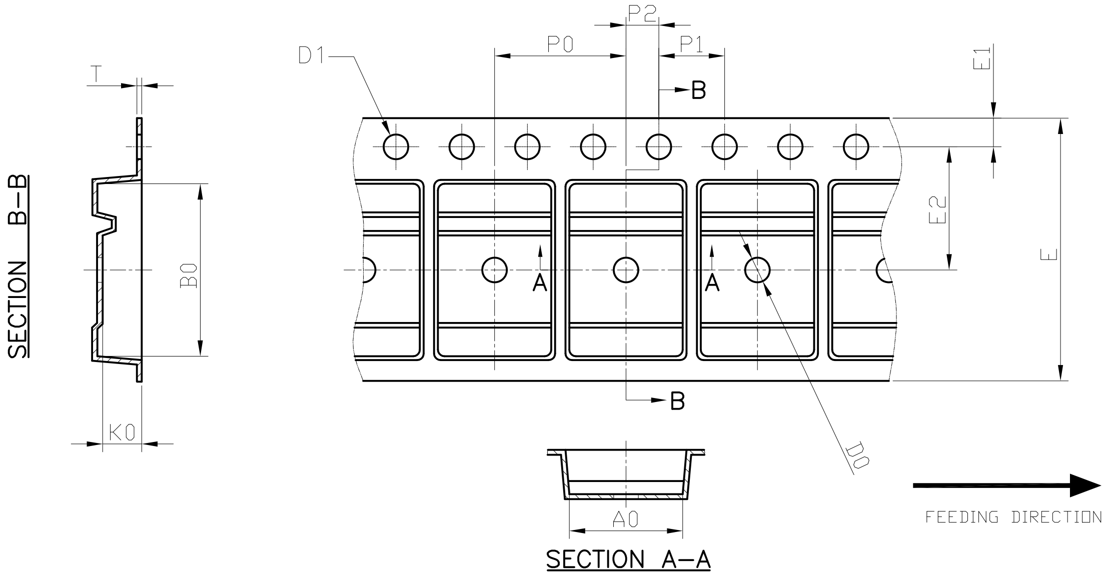
UNIT: mm

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)

ALPHA & OMEGA
SEMICONDUCTOR

DPAK Tape and Reel Data

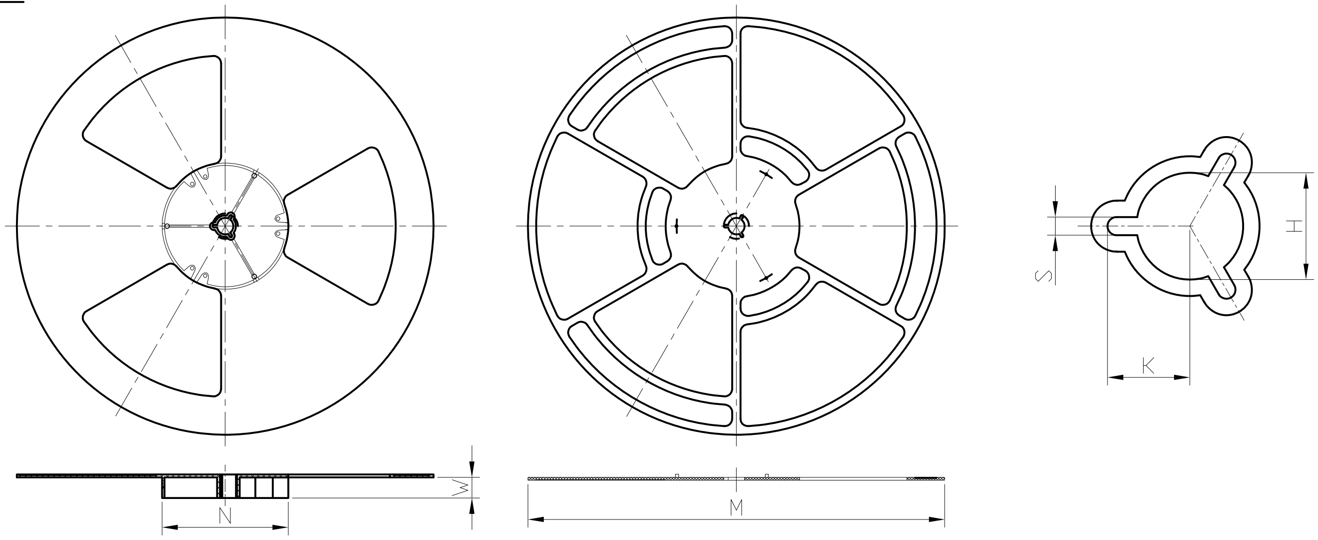
DPAK Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DPAK (16 mm)	6.90 ±0.10	10.50 ±0.10	2.50 ±0.10	1.50 +0.1 −0	1.50 +0.1 −0	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

DPAK Reel

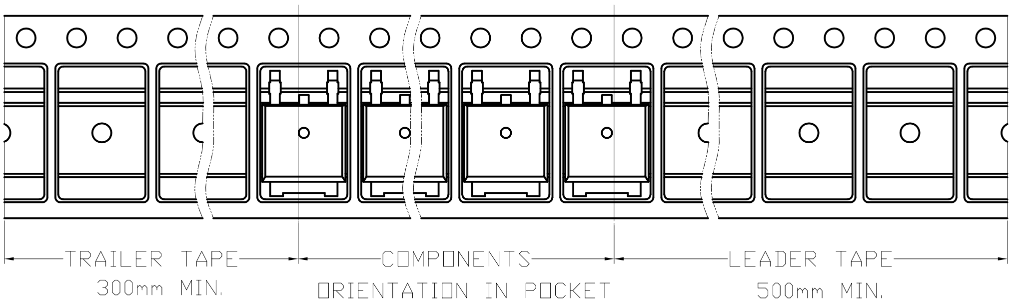


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
16 mm	ø330	ø330.00 +0.25 −4.00	ø100.00 ±0.2	16.4 +2.0 −0.0	ø13.00 +0.50 −0.20	10.5 ±0.25	2.2 ±0.25

DPAK Tape

Leader / Trailer
& Orientation



Unit Per Reel:
2500pcs

AOS Semiconductor
Product Reliability Report

AOD5T40P, rev B

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

This AOS product reliability report summarizes the qualification result for AOD5T40P. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOD5T40P passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

Table of Contents:

I. Product Description:

- Trench Power AlphaMOS-II technology
- Low $R_{DS(ON)}$
- Low Ciss and Crss
- High Current Capability
- RoHS and Halogen Free Compliant

Details refer to the datasheet.

II. Die / Package Information:

	AOD5T40P
Process	Standard sub-micron 400V N-Channel MOSFET
Package Type	TO252
Lead Frame	Bare Cu
Die Attach	Solder Paste
Bond	Al & Cu wire
Mold Material	Epoxy resin with silica filler
Moisture Level	Level 1

III. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	**Temp = 150°C , Vgs=100% of Vgsmax**	**168 / 500 / 1000 hours**	**462 pcs**	**0**	**JESD22-A108**
HTRB	**Temp = 150°C , Vds=80% of Vdsmax**	**168 / 500 / 1000 hours**	**462 pcs**	**0**	**JESD22-A108**
MSL Precondition	**168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)**	**-**	**5313 pcs**	**0**	**JESD22-A113**
HAST	**130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax Up to 42V**	**96 hours**	**924 pcs**	**0**	**JESD22-A110**
H3TRB	**85°C , 85%RH, Vds = 80% of Vdsmax Up to 100V**	**1000 hours**	**924 pcs**	**0**	**JESD22-A101**
Autoclave	**121°C , 29.7psia, RH=100%**	**96 hours**	**924 pcs**	**0**	**JESD22-A102**
Temperature Cycle	**-65°C to 150°C , air to air,**	**250 / 500 cycles**	**924 pcs**	**0**	**JESD22-A104**
HTSL	**Temp = 150°C**	**1000 hrs**	**924 pcs**	**0**	**JESD22-A103**
Power Cycling	**Δ Tj = 100°C**	**15000 cycles**	**693 pcs**	**0**	**AEC Q101**

Note: The reliability data presents total of available generic data up to the published date.

IV. Reliability Evaluation

FIT rate (per billion): 6.53
MTTF = 17473 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = Chi^2 x 10^9 **/** **[**2 (N) (H) (Af)**]** **=** 6.53
MTTF = 10^9 / FIT = 17473 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]
Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	**259**	**87**	**32**	**13**	**5.64**	**2.59**	**1**

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K