

CMOS LSI FOR 12 lines × 24 columns CHARACTER DISPLAY ON SCREEN

The μ PD6453 is a CMOS LSI device for on-screen character displays designed to display characters such as the time of day, channel numbers, and chapter numbers on a TV screen when used in a TV or video disk in combination with a microcomputer. By using this IC in a video camera or VCR, the time of day and date can also be recorded over video signals.

Each character is in a 12 x 18 dot pattern and by combining two or more characters, Chinese characters (Kanji) or graphics may be displayed. By using a character RAM for 16 characters, a character or graphic pattern can be changed while it is being displayed.

In addition, thanks to its Power ON Reset function, Video RAM All Reset command and other built-in functions, the μ PD6453 helps lighten a burden on the microcomputer.

NEC offers two types of devices μ PD6453CY-001 and μ PD6453GT-101 as standard products. Both the μ PD6453CY-001 and μ PD6453GT-101 have the same character specifications, but the former is housed in a 20-pin plastic DIP (Dual In-line Package) and the latter in a 20-pin plastic SOP (Small Out-line Package).

FEATURES

- No. of Display Characters : 12 lines x 24 columns
- Types of Characters : 256 types (ROM: 240 types; RAM: 16 types.)
- Character Size : Any one of 1H, 2H, 3H, and 4H per dot can be selected.
- Character Colors : Any one of 8 different colors can be selectable for each character.
- Background : One of "No background", "Square background" and "Solid background" is selectable per screen, together with fringe ON/OFF function. Any of eight different colors is selectable as the background color and together with the fringe color (black or white) selectable per screen.
- Dot Matrix : 12 x 18 pattern without spacing between characters
- Smooth function : Two different interpolations are available for selection per line with characters two to four times the normal size.
- Blinking Control : Blinking ON/OFF can be specified per character. The ON/OFF time ratio of blinking is 1:1 with a blinking frequency selectable from among about 2 Hz, about 1 Hz, and about 0.5 Hz.
- Mask Pulse (Code Option) : To be output in vertical direction for each line.
- Adaptability to Progressive Scan TV : Vertical and horizontal directions can be specified independently of each other.
- Video RAM Data Clear : Video RAM data can be reset with either the Video RAM All Clear command or the Power ON Clear function.
- Interface with Microcomputer : Variable-length serial input format in units of 8 bits
- Power Supply : +5 V single power supply
- Construction : CMOS low power consumption

ORDERING INFORMATION

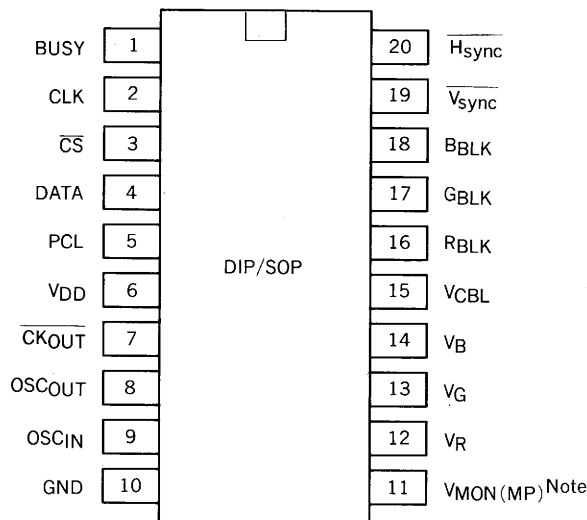
PART NUMBER	PACKAGE	QUALITY GRADE
μPD6453CY-001	20-pin plastic DIP (400 mil)	Standard
μPD6453GT-101	20-pin plastic SOP (375 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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CONNECTION DIAGRAM (Top View)

μPD6453CY, μPD6453GT



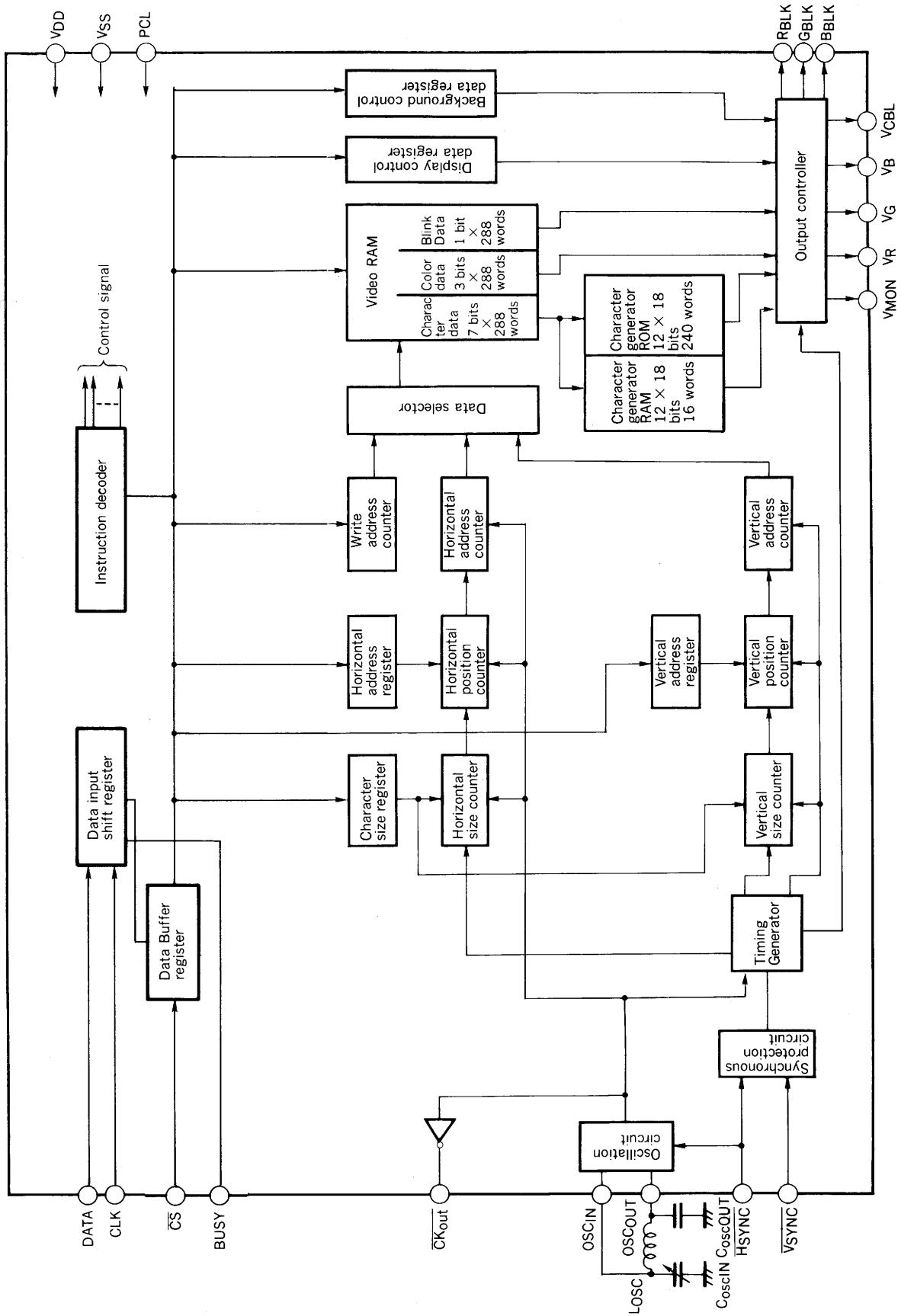
Note: Pin 10 (μPD6453CY/μPD6453GT) within parentheses is the mask code option to be used as the mask pulse. However, μPD6453CY-001/μPD6453GT-101 does not use the mask pulse, so pin 11 is used as monitor output V_{MON}.

PIN DESCRIPTION

SYMBOL	PIN NAME	FUNCTION
V _{DD}	Power supply terminal	This terminal supplies +5 V power.
V _{SS}	Grounding terminal	This is connected to the system GND.
DATA	Serial data input terminal	This terminal inputs control data. It reads data synchronizing with the clock input to the CLK terminal.
CLK	Clock input terminal	This terminal inputs the clock for reading data. At the rise of this clock, the data input to the DATA terminal is read.
\overline{CS}	Chip select terminal	Normal operation is performed when this is Low.
OSC _{IN} OSC _{OUT}	Oscillation terminals	These terminals are connected to the oscillation capacitor or coil.
\overline{HSYNC}	Horizontal synchronous signal input terminal	This terminal inputs the horizontal synchronizing signal. The oscillator oscillates when this signal is high, synchronizing with the rise of the signal. Be sure to input the horizontal synchronizing signal when it is active low.
\overline{VSYNC}	Vertical synchronizing signal input terminal	This terminal inputs the vertical synchronizing signal. Be sure to input this signal when it is active low.
V _R V _G V _B	Character signal output terminals	These terminals output the character signal corresponding to R, G, and B.
V _{BLK}	Blanking signal output terminal	This terminal outputs the blanking signal to cut the video signal.
R _{BLK} G _{BLK} B _{BLK}	Blanking signal output terminal	These terminals output the blanking signal which correspond to character signal (V _R , V _G , V _B).
PCL	Power ON reset terminal	The state will be initialize by this terminal Low to High when Power is ON.
\overline{CKOUT}	Clock output terminal	This is the inverted output of OSC _{OUT} . To connect another type of on-screen IC in parallel, be sure to connect this terminal to OSC _{IN} of the IC.
BUSY	Data input enable terminal	Output terminal to notify the microcomputer that data is enabled or disabled for input. Data can be input at a low level.
V _{MON} ^{Note}	Character signal output monitor terminal	If any of character signal outputs V _R , V _G , and V _B is High, the high-level signal is output.

Note: The mask code option enables this terminal to be used as the mask pulse output terminal. However, μ PD6453CY-001/ μ PD6453GT-101 does not use the mask pulse, so pin 11 is used as monitor output V_{MON}.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V _{DD} - V _{SS}	7.0	V
Input Voltage	V _{IN}	V _{DD} + 0.3 > V _{IN} > V _{SS} - 0.3	V
Output Voltage	V _{OUT}	V _{DD} + 0.3 > V _{OUT} > V _{SS} - 0.3	V
Output Current	I _O	±5	mA
Operating Temperature	T _{opt}	-20 to +75	°C
Storage Temperature	T _{stg}	-40 to +125	°C

RECOMMENDED OPERATING RANGE

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD} - V _{SS}	4.5	5.0	5.5	V
Oscillation Frequency	f _{osc}	4.0	7.0	12	MHz

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = 5.0 V, V_{SS} = 0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V _{DD} - V _{SS}	4.5	5.0	5.5	V	
Current Consumption	I _{DD}			15	mA	
Control Input High Level Voltage	V _{CIH}	2.4			V	
Control Input Low Level Voltage	V _{CIL}			0.8	V	
Synchronous Signal Input High Level Voltage	V _{SIH}	2.4			V	
Synchronous Signal Input Low Level Voltage	V _{SIL}			0.8	V	
Signal Output High Level Voltage	V _{OH}	4.5			V	I _{OH} = -1.0 mA
Signal Output Low Level Voltage	V _{OL}			0.5	V	I _{OL} = 1.0 mA
Clock Output High Level Voltage	V _{CKH}	4.5			V	I _{CKH} = -0.5 mA
Clock Output Low Level Voltage	V _{CKL}			0.5	V	I _{CKL} = 0.5 mA

Note: Control input DATA, CLK, \overline{CS} , PCL
 Synchronous signal input \overline{HSYNC} , \overline{VSYNC}
 Signal output V_R, V_G, V_B, V_{CBL}, V_{MON} (MP), BUSY, R_{BLK}, G_{BLK}, B_{BLK}.
 Clock output \overline{CKOUT}

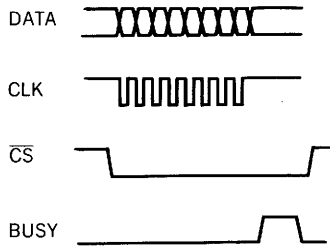
COMMAND FORMATS

All control commands are in a variable-length serial input format in units of eight bits. These commands are available in three types: 1-byte (8-bit) command consisting of an instruction part and data; 2-byte (16-bit) command consisting of an instruction part and data and 2nd byte continuous command which consists of two or more bytes and can be input in an abbreviated format.

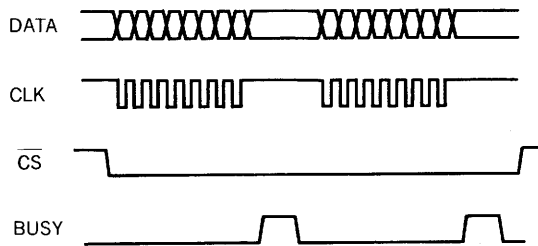
Each of these commands can be input while the \overline{CS} signal is in the Low (active) state and is followed by the BUSY signal on input of each 8-bit serial data. Please input datas from MSB.

Command Input Methods

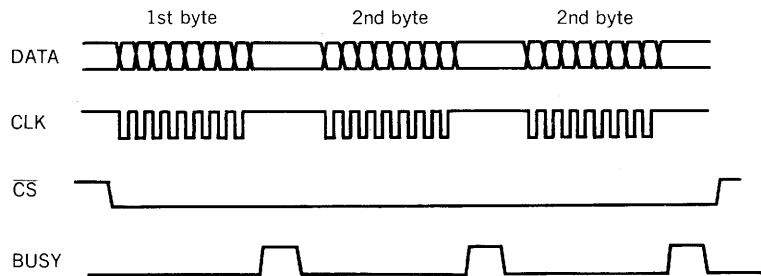
- To input one 1-byte command



- To input one 2-byte command



- To input one 2nd byte continuous command



The internal data processing is performed on input of every one byte (8 bits).
 (See the paragraph "Recommended Timing" on page 17 for \overline{CS} and BUSY.)

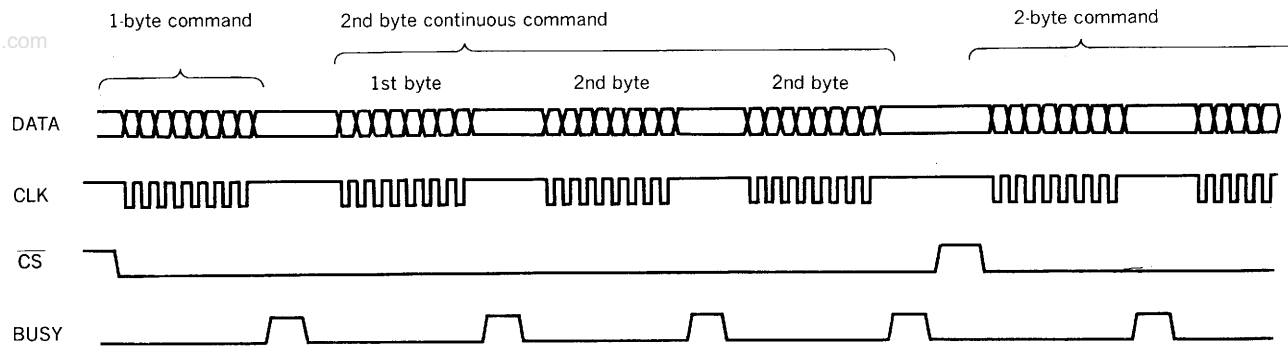
Method of Continuous Command Input

A 1-byte command, a 2-byte command, or a 2nd byte continuous command can be input continuously either individually or in combination with the other commands while keeping the \overline{CS} signal in the Low state (without setting the signal to the High state for delimiting each command input) with the exception of the case indicated below.

Restriction on Continuous Command Input

At the input of a 2nd byte continuous command, set the \overline{CS} signal to High (inactive) once and then to Low (active) and then enter the 1-byte or 2-byte command following the 2nd byte continuous command.

Example: Continuous input of 1-byte command, 2nd byte continuous command, and 2-byte command



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μPD6453CY-XXX/μPD6453GT-XXX Command List

1. 1-byte command

Content	(MSB)							(LSB)	
	D7	D6	D5	D4	D3	D2	D1	D0	
Display control	0	0	0	0	D0	LOSC	BL1	BL0	
Background control	0	1	0	0	0	BS1	BS0	Eg	
Background color control	0	0	0	1	Rb	Gb	Bb	Egc	
Progressive scan control	0	0	1	1	0	0	VC	HC	
Video RAM all reset	0	0	1	1	0	1	0	0	

2. 2-byte command

Content	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Character write address control	1	0	0	0	0	1	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Character RAM write address control	1	0	0	0	0	1	1	RW3	RW2	RW1	RW0	RL4	RL3	RL2	RL1	RL0
Character size, smooth, mask pulse control	1	0	0	0	1	MP	S1	S0	0	0	SM1	SM0	AR3	AR2	AR1	AR0
Character RAM write data control	1	0	0	1	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Test mode control: (don't use)	1	0	1	0	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

3. 2nd byte continuous command

Content	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	0	0	R	G	B	Blink	C7	C6	C5	C4	C3	C2	C1	C0

POWER ON RESET

At the time of power on, the internal states of this IC are indefinite (unknown). For this reason, be sure to perform the Power ON Reset operation to set the IC to the initialized states by turning the voltage level of the PCL pin from Low to High. The commands to be set by this Power ON Reset operation are as follows:

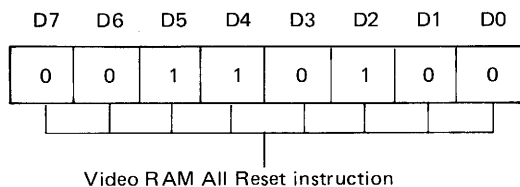
- The contents of the character RAM are all Reseted to "0" (without dot).
- The word address and line address values of the character RAM are initialized to the first word and first line, respectively.
- The Progressive scan Control command is initialized to "Normal TV mode" (VC bit, HC bit = 0, 0).
- Test mode is released.

The time required for POWER ON RESET can be obtained from the following expression:

$$t = t_{PCLL} + \text{Video RAM Reset time} \\ = 10 (\mu\text{s}) + 12/f_{OSC} (\text{MHz}) \times 288$$

- Video RAM related parameters are also initialized. For details, see the paragraph "Video RAM All Reset Command" below.

Video RAM All Reset Command



When this command is executed, Display OFF, Locsc Oscillation ON, and Video RAM Write mode are automatically set and these settings remain unchanged until execution of other commands even after the Video RAM All Reset command.

The commands to be set by the Video RAM All Reset command are as follows:

- All the character data of the video RAM are Reseted to "EFH" (namely, they become display OFF data).
- The line and column address values of the video RAM are set to "0".
- The character color and blinking control specifications are set to "Black" and "OFF" respectively.
- The character size specification is set to "1 H" (normal size) with respect to all lines.
- The smooth function specification is set to "OFF" with respect to all lines.
- The mask pulse data of all lines are reset, inhibiting any mask pulse from being output.

With respect to the character RAM, the data stored and the line address and word address values will remain unchanged.

OSCILLATION CONTROL

With this IC, oscillation ON/OFF control can be effected with the Display Control command and thus power can be saved by stopping oscillation while characters are not being displayed on the screen. Even if oscillation is stopped by the oscillation OFF function, characters may or may not be output. So, be sure to use this function in conjunction with the Display OFF function.

Neither the video RAM nor the character RAM can be rewritten with oscillation being stopped.

Note: When display is ON, the oscillation synchronizes $\overline{H_{sync}}$, so the oscillation is stopping at the low level term of $\overline{H_{sync}}$.
When display is OFF, the oscillation keeps on irrespective of $\overline{H_{sync}}$.

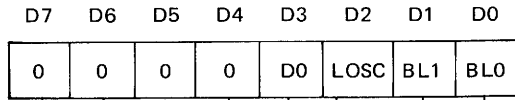
CHARACTER BLINKING

With this IC, blinking can be effected for each character by executing the Display Control command.

The character to blink must be specified with the Display Character, Blinking, and Character Data Control commands.

The blinking ON/OFF ratio (the ratio of the blink ON time to the blink OFF time) is 1 : 1 and the blinking frequency is selectable from among about 2 Hz, about 1 Hz, and about 0.5 Hz.

Display Control Command



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 Display control instruction part

Blinking control bits		
BL1	BLO	Function
0	0	Blinking OFF
0	1	Blinking frequency: about 2 Hz Blinking ratio: 1 : 1
1	0	Blinking frequency: about 1 Hz Blinking ratio: 1 : 1
1	1	Blinking frequency: about 0.5 Hz Blinking ratio: 1 : 1

Oscillation control bit	
LOSC	Function
0	Oscillation OFF
1	Oscillation ON

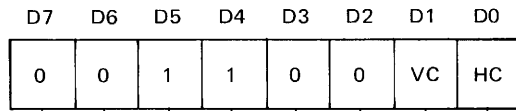
Display ON/OFF control bit	
D0	Function
0	Display OFF
1	Display ON

Note: The Display ON/OFF function is activated in synchronization with the Low-to-High transition of the $\overline{H_{sync}}$ signal.

PROGRESSIVE SCAN CONTROL

Progressive scan can be specified independently in the vertical and horizontal directions. By combining the Progressive scan Control command with oscillation frequency f_{OSC} , character design may be changed. μPD6453 builds in 1/2 cycle dividers. So it is possible to indicate the same size characters on normal and progressive scan TV screen in according to switching by command.

Progressive scan Control Command



Progressive scan control instruction part

Progressive scan control bits		
VC	HC	Function
0	0	Normal TV mode
0	1	Selectable Normal TV mode
1	1	Dedicated/Selectable Progressive TV mode
1	1	Progressive TV mode

Conceptual Diagram of Character Design (TV mode/ f_{osc} / Command)

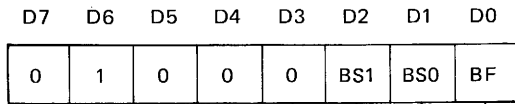
VC	HC	Normal TV mode $f_{osc} = f_x$	DS/Normal selectable TV mode	
			Double-speed TV mode $f_{osc} = 2 f_x$	Normal TV mode $f_{osc} = 2 f_x$
0	0			
0	1			
1	0			
1	1			

- When using this IC in Normal TV mode only, use $f_{osc} = f_x$ with (VC, HC = 0, 0).
 - When using this IC in Progressive scan TV mode only, use $f_{osc} = 2 f_x$ with (VC, HC = 1, 0).
 - When using this IC in Normal TV and Progressive scan TV modes selectively for EDTV system, use
 - $f_{osc} = 2 f_x$ with (VC, HC = 0, 1) in Normal TV mode
 - $f_{osc} = 2 f_x$ with (VC, HC = 0, 1) in Progressive scan mode
- f_x : oscillation frequency for normal scan TV.
 $2f_x$: oscillation frequency for progressive scan TV.

BACKGROUND SPECIFICATION

The type of background (no background, Square background, or solid background) and the background fringing ON/OFF function can be specified for each screen with the Background Control command. Background fringing is carried out irrespective of the character size and is effective only for one dot which is the minimum size.

Background Control Command



Background control instruction part

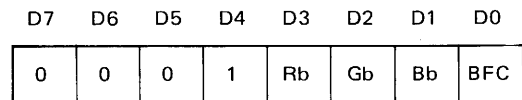
Fringing control bit	
BF	FUNCTION
0	Fringing OFF
1	Fringing ON

Background select bits		
BS1	BS0	Background format
0	0	No background
0	1	Video-reversed background
1	0	Do not use this combination
1	1	Solid background

BACKGROUND COLOR SPECIFICATION

The background color (black, blue, green, cyan, red, magenta, yellow, or white) can be specified for each character and the background fringe color (black or white) can be specified for each screen. Both colors can be set at the same time by using the Background Color Control command.

Background Color Control Command



Background color control instruction part

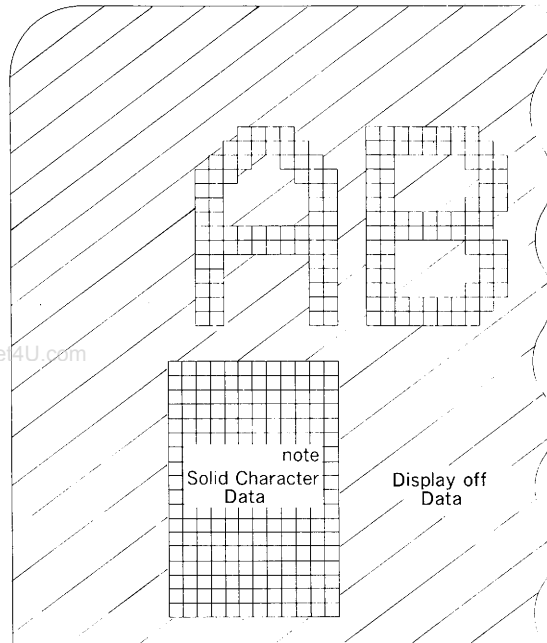
Fringe color control bit	
BFC	Fringe color
0	Black
1	White

Background color control bits			
Rb	Gb	Bb	Background color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Note: The background color and background fringe color specifications are valid only when "Solid background" or "Square background" and "Fringe ON" have been specified with the Background Control command.

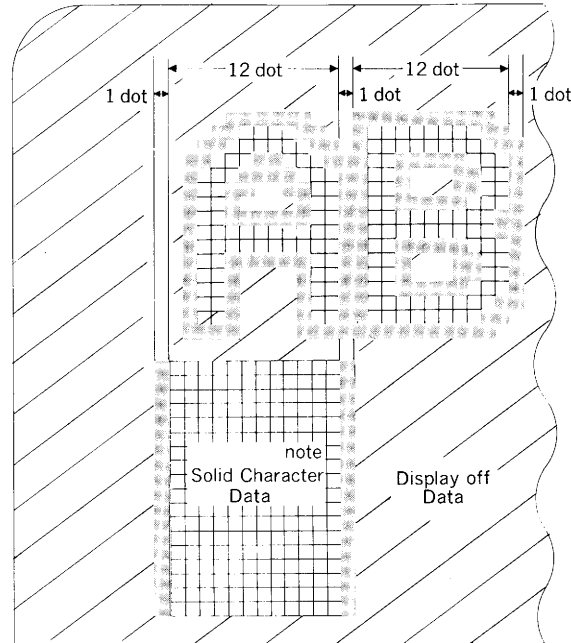
Display format in Each Background Mode

No background



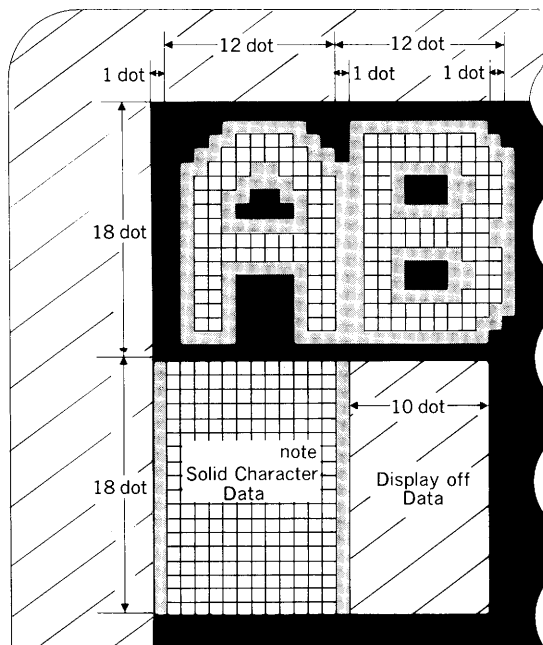
- Character color
- Picture

Fringe



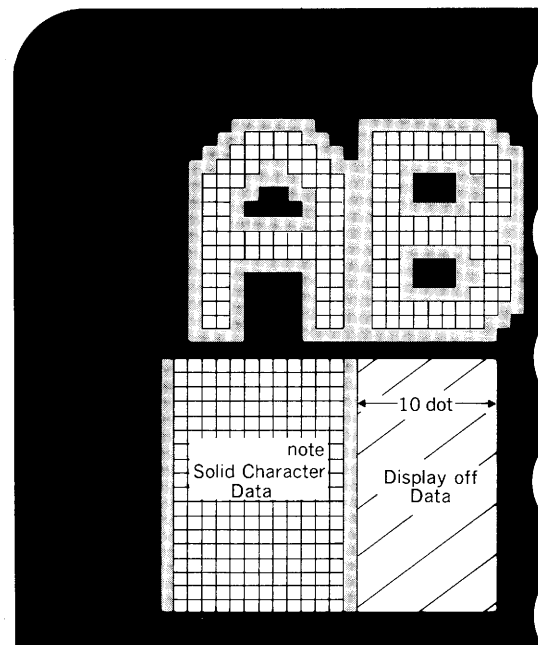
- Character color
- Fringe
- Picture

Square background + Fringe



- Character color
- Fringe
- Background color
- Picture

Solid background + Fringe



- Character color
- Fringe
- Background color
- Picture

Note: The solid character data means the data of character code 1 F_H (Standard type of NEC).
It is possible to establish the background and the fringe at the same time.

1. No background

Only characters are displayed.

2. Fringe

Characters with black fringe are displayed. Black fringe of a character which is used the edge of dot-matrix (right and left) is displayed in neighbor character area for 1 dot.

The fringe is the dot of the smallest character size and irrespective of character size.

3. Square background

The black square background is displayed in character display area.

In this case, the background is displayed in outside of character display area (right and left) for 1 dot.

In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

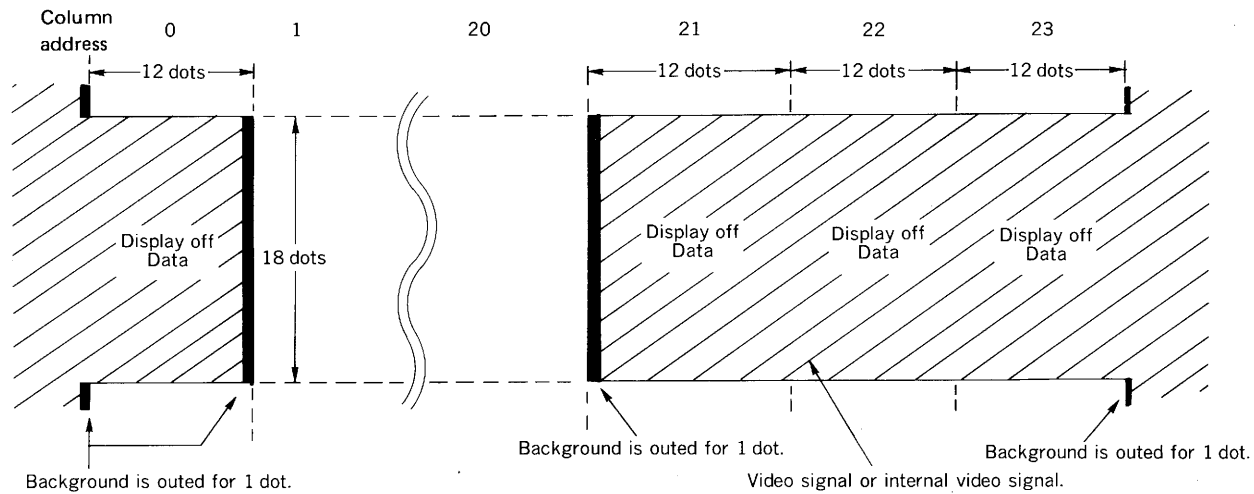
4. Solid background

The black solid background is displayed in the all area of screen.

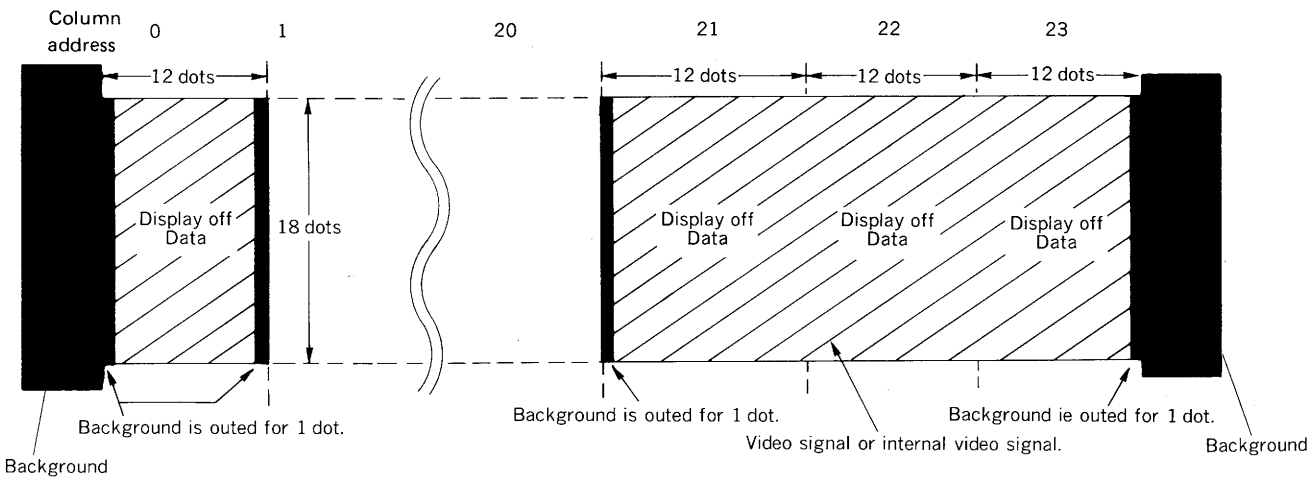
In case of using "Display OFF data", the background is displayed in the inside edge of "Display OFF data" for 1 dot.

In case of using "Display OFF data".

○ **Square background**



○ **Solid background**



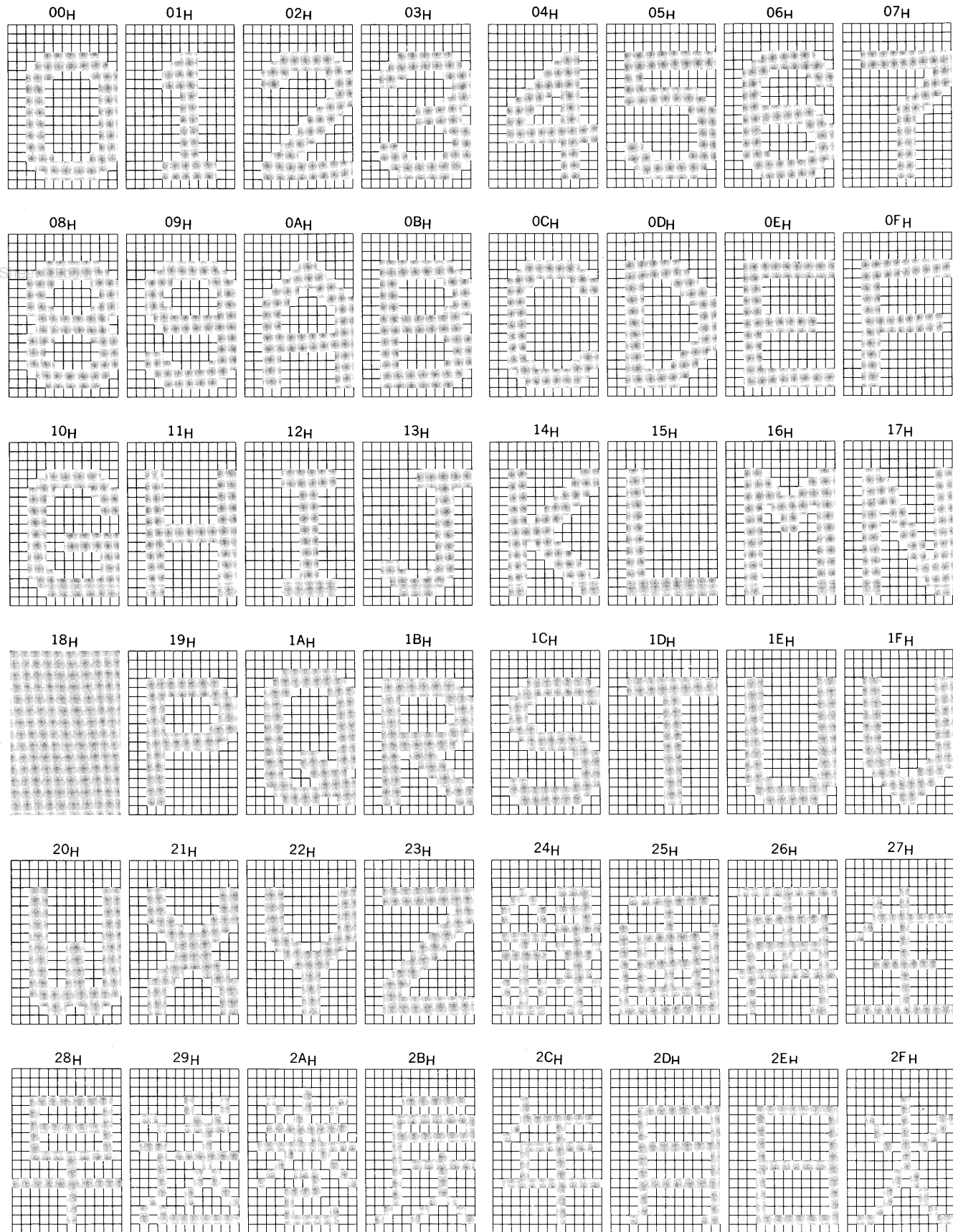
Note: The "1 dot" is the dot of the smallest character size and irrespective of character size.

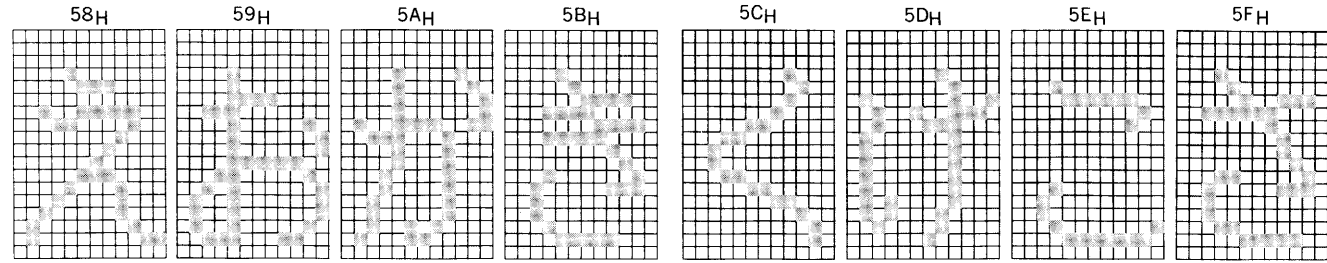
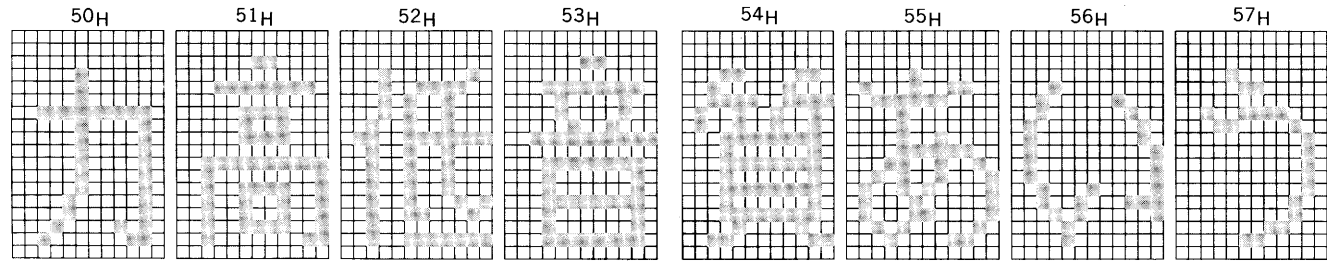
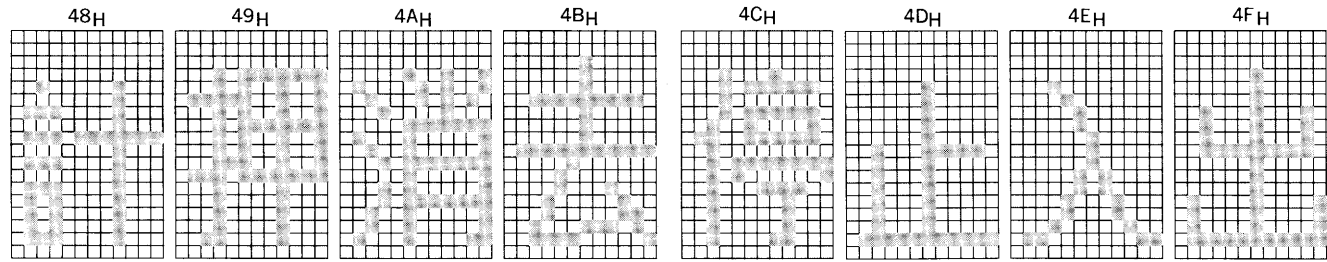
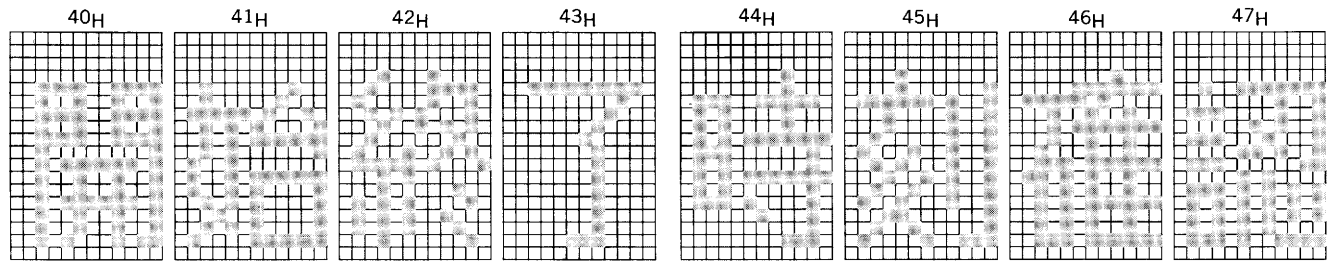
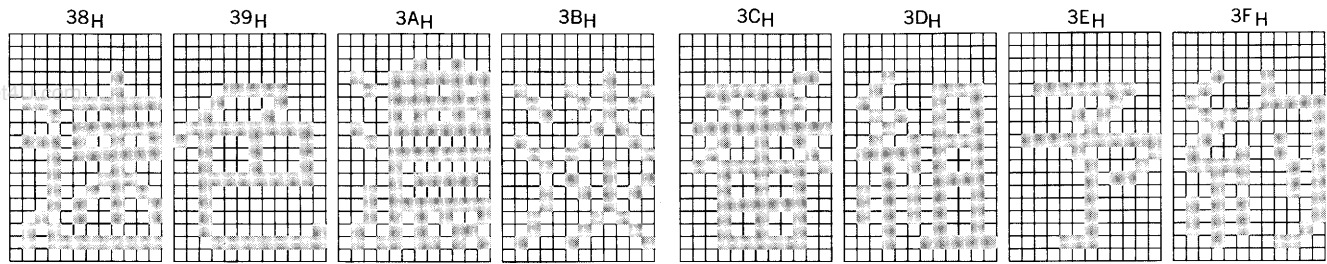
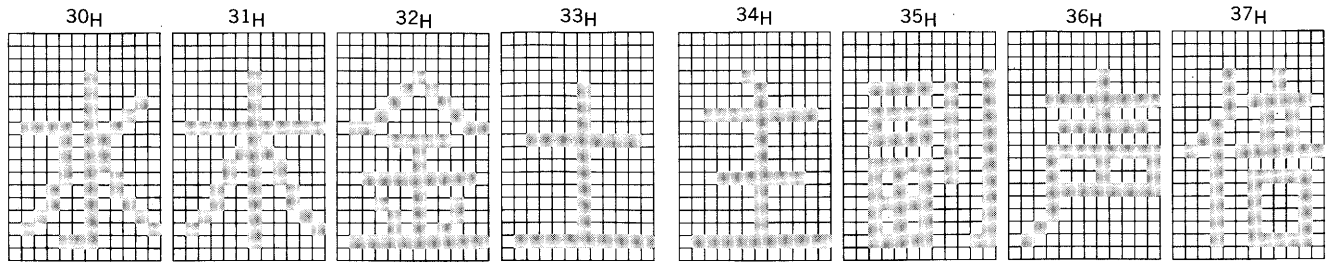
μ PD6453CY-001/ μ PD6453GT-101 Character Pattern

As shown in the following, μ PD6453CY-001/ μ PD6453GT-101 enables display of 240 character generator ROM patterns and 16 patterns to be set in the character generator RAM by the CRAM write data command. The 240 character generator ROM patterns can be changed by the mask code option. However, character code "EFH" is fixed to the display OFF code so that no character pattern can be input to this code.

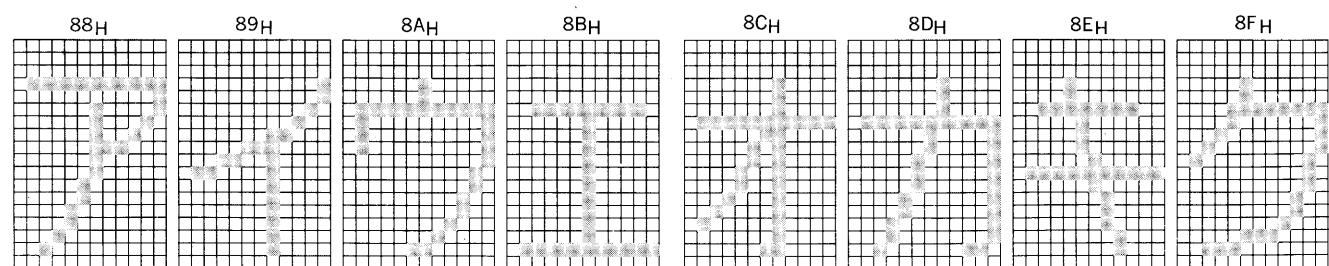
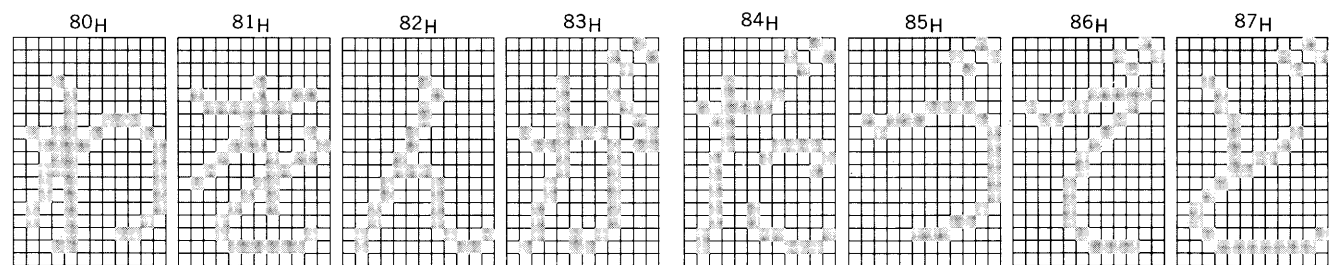
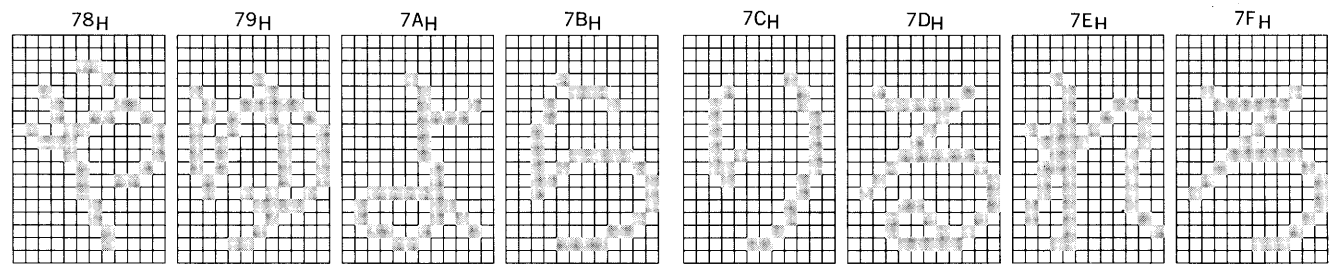
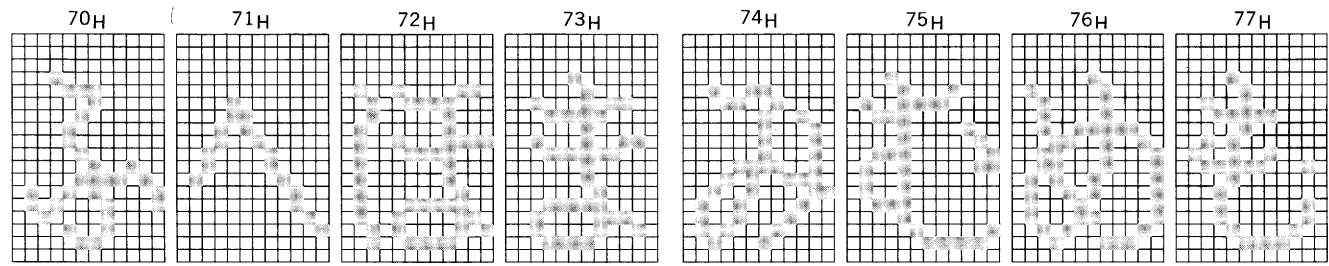
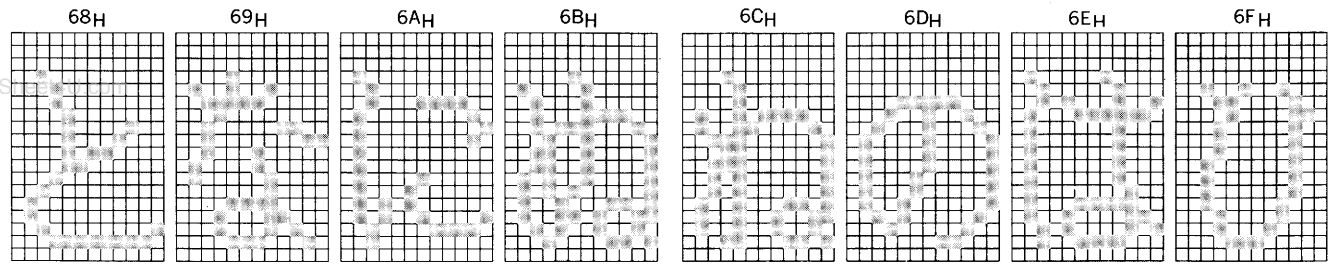
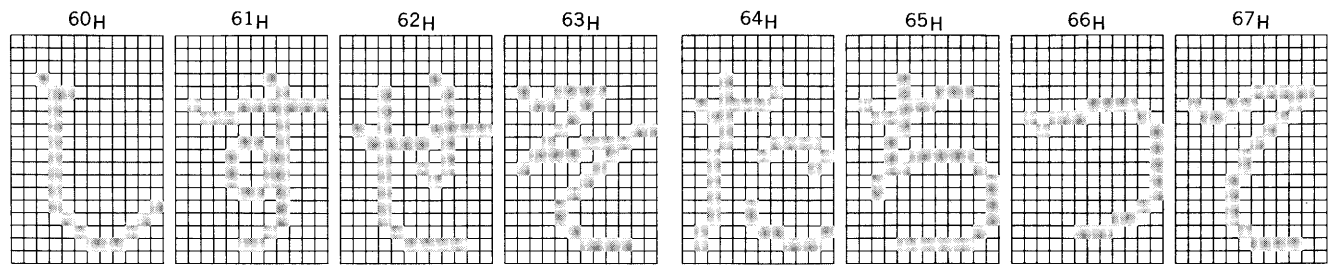
μ PD6453CY-001 and μ PD6453GT-101 have the same character patterns in the character generator ROM though their packages are different.

μPD6453CY-001, μPD6453GT-101 Character Pattern



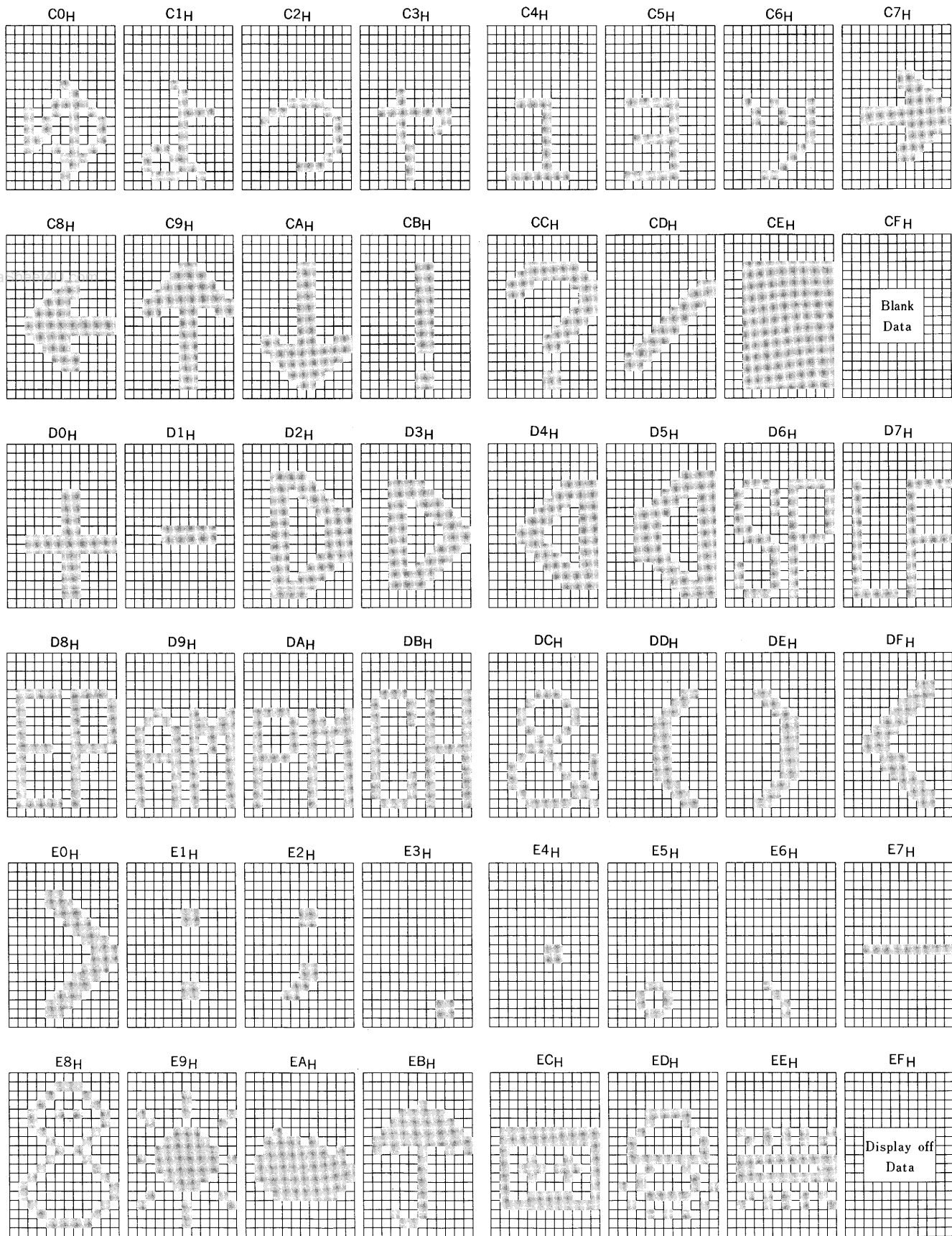


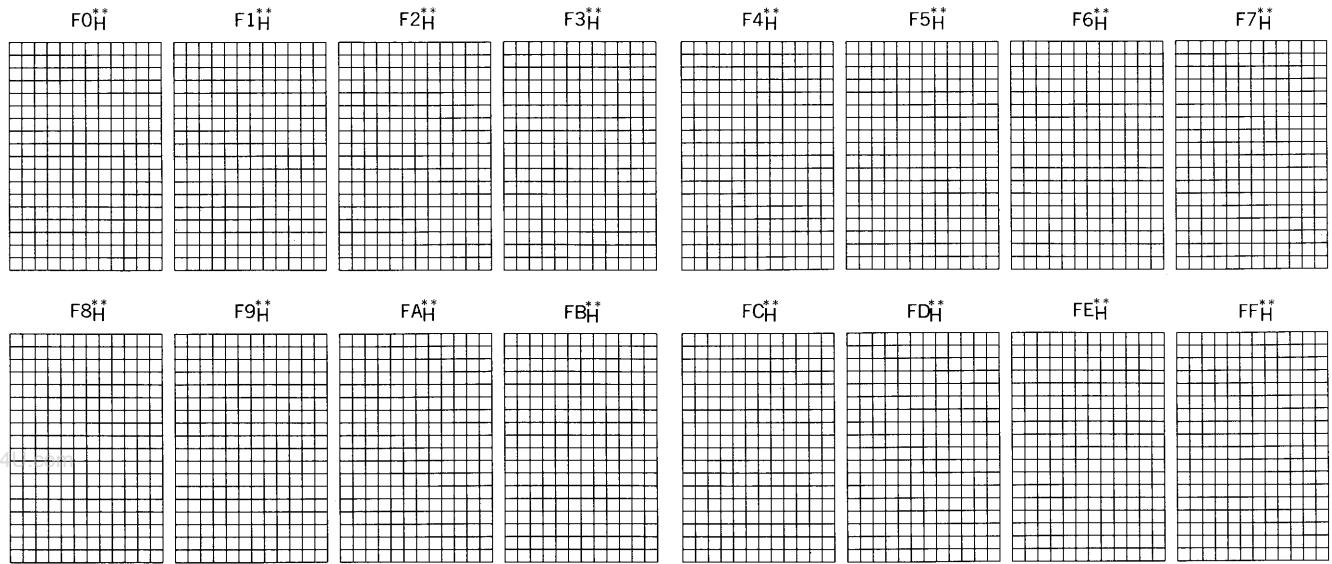
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** Character generator RAM area
(The character patterns are set in this area with the data sent from the microcomputer.)

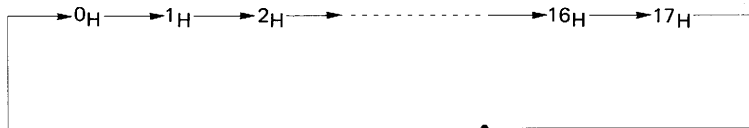
Character Display

The number of characters displayed is 12 lines x 24 columns; that is, 288 as shown below:

AC4,AC3,AC2,AC1,AC0	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011	10100	10101	10110	10111
AR3 AR2 AR1 AR0	0000																							
	0001																							
	0010																							
	0011																							
	0100																							
	0101																							
	0110																							
	0111																							
	1000																							
	1001																							
	1010																							
	1011																							

The write address is incremented automatically after the display character data is input.

Column address counter AC₄, AC₃, AC₂, AC₁, AC₀



Line address counters AR₃, AR₂, AR₁, AR₀



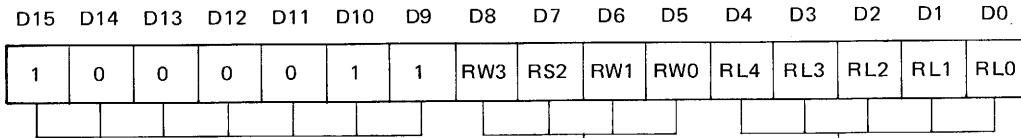
CHARACTER RAM WRITE ADDRESS CONTROL

The write word address and write line address of the character RAM can be specified with the Character RAM Write Address Control command.

Each time data is input, both the line address and word address are automatically incremented by 1. For the method of writing data into the character RAM, see the paragraph "Character RAM Write Data Control" on the next page.

Character RAM Write Address Control Command

(Because this command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)



Character RAM Write Address Control instruction part

Line address specification bits					
RL4	RL3	RL2	RL1	RL0	Function
0	0	0	0	0	Set 1st line.
0	0	0	0	1	Set 2nd line.
1	0	0	0	1	Set 18th line.
Do not use combinations other than above, or the device may malfunction.					

Word address specification bits				
RW3	RW2	RW1	RW0	Function
0	0	0	0	Set 1st word.
0	0	0	1	Set 2nd word.
1	1	1	1	Set 16th word.

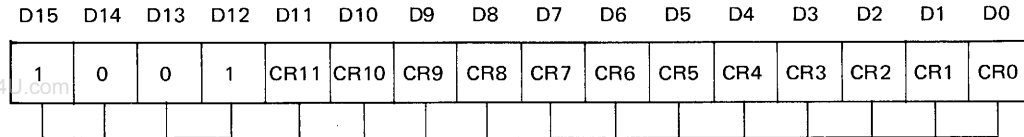
CHARACTER RAM WRITE DATA CONTROL

Input data for writing into the character RAM can be specified with the Character RAM Write Data Control command. This command is valid only when the word address and line address of the character RAM have been specified with the Character RAM Write Address Control command. This command must be input with the Losc being set in the Oscillation ON state.

As long as the CS signal remains Low (active), both the line address and word address of the character RAM are automatically incremented by 1 each time the data for one command is input.

Character RAM Write Data Control Command

(Because this command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)



Character RAM Write Data Control instruction part

Character RAM write data control bits	
CRXX	Function
0	Without dots <input type="checkbox"/>
1	With dots <input checked="" type="checkbox"/>

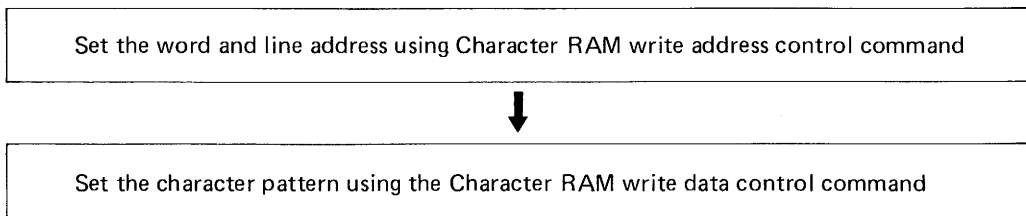
Correspondence of Character RAM Data with Character Pattern

	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
(RL4. 3.2.1.0)	0	0000										
	0	0001										
	0	0010										
	0	0011										
	0	0100										
	0	0101										
	0	0110										
	0	0111										
	0	1000										
	0	1001										
	0	1010										
	0	1011										
	0	1100										
	0	1101										
	0	1110										
	0	1111										
	1	0000										
	1	0001										

Writing of Character Generator RAM Data

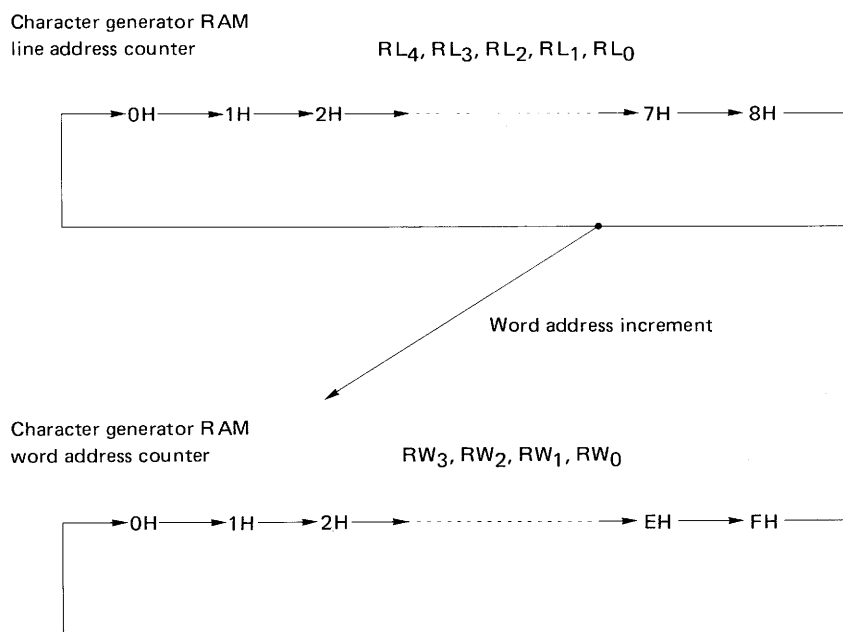
As shown in the section for the character patterns, any character patterns can be set in 16 character codes E0_H through EF_H. The character patterns for character generator RAM are set as shown below:

Character Generator RAM Data Setting Method

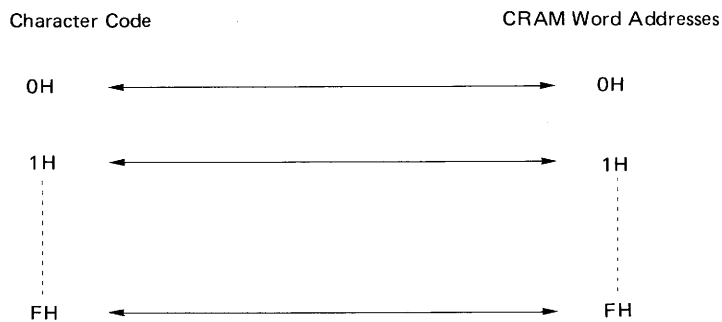


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Both the CRAM word address and line address are incremented by the STB signal as shown below. Therefore, this address may be set only once to write 16 characters continuously.



Correspondence between Character Codes and CRAM Word Addresses



CHARACTER SIZE, SMOOTH, & MASK PULSE CONTROL

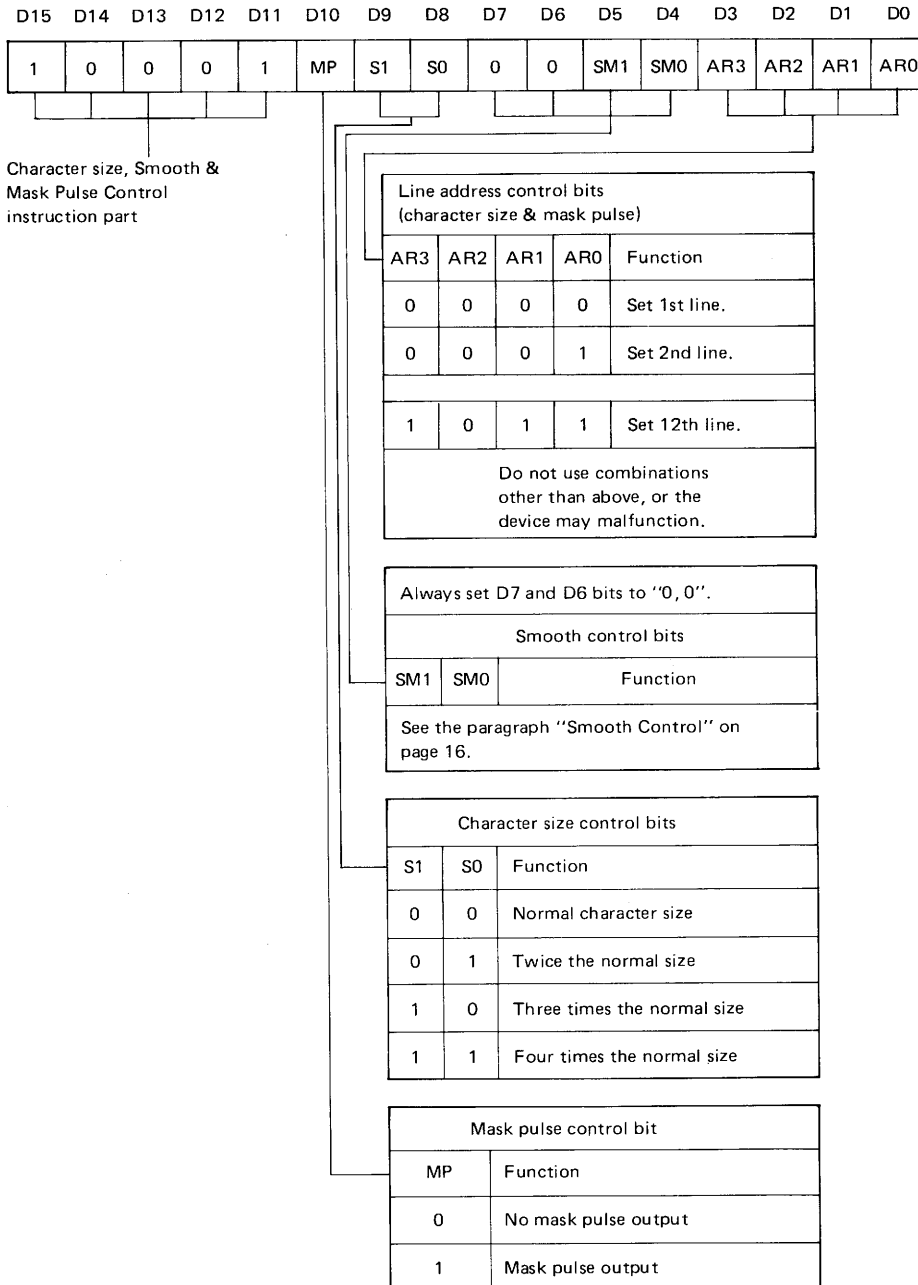
Character size, smooth function (in Character Enlarged mode), and mask pulse (Mask code option) can be specified with the Character Size, Smooth, and Mask Pulse Control command.

A character size common to both the vertical and horizontal directions is selectable in units of lines from among 1H (normal size) to 4H (four times the normal size).

For the method of writing character data, see the paragraph "Display Character Control" on page 33.

Character Size, Smooth, & Mask Pulse Control Command

(Because this command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)



Note: The MP (mask pulse) control bit is valid only when the mask pulse function has been selected with the Mask code option. If this function has not been selected, set the MP bit to "0".

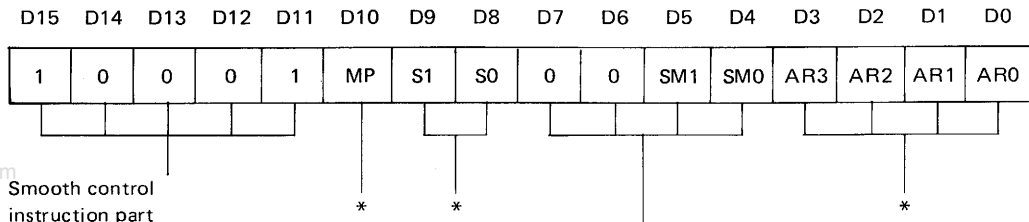
The horizontal size of one character depends on the oscillation frequency (f_{OSC}), and the vertical size of one character depends on the number of scanning lines. In case of the smallest character size, one horizontal dot size is $1/f_{OSC}$, and one vertical dot size is two scanning lines (in the frame).

SMOOTH (INTERPOLATION) CONTROL

In the Character Enlarged mode (two to four times the normal size), the smooth function can be set in units of lines to smooth each displayed character.

Smooth Control Command

(Because this command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)



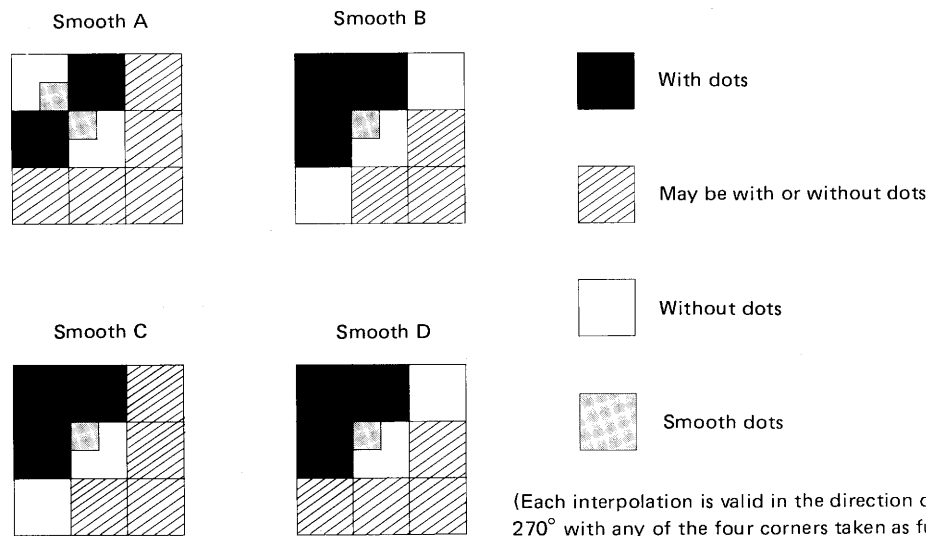
Smooth control instruction part

* See page 12 for explanation of these bits.

Always set D7 and D6 bits to "0, 0".		
Smooth control bits		
SM1	SM0	Function
0	X	No smooth function
1	0	Class 1 smooth
1	1	Class 2 smooth

X: Don't care.

Description of each smooth type



(Each interpolation is valid in the direction of 90°, 180°, or 270° with any of the four corners taken as fulcrum.)

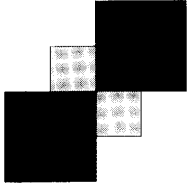
Class I smooth = Smooth A + Smooth B
 Class II smooth = Smooth A + Smooth B + Smooth C + Smooth D

An Example of Smooth

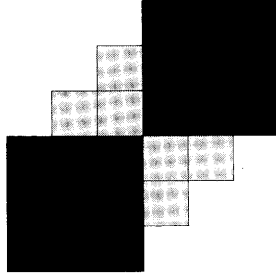
1H/dot



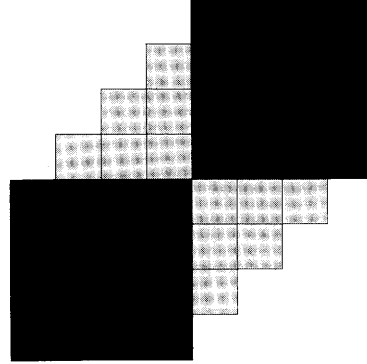
2H/dot



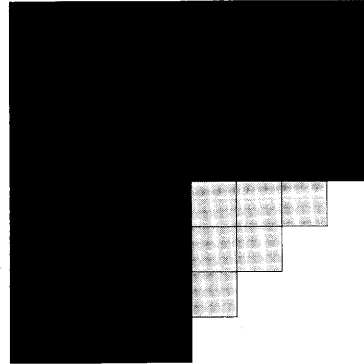
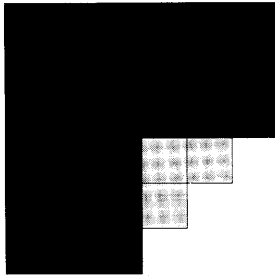
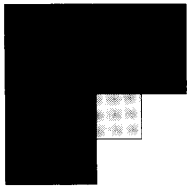
3H/dot



4H/dot



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With dots



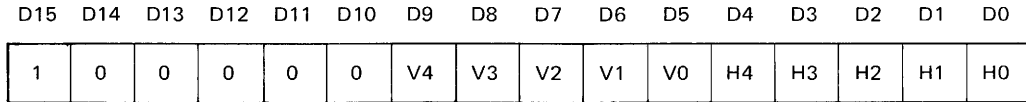
Smooth dots

DISPLAY POSITION CONTROL

It is possible to set 32 steps for vertical and horizontal direction.

Display Position Control Command

(Because the command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)

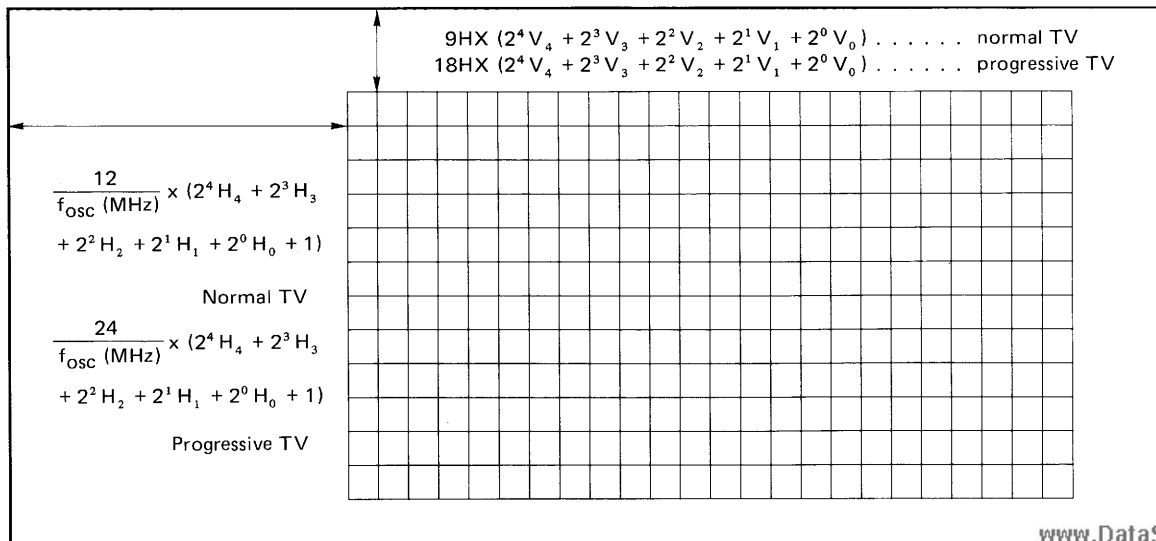


Display position control instruction part

Horizontal address specification bits					
H4	H3	H2	H1	H0	Start address
0	0	0	0	0	From the trailing edge of the horizontal synchronizing pulse Note: 12 (24)/f _{osc} (MHz) × 1 [μs]
0	0	0	0	1	From the trailing edge of the horizontal synchronizing pulse Note: 12 (24)/f _{osc} (MHz) × 2 [μs]
}					
1	1	1	1	1	From the trailing edge of the horizontal synchronizing pulse Note: 12 (24)/f _{osc} (MHz) × 32 [μs]

Vertical address specification bits					
V4	V3	V2	V1	V0	Start address
0	0	0	0	0	From the trailing edge of the vertical synchronizing pulse Note: 9 (18) × 0H
0	0	0	0	1	From the trailing edge of the vertical synchronizing pulse Note: 9 (18) × 1H
}					
1	1	1	1	1	From the trailing edge of the vertical synchronizing pulse Note: 9 (18) × 31H

(): Progressive TV



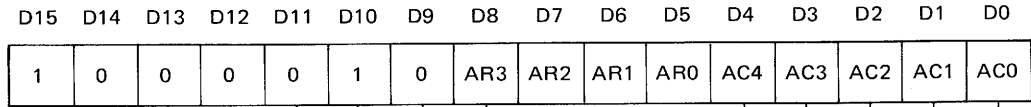
Character Write Address Control

Line and column address of VRAM which is written the character data can be specified with the character write address control command.

Please refer to the section of Display Character Control command about writing the character data.

Character Write Address Control Command

(Because this command is a 2-byte command, 16 bits must be fully input for this command at the time of continuous command input.)



Character write address control instruction part

Column addressing bits					Function
AC4	AC3	AC2	AC1	AC0	
0	0	0	0	0	Set the 1st line.
0	0	0	0	1	Set the 2nd line.
}					
1	0	1	1	1	Set the 24th line.
}					Do not set an address other than the addresses 0H through 17H.

Line addressing bits				Function
AR3	AR2	AR1	AR0	
0	0	0	0	Set the 1st line.
0	0	0	1	Set the 2nd line.
}				
1	0	1	1	Set the 12th line.
}				Do not set an address other than addresses 0H through BH.

WRITING DISPLAY CHARACTER DATA, CHARACTER COLOR, AND BLINKING DATA

The write address of data can be set directly in the address counter by using the Character Write Address Control command.

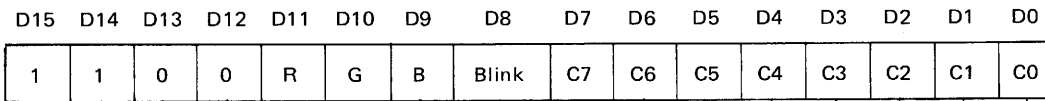
After the write address has been set, the display character data must be entered. The character color and blinking data are written into the video RAM and at the same time retained in the internal registers. The display character data is written into the video RAM and the write address is automatically incremented by 1.

When character data is to be input without changing the character color and blinking data, the Display Character Control command can be input in an abbreviated format by entering only its low-order 8 bits (character address) while the CS signal is being held in the Low state. After the command input, the write address is automatically incremented by 1.

The character data, character color, and blinking data can be set with the Display Character Control command.

Display Character Control Command

As mentioned above, the character data, character color, and blinking data to be written into the video RAM can be specified with the Display Character Control command. This command must be input with the Losc being set in the Oscillation ON state. When characters are to be input successively without changing the character color and blinking data, only the low-order 8 bits of this command need to be input for the second and subsequent characters, because this command is a 2nd byte continuous command.



Display Character Control instruction part

Character specification bits								Function
C7	C6	C5	C4	C3	C2	C1	C0	
0	0	0	0	0	0	0	0	Outputs the data for character code 00H.
0	0	0	0	0	0	0	1	Outputs the data for character code 01H.
⋮								
1	1	1	1	1	1	1	1	Outputs the data for character code 6EH.

00H to EEH; CROM, F0H to FFH; CRAM, EFH; Display off data

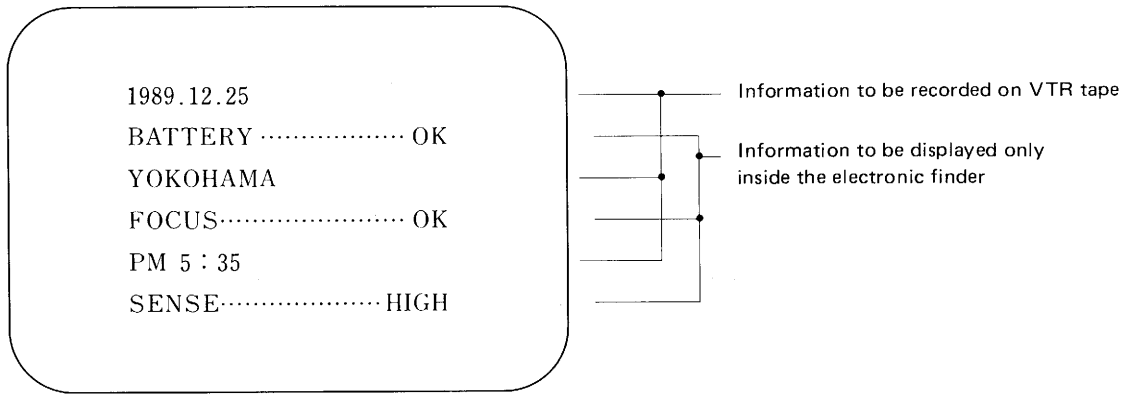
Blink selecting bits	
Blink	Function
0	No blinking
1	Blinking

Character color selecting bits			
R	G	B	Character color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

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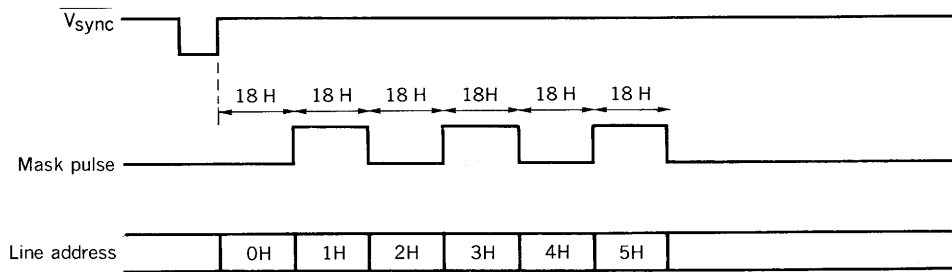
Mask Pulse Function (Mask Code Option)

When used in a VCR camera, the on-screen ICs provide two types of information; information to be recorded on VCR tape, such as the date and title, and information to be displayed only inside the electronic view finder, such as the battery, focus, sensitivity, and mode. For proper use of these two types of information, the mask option allows the V_{MON} terminal to be used as the character-by-character signal output terminal.

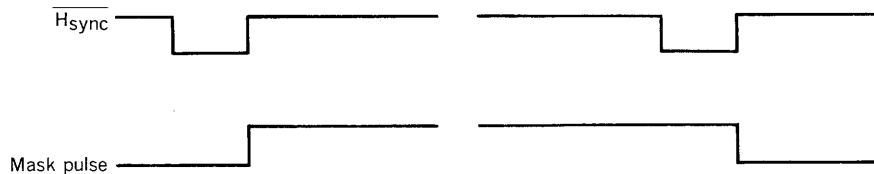


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Example: The mask pulse is to be output to line addresses 1 H, 3 H, and 5 H with vertical address 0 H and a character size of 1 H/dot.



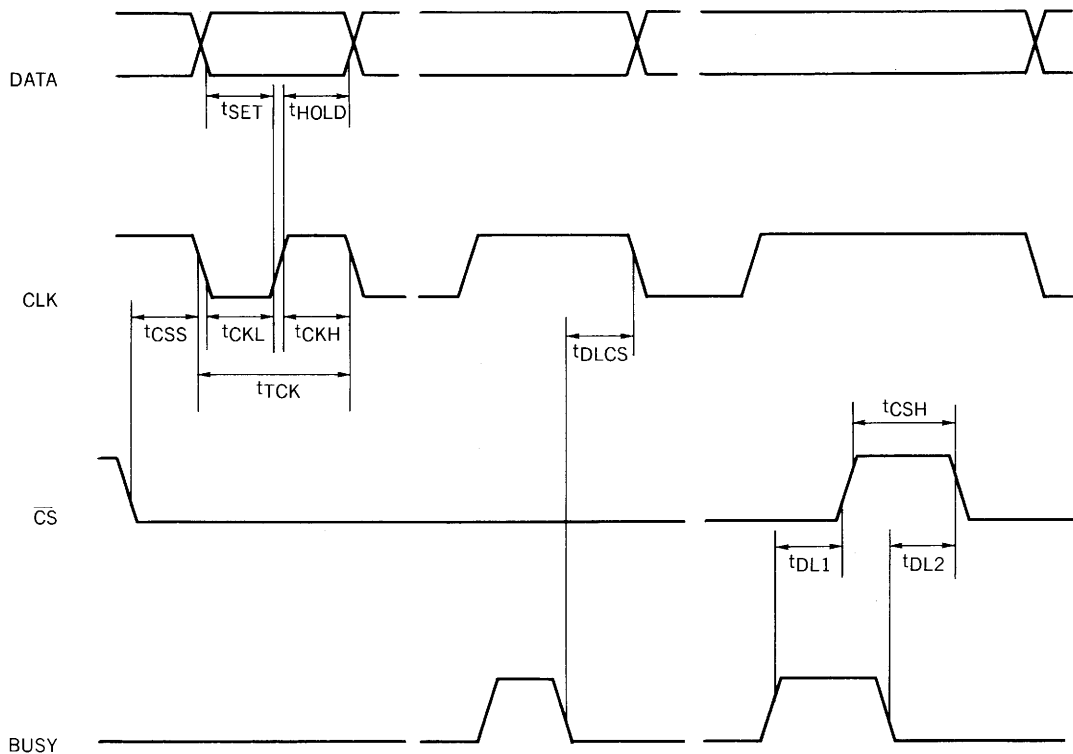
The leading and trailing edges of the mask pulse are synchronized with the trailing edge of $\overline{H_{SYNC}}$.



RECOMMENDED CONDITIONS FOR OPERATION TIMING

($T_a = 25^\circ\text{C}$, $V_{DD} - V_{SS} = 5.0\text{ V}$)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Minimum Setup Time	t_{SET}		400			ns
Minimum Hold Time	t_{HOLD}		400			ns
Minimum Clock Width at Low Level	t_{CKL}		400			ns
Minimum Clock Width at High Level	t_{CKH}		400			ns
Clock Cycle	t_{TCK}		1.0			μs
$\overline{\text{CS}}$ Minimum Setup Time	t_{CSS}		400			ns
$\overline{\text{CS}}$ Minimum Hold Time	t_{CSH}		400			ns
Delay Time 1 (from BUSY rising)	t_{DL1}		400			ns
Delay Time 2 (from BUSY falling)	t_{DL2}		400			ns
Minimum Busy to CLK Time	t_{DLCS}		400			ns
Minimum $\overline{\text{VSYNC}}$ Width at Low Level	t_{VWL}		4			μs
Minimum $\overline{\text{HSYNC}}$ Width at High Level	t_{HWL}		4			μs

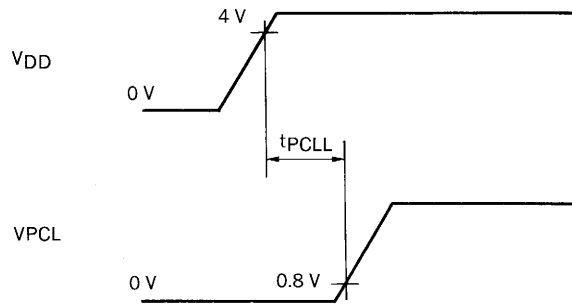


For format data, the BUSY signal goes low after the internal state is completely established. It also goes low when writing data into the VRAM is finished.

When writing data into the VRAM extends to the horizontal flyback time, the BUSY signal lasts longer than usual. (This is because oscillation is off and data cannot be written into the VRAM during the horizontal flyback time.)

Power ON Reset

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
PCL terminal Minimum Low Hold Time	tPCLL		10			μs

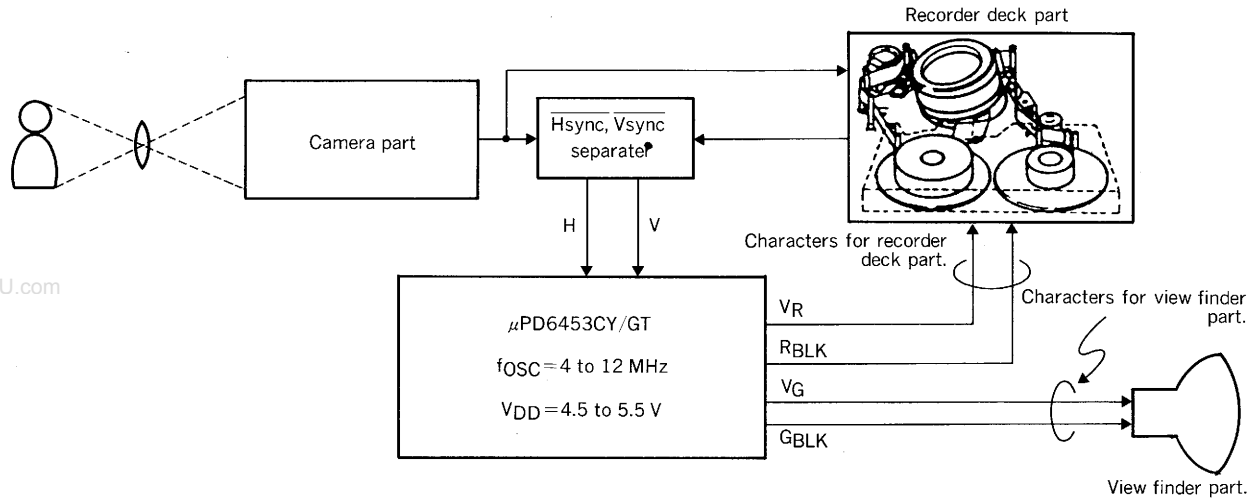


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Application of μPD6453

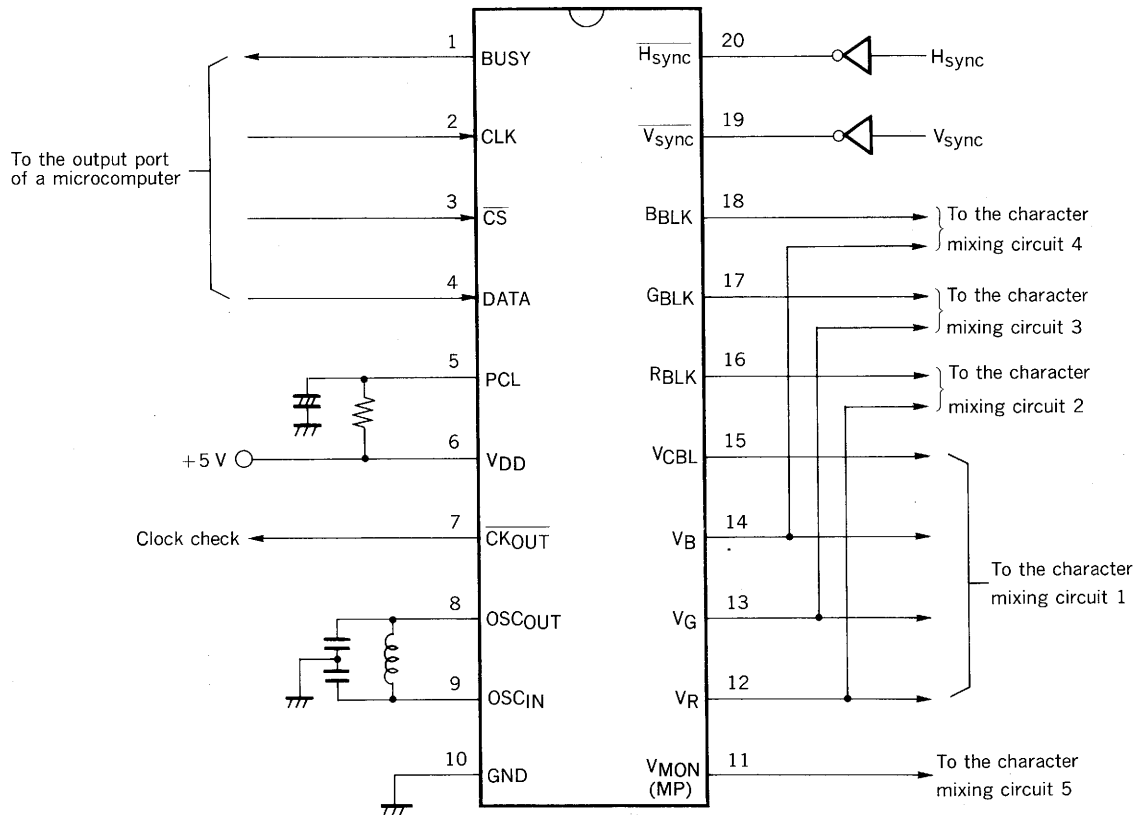
μPD6453 has 3 blanking signals output terminals. These terminals (R_{BLK} , G_{BLK} , B_{BLK}) outputs the blanking signals which correspond to all character signals output (V_R , V_G , V_B).

This diagram shows application of μPD6453 for camera recorder.



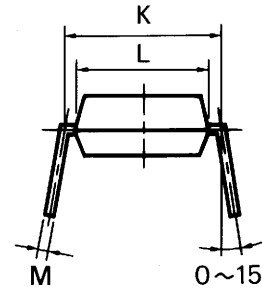
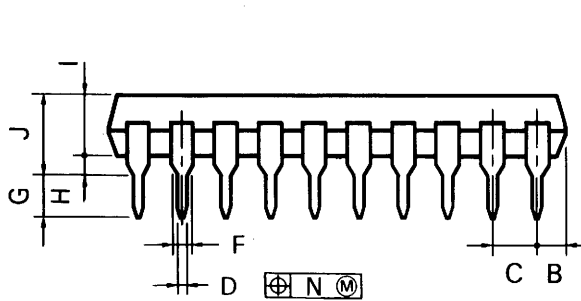
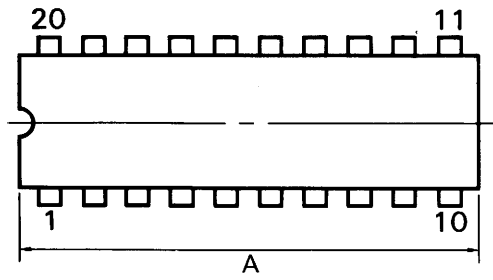
For example, V_G and G_{BLK} terminals are connected to the view finder part, V_R and R_{BLK} terminals are connected to the recorder deck part.

It is possible to indicate characters only on view finder part by specifying character color G, and it is possible to indicate characters on both parts (the view finder part and the recorder deck part) by specifying character color R + G.



μPD6453CY-001

20-pin plastic DIP (400 mil)



P20C-100-400B

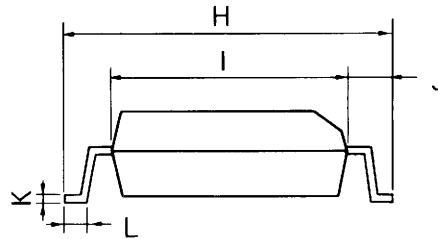
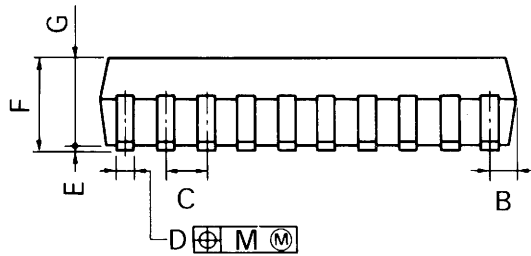
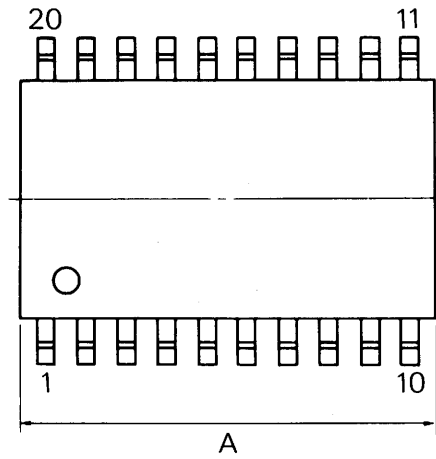
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	27.94 MAX.	1.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ^{+0.10}	0.020 ^{+0.004} _{-0.005}
F	1.2 MIN.	0.047 MIN.
G	3.5 ^{-0.3}	0.138 ^{+0.012}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	0.25 ^{-0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.25	0.01

μPD6453GT-101

20-pin plastic SOP (375 mil)



P20GM-50-375B-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} / _{-0.05}	0.016 ^{+0.004} / _{-0.003}
E	0.1 ^{±0.1}	0.004 ^{±0.004}
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ^{+0.3}	0.406 ^{+0.013} / _{-0.013}
I	7.2	0.283
J	1.6	0.063
K	0.15 ^{+0.10} / _{-0.05}	0.006 ^{+0.004} / _{-0.002}
L	0.8 ^{±0.2}	0.031 ^{+0.009} / _{-0.008}
M	0.12	0.005

[MEMO]

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