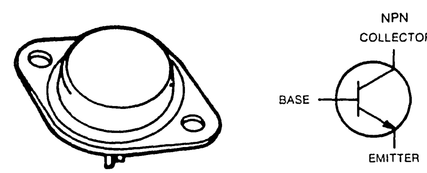
HIGH VOLTAGE/HIGH SPEED
NPN POWER TRANSISTORS
JEDEC EQUIVALENT - 2N6676, 77, 78

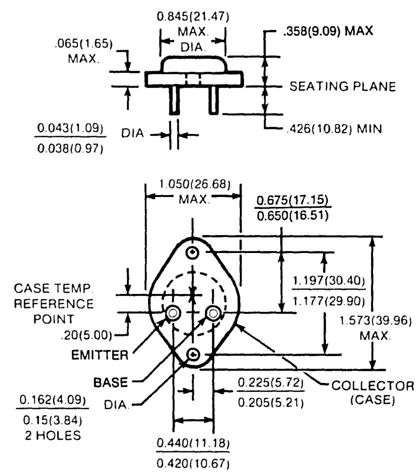
D64VS3,4,5

300-400 VOLTS
15 AMP, 195 WATTS

The D64VS series of NPN power transistors is designed for use in power switching applications requiring high-voltage capability, fast switching speeds and low-saturation voltages. These devices are optimized to provide a unique combination of ultra-low switching losses and high safe-operating area (SOA), ideally suited for off-line switching power supplies, converter circuits and pulse width modulated regulators.



CASE STYLE TO-204AA (TO-3)
DIMENSIONS ARE IN INCHES AND (MILLIMETERS)



Features:

- Performance information tailored for switching
- 100°C maximum limits specified for:
  - Switching times
  - Saturation voltages
  - Leakage currents
- RBSOA (V_{CEX} = 300 to 400V) at rated I_C continuous.
- Very fast turn-off, $t_f < 100$ nsec (typ.) @ 15A — Inductive Load

maximum ratings

RATING	SYMBOL	D64VS3	D64VS4	D64VS5	UNITS
Collector-Emitter Voltage	V_{CEO}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEX}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEV}	450	500	550	Volts
Emitter Base Voltage	V_{EBO}	7	7	7	Volts
Collector Current — Continuous Peak(1)	I_C I_{CM}	15 30	15 30	15 30	A
Base Current — Continuous Peak(1)	I_B I_{BM}	5 10	5 10	5 10	A
Emitter Current — Continuous Peak(1)	I_E I_{EM}	20 35	20 35	20 35	A
Total Power Dissipation @ Tc = 25°C @ Tc = 100°C Derate above 25°C	P_D	195 111 1.11	195 111 1.11	195 111 1.11	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-65 to +200	-65 to +200	-65 to +200	°C

thermal characteristics

Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.9	0.9	0.9	°C/W
Maximum Lead Temperature for Soldering Purpose: ⅛" from Case for 5 Seconds	T_L	235	235	235	°C

(1) Pulse condition, $t_p \leq 5$msec.

electrical characteristics ($T_C = 25°C$) (unless otherwise specified)

CHARACTERISTIC		SYMBOL	MIN	MAX	UNIT

off characteristics

Collector-Emitter Sustaining Voltage[1] (I_C = 100mA)	D64VS3 D64VS4 D64VS5	$V_{CEO(sus)}$	300 350 400	— — —	Volts
Collector-Emitter Voltage (I_C = 15A, I_{B1} = 2.5A, I_{B2} = 3.0A) ($V_{BE(OFF)}$ = -6V, L = 200 μh)	D64VS3 D64VS4 D64VS5	V_{CEX}	300 350 400	— — —	Volts
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(OFF)}$ = -1.5V) (V_{CEV} = Rated Value, $V_{BE(OFF)}$ = -1.5V, T_C = 100°C)		I_{CEV}	 — —	 0.1 1.0	mA
Emitter Cutoff Current (V_{EB} = 7V)		I_{EBO}	—	1.0	mA

second breakdown

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 13
Clamped Inductive SOA with Base Reversed Bias	RBSOA	SEE FIGURE 14

on characteristics

DC Current Gain (I_C = 10A, V_{CE} = 2V) (I_C = 15A, V_{CE} = 2V)	h_{FE}	 10 8	 — —	—
Collector-Emitter Saturation Voltage (I_C = 10A, I_B = 1.67A) (I_C = 15A, I_B = 2.5A) (I_C = 15A, I_B = 2.5A, T_C = 100°C)	$V_{CE(SAT)}$	 — — —	 0.7 1.0 1.5	Volts
Base-Emitter Saturation Voltage (I_C = 15A, I_B = 2.5A) (I_C = 15A, I_B = 2.5A, T_C = 100°C)	$V_{BE(SAT)}$	 — —	 1.5 1.5	Volts

dynamic characteristics

Current Gain — Bandwidth Product (I_C = 1.0A, V_{CE} = 10V, f_{test} = 1.0 MHz)	f_T	15	50	MHz
Output Capacitance (V_{CB} = 10V, I_E = 0, f = 0.1 MHz)	C_{OB}	150	360	pF

switching characteristics

			MAXIMUM		
Resistive Load (See Figure 17 for Test Circuit)		T_C	25°C	100°C	
Delay Time	V_{CC} = 250V, I_C = 15A	t_d	0.1	0.2	μs
Rise Time	I_{B1} = 2.5, I_{B2} = 3.0A, t_p = 50 μsec	t_r	0.5	0.7	μsec
Storage Time		t_s	2.5	3.0	μsec
Fall Time		t_f	0.4	0.7	μsec
Inductive Load, Clamped (See Figure 17 for Test Circuit)					
Storage Time	I_C = 15A, V_{CLAMP} = 250V	t_s	3.0	3.5	μs
Fall Time	I_{B1} = 2.5A, I_{B2} = 3.0A, $V_{BE(OFF)}$ = -6V L = 200 μh, t_p = 25μsec	t_f	0.3	0.6	μsec
		TYPICAL			
Storage Time		t_s	1.8	2.5	μsec
Fall Time		t_f	.085	.13	μsec

(1) Pulse Duration = 300μs, Duty Factor ≤ 2%. Do not measure on a curve tracer.

TYPICAL DC CHARACTERISTICS

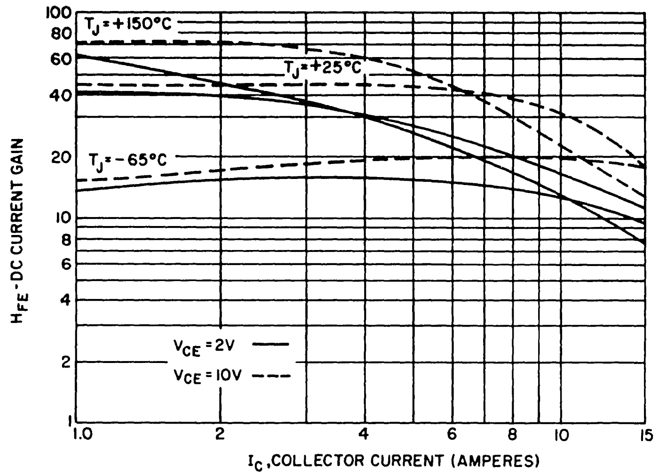


FIGURE 1. DC CURRENT GAIN

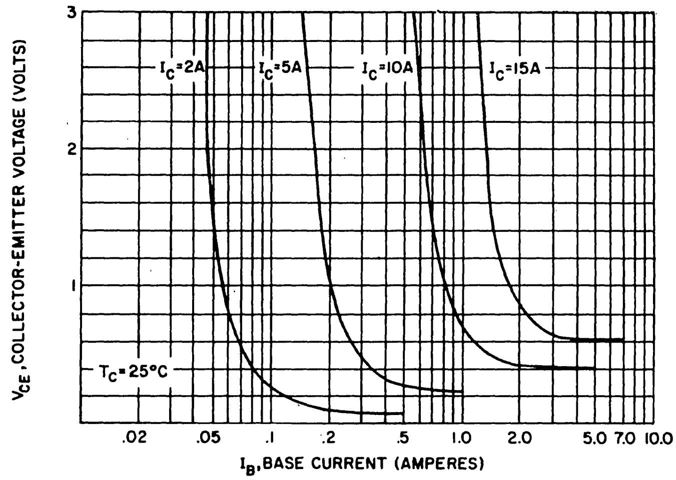


FIGURE 2. COLLECTOR SATURATION REGION

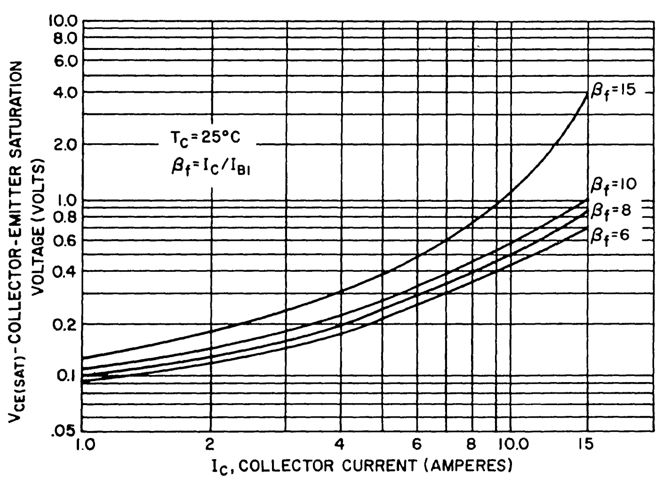


FIGURE 3. $V_{CE(sat)}$ vs I_C, T_C = 25°C

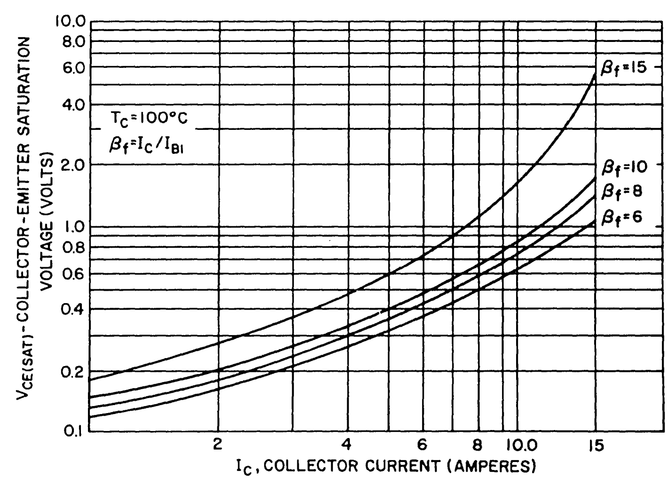


FIGURE 4. $V_{CE(sat)}$ vs I_C, T_C = 100°C

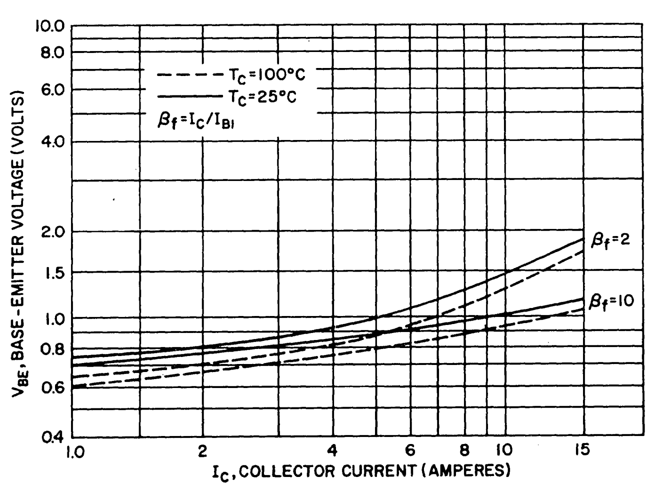


FIGURE 5. $V_{BE(sat)}$ vs I_C

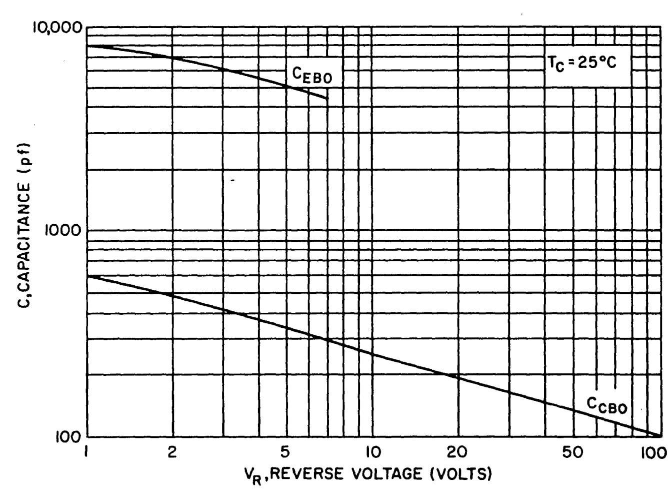


FIGURE 6. CAPACITANCE

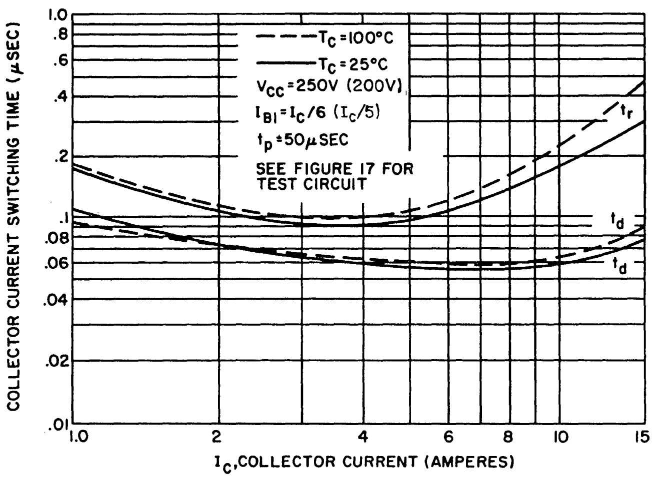


FIGURE 7. TURN-ON TIME RESISTIVE LOAD

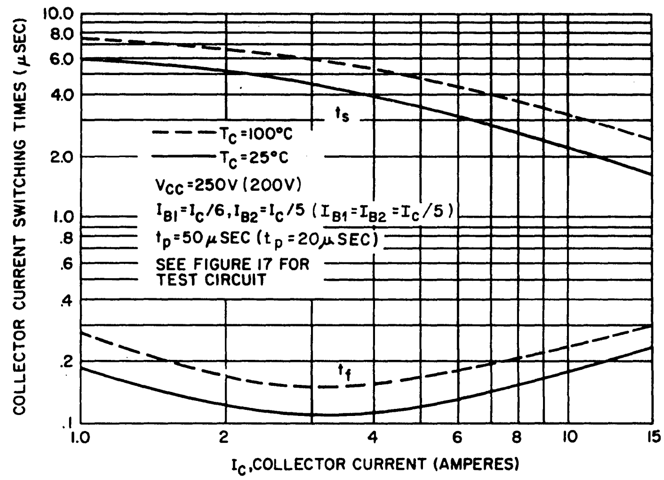


FIGURE 8. TURN-OFF TIME RESISTIVE LOAD

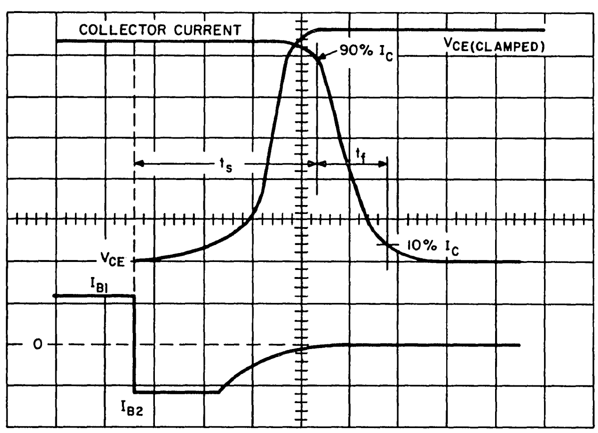


FIGURE 9. INDUCTIVE TURN-OFF WAVEFORMS

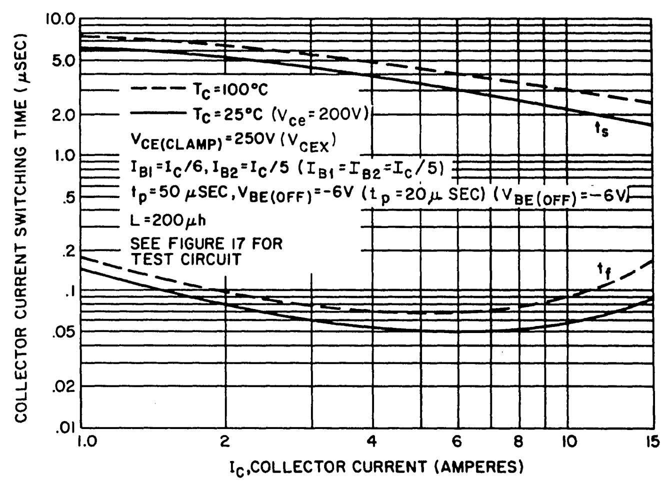


FIGURE 10. CLAMPED INDUCTIVE TURN-OFF TIME

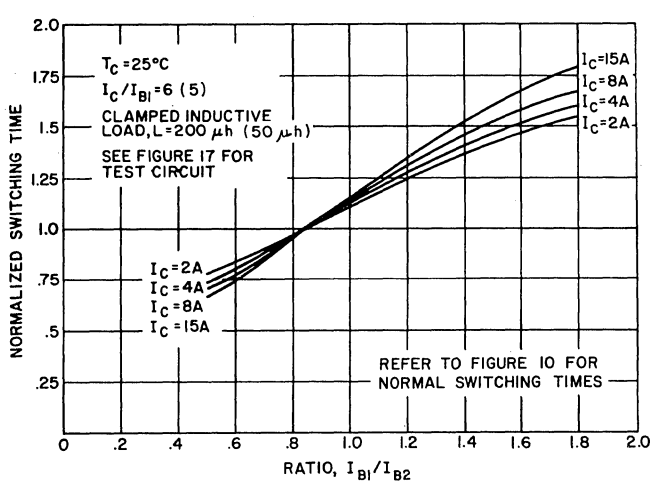


FIGURE 11. STORAGE TIME VARIATION WITH I_{B2}

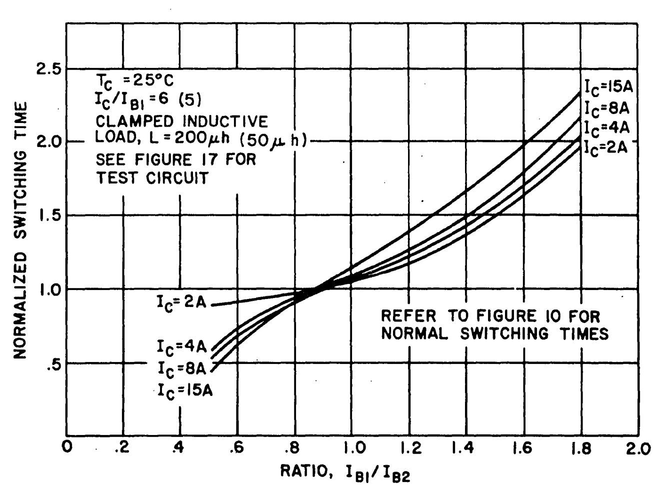


FIGURE 12. FALL TIME VARIATION WITH I_{B2}

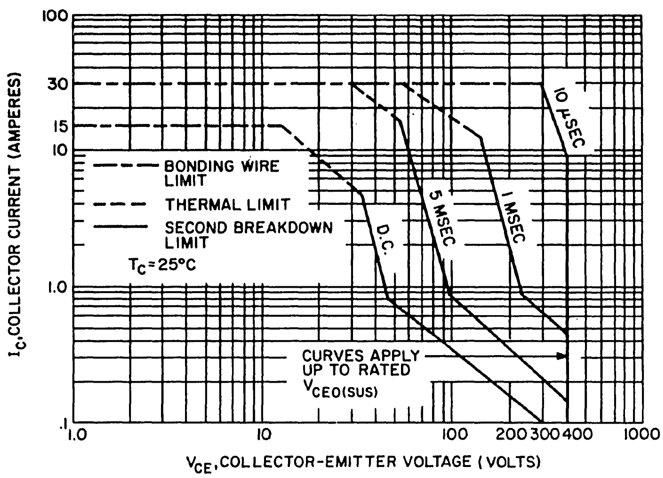


FIGURE 13. FORWARD BIAS SAFE OPERATING AREA

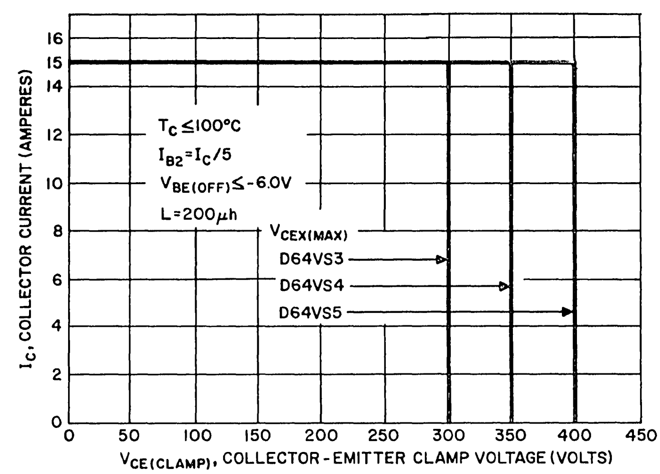


FIGURE 14. CLAMPED REVERSE BIAS SAFE OPERATING AREA

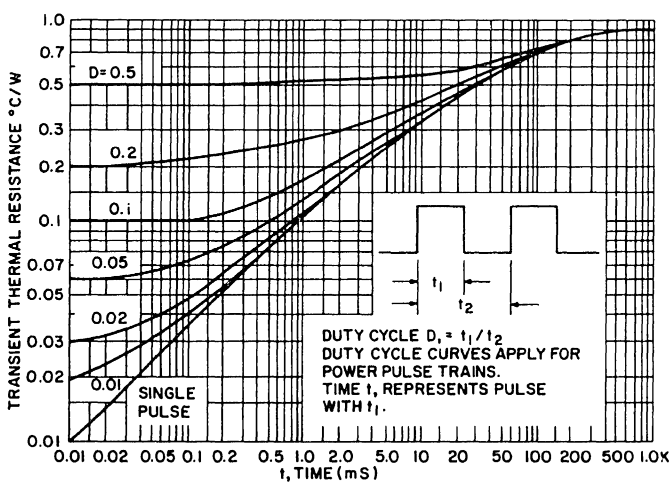


FIGURE 15. TRANSIENT THERMAL RESPONSE

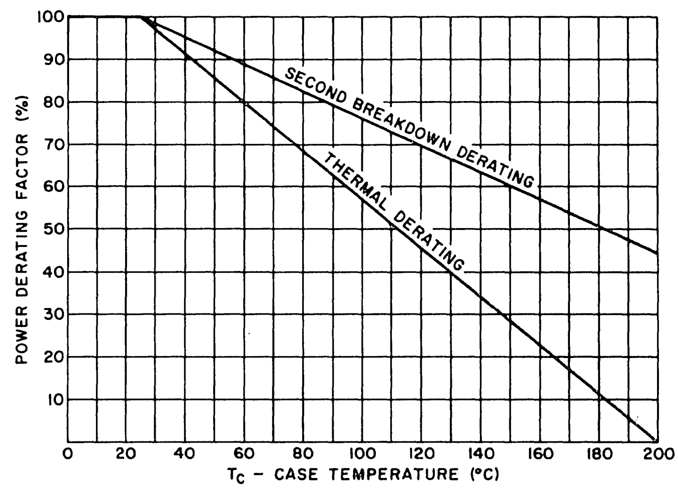


FIGURE 16. POWER DERATING

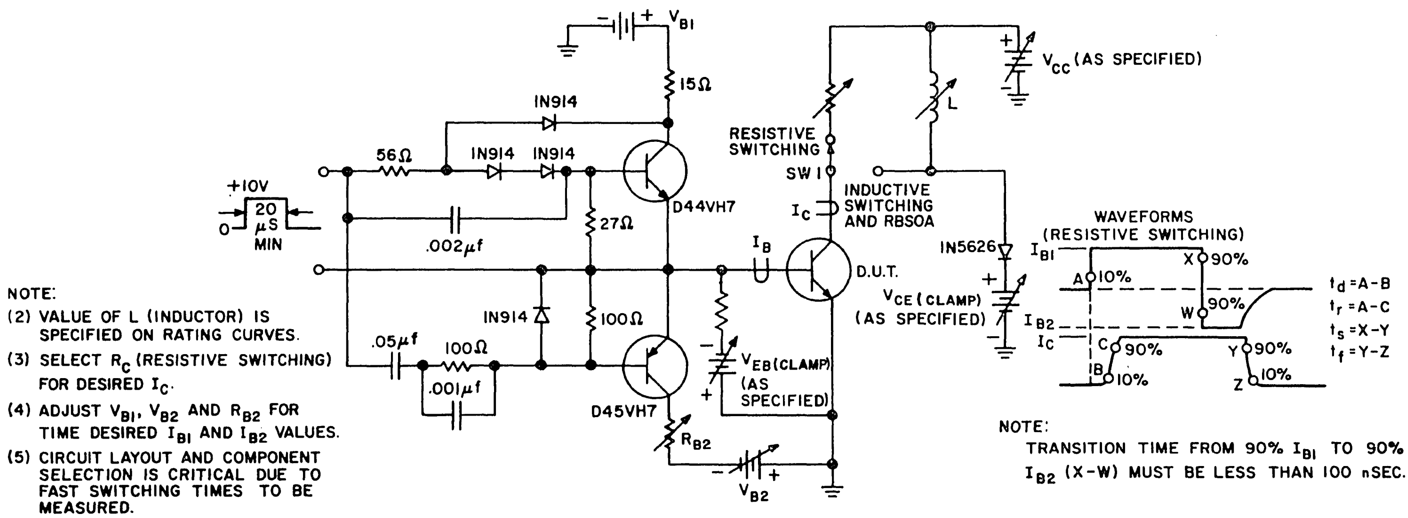


FIGURE 17. TEST CIRCUIT FOR SWITCHING TIMES AND RBSOA