

## USB 2.0 HUB CONTROLLER



The μPD720112 is a USB 2.0 hub device that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and works up to 480 Mbps. USB 2.0 compliant transceivers are integrated for upstream and all downstream ports. The μPD720112 works backward compatible either when any one of the downstream ports is connected to a USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

**μPD720112 User's Manual: S16617E**

### FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- Certified by USB implementers forum and granted the USB 2.0 high-speed Logo
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction on downstream facing ports when Hub controller is working in high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Supports self-powered and bus-powered mode
- Supports Over-current detection and Individual or ganged power control
- Supports configurable vendor ID, product ID, string descriptors and others with external Serial ROM
- Supports "non-removable" attribution on individual port
- Uses 30 MHz X'tal, or clock input
- Supports downstream port status with LED
- 2.5 V and 3.3 V power supplies

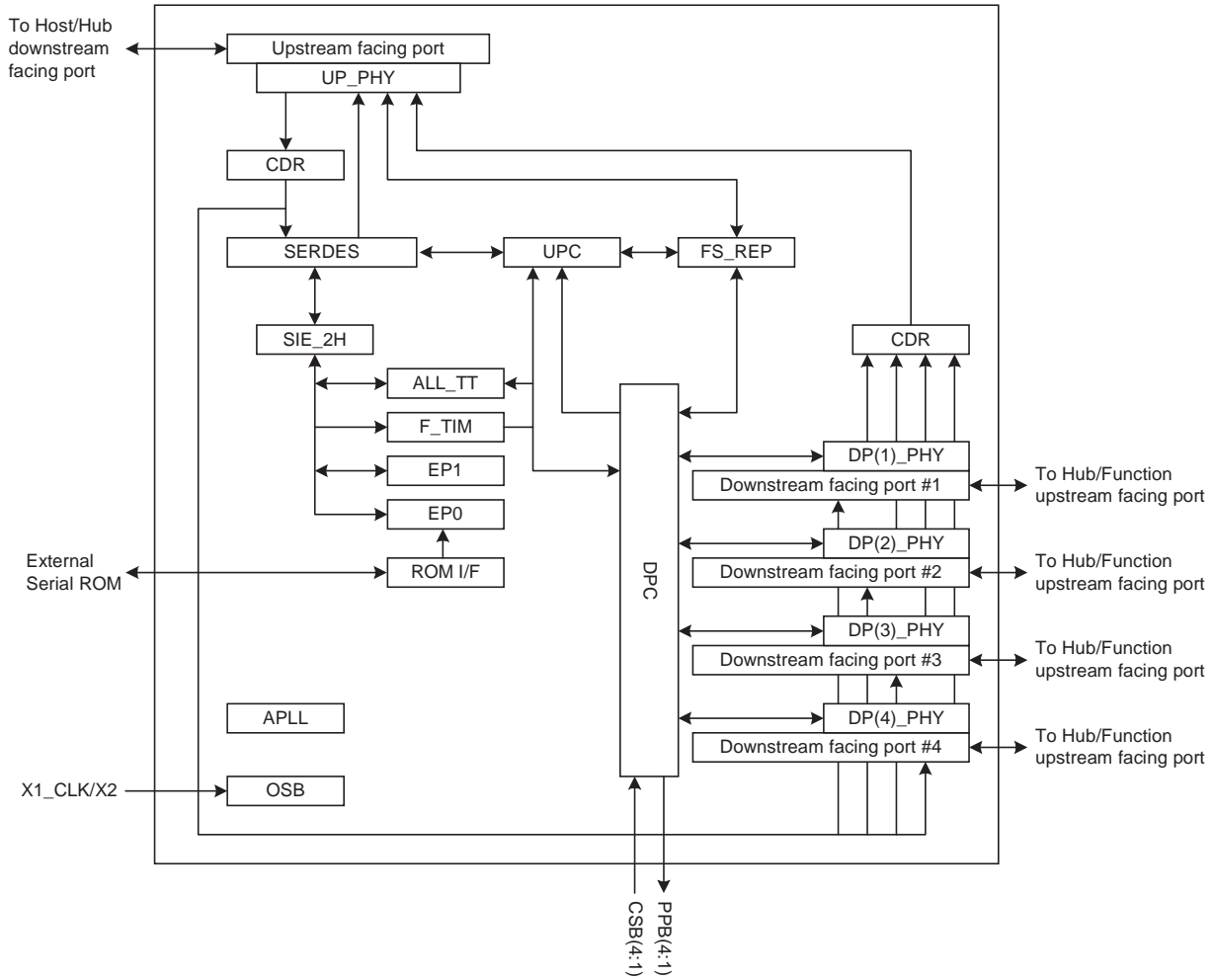
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**ORDERING INFORMATION**

Part Number	Package
μPD720112GK-9EU	80-pin plastic TQFP (Fine pitch) (12 × 12)

**BLOCK DIAGRAM**

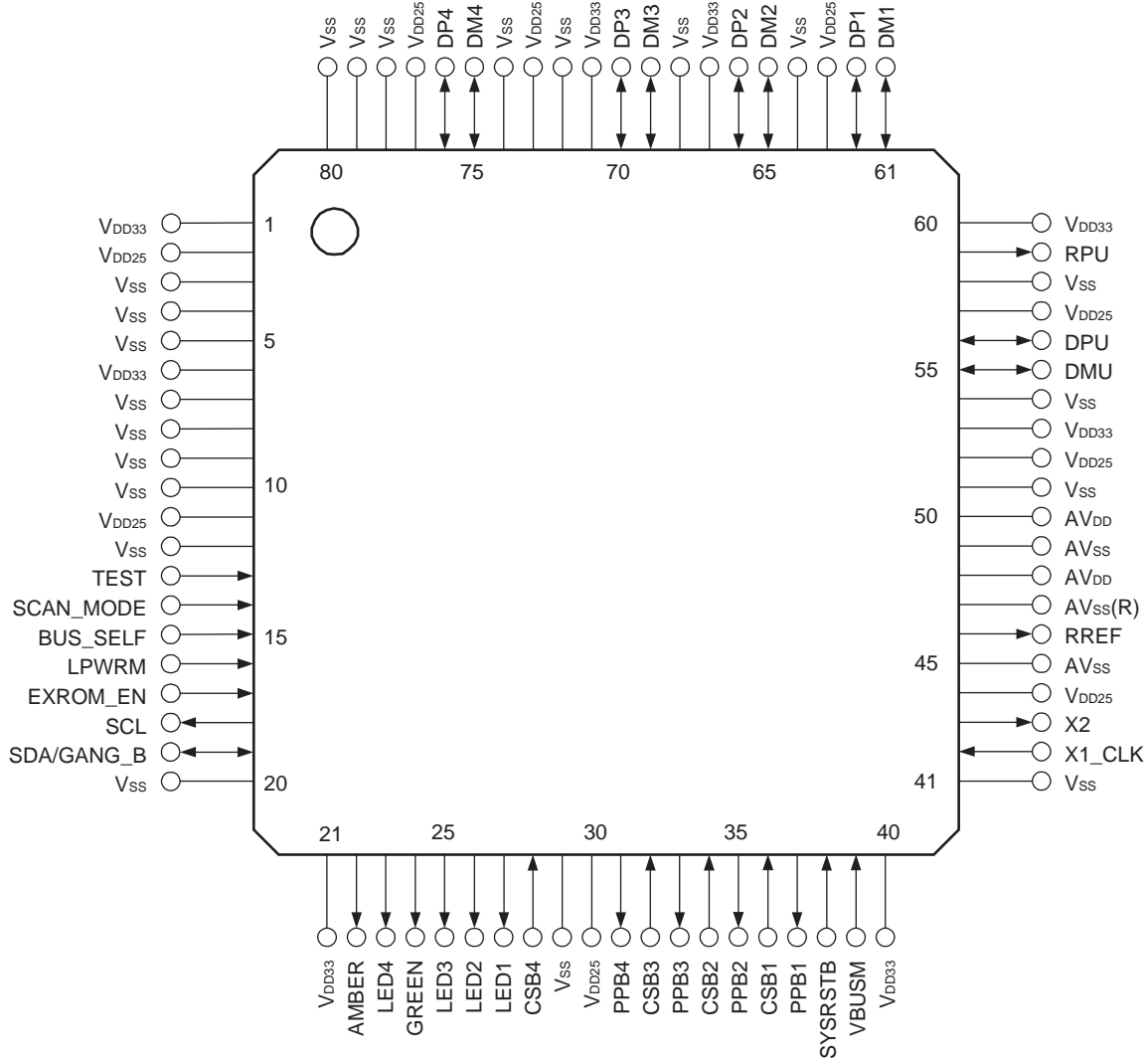


APLL	: Generates all clocks of Hub.
ALL_TT	: Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	: Data & clock recovery circuit
DPC	: Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	: Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	: Endpoint 0 controller
EP1	: Endpoint 1 controller
F_TIM (Frame Timer)	: Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	: Full/low-speed repeater is enabled when the $\mu$ PD720112 are worked at full-speed mode
OSB	: Oscillator Block
ROM I/F	: Interface block for external Serial ROM which contains user-defined descriptors
SERDES	: Serializer and Deserializer
SIE_2H	: Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer.
UP_PHY	: Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	: Upstream Port Controller handles Suspend and Resume

PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic TQFP (Fine pitch) (12 × 12)

μPD720112GK-9EU



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>DD33</sub>	21	V <sub>DD33</sub>	41	V <sub>SS</sub>	61	DM1
2	V <sub>DD25</sub>	22	AMBER	42	X1_CLK	62	DP1
3	V <sub>SS</sub>	23	LED4	43	X2	63	V <sub>DD25</sub>
4	V <sub>SS</sub>	24	GREEN	44	V <sub>DD25</sub>	64	V <sub>SS</sub>
5	V <sub>SS</sub>	25	LED3	45	AV <sub>SS</sub>	65	DM2
6	V <sub>DD33</sub>	26	LED2	46	RREF	66	DP2
7	V <sub>SS</sub>	27	LED1	47	AV <sub>SS</sub> (R)	67	V <sub>DD33</sub>
8	V <sub>SS</sub>	28	CSB4	48	AV <sub>DD</sub>	68	V <sub>SS</sub>
9	V <sub>SS</sub>	29	V <sub>SS</sub>	49	AV <sub>SS</sub>	69	DM3
10	V <sub>SS</sub>	30	V <sub>DD25</sub>	50	AV <sub>DD</sub>	70	DP3
11	V <sub>DD25</sub>	31	PPB4	51	V <sub>SS</sub>	71	V <sub>DD33</sub>
12	V <sub>SS</sub>	32	CSB3	52	V <sub>DD25</sub>	72	V <sub>SS</sub>
13	TEST	33	PPB3	53	V <sub>DD33</sub>	73	V <sub>DD25</sub>
14	SCAN_MODE	34	CSB2	54	V <sub>SS</sub>	74	V <sub>SS</sub>
15	BUS_SELF	35	PPB2	55	DMU	75	DM4
16	LPWRM	36	CSB1	56	DPU	76	DP4
17	EXROM_EN	37	PPB1	57	V <sub>DD25</sub>	77	V <sub>DD25</sub>
18	SCL	38	SYSRSTB	58	V <sub>SS</sub>	78	V <sub>SS</sub>
19	SDA/GANG_B	39	VBUSM	59	RPU	79	V <sub>SS</sub>
20	V <sub>SS</sub>	40	V <sub>DD33</sub>	60	V <sub>DD33</sub>	80	V <sub>SS</sub>

**Remark** AV<sub>SS</sub>(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

Pin Name	I/O	Buffer Type	Active Level	Function
X1_CLK	I	2.5 V input		Crystal oscillator in or clock input
X2	O	2.5 V output		Oscillator out
SYSRSTB	I	5 V tolerant Schmitt input	Low	Asynchronous chip reset
RPU	A (O)	USB pull-up control		External 1.5 kΩ pull-up resistor control
DP(4:1)	I/O	USB D+ signal I/O		USB's downstream facing port D+ signal
DM(4:1)	I/O	USB D- signal I/O		USB's downstream facing port D- signal
DPU	I/O	USB D+ signal I/O		USB's upstream facing port D+ signal
DMU	I/O	USB D- signal I/O		USB's upstream facing port D- signal
BUS_SELF	I	3.3 V Schmitt input		Power mode select
LPWRM	I	3.3 V Schmitt input		Local power monitor
RREF	A (O)	Analog		Reference resistor
CSB(4:1)	I	5 V tolerant input	Low	Port's over-current status input
PPB(4:1)	O	5 V tolerant N-ch open drain	Low	Port's power supply control output
VBUSM	I	5 V tolerant Schmitt input		V <sub>BUS</sub> monitor
SCL	O	3.3 V output		External serial ROM clock out
SDA/GANG_B	I/O	3.3 V Schmitt I/O		External serial ROM data IO or power management mode select
EXROM_EN	I	3.3 V Schmitt input		External serial ROM input enable
AMBER	O	5 V tolerant output		Amber colored LED control output
GREEN	O	5 V tolerant output		Green colored LED control output
LED(4:1)	O	5 V tolerant output	Low	LED indicator output for downstream port status
TEST	I	3.3 V input		Test signal
SCAN_MODE	I	3.3 V input		Test signal
V <sub>DD33</sub>				3.3 V V <sub>DD</sub>
V <sub>DD25</sub>				2.5 V V <sub>DD</sub>
AV <sub>DD</sub>				2.5 V V <sub>DD</sub> for analog circuit
V <sub>SS</sub>				V <sub>SS</sub>
AV <sub>SS</sub>				V <sub>SS</sub> for analog circuit
AV <sub>SS</sub> (R)				V <sub>SS</sub> for reference resistor. Connect to AV <sub>SS</sub> .

**Remark** "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

## 2. ELECTRICAL SPECIFICATIONS

### 2.1 Buffer List

- 2.5 V Oscillator interface  
X1\_CLK, X2
- 5 V Schmitt input buffer  
SYSRSTB, CSB(4:1), VBUSM
- 3.3 V Schmitt input buffer  
BUS\_SELF, LPWRM
- 3.3 V input buffer  
EXROM\_EN, TEST, SCAN\_MODE
- 3.3 V  $I_{OL} = 3$  mA bi-directional Schmitt input buffer with input enable (OR-type)  
SDA/GANG\_B
- 3.3 V  $I_{OL} = 3$  mA output buffer  
SCL
- 5 V  $I_{OL} = 12$  mA output buffer  
AMBER, GREEN, LED2
- 5 V  $I_{OL} = 12$  mA N-ch open drain buffer  
PPB(4:1), LED4, LED3, LED1
- USB2.0 interface  
RPU, DPU, DMU, DP(4:1), DM(4:1), RREF

Above, "5 V" refers to a 3 V input buffer that is 5 V tolerant (has 5 V maximum input voltage). Therefore, it is possible to have a 5 V connection for an external bus.

2.2 Terminology

**Terms Used in Absolute Maximum Ratings**

Parameter	Symbol	Meaning
Power supply voltage	V <sub>DD33</sub> V <sub>DD25</sub> A <sub>VDD</sub>	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V <sub>DD</sub> pin.
Input voltage	V <sub>I</sub>	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V <sub>O</sub>	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I <sub>O</sub>	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into an output pin.
Operating temperature	T <sub>A</sub>	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T <sub>stg</sub>	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

**Terms Used in Recommended Operating Range**

Parameter	Symbol	Meaning
Power supply voltage	V <sub>DD33</sub> V <sub>DD25</sub> A <sub>VDD</sub>	Indicates the voltage range for normal logic operations to occur when V <sub>SS</sub> = 0 V.
High-level input voltage	V <sub>IH</sub>	Indicates the voltage, applied to the input pins of the device, which indicates the high level state for normal operation of the input buffer.  * If a voltage that is equal to or greater than the "MIN." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V <sub>IL</sub>	Indicates the voltage, applied to the input pins of the device, which indicates the low level state for normal operation of the input buffer.  * If a voltage that is equal to or less than the "MAX." value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V <sub>H</sub>	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t <sub>ri</sub>	Indicates allowable input signal transition time from 0.1 × V <sub>DD</sub> to 0.9 × V <sub>DD</sub> .
Input fall time	t <sub>fi</sub>	Indicates allowable input signal transition time from 0.9 × V <sub>DD</sub> to 0.1 × V <sub>DD</sub> .



**Terms Used in DC Characteristics**

Parameter	Symbol	Meaning
Off-state output leakage current	$I_{OZ}$	Indicates the current that flows into a 3-state output pin when it is in a high-impedance state and a voltage is applied to the pin.
Output short circuit current	$I_{OS}$	Indicates the current that flows from an output pin when it is shorted to GND while it is at high-level.
Input leakage current	$I_I$	Indicates the current that flows into an input pin when a voltage is applied to the pin.
Low-level output current	$I_{OL}$	Indicates the current that can flow into an output pin in the low-level state without raising the output voltage above the specified $V_{OL}$ .
High-level output current	$I_{OH}$	Indicates the current that can flow out of an output pin in the high-level state without reducing the output voltage below the specified $V_{OH}$ . (A negative current indicates current flowing out of the pin.)

**2.3 Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	$V_{DD33}$		-0.5 to +4.6	V
	$V_{DD25}$		-0.5 to +3.6	V
	$AV_{DD}$		-0.5 to +3.6	V
Input/output voltage	$V_I/V_O$			
2.5 V input/output voltage		$2.3\text{ V} \leq V_{DD25} \leq 2.7\text{ V}$ $V_I/V_O < V_{DD25} + 0.9\text{ V}$	-0.5 to +3.6	V
3.3 V input/output voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 1.0\text{ V}$	-0.5 to +4.6	V
5 V input/out voltage		$3.0\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$ $V_I/V_O < V_{DD33} + 3.0\text{ V}$	-0.5 to +6.6	V
Output current	$I_O$	$I_{OL} = 3\text{ mA}$	10	mA
		$I_{OL} = 6\text{ mA}$	20	mA
		$I_{OL} = 12\text{ mA}$	40	mA
Operating temperature	$T_A$		0 to +70	°C
Storage temperature	$T_{stg}$		-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

**Recommended Operating Ranges**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	V <sub>DD33</sub>	3.3 V for V <sub>DD33</sub> pins	3.14	3.30	3.46	V
	V <sub>DD25</sub>	2.5 V for V <sub>DD25</sub> pins	2.3	2.5	2.7	V
	AV <sub>DD</sub>	2.5 V for AV <sub>DD</sub> pins	2.3	2.5	2.7	V
High-level input voltage	V <sub>IH</sub>					
2.5 V High-level input voltage			1.7		V <sub>DD25</sub>	V
3.3 V High-level input voltage			2.0		V <sub>DD33</sub>	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V <sub>IL</sub>					
2.5 V Low-level input voltage			0		0.7	V
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V <sub>H</sub>					
5 V Hysteresis voltage			0.3		1.5	V
3.3 V Hysteresis voltage			0.2		1.0	V
Input rise time for SYSRSTB	t <sub>rst</sub>				10	ms
Input rise time	t <sub>ri</sub>					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t <sub>fi</sub>					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

**Two power supply rails limitation.**

The μPD720112 has two power supply rails (2.5 V, 3.3 V). The μPD720112 requires that V<sub>DD25</sub> should be stable before V<sub>DD33</sub> becomes stable. The system will require the time when power supply rail is stable at V<sub>DD</sub> level. And, there will be difference between the time of V<sub>DD25</sub> and V<sub>DD33</sub>. At any case, the system must ensure that the absolute maximum ratings for V<sub>i</sub>/V<sub>o</sub> are not exceeded. System reset signaling should be asserted more than specified time after both V<sub>DD25</sub> and V<sub>DD33</sub> are stable.

DC Characteristics

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output leakage current	$I_{OZ}$	$V_O = V_{DD33}, V_{DD25}$ or $V_{SS}$		±10	μA
Output short circuit current	$I_{OS}$ <sup>Note</sup>			-250	mA
Low-level output current	$I_{OL}$				
3.3 V low-level output current		$V_{OL} = 0.4$ V	3		mA
3.3 V low-level output current		$V_{OL} = 0.4$ V	6		mA
5.0 V low-level output current		$V_{OL} = 0.4$ V	12		mA
High-level output current	$I_{OH}$				
3.3 V high-level output current		$V_{OH} = 2.4$ V	-3		mA
3.3 V high-level output current		$V_{OH} = 2.4$ V	-6		mA
5.0 V high-level output current		$V_{OH} = 2.4$ V	-2		mA
Input leakage current	$I_I$				
3.3 V buffer		$V_I = V_{DD}$ or $V_{SS}$		±10	μA
5.0 V buffer		$V_I = V_{DD}$ or $V_{SS}$		±10	μA

**Note** The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

**USB Interface Block**

Parameter	Symbol	Conditions	MIN	MAX	Unit
Output pin impedance	Z <sub>HSDRV</sub>	Includes R <sub>s</sub> resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R <sub>PU</sub>		1.425	1.575	kΩ
Bus pull-up resistor on downstream facing port	R <sub>PD</sub>		14.25	15.75	kΩ
Termination voltage for upstream facing port pullup (full-speed)	V <sub>TERM</sub>		3.0	3.6	V
<b>Input Levels for Low-/full-speed:</b>					
High-level input voltage (drive)	V <sub>IH</sub>		2.0		V
High-level input voltage (floating)	V <sub>IHZ</sub>		2.7	3.6	V
Low-level input voltage	V <sub>IL</sub>			0.8	V
Differential input sensitivity	V <sub>DI</sub>	(D+) - (D-)	0.2		V
Differential common mode range	V <sub>CM</sub>	Includes V <sub>DI</sub> range	0.8	2.5	V
<b>Output Levels for Low-/full-speed:</b>					
High-level output voltage	V <sub>OH</sub>	R <sub>L</sub> of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V <sub>OL</sub>	R <sub>L</sub> of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V <sub>OSE1</sub>		0.8		V
Output signal crossover point voltage	V <sub>CRS</sub>		1.3	2.0	V
<b>Input Levels for High-speed:</b>					
High-speed squelch detection threshold (differential signal)	V <sub>HSSQ</sub>		100	150	mV
High-speed disconnect detection threshold (differential signal)	V <sub>HSDSC</sub>		525	625	mV
High-speed data signaling common mode voltage range	V <sub>HSCM</sub>		-50	+500	mV
High-speed differential input signaling levels	See Figure 2-4.				
<b>Output Levels for High-speed:</b>					
High-speed idle state	V <sub>HSOI</sub>		-10.0	+10	mV
High-speed data signaling high	V <sub>HSOH</sub>		360	440	mV
High-speed data signaling low	V <sub>HSOL</sub>		-10.0	+10	mV
Chirp J level (different signal)	V <sub>CHIRPJ</sub>		700	1100	mV
Chirp K level (different signal)	V <sub>CHIRPK</sub>		-900	-500	mV

Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed

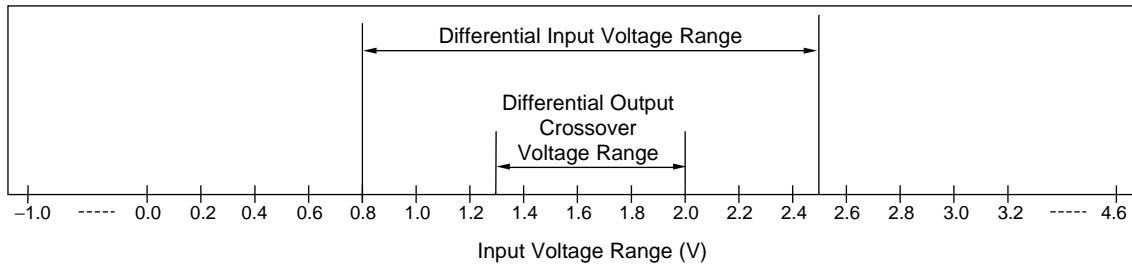


Figure 2-2. Full-speed Buffer  $V_{OH}/I_{OH}$  Characteristics for High-speed Capable Transceiver

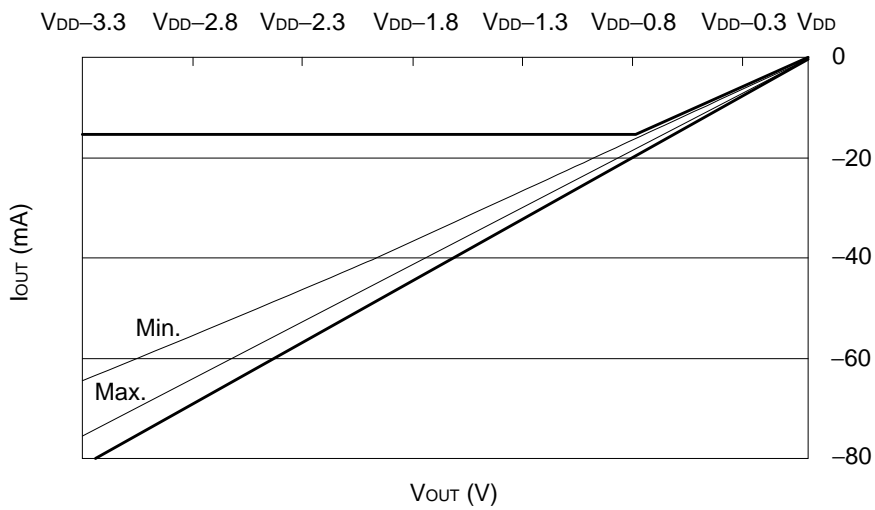


Figure 2-3. Full-speed Buffer  $V_{OL}/I_{OL}$  Characteristics for High-speed Capable Transceiver

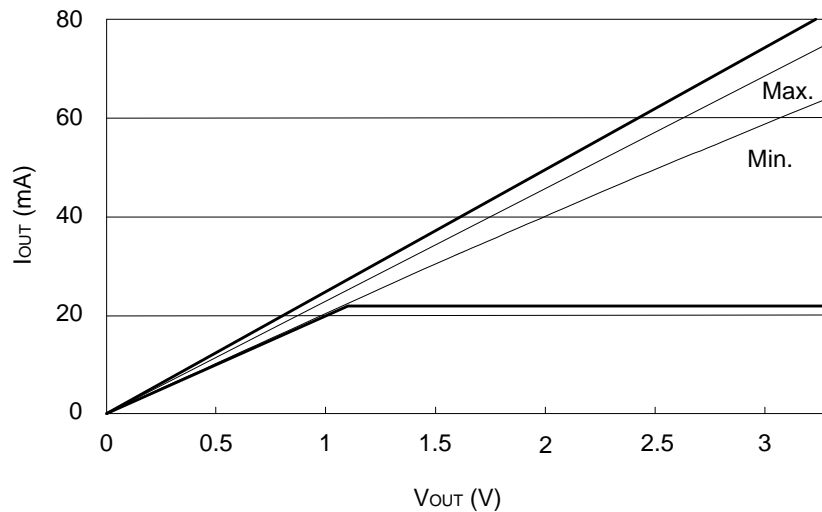


Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM

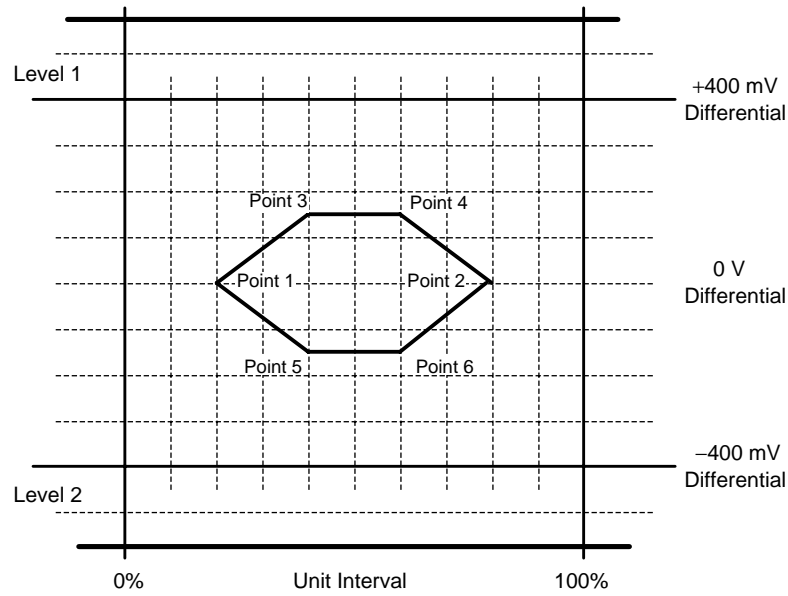
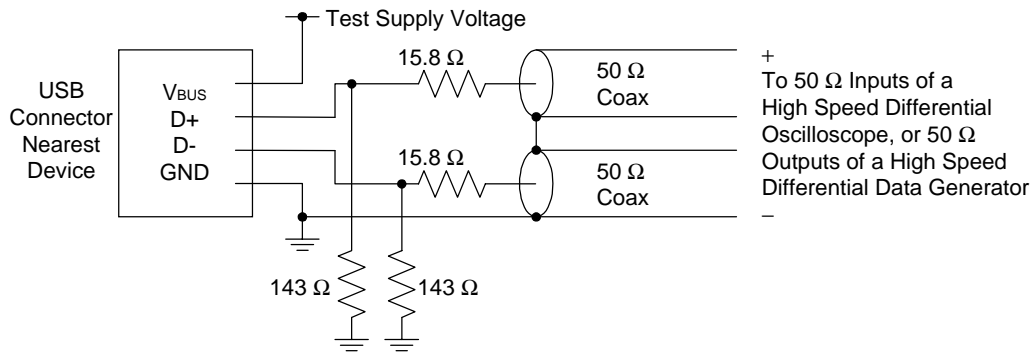


Figure 2-5. Receiver Measurement Fixtures



**Power Consumption**

Parameter	Symbol	Condition	TYP.	Unit	
Power Consumption	P <sub>W-0</sub>	The power consumption under the state without suspend. All the ports do not connect to any function. <sup>Note</sup>			
		Hub controller is operating at full-speed mode.	43	mA (2.5 V)	
			2.4	mA (3.3 V)	
		Hub controller is operating at high-speed mode.	83	mA (2.5 V)	
			23	mA (3.3 V)	
		P <sub>W-2</sub>	The power consumption under the state without suspend. The number of active ports is 2.		
			Hub controller is operating at full-speed mode.	43	mA (2.5 V)
				6.0	mA (3.3 V)
	Hub controller is operating at high-speed mode.		108	mA (2.5 V)	
			49	mA (3.3 V)	
	P <sub>W-3</sub>	The power consumption under the state without suspend. The number of active ports is 3.			
		Hub controller is operating at full-speed mode.	43	mA (2.5 V)	
			7.7	mA (3.3 V)	
		Hub controller is operating at high-speed mode.	118	mA (2.5 V)	
			62	mA (3.3 V)	
	P <sub>W-4</sub>	The power consumption under the state without suspend. The number of active ports is 4.			
Hub controller is operating at full-speed mode.		43	mA (2.5 V)		
		9.3	mA (3.3 V)		
Hub controller is operating at high-speed mode.		127	mA (2.5 V)		
		75	mA (3.3 V)		
P <sub>W-s</sub>	The power consumption under suspend state.		0.66	mA (2.5 V)	
	The internal clock is stopped.		0.50	mA (3.3 V)	

**Note** When any device is not connected to all the ports, the power consumption does not depend on the number of active ports.

**System Clock Ratings**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f <sub>CLK</sub>	X'tal	-500 ppm	30	+500 ppm	MHz
		Oscillator block	-500 ppm	30	+500 ppm	MHz
Clock Duty cycle	t <sub>DUTY</sub>		40	50	60	%

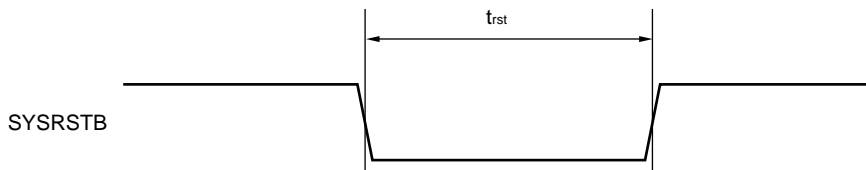
- Remarks**
1. Recommended accuracy of clock frequency is ± 100 ppm.
  2. Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

**AC Characteristics (V<sub>DD</sub> = 3.14 to 3.46 V, T<sub>A</sub> = 0 to +70°C)**

**System Reset Timing**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Reset active time (Figure 2-6)	t <sub>rst</sub>		5		μs

**Figure 2-6. System Reset Timing**

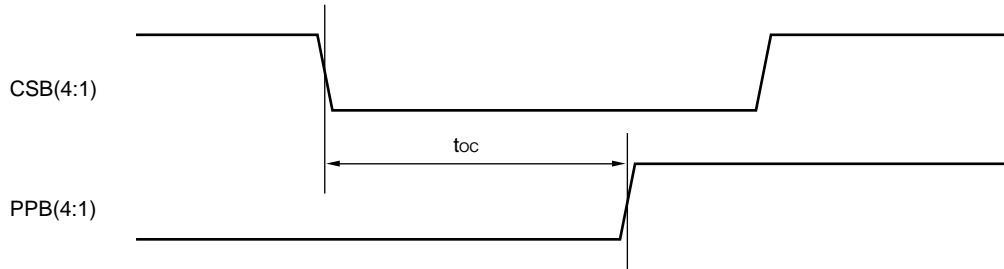




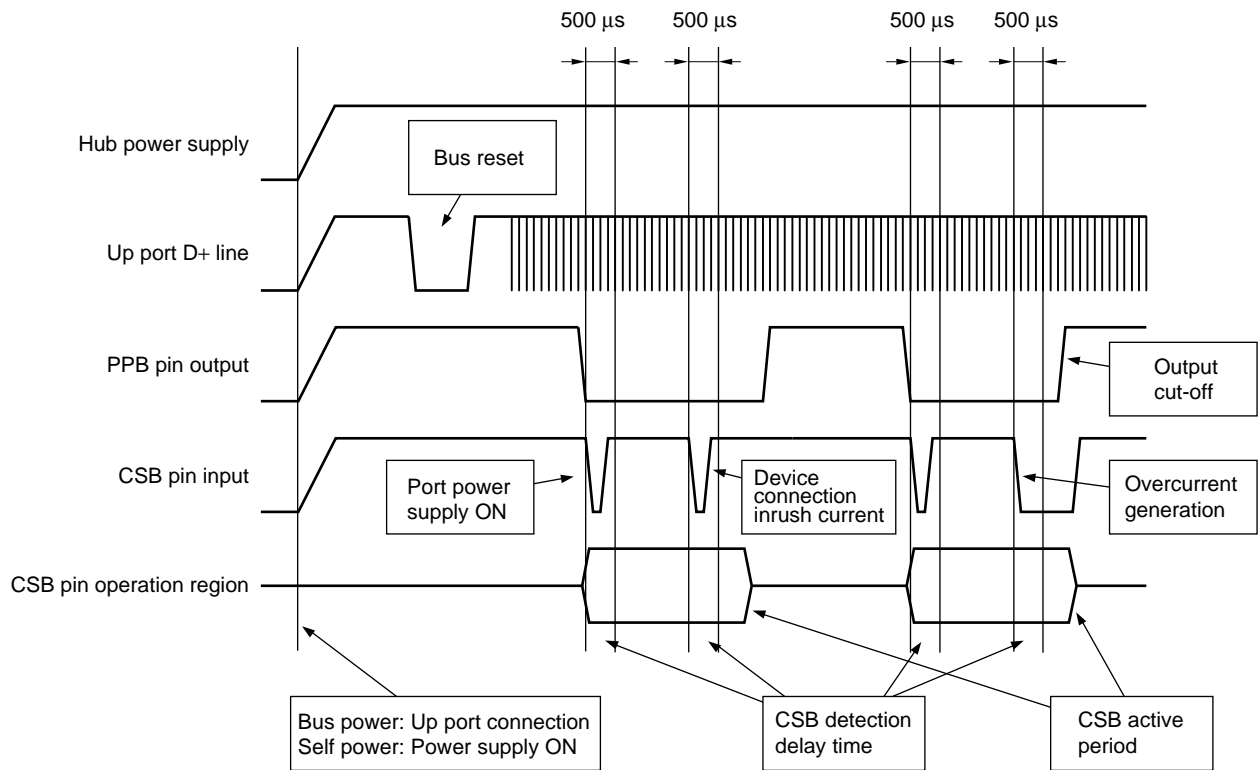
**Over-current Response Timing**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Over-current response time from CSB low to PPB high (Figure 2-7)	$t_{oc}$		500		625	$\mu s$

**Figure 2-7. Over-current Response Timing**



**Figure 2-8. CSB/PPB Timing**

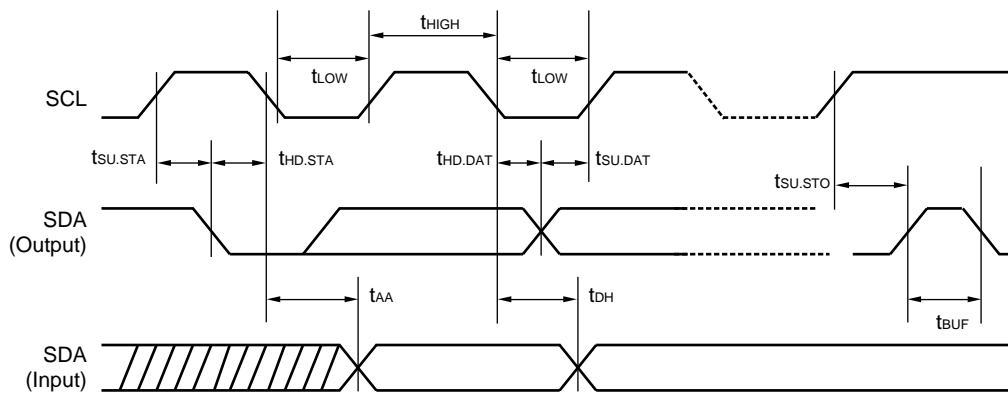


**Remark** The active period of the CSB pin is in effect only when the PPB pin is ON.  
 There is a delay time of approximately 500  $\mu s$  duration at the CSB pin.

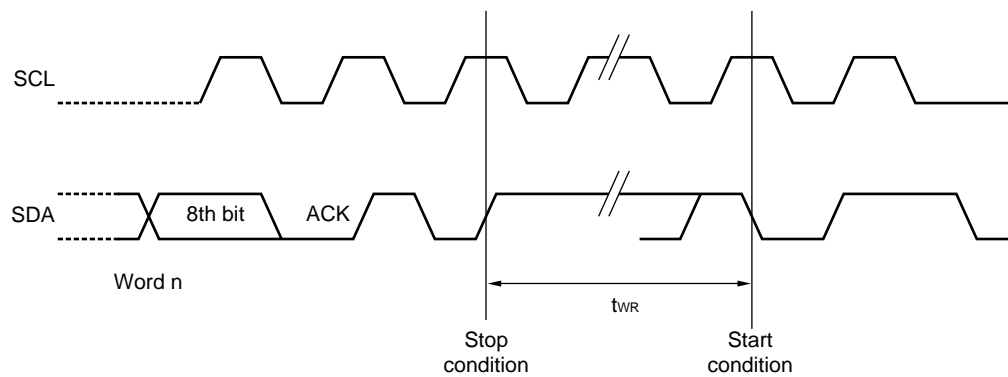
**External Serial ROM Timing**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f <sub>SCL</sub>			94.6	100	kHz
Clock pulse width low	t <sub>LOW</sub>		4700			ns
Clock pulse width high	t <sub>HIGH</sub>		4000			ns
Clock low to data out valid	t <sub>AA</sub>		100		3500	ns
Time the bus must be free before a new transmission can start	t <sub>BUF</sub>		4700			ns
Start hold time	t <sub>HD.STA</sub>		4000			ns
Start setup time	t <sub>SU.STA</sub>		4700			ns
Data in hold time	t <sub>HD.DTA</sub>		0			ns
Data in setup time	t <sub>SU.DTA</sub>		250			ns
Stop setup time	t <sub>SU.STO</sub>		4700			ns
Data out hold time	t <sub>DH</sub>		300			ns
Write cycle time	t <sub>WR</sub>				15	ms

**Figure 2-9. External Serial ROM Bus Timing**



**Figure 2-10. External Serial ROM Write Cycle Timing**



USB Interface Block

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
<b>Low-speed Electrical Characteristics</b>					
Rise time (10% to 90%)	t <sub>LR</sub>	C <sub>L</sub> = 200 pF to 600 pF	75	300	ns
Fall time (90% to 10%)	t <sub>LF</sub>	C <sub>L</sub> = 200 pF to 600 pF	75	300	ns
Differential rise and fall time matching	t <sub>LRFM</sub>	(t <sub>LR</sub> /t <sub>LF</sub> ) <sup>Note</sup>	80	125	%
Low-speed data rate	t <sub>LDRAHS</sub>	Average bit rate	1.49925	1.50075	Mbps
Downstream facing port source jitter total (including frequency tolerance) (Figure 2-15):					
To next transition	t <sub>DDJ1</sub>		-25	+25	ns
For paired transitions	t <sub>DDJ2</sub>		-14	+14	ns
Downstream facing port differential receiver jitter total (including frequency tolerance) (Figure 2-17):					
To next transition	t <sub>UJR1</sub>		-152	+152	ns
For paired transitions	t <sub>UJR2</sub>		-200	+200	ns
Source SE0 interval of EOP (Figure 2-16)	t <sub>LEOPT</sub>		1.25	1.5	μs
Receiver SE0 interval of EOP (Figure 2-16)	t <sub>LEOPR</sub>		670		ns
Width of SE0 interval during differential transition	t <sub>LST</sub>			210	ns
Hub differential data delay (Figure 2-13)	t <sub>LHDD</sub>			300	ns
Hub differential driver jitter (including cable) (Figure 2-13):					
Downstream facing port					
To next transition	t <sub>LDHJ1</sub>		-45	+45	ns
For paired transitions	t <sub>LDHJ2</sub>		-15	+15	ns
Upstream facing port					
To next transition	t <sub>LUHJ1</sub>		-45	+45	ns
For paired transitions	t <sub>LUHJ2</sub>		-45	+45	ns
Data bit width distortion after SOP (Figure 2-13)	t <sub>LSOP</sub>		-60	+60	ns
Hub EOP delay relative to t <sub>HDD</sub> (Figure 2-14)	t <sub>LEOPD</sub>		0	200	ns
Hub EOP output width skew (Figure 2-14)	t <sub>LHESK</sub>		-300	+300	ns
<b>Full-speed Electrical Characteristics</b>					
Rise time (10% to 90%)	t <sub>FR</sub>	C <sub>L</sub> = 50 pF, R <sub>S</sub> = 36 Ω	4	20	ns
Fall time (90% to 10%)	t <sub>FF</sub>	C <sub>L</sub> = 50 pF, R <sub>S</sub> = 36 Ω	4	20	ns
Differential rise and fall time matching	t <sub>FRFM</sub>	(t <sub>FR</sub> /t <sub>FF</sub> )	90	111.11	%
Full-speed data rate	t <sub>FDRATHS</sub>	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t <sub>FRAME</sub>		0.9995	1.0005	ms

**Note** Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
<b>Full-speed Electrical Characteristics (Continued)</b>					
Consecutive frame interval jitter	t <sub>RFI</sub>	No clock adjustment		42	ns
Source jitter total (including frequency tolerance) (Figure 2-15):		<b>Note</b>			
To next transition	t <sub>DJ1</sub>		-3.5	+3.5	ns
For paired transitions	t <sub>DJ2</sub>		-4.0	+4.0	ns
Source jitter for differential transition to SE0 transition (Figure 2-16)	t <sub>FDEOP</sub>		-2	+5	ns
Receiver jitter (Figure 2-17):					
To Next Transition	t <sub>JR1</sub>		-18.5	+18.5	ns
For Paired Transitions	t <sub>JR2</sub>		-9	+9	ns
Source SE0 interval of EOP (Figure 2-16)	t <sub>FEOPT</sub>		160	175	ns
Receiver SE0 interval of EOP (Figure 2-16)	t <sub>FEOPR</sub>		82		ns
Width of SE0 interval during differential transition	t <sub>FST</sub>			14	ns
Hub differential data delay (Figure 2-13)					
(with cable)	t <sub>HDD1</sub>			70	ns
(without cable)	t <sub>HDD2</sub>			44	ns
Hub differential driver jitter (including cable) (Figure 2-13):					
To next transition	t <sub>HDJ1</sub>		-3	+3	ns
For paired transitions	t <sub>HDJ2</sub>		-1	+1	ns
Data bit width distortion after SOP (Figure 2-13)	t <sub>FSOP</sub>		-5	+5	ns
Hub EOP delay relative to t <sub>HDD</sub> (Figure 2-14)	t <sub>FEOPD</sub>		0	15	ns
Hub EOP output width skew (Figure 2-14)	t <sub>FHESK</sub>		-15	+15	ns
<b>High-speed Electrical Characteristics</b>					
Rise time (10% to 90%)	t <sub>HSR</sub>		500		ps
Fall time (90% to 10%)	t <sub>HSF</sub>		500		ps
Driver waveform	See Figure 2-11.				
High-speed data rate	t <sub>HSDRAT</sub>		479.760	480.240	Mbps
Microframe interval	t <sub>HSFRAM</sub>		124.9375	125.0625	μs
Consecutive microframe interval difference	t <sub>HSRFI</sub>			4 high-speed	Bit times
Data source jitter	See Figure 2-11.				
Receiver jitter tolerance	See Figure 2-4.				
Hub data delay (without cable)	t <sub>HSHDD</sub>			36 high-speed+4 ns	Bit times
Hub data jitter	See Figure 2-4, Figure 2-11.				
Hub delay variation range	t <sub>HSHDV</sub>			5 high-speed	Bit times

**Note** Excluding the first transition from the Idle state.

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Parameter	Symbol	Conditions	MIN.	MAX.	Unit
<b>Hub Event Timings</b>					
Time to detect a downstream facing port connect event (Figure 2-19): Awake hub Suspended hub	t <sub>DCNN</sub>		2.5	2000	μs
			2.5	12000	μs
Time to detect a disconnect event at a hub's downstream facing port (Figure 2-18)	t <sub>DDIS</sub>		2.0	2.5	μs
Duration of driving resume to a downstream port (only from a controlling hub)	t <sub>DRSMON</sub>		20		ms
Time from detecting downstream resume to rebroadcast	t <sub>URSM</sub>			1.0	ms
Duration of driving reset to a downstream facing port (Figure 2-20)	t <sub>DRST</sub>	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
Time to detect a long K from upstream	t <sub>URLK</sub>		2.5	100	μs
Time to detect a long SE0 from upstream	t <sub>URLSE0</sub>		2.5	10000	μs
Duration of repeating SE0 upstream (for low-/full-speed repeater)	t <sub>URPSE0</sub>			23	FS Bit times
Inter-packet delay (for high-speed) of packets traveling in same direction	t <sub>HSIPDSD</sub>		88		Bit times
Inter-packet delay (for high-speed) of packets traveling in opposite direction	t <sub>HSIPDOD</sub>		8		Bit times
Inter-packet delay for device/root hub response with detachable cable for high-speed	t <sub>HSRSPID1</sub>			192	Bit times
Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	t <sub>FILT</sub>		2.5		μs
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence	t <sub>WTDCH</sub>			100	μs
Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset	t <sub>DCHBIT</sub>		40	60	μs
Time before end of reset by which a hub must end its downstream chirp sequence	t <sub>DCHSE0</sub>		100	500	μs
Time from internal power good to device pulling D+ beyond V <sub>IHZ</sub> (Figure 2-20)	t <sub>SIGATT</sub>			100	ms
Debounce interval provided by USB system software after attach (Figure 2-20)	t <sub>ATTDB</sub>			100	ms
Maximum duration of suspend averaging interval	t <sub>SUSAVGI</sub>			1	s
Period of idle bus before device can initiate resume	t <sub>WTRSM</sub>		5		ms
Duration of driving resume upstream	t <sub>DRSMUP</sub>		1	15	ms

(4/4)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
<b>Hub Event Timings (Continued)</b>					
Resume recovery time	t <sub>RSMRCY</sub>	Remote-wakeup is enabled	10		ms
Time to detect a reset from upstream for non high-speed capable devices	t <sub>DETRST</sub>		2.5	10000	μs
Reset recovery time (Figure 2-20)	t <sub>RSTRCY</sub>			10	ms
Inter-packet delay for full-speed	t <sub>IPD</sub>		2		Bit times
Inter-packet delay for device response with detachable cable for full-speed	t <sub>RSPID1</sub>			6.5	Bit times
SetAddress() completion time	t <sub>DSETADDR</sub>			50	ms
Time to complete standard request with no data	t <sub>DRQCMLTND</sub>			50	ms
Time to deliver first and subsequent (except last) data for standard request	t <sub>DRETDATA1</sub>			500	ms
Time to deliver last data for standard request	t <sub>DRETDATAN</sub>			50	ms
Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake	t <sub>FILTSE0</sub>		2.5		μs
Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake	t <sub>WTRSTFS</sub>		2.5	3000	ms
Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed	t <sub>WTREV</sub>		3.0	3.125	ms
Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed	t <sub>WTRSTHS</sub>		100	875	ms
Minimum duration of a Chirp K on upstream from a hub within the reset protocol	t <sub>UCH</sub>		1.0		ms
Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol	t <sub>UCHEND</sub>			7.0	ms
Time between detection of downstream chip and entering high-speed state	t <sub>WTHS</sub>			500	μs
Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected	t <sub>WTFS</sub>		1.0	2.5	ms

Figure 2-11. Transmit Waveform for Transceiver at DP/DM

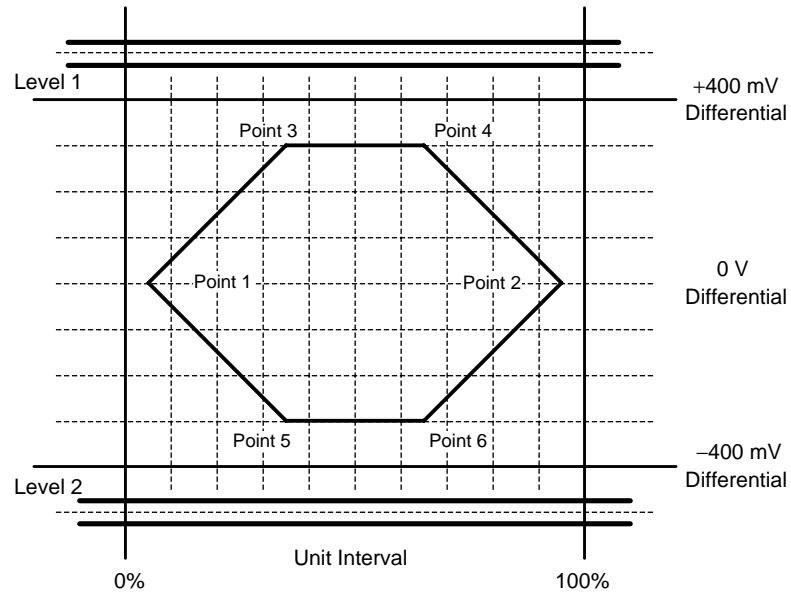
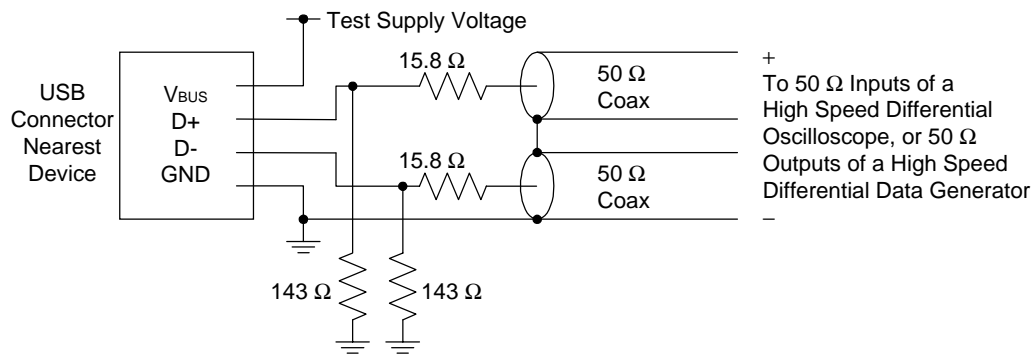
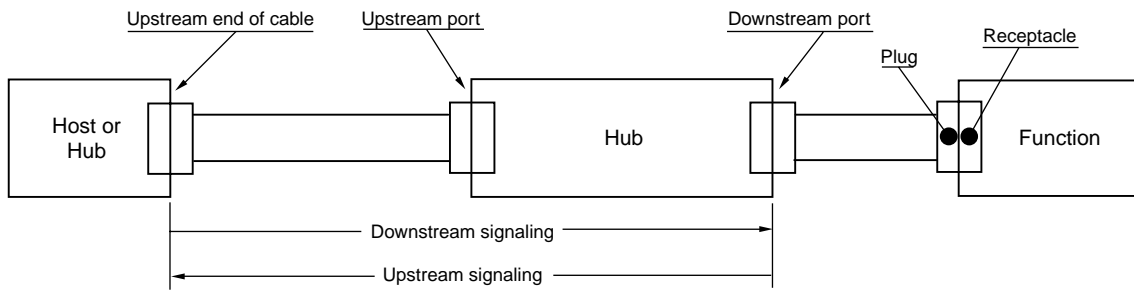
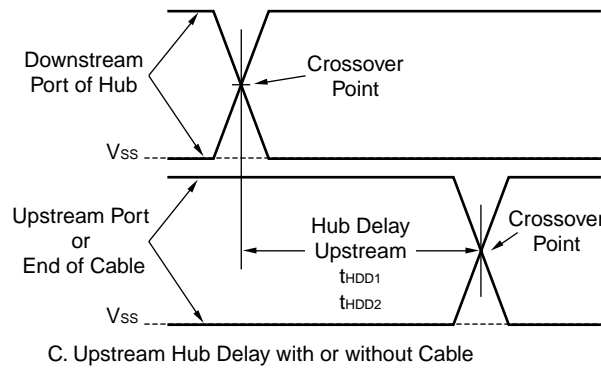
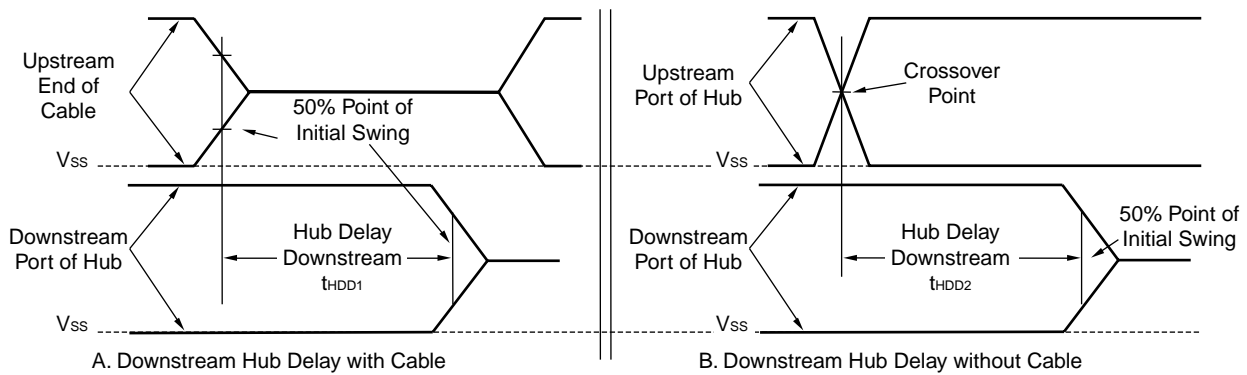


Figure 2-12. Transmitter Measurement Fixtures



Timing Diagram

Figure 2-13. Hub Differential Delay, Differential Jitter, and SOP Distortion



D. Measurement Points

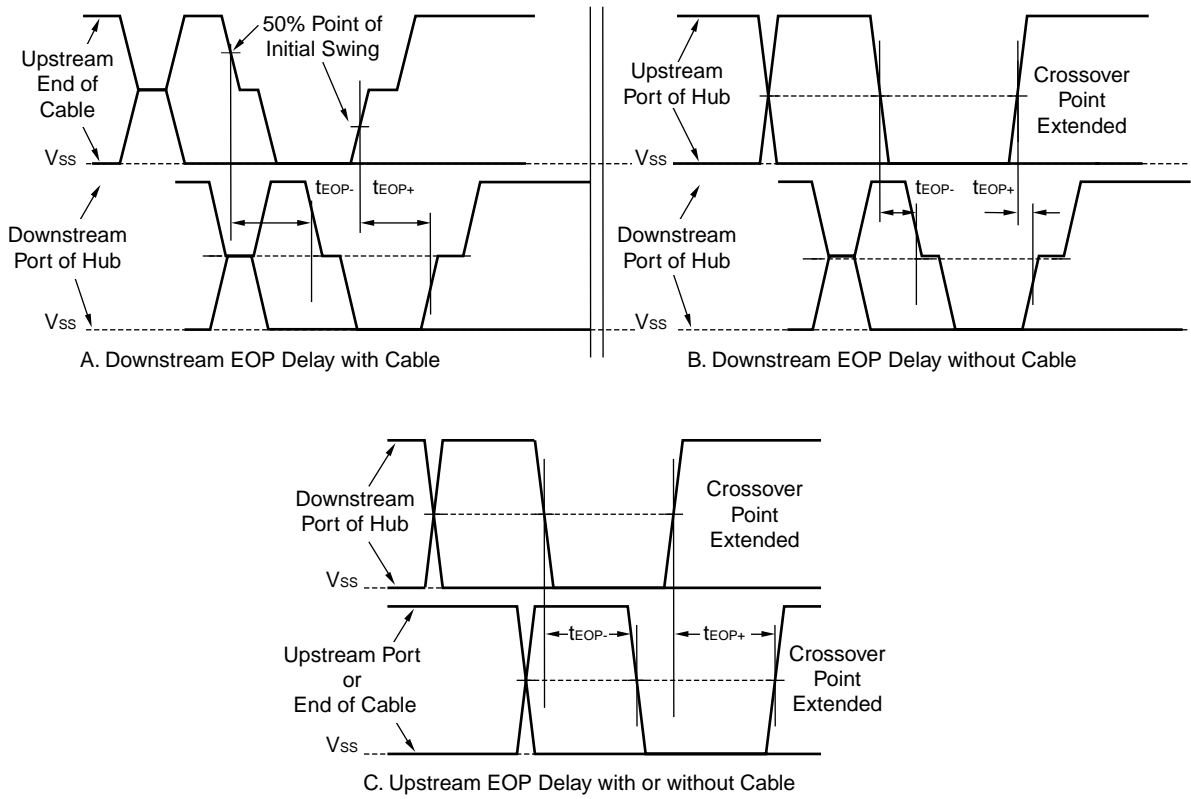
Hub Differential Jitter:  
 $t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$  or  $t_{HDDx}(K) - t_{HDDx}(J)$  Consecutive Transitions  
 $t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$  or  $t_{HDDx}(K) - t_{HDDx}(K)$  Paired Transitions

Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):  
 $t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$

Low-speed timings are determined in the same way for:  
 $t_{LHDD}$ ,  $t_{LDHJ1}$ ,  $t_{LDJH2}$ ,  $t_{LUHJ1}$ ,  $t_{LUJH2}$ , and  $t_{LSOP}$



Figure 2-14. Hub EOP Delay and EOP Skew



EOP Delay:  
 $t_{FEOPD} = t_{EOPy} - t_{HDDx}$   
 ( $t_{EOPy}$  means that this equation applies to  $t_{EOP-}$  and  $t_{EOP+}$ )

EOP Skew:  
 $t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:  
 $t_{LEOPD}$  and  $t_{LHESK}$

Figure 2-15. USB Differential Data Jitter for Low-/full-speed

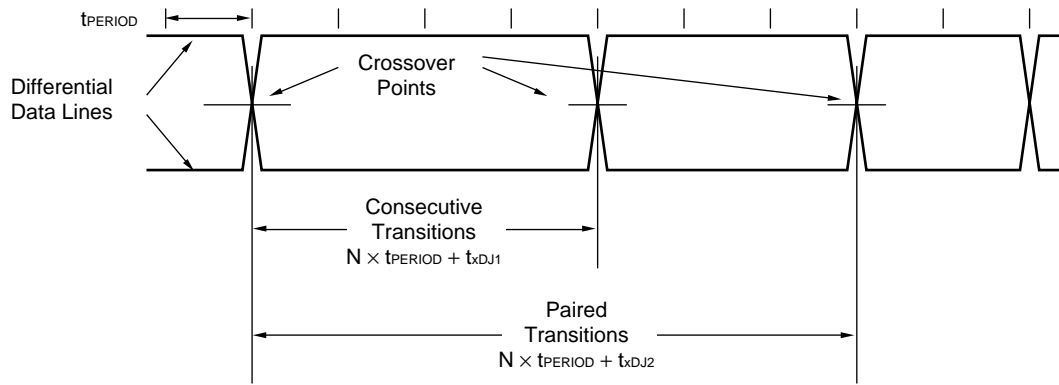


Figure 2-16. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed

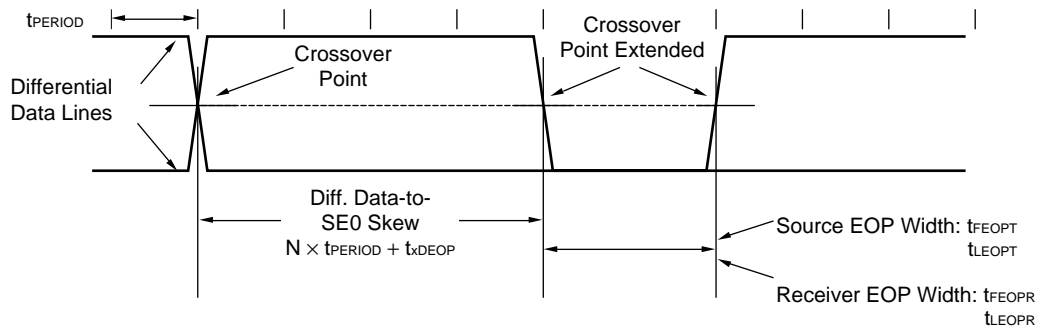


Figure 2-17. USB Receiver Jitter Tolerance for Low-/full-speed

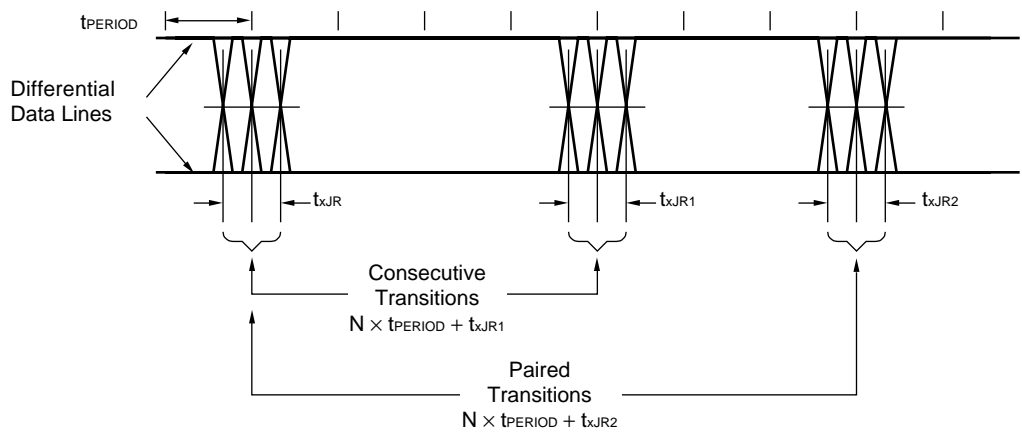


Figure 2-18. Low-/full-speed Disconnect Detection

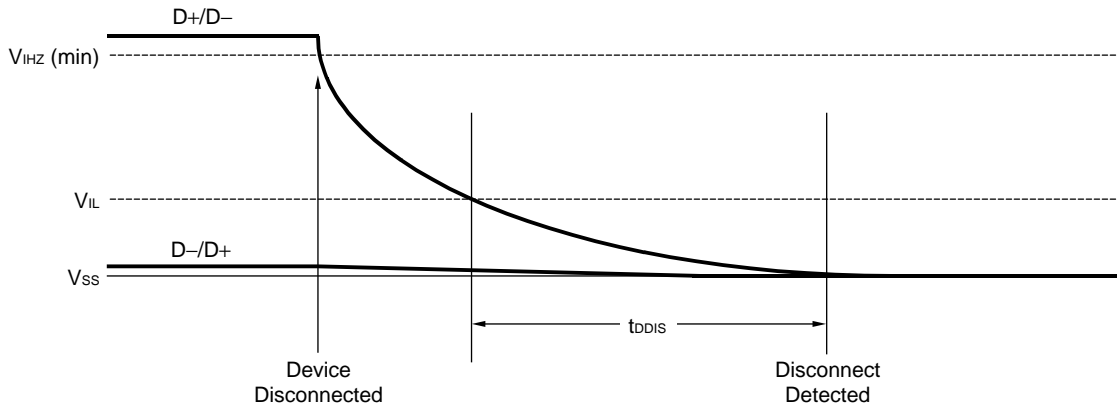


Figure 2-19. Full-/high-speed Device Connect Detection

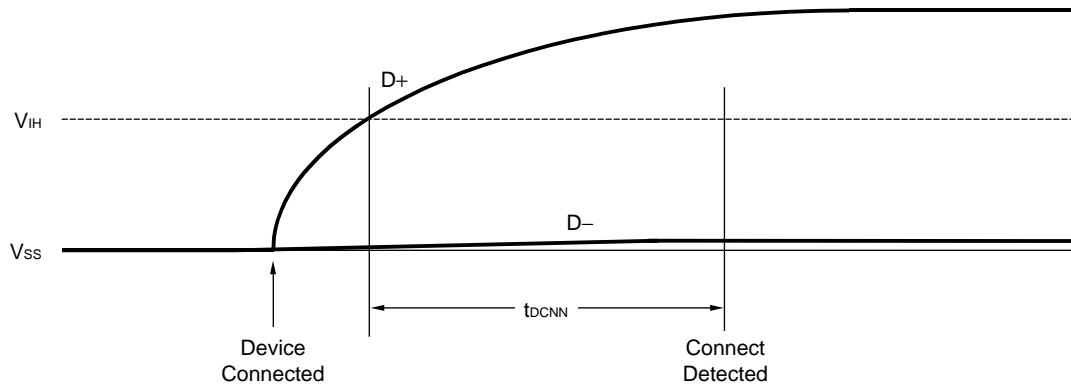
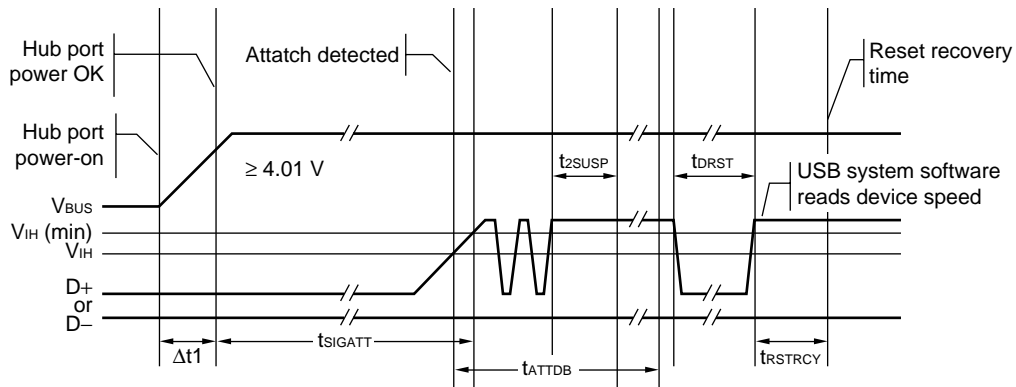
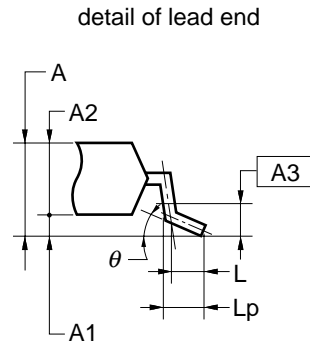
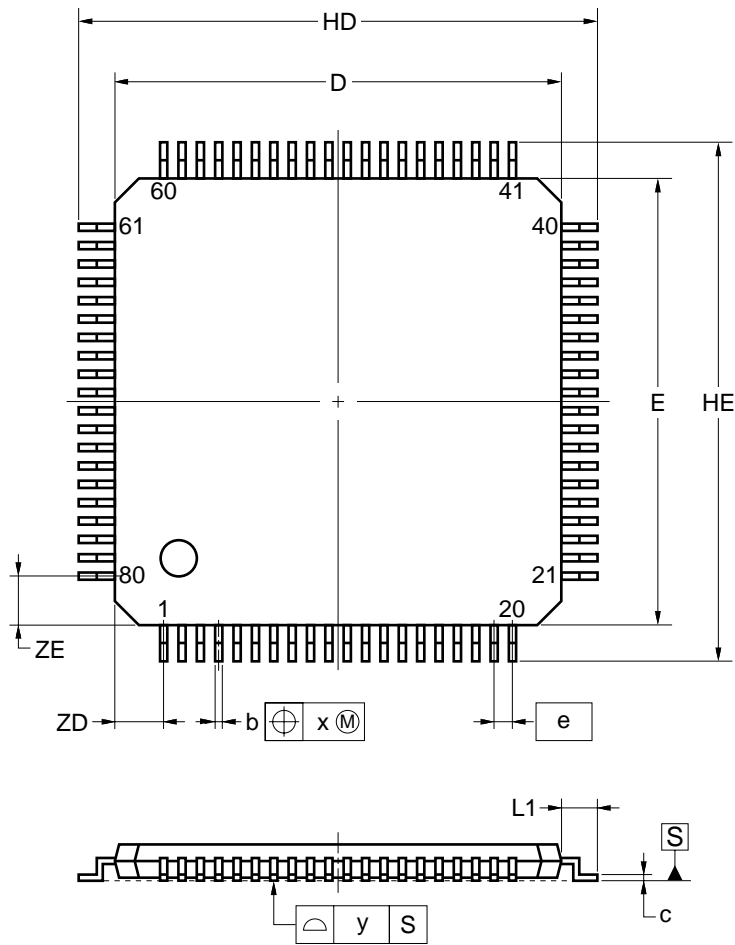


Figure 2-20. Power-on and Connection Events Timing



3. PACKAGE DRAWING

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
A2	1.00
HD	14.00±0.20
HE	14.00±0.20
A	1.10±0.10
A1	0.10±0.05
A3	0.25
Lp	0.60±0.15
b	0.22±0.05
c	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
θ	3° <sup>+4°</sup> <sub>-3°</sub>
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25
L	0.50
L1	1.00±0.20

K80GK-50-9EU

NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

**4. RECOMMENDED SOLDERING CONDITIONS**

The μPD720112 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

**μPD720112GK-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-103-3
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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