IEEE1394a-2000 COMPLIANT 400 Mbps TWO-PORT PHY LSI

The μPD72852 is a two-port physical layer LSI that complies with the IEEE1394a-2000 specifications.

The μPD72852 supports transfers of up to 400 Mbps and consumes less power than the μPD72850B. The μPD72852 is suitable for battery systems with an IEEE1394 interface.
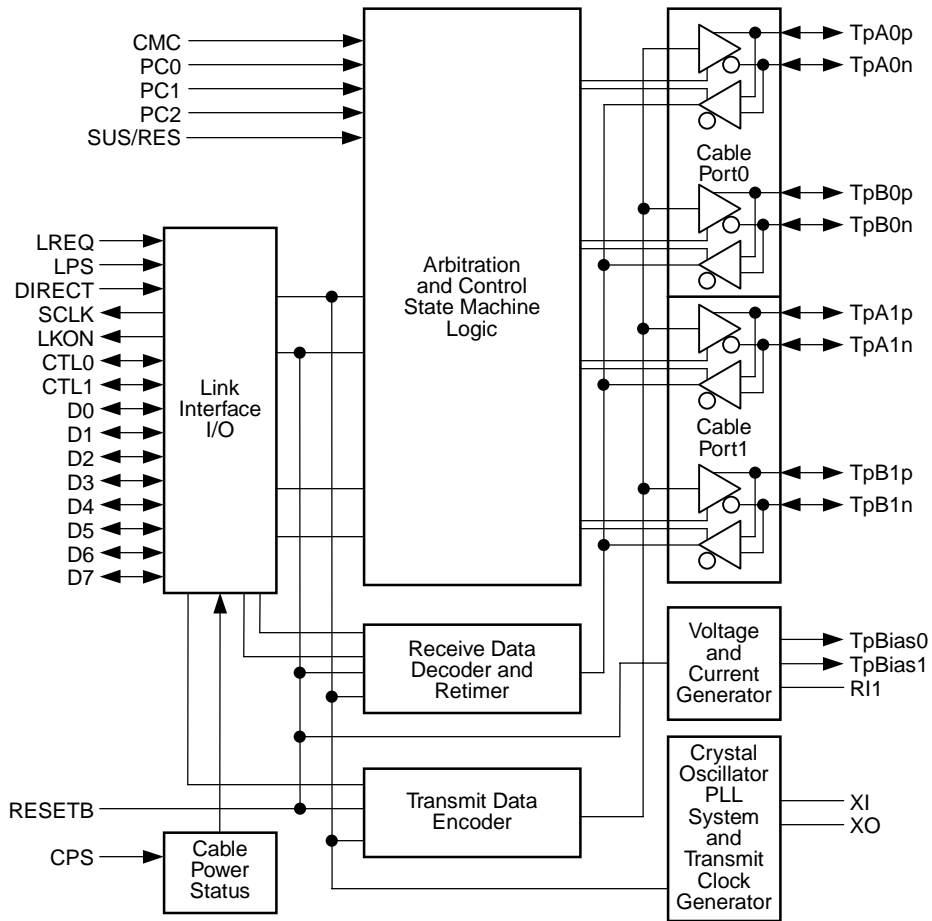
FEATURES

- The two-port physical layer LSI complies with IEEE1394a-2000
- Fully interoperable with IEEE1394 std 1394 Link (FireWire™, i.LINK™)
- Meets Intel™ Mobile Power Guideline 2000
- Full IEEE1394a-2000 support includes: Suspend/Resume, connection debounce, arbitrated short bus reset, multi-speed concatenation, arbitration acceleration, fly-by concatenation
- Fully compliant with OHCI requirements
- Small package: 64-pin plastic LQFP
- Super low power: 68 mA (Operating mode)
  : 115 μA (Suspend mode)
- Data rate: 400/200/100 Mbps
- Supports PHY pinging and remote PHY access packets
- 3.3 V single power supply (if power not supplied via node: 3.0 V single power supply)
- 24.576 MHz crystal clock generation, 393.216 MHz PLL multiplying frequency
- 64-bit flexible register incorporated in PHY register
- Electrically isolated Link interface
- Supports LPS/Link-on as part of PHY/Link interface
- External filter capacitors for PLL not required
- Extended Resume signaling for compatibility with legacy DV devices
- System power management by signaling of node power class information
- Cable power monitor (CPS) is equipped

ORDERING INFORMATION

Part number	Package
μPD72852GB-8EU	64-pin plastic LQFP (10 x 10)

The mark ★ shows major revised points.

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BLOCK DIAGRAM

PIN CONFIGURATION (Top View)

• μ**PD72852GB-8EU**

    64-pin plastic LQFP (10 x 10)

Top pins (64–49): DGND, LREQ, TEST, SPD, DV_{DD}, LPS, LKON, DGND, DV_{DD}, RESETB, AV_{DD}, AGND, AGND, IC(AL), DIRECT, AGND

Left pins (1–16):
1 DGND
2 SCLK
3 IC(DL)
4 DV_{DD}
5 CTL0
6 CTL1
7 DGND
8 D0
9 D1
10 DV_{DD}
11 D2
12 D3
13 DGND
14 D4
15 D5
16 DGND

Right pins (48–33):
48 TpBias1
47 AV_{DD}
46 TpA1p
45 TpA1n
44 TpB1p
43 TpB1n
42 AGND
41 TpBias0
40 AV_{DD}
39 TpA0p
38 TpA0n
37 TpB0p
36 TpB0n
35 AGND
34 RI1
33 AGND

Bottom pins (17–32): D6, D7, SUS/RES, DV_{DD}, DGND, XO, XI, AGND, AV_{DD}, PC0, PC1, PC2, IC(AL), CMC, AV_{DD}, CPS

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PIN NAME

AGND	: Analog GND
AV$_{DD}$	: Analog Power
CMC	: Configuration Manager Capable
CPS	: Cable Power Status
CTL0	: Link Interface Control (bit 0)
CTL1	: Link Interface Control (bit 1)
D0-D7	: Data Input/Output
DGND	: Digital GND
DIRECT	: PHY/Link Isolation Barrier Control Input
DV$_{DD}$	: Digital V$_{DD}$
IC(AL)	: Internally Connected (Low Clamped)
IC(DL)	: Internally Connected (Low Clamped)
LKON	: Link-on Signal Output
LPS	: Link Power Status Input
LREQ	: Link Request Input
PC0-PC2	: Power Class Set Input
RESETB	: Power-on Reset Input
RI1	: Reference Power Set, Connect Resistor 1
SCLK	: Link Control Output Clock
SPD	: Speed Select
SUS/RES	: Suspend/Resume Function Select
TEST	: Test Pin (Low Clamped)
TpA0n	: Port 0 Twisted Pair Cable A Negative Phase I/O
TpA0p	: Port 0 Twisted Pair Cable A Positive Phase I/O
TpA1n	: Port 1 Twisted Pair Cable A Negative Phase I/O
TpA1p	: Port 1 Twisted Pair Cable A Positive Phase I/O
TpB0n	: Port 0 Twisted Pair Cable B Negative Phase I/O
TpB0p	: Port 0 Twisted Pair Cable B Positive Phase I/O
TpB1n	: Port 1 Twisted Pair Cable B Negative Phase I/O
TpB1p	: Port 1 Twisted Pair Cable B Positive Phase I/O
TpBias0	: Port 0 Twisted Pair Output
TpBias1	: Port 1 Twisted Pair Output
XI	: Crystal Oscillator Connection XI
XO	: Crystal Oscillator Connection XO

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CONTENTS

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1. PIN FUNCTIONS

1.1 Cable Interface Pins

Name	Pin No.	I/O	Function
TpA0p	39	I/O	Port 0 twisted pair cable A positive phase I/O
TpA0n	38	I/O	Port 0 twisted pair cable A negative phase I/O
TpB0p	37	I/O	Port 0 twisted pair cable B positive phase I/O
TpB0n	36	I/O	Port 0 twisted pair cable B negative phase I/O
TpA1p	46	I/O	Port 1 twisted pair cable A positive phase I/O
TpA1n	45	I/O	Port 1 twisted pair cable A negative phase I/O
TpB1p	44	I/O	Port 1 twisted pair cable B positive phase I/O
TpB1n	43	I/O	Port 1 twisted pair cable B negative phase I/O
SUS/RES	19	I	Suspend/Resume function select 1: Suspend/Resume on (IEEE1394a-2000 compliant) 0: Suspend/Resume off (P1394a draft 1.3 compliant)
CPS	32	I	Cable power status Connect to the cable through a 390 kΩ resistor and to GND through a 100 kΩ resistor. 0: Cable power fail 1: Cable power on

1.2 Link Interface Pins

Name	Pin No.	I/O	Function
D0	8	I/O	Data input/output (bit 0)
D1	9	I/O	Data input/output (bit 1)
D2	11	I/O	Data input/output (bit 2)
D3	12	I/O	Data input/output (bit 3)
D4	14	I/O	Data input/output (bit 4)
D5	15	I/O	Data input/output (bit 5)
D6	17	I/O	Data input/output (bit 6)
D7	18	I/O	Data input/output (bit 7)
CTL0	5	I/O	Link interface control (bit 0)
CTL1	6	I/O	Link interface control (bit 1)
LREQ	63	I	Link request input
SCLK	2	O	Link control output clock LPS 1: 49.152 MHz output LPS 0: Clamp to 0 (The clock signal will be output within 25 μsec after change to "0")
LPS	59	I	Link power status input 0: Link power off 1: Link power on (PHY/Link direct connection)
LKON	58	O	Link-on signal output Link-on signal is 6.144 MHz clock output. Please refer to **4.2 Link-on Indication**.
DIRECT	50	I	PHY/Link isolation barrier control input 0: Isolation barrier 1: PHY/Link direct connection

1.3 Control Pins

Name	Pin No.	I/O	Function
PC0	26	I	Power class set input
PC1	27	I	This pin status will be loaded to Pwr_class bit which allocated to PHY register 4H.
PC2	28	I	IEEE1394a-2000 chapter [4.3.4.1]
CMC	30	I	Configuration manager capable setting This pin status will be loaded to Contender bit which allocated to PHY register 4H. 　0: Non contender 　1: Contender
RESETB	55	I	Power-on reset input Connect to GND through a 0.1 μF capacitor. 　0: Reset 　1: Normal
SPD	61	I	Speed select 　0: MAX. S200 　1: MAX. S400

1.4 IC

Name	Pin No.	I/O	Function
IC(AL)	29, 51	-	Internally Connected (Low Clamped) Connect to GND.
IC(DL)	3	-	Internally Connected (Low Clamped) Connect to GND.

1.5 Power Supply Pins

Name	Pin No.	I/O	Function
AV_{DD}	25, 31, 40, 47, 54	-	Analog power
AGND	24, 33, 35, 42, 49, 52, 53	-	Analog GND
DV_{DD}	4, 10, 20, 56, 60	-	Digital V_{DD}
DGND	1, 7, 13, 16, 21, 57, 64	-	Digital GND

1.6 Other Pins

Name	Pin No.	I/O	Function
TpBias0	41	O	Port 0 twisted pair output
TpBias1	48	O	Port 1 twisted pair output
RI1	34	-	Resistor connection pin1 for reference current generator Connect to GND through a 9.1 kΩ resistor.
XI	23	-	Crystal oscillator connection XI
XO	22	-	Crystal oscillator connection XO
TEST	62	-	Test pin Internally connected (Low clamped). Connect to GND.

2. PHY REGISTERS

2.1 Complete Structure for PHY Registers

Figure 2-1. Complete Structure of PHY Registers

	0	1	2	3	4	5	6	7
0000	Physical_ID						R	PS
0001	RHB	IBR	Gap_count					
0010	Extended (7)			Reserved	Total_ports			
0011	Max_speed			Reserved	Delay			
0100	Link_active	Contender	Jitter			Pwr_class		
0101	Watchdog	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110	Reserved							
0111	Page_select			Reserved	Port_select			
1000	Register0 (page_select)							
1001	Register1 (page_select)							
1010	Register2 (page_select)							
1011	Register3 (page_select)							
1100	Register4 (page_select)							
1101	Register5 (page_select)							
1110	Register6 (page_select)							
1111	Register7 (page_select)							

Table 2-1. Bit Field Description (1/3)

Field	Size	R/W	Reset value	Description
Physical_ID	6	R	000000	Physical_ID value selected from Self_ID period.
R	1	R	0	If this bit is 1, the node is root. 1: Root 0: Not root
PS	1	R		Cable power status. 1: Cable power on 0: Cable power off
RHB	1	R/W	0	Root Hold -off bit. If 1, becomes root at the bus reset.
IBR	1	R/W	0	Initiate bus reset. Setting to 1 begins a long bus reset. Long bus reset signal duration: 166 μsec. Returns to 0 at the beginning of bus reset.
Gap_count	6	R/W	111111	Gap count value. It is updated by the changes of transmitting and receiving the PHY configuration packet Tx/Rx. The value is maintained after first bus reset. After the second bus reset it returns to reset value.
Extended	3	R	111	Shows the extended register map.

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Table 2-1. Bit Field Description (2/3)

Field	Size	R/W	Reset value	Description
Total_ports	4	R	0010	Supported port number. 0010: 2 ports
Max_speed	3	R	See Description	Indicate the maximum speed that this node supports. Set variable by SPD pin(61 pin). When SPD = "0" then 001: 98.304 and 196.608 Mbps. When SPD = "1" then 010: 98.304, 196.608 and 393.216 Mbps.
Delay	4	R	0000	Indicate worst case repeating delay time. 144 + (Delay x 20) = 144 nsec

Link_active	1	R/W	1	Link active.
				  1: Enable
				  0: Disable
				The logical AND status of this bit and LPS pin.
				State will be referred to "L bit" of Self-ID Packet#0.

Contender	1	R/W	See Description	Contender.
				"1" indicate this node support bus manager function. This bit will be referred to "C bit" of Self-ID Packet#0.
				The reset data is depending on CMC pin setting.
				CMC pin condition
				  1: Pull up (Contender)
				  0: Pull down (Non Contender)

Jitter	3	R	010	The difference of repeating time (Max.-Min.). (2+1) x 20=60 nsec
Pwr_class	3	R/W	See Description	Power class. Please refer to IEEE1394a-2000 [4.3.4.1]. This bit will be referred to Pwr field of Self-ID Packet#0. The reset data will be determined by PC0-PC2 Pin status.
Watchdog	1	R/W	0	Watchdog Enable. This bit serves two purposes. When set to 1, if any one port does resume, the Port_event bit becomes 1. This function has no effect when SUS/RES(19pin) = "0". To determine whether or not an interrupt condition shall be indicated to the Link. On condition of LPS = 0 and Watchdog = 0, LKON as interrupt of Loop, Pwr_fail, Timeout is not output. This function has effect both when SUS/RES(19pin) = "1" or "0".
ISBR	1	R/W	0	Initiate short (arbitrated) bus reset. Setting to 1 acquires the bus and begins short bus reset. Short bus reset signal output : 1.3 μsec Returns to 0 at the beginning of the bus reset.
Loop	1	R/W	0	Loop detection output. 1: Detection Writing 1 to this bit clears it to 0. Writing 0 has no effect.
Pwr_fail	1	R/W	1	Power cable disconnect detect. It becomes 1 when there is a change from 1 to 0 in the CPS bit. Writing 1 to this bit clears it to 0. Writing 0 has no effect.

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2.2 Port Status Page (Page 000)

Figure 2-2. Port Status Page

	0	1	2	3	4	5	6	7
1000	AStat		BStat		Child	Connected	Bias	Disabled
1001	Negotiated_speed			Int_enable	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 2-2. Bit Field Description

Field	Size	R/W	Reset value	Description
AStat	2	R	XX	A port status value. 00: invalid, 10: "0" 01: "1", 11: "Z"
BStat	2	R	XX	B port status value. 00: invalid, 10: "0" 01: "1", 11: "Z"
Child	1	R		Child node status value. 1: Connected to child node 0: Connected to parent node
Connected	1	R	0	Connection status value. 1: Connected 0: Disconnected
Bias	1	R		Bias voltage status value. 1: Bias voltage 0: No bias voltage
Disabled	1	R/W	See Description	The reset value is set to 0: Enabled.
Negotiated_ speed	3	R		Shows the maximum data transfer rate of the node connected to this port. 000: 100 Mbps 001: 200 Mbps 010: 400 Mbps
Int_enable	1	R/W	0	When set to 1, the Port_event is set to 1 if any of this port's Connected, Bias, Disabled or Fault bits change state. This bit has no effect when SUS/RES(19pin) = "0".
Fault	1	R/W	0	Set to 1 if an error occurs during Suspend/Resume. Writing 1 to this bit clears it to 0. Writing 0 has no effect. This bit has no effect when SUS/RES(19pin) = "0"
Reserved	-	R	000…	Reserved. Read as 0.

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2.3 Vendor ID Page (Page 001)

Figure 2-3. Vendor ID Page

	0	1	2	3	4	5	6	7
1000				Compliance_level				
1001				Reserved				
1010								
1011				Vendor_ID				
1100								
1101								
1110				Product_ID				
1111								
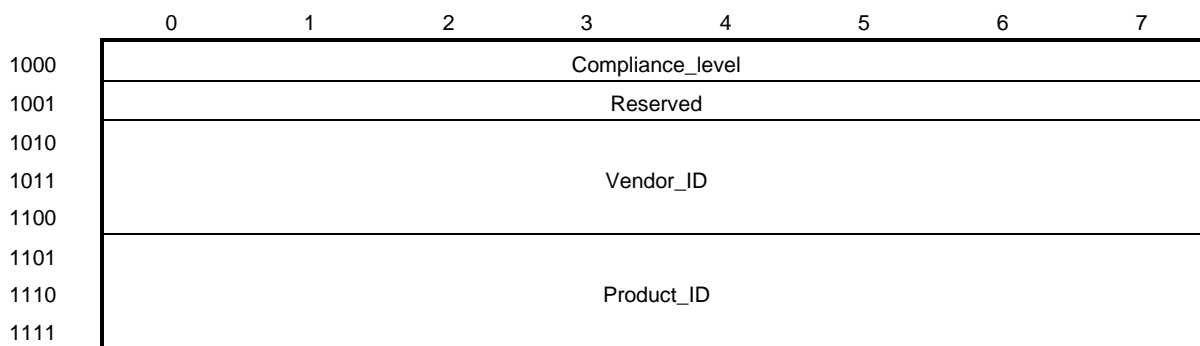
Table 2-3. Bit Field Description

Field	Size	R/W	Reset value	Description
Compliance_level	8	R	00000001	According to IEEE1394a-2000.
Vendor_ID	24	R	00004CH	Company ID Code value, NEC IEEE OUI.
Product_ID	24	R		Product code.
Reserved	-	R	000…	Reserved. Read as 0.

2.4 Vendor Dependent Page (Page 111 : Port_select 0001)
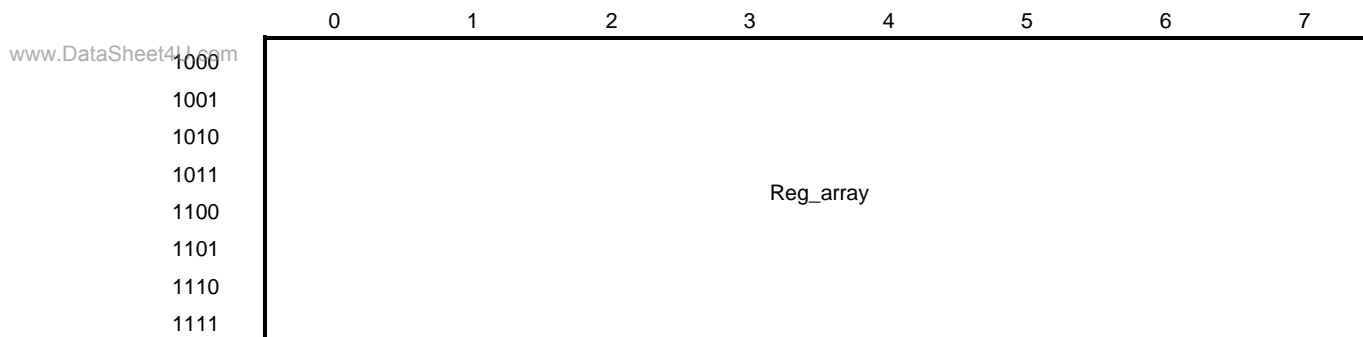
Figure 2-4. Vendor Dependent Page

	0	1	2	3	4	5	6	7
1000								
1001								
1010								
1011								
1100				Reg_array				
1101								
1110								
1111								

Table 2-4. Bit Field Description

Field	Size	R/W	Reset value	Description
Reg_array	64	R/W	0	This register array is possible R/W.

3. INTERNAL FUNCTION

3.1 Link Interface

3.1.1 Connection Method

Figure 3-1. PHY/Link Connection Method
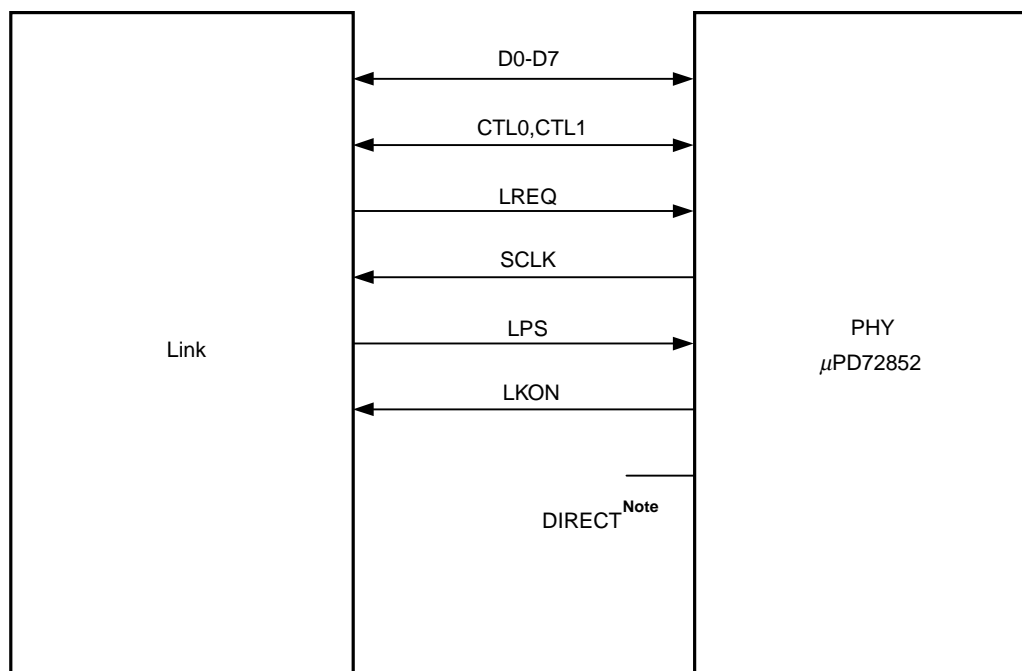
Note   Clamping to V_{DD} provides direct connection to Link.
Clamping to GND connects through isolation barrier to Link.
The isolation barrier connection circuit is described in **3.1.7 Isolation Barrier.**

3.1.2 LPS (Link Power Status)

LPS is a function to monitor the On/Off status of the Link power supply. After 1.2 μsec or more, LPS is Low, the PHY/Link is reset and D and CTL are output Low (when the isolation barrier is Hi-Z). After 2.5 μsec or more, LPS is Low, moreover, the PHY stops the supply of SCLK and SCLK outputs Low (when the isolation barrier is Hi-Z).

3.1.3 LREQ, CTL0, CTL1 and D0-D7 Pins

LREQ   : Indicates that a request is received from Link.

CTL0, CTL1 : Bi-directional pin which controls the functions between the PHY/Link interface.

D0-D7   : Bi-directional pin which controls the data Transfer/Receive status signal, and the speed code Transfer/Receive status signal.

3.1.4 SCLK

49.152 MHz clock supplied by PHY for the PHY/Link interface synchronization.

3.1.5 LKON

When the Link power is off, it outputs a clock of 6.144 MHz. LKON outputs under the following conditions: LPS is Low and the internal PHY register of the Link_active bit is 0.

- Link-on packet is received.
- Any bit of Loop, Pwr_fail, Timeout or Port_event is the PHY internal register becomes 1, and moreover either LPS or Link_active bit is 0.

When LPS is asserted, LKON returns to Low.

3.1.6 DIRECT

Set DIRECT to Low for using the isolation barrier.

3.1.7 Isolation Barrier

The IEEE1394 cable holds signals for Data/Strobe in addition to power and ground.

When the ground potential is different between connecting devices, the DC and AC current flows through the ground line in the cable and there is a possibility of malfunction due to ground difference between the two PHY.

The μPD72852 uses the isolation barrier to couple the AC between the PHY/Link interface to overcome the ground difference problem. Connecting the DIRECT pin to Low enables the digital differential circuit of the μPD72852. The differential circuit propagates only the change in the signal; the interface will be driven only during transitions High → Low or Low → High. The interface will assume the high impedance state when there is no signal change. The μPD72852 uses Schmitt trigger input buffers for D, CTL, LREQ and LPS pins to prevent noise when the bus assumes a high impedance state.

The digital differential circuit and the Schmitt trigger input buffers are needed on the Link layer controller LSI to implement the isolation barrier.
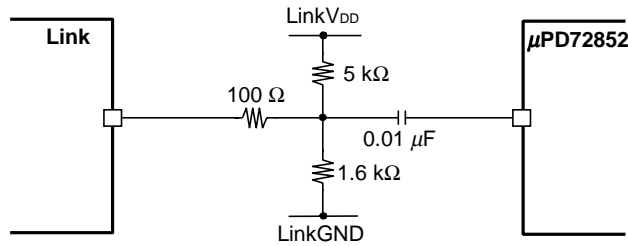
Figure 3-2. Waveforms of the Isolation Barrier

Isolation Barrier not used

0 1 1 0 0 0 1 0 0

Using Isolation Barrier
(Digital differential circuit)

0 1 Z 0 Z Z 1 0 Z
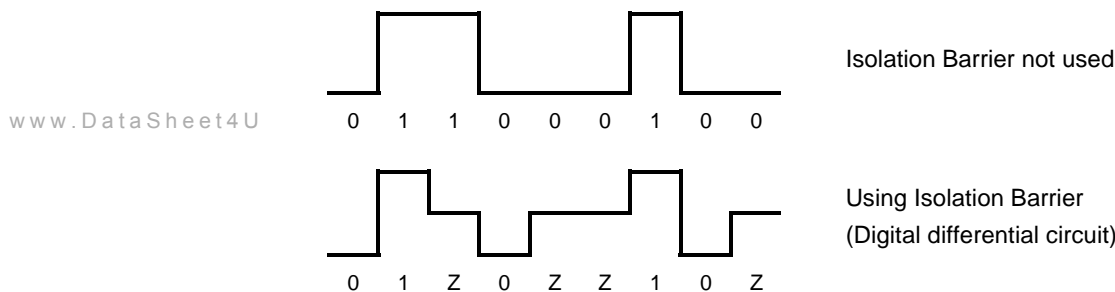
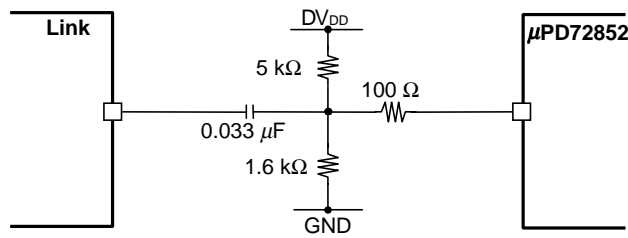★ **Figure 3-3. Isolation Barrier Circuits**

(a) CTL0, CTL1, D0-Dn Isolation Barrier Circuit
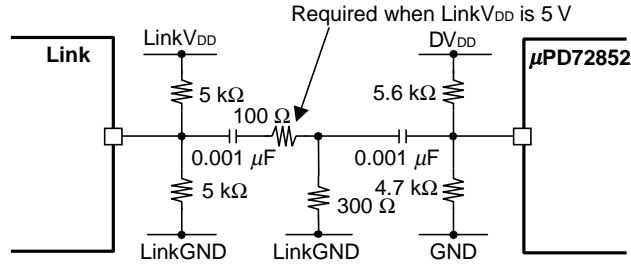
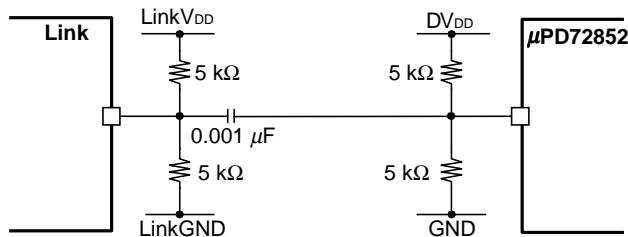**(b) Link-on Isolation Barrier Circuit**

(c) LPS Isolation Barrier Circuit

(d) LREQ Isolation Barrier Circuit

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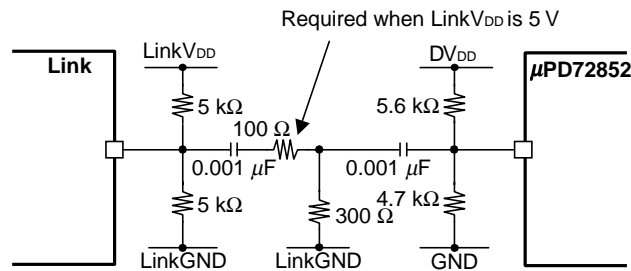
(e) SCLK Isolation Barrier Circuit
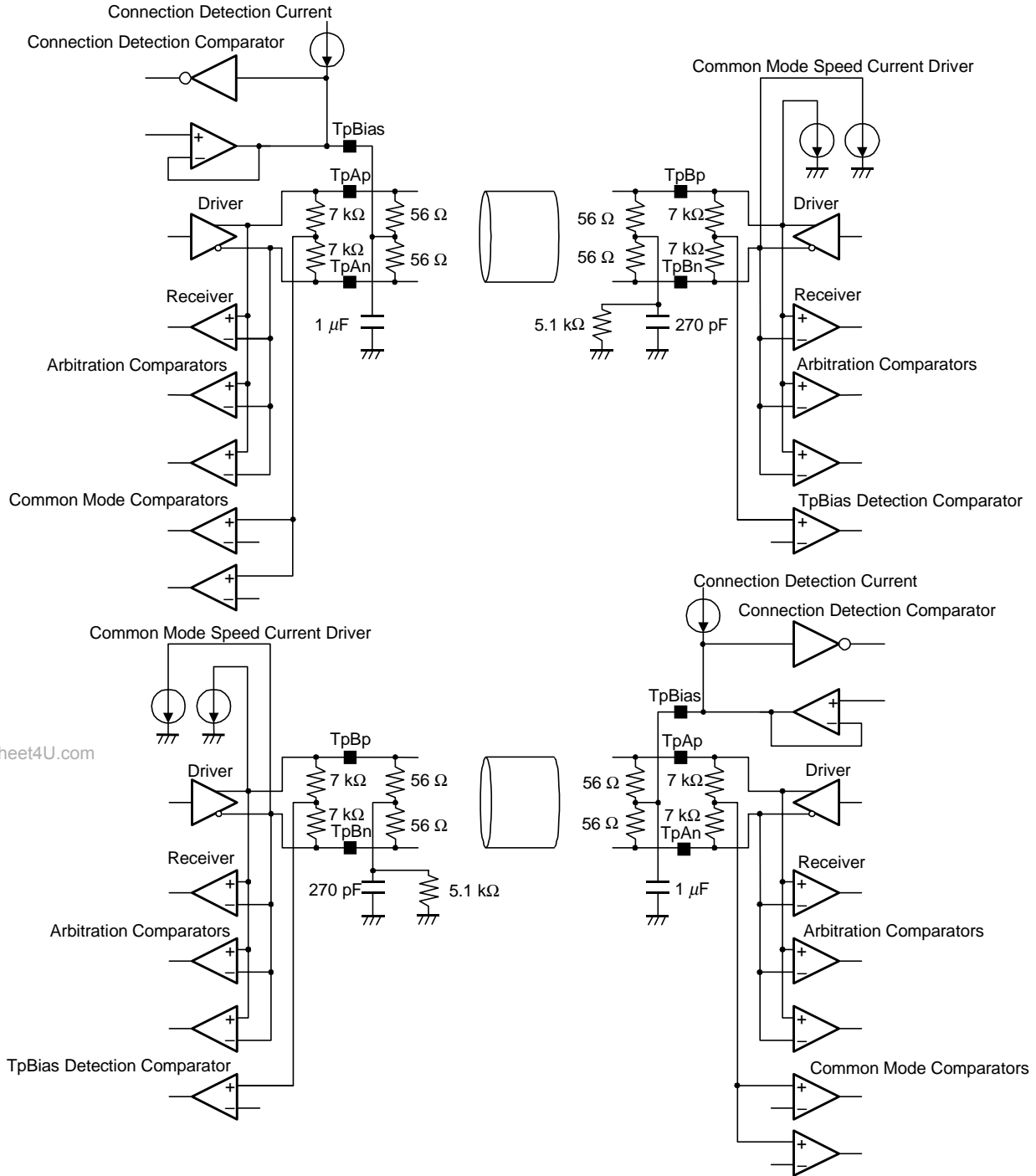

The Operating range of the power supply voltage is between 3.0 V and 3.45 V.

Please refer to **IEEE1394a-2000 [5A.8.4]**.

3.2 Cable Interface

3.2.1 Connections

Figure 3-4. Cable Interface

3.2.2 Cable Interface Circuit

Each port is configured with two twisted-pairs of TpA and TpB.

TpA and TpB are used to monitor the state of the Transmit/Receive line, control signals, data and cables.

During transmission to the IEEE1394 bus, the Data/Strobe signal received from the Link layer controller is encoded, converted from parallel to serial and transmitted.

While receiving from the IEEE1394 bus, the Data/Strobe signal from TpA, TpB is converted from serial to parallel after synchronization by SCLK, then transmitted to the Link layer controller in 2/4/8 bits according to the data rate of 100/200/400 Mbps.

The bus arbitration for TpA and TpB and the state of the line are monitored by the built-in comparator. The state of the IEEE1394 bus is transmitted to the state machine in the LSI.

3.2.3 Unused Ports

TpAp, TpAn : Not connected

TpBp, TpBn : GND

TpBias   : Not connected

3.2.4 CPS

Connect an external resistor of 390 kΩ between the CPS pin and the power cable, and an external resistor of 100 kΩ between the CPS pin and GND to monitor the power of the power cable.

If the cable power falls under 7.5 V there is an indication to the Link layer controller that the power has failed.

3.3 Suspend/Resume

3.3.1 Suspend/Resume On Mode (SUS/RES = "H")

There are two ways of transition from the active status to the suspended status.

One is when the receipt of a remote command packet that sets the initiate suspend command. After that, the PHY transmits a remote confirmation packet with the ok bit set, subsequently signals TX_SUSPEND to the connected peer PHY with the port which specified by the port field in the remote command packet, and then the PHY port transitions to the suspended state.

www.DataSheet4U.com The other is when the receipt of a RX_SUSPEND or RX_DISABLE_NOTIFY signal. When the port observes RX_SUSPEND, it transmits TX_SUSPEND to the active ports.

The TX_SUSPEND transmitted propagates until it reaches a leaf node. The PHY port transitions to the suspended state. The propagation of the suspended domain may be blocked by a PHY compliant with IEEE1394a-2000, a disabled or a suspended port.

Any one of a number of reasons may cause a suspended port to attempt to resume normal operations:

• Bias is detected and there is no fault condition;

• A resume packet is received or transmitted by the PHY;

• A remote command packet that sets the resume port command is received; or

• Either port of a node without active ports detects bias.

3.3.2 Suspend/Resume Off Mode (SUS/RES = "L")

• Remote command packet is ignored.

• Resume packet is ignored.

• Disabled, Int_enable and resume_int bits in PHY register are ignored.

• Responses to Remote access packet.

• Detects the connection of the port in TpBias.

• Output the 1.85 V voltage of the port in TpBias.

3.4 PLL and Crystal Oscillation Circuit

3.4.1 Crystal Oscillation Circuit
To supply the clock of 24.576 MHz ± 100 ppm, use an external capacitor of 10 pF and a crystal of 50 ppm.

3.4.2 PLL
The crystal oscillator multiplies the 24.576 MHz frequency by 16 (393.216 MHz).

3.5 CMC
CMC shows the bus manager function which corresponds to the c bit of the Self_ID packet and the Contender bit in the PHY register when the input is High.

The value of CMC can be changed with software through the Link layer; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ, based on the device's specification.

3.6 PC0-PC2
The PC0-PC2 pin corresponds to the power field of the Self_ID packet and Pwr_class in the PHY register. Refer to Section 4.3.4.1 of the IEEE1394a-2000 specification for information regarding the Pwr_class. The value of Pwr can be changed with software through the Link layer controller; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ based on the application.

3.7 RESETB
Connect an external capacitor of 0.1 μF between the RESETB pin and GND. If the voltage drops below 0 V, a reset pulse is generated. All of the circuits are initialized, including the contents of the PHY register.

3.8 RI1
Connect an external resistor of 9.1 kΩ between the RI1 pin and GND to limit the LSI's current.

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4. PHY/LINK INTERFACE

4.1 Initialization of Link Power Status (LPS) and PHY/Link Interface

The LPS pin monitors the On/Off status of the Link power state. This pin is used during the PHY/Link interface Enable/Disable (initialization).

Reset

When the LPS input pin is Low for TLPS_RESET:
• CTL0, CTL1 and D0-D7 output Low (When the isolation barrier is Hi-Z).
• SCLK continuously supplies the clock signal to the Link.

Disable

When the LPS input pin is Low for TLPS_DISABLE:
• CTL0, CTL1, D0-D7 continue to output Low as TLPS_RESET has already occurred (When the isolation barrier is Hi-Z).
• SCLK to Link stops and it outputs Low (When the isolation barrier is Hi-Z).

Table 4-1. LPS Timing Parameters

Parameter	Symbol	MIN.	MAX.	Unit
LPS = Low propagation delay (with isolation barrier)	t_{LPSL}	0.09	1.00	μs
LPS = High propagation delay (with isolation barrier)	t_{LPSH}	0.09	1.00	μs
Reset active	t_{LPS_RESET}	1.2	2.75	μs
Disable active	$t_{LPS\_DISABLE}$	25	30	μs
Setup time when using isolation barrier	$t_{RESTORE}$	15	20	μs

Figure 4-1. LPS Waveform when Connected to Isolation Barrier

t_{LPSH} t_{LPSL}
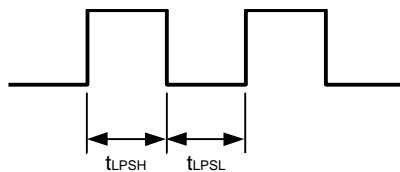
Figure 4-2. PHY/Link Interface Reset and Disable

(a) Reset

(b) Disable
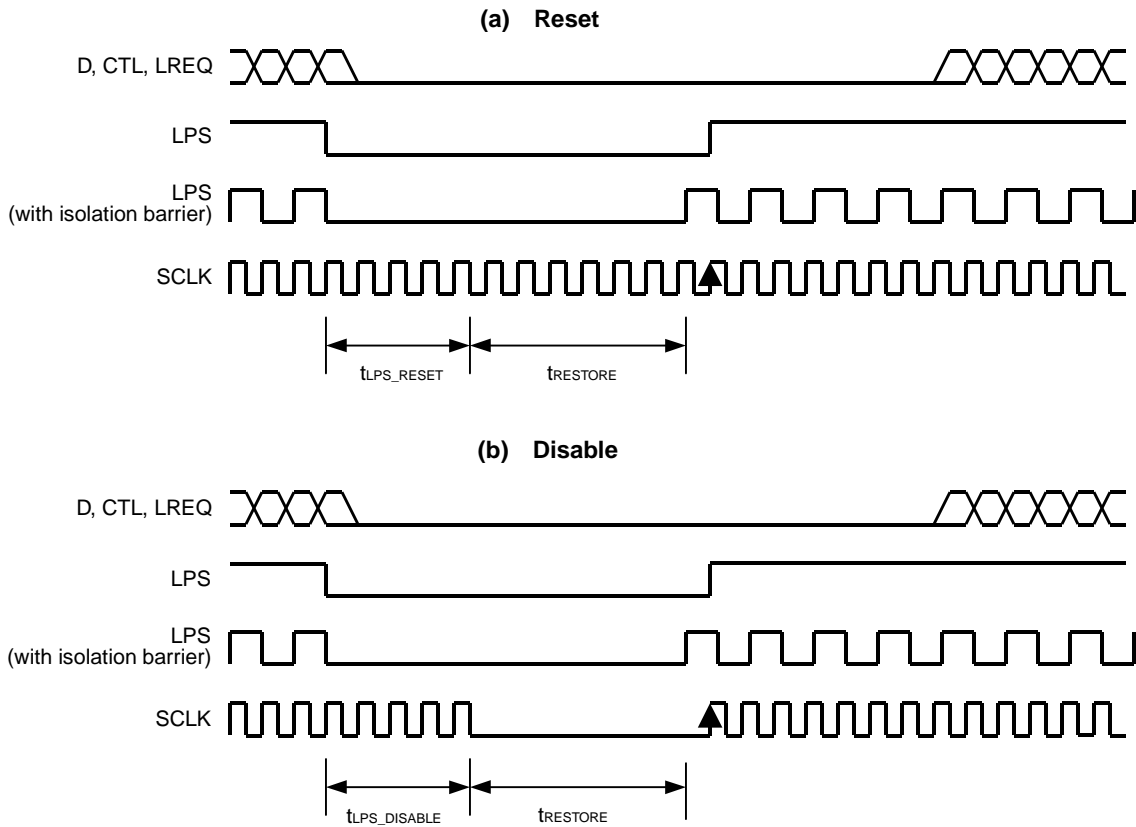
4.2 Link-on Indication

When the power supply of Link is off (LPS is Low and the internal PHY register Link_active bit is 0), the pin LKON outputs a clock of 6.144 MHz according to the following conditions:

• Link-on packet is received.

• When any bit of the µPD72852 PHY register's loop, Pwr_fail, Timeout or Port_event becomes 1, and either LPS or the Link_active bit is 0.

Table 4-2. Link-on Timing

Parameter	MIN.	MAX.	Unit
Frequency	4	8	MHz
Duty Cycle	40	60	%
Propagation delay before the Link becomes active (LPS is asserted and the Link_active bit in the PHY register is 1).		500	ns

• If LPS or the Link_active bit is 0, the Link is considered inactive.

When the Link is inactive and any of Loop, Pwr_fail, Timeout, Port_event becomes 1, then Link-on is asserted High.

• When the Link is active (both LPS and Link_active become 1) and Loop, Pwr_fail, Timeout and Port_event become 1, Status transfer is sent on the PHY/Link interface.

• The µPD72852 activates the PHY/Link interface when LPS is 1, regardless of the value of the Link active bit.

4.3 PHY/Link Interface Operation (CTL0, CTL1, LREQ, D0-D7)

The PHY/Link Interface consists of the following operations:

• Status transfer to the Link layer controller by CTL

• Transmit packet

• Receive packet

• Request from the Link layer controller by LREQ

4.3.1 CTL0, CTL1

CTL0, CTL1 controls the PHY/Link interface as shown in the Table 4-3.

Table 4-3. CTL Controls PHY

CTL0,CTL1	Type	Content
00	Idle	PHY is in idle function
01	Status	PHY transmitting status information to Link
10	Receive	PHY receiving data from the Link
11	Grant	PHY allows Link to transmit data

This is the operation by which, after Grant, the Link obtains the right to control the interface.

Table 4-4. CTL Controls Link

CTL0,CTL1	Type	Content
00	Idle	Link completes the packet transmission and releases the PHY/Link interface.
01	Hold	1) Link transmits Hold until the data is ready for transmission. 2) Link transmits the interface connect packet.
10	Transmit	Link transmits the data to PHY.
11	-	Not used.

4.3.2 LREQ

Access to the PHY register and the bus is controlled from the Link layer controller through the LREQ pin of PHY.

Figure 4-3. LREQ and CTL Timing
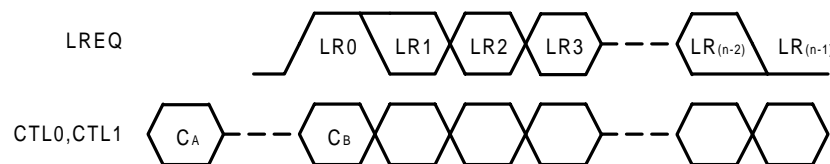
C_A : CTL before generation of LREQ
C_B : CTL during LREQ execution

(1) LREQ format

• Bus Request

Table 4-5. Bus Request Format

Bit	Type	Content
0	start	Signal that starts a request : 1

1-3	request	Bus request type:
		    000: ImmReq acknowledge packet transmit
		    001: IsoReq isochronous packet transmit
		    010: PriReq cycle start packet transmit
		    011: FairReq asynchronous packet transmit

4-6	speed	Transmit speed:
		    000: 100 Mbps
		    010: 200 Mbps
		    100: 400 Mbps
		    other: reserved

7	stop	End request signal : 0 (optional)

• PHY Register Read Request

Table 4-6. Read Request Register Format

Bit	Type	Content
0	start	Signal that starts a request : 1
1-3	request	Read Request. 100 : ReadReq
4-7	access address	PHY register address.
8	stop	End request signal : 0

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• PHY Register Write Request

Table 4-7. Write Request Register Format

Bit	Type	Content
0	start	Signal that starts a request : 1
1-3	request	Write Request. 101 : WriteReq
4-7	access address	PHY register address.
8-15	write data	Write data.
16	stop	End request signal : 0

• **Acceleration Controller**

Table 4-8. Acceleration Controller Request Format

Bit	Type	Content
0	start	Signal that starts a request : 1
1-3	request	110 : Acc Ctrl accelerate controller
4	access address	0: Accelerate disable 1: Accelerate enable
5	stop	End request signal : 0

Table 4-9. Request Type List

Bit	Type	Content
000	ImmReq	Used to acknowledge packet transmit. When Idle is detected, PHY immediately controls the bus.
001	IsoReq	Used to transmit isochronous packet. PHY does arbitration after isochronous gap is detected and acquires the bus.
010	PriReq	Used for Cycle master request.
011	FairReq	Fair request.
100	RdReg	PHY register read request.
101	WrReg	PHY register write request.
110	AccCtrl	Disable/enable of arbitration acceleration.
111	-	Unused.

For the Link to execute Priority request and Fair, start the request using LREQ when CTL0, CTL1 becomes idle, after one clock. When request is acknowledged, the μPD72852 outputs Grant to CTL0, CTL1.

The Link of cycle master uses PriReq to transmit the cycle start packet. IsoReq transmits the isochronous packet.

IsoReq becomes effective only as follows:

• The transmission of the cycle start packet is performed on the same isochronous period as Receive. (The period until the subaction gap is detected.)

• During isochronous packet Transmit or Receive.

The μPD72852 cancels IsoReq with the subaction gap detection or bus reset. To meet the timing, do not issue the IsoReq to PHY when CRC operation is performed.

The Link cancel method is described later.

After the packet is received, Link issues ImmReq as the acknowledge packet transmission. The purpose is to prevent another node from detecting subaction gap as ACK_RESPONSE_TIME. The μPD72852 acquires the bus after packet receive and returns Grant to CTL0, CTL1. When CRC fails, before Link detects Grant, assert 3 Idle cycles to CTL0, CTL1.

When the bus reset is generated, the unprocessed requests are canceled.

The μPD72852 updates the data of the Write request register and the contents of the Read register are changed. The contents of the register of the specified address are output to the Link as a status transfer in the Read request register, When the status transmission is interrupted by transmitting/receiving packets, the status transmission will re-start from the first bit after completing the transmit/receive of the packets.

The bus request (ImmReq, IsoReq, PriReg, FairReq) is completed (in case of ImmReq, IsoReq, when the subaction gap is detected) when the packet is transmitted or canceled by canceling the bus request.

(2) LREQ rules
The Link request and the status of the serial bus are asynchronous; the bus request can be canceled by the status of the serial bus.
The following rules apply to a request by LREQ:
• Link cannot issue a bus request (ImmReq, IsoReq, PriReq, FairReq) if Grant is given to an LREQ request or until the Link's request is canceled. The request can be canceled by the μPD72852 if it detects subaction gap at ImmReq, IsoReq.
• Do not issue a RdReg or WrReg request when the status transmission is not completed by the Read request register.
• All of the bus requests (ImmReq, IsoReq, PriReq, FairReq) are canceled by a bus reset.

In addition, there is a limitation in the request of LREQ according to the state of CTL as shown in Table 4-10.

Table 4-10. Rules for Other Requests

Request	State of CTL in C$_A$ to which LREQ is allowed when PHY drives CTL	LREQ issues permission when Link drives CTL	Note
Fair, Priority	Idle, Status	wrong	Fair, Priority request cannot be issued until the unprocessed bus request is completed.
Immediate	Receive, Idle	wrong	Link issues the request after completing the decoding of Destination_ID, when the acknowledge packet is ready. After the packet is received, it is necessary to transmit the first bit of the request within four cycles.
Isochronous	any	correct	If the isochronous packet transmission is prepared for the isochronous period, it is issued. Do not issue the request to transmit the isochronous packet appending to the currently transmitted isochronous packet (Using Hold).
Register Read Register Write	any	correct	Do not issue this request if the unprocessed Read request has not been completed.
AccCtrl	any	correct	To set acceleration bit 0: When the isochronous period starts, if the Enab_accel bit is one, Cycle slave should adjust accelerate bit to 0. To set acceleration bit 1: Do not set the cycle master. It is issued when the isochronous period ends.

Table 4-11. PHY Operation Before LREQ Request to the CTL Function Changes

Request	State of CTL in C$_B$ after LREQ was issued	Operation of the PHY
Fair, Priority	Receive	• Hold the request if the acceleration of arbitration packet transmitted with enable is 8 bits (ACK). Except for 8 bits, the requests are ignored. • Ignore the request when the acceleration of arbitration is disabled.
	Grant	Arbitration Won.
	Idle, Status	Excluding when the bus reset is generated, Hold the requests.
Immediate	Grant	
	Receive	The packet is being transmitted to Link. Request Hold.
	Idle, Status	Excluding when the bus reset is generated, hold the request.
Isochronous	Transmit Idle (driven by Link)	Request Hold.
	Grant	Arbitration Won.
	Receive	Request Hold.
	Status	Request is ignored when sub-action gap is detected.
	Idle	
Register Read	Any (driven by Link)	
	Grant	Request Hold.
	Receive	Request Hold.
	Status	Hold the request until the corresponding register value is returned.
	Idle	
Register Write, Acceleration control	Any	Request is completed.

4.3.3 SCLK Timing

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Table 4-12. SCLK Timing

Timing Constant	Comment	MIN.	MAX.	Unit
BUS_TO_LINK_DELAY	Period from receiving RX_DATA_PREFIX until Receive to CTL is output.	2	9	SCLK cycle
DATA_PREFIX_TO_GRANT	Period when the Grant is output to CTL after TX_DATA_PREFIX is output to a port.		25	SCLK cycle
LINK_TO_BUS_DELAY	Period when TX_DATA_END is output to all ports after transmitting the packet by Link after idle was asserted to CTL.	2	5	SCLK cycle
MAX_HOLD	Maximum period when Hold can be asserted by Link to confirm Grant.		47	SCLK cycle

4.4 Acceleration Control

Enable of ack-acceleration and fly-by on the same isochronous period may create a problem. The isochronous cycle may extend unintentionally when transmitting the asynchronous packet by a node using ack-acceleration and fly-by.

To avoid this problem, Link should control Disable/Enable of these enhancements (ack-Acceleration, fly-by), by Acceleration Control requests. Cycle master cannot issue the Acceleration Control request.

The enhancements should not be used from the generation of the local cycle synchronization event to the confirmation of cycle start. In this period, all Links except for Cycle Master use Acceleration Control as follows:

• Do not issue Fair nor Priority request to Link after generating local cycle synchronization, if the Acceleration Control request's Accelerate bit is not set to 0.

• Link must not use Hold when transmitting continuous primary asynchronous packet after the Acknowledge packet, except after ack_pending to complete the split transaction.

• Ending the Link during the isochronous period issues the acceleration control request to set the Accelerate bit to 1, enabling these enhancements.

The μPD72852 does not require setting the Acceleration Control during isochronous transmit to enable the isochronous request fly-by acceleration.

It is not necessary to issue Acceleration Control request when the cycle master is absent from the serial bus. These enhancements are enabled if the Enab_accel bit in the PHY register is set. The μPD72852 supports Variable Acceleration controlled by the Acceleration Control during power-on reset.

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Transmit Status content as shown.

4.6 Transmit

The μPD72852 arbitrates the serial bus using Link's LREQ.

• When the μPD72852 acquires the bus, a Grant period of 1 SCLK is executed to CTL0, CTL1. After that, an Idle period of 1 SCLK cycle is executed.

• Link controls the interface executing Idle, Hold of Transmit to CTL0, CTL1 after 1 SCLK cycle when Grant from PHY is detected.

• Before asserting Hold and Transmit, assert 1 Idle cycle. Do not execute Idle for 2 or more cycles.

• If the packet transmit is not ready, the Hold period can be extended up to MAX_HOLD.

• The μPD72852 outputs DATA_PREFIX to the serial bus while Hold is being asserted to CTL.

• When the packet transmit is ready, Link outputs the first bit of the packet and Transmit is asserted to CTL at the same time.

• After transmitting the last bit of the packet, Link outputs for Idle or Hold to CTL for 1 cycle. After that, it outputs Idle for 1 cycle.
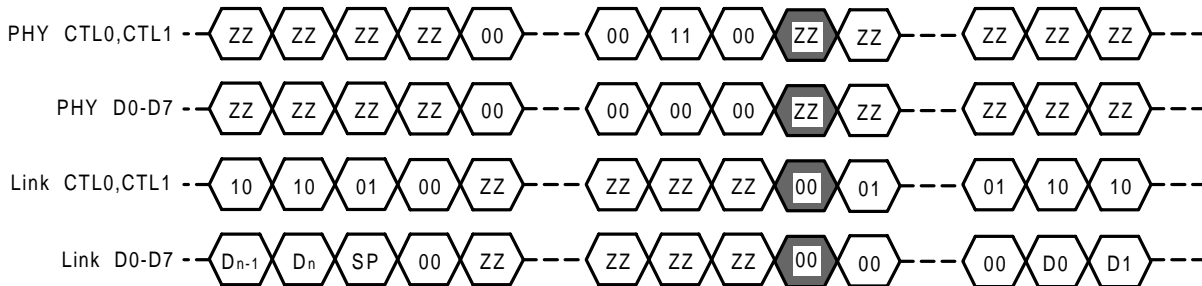
When PHY/Link releases the bus, output Low to CTL and D0-D7 within 1 cycle.

Figure 4-5. Transmit Timing

(a) Single Packet
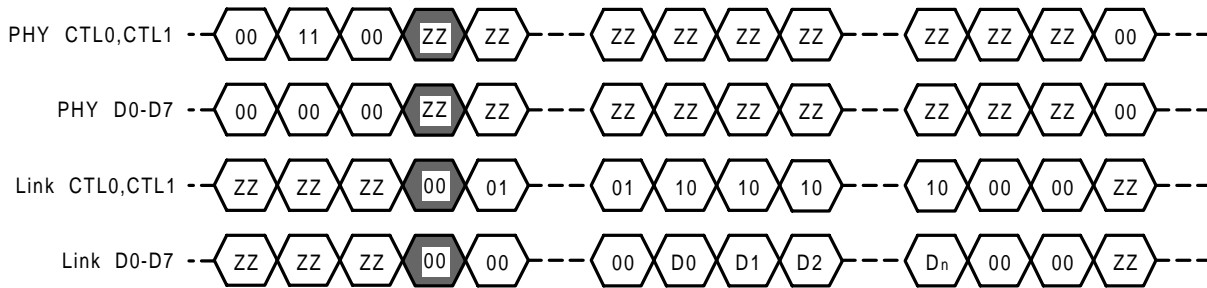
(b) Concatenated Packet

Note In case of packet transmission after Grant, before actual transmission, Hold does not need to be asserted.

Link can transmit continuous packets without releasing the bus.

• Hold is asserted to CTL. This function is used when the Link transmits continuous packets after acknowledge and isochronous packets. Link outputs the transfer rate signal of the following packet to D0-D7 and asserts Hold simultaneously.

• After Hold is detected by MIN_PACKET_SEPARATION, the μPD72852 outputs Grant to CTL.

• Link controls the interface by generating Idle, Hold or Transmit to CTL0, CTL1, after 1 SCLK cycle when Grant from PHY is detected.
• Assert 1 Idle cycle before asserting Hold and Transmit (do not output 2 or more Idle cycles). When the packet transmission is not ready, assert Hold. The Hold output period after Grant is detected should not exceed the period provided by MAX_HOLD.

The following limitations exist though Link can transmit the concatenated packet with a different transfer rate. Link cannot transmit other than S100 connecting packets after S100 (concatenated) packets have been transmitted. A new request to transmit must be issued in order to transmit S100 packets at a transfer rate of S200 or more.

If the Enab_Multi bit in the PHY register is 0, the μPD72852 assumes the same speed as the first packet, for all of the concatenated packets.

At the end of packet transmission, Link asserts Idle to CTL for a period of 2 cycles.

After sampling Idle from Link, the μPD72852 asserts Idle to CTL for a period of 1 cycle.
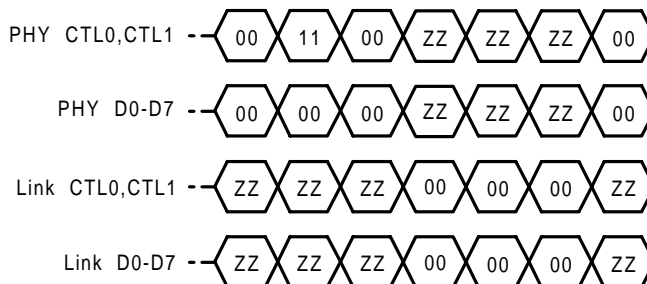
4.7 Cancel

This section describes how Link operates, when after the bus has been acquired by the request of LREQ, there is no data transmission. In this case, a Null packet with no data is transmitted to the serial bus (DATA_PREFIX →
DATA_END).

Following are two method for canceling the Link:

1. As explained in Section 4.6, the Link outputs Idle or Hold, then outputs Transmit to CTL after confirming Grant. Here, the Link asserts Idle for two cycles to CTL, then switches to high impedance.
   The μPD72852 confirms Cancel at the second Idle cycle. To prevent the bus from switching to high impedance, a third Idle cycle is needed.
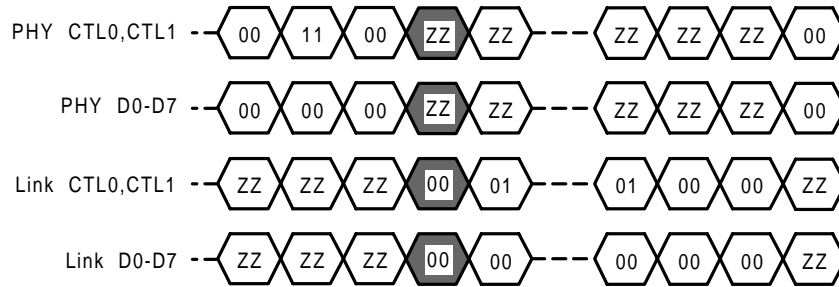
Figure 4-6. Link Cancel Timing (After Grant)

2. To cancel after asserting Hold, assert Idle between two cycles; it switches to high impedance. This method cancels the packet transmission connection (concatenated) after Grant is received. The μPD72852 cancels with the next Idle cycle of Hold. To prevent CTL from switching to high impedance, assert a second Idle cycle.

Figure 4-7. Link Cancel Timing (After Hold)

PHY CTL0,CTL1 — 00 / 11 / 00 / **ZZ** / ZZ — — — ZZ / ZZ / ZZ / 00

PHY D0-D7 — 00 / 00 / 00 / **ZZ** / ZZ — — — ZZ / ZZ / ZZ / 00

Link CTL0,CTL1 — ZZ / ZZ / ZZ / **00** / 01 — — — 01 / 00 / 00 / ZZ

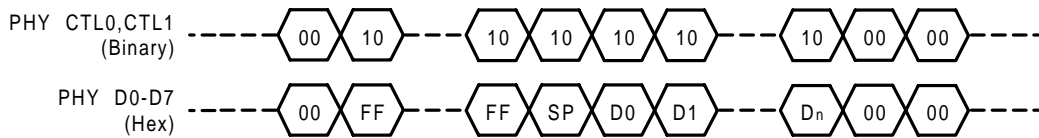Link D0-D7 — ZZ / ZZ / ZZ / **00** / 00 — — — 00 / 00 / 00 / ZZ

4.8 Receive

This section shows the operation when the packet is received from the serial bus.

• When the μPD72852 detects DATA_PREFIX on the serial bus, it asserts receive to CTL and all of the D pins assume the logic value of 1.

• The μPD72852 shows the speed code of the transfer rate ahead of the packet using bits D0-D7. Transmitting the speed code with the speed signal is the protocol of the PHY/Link interface. The speed code is not included in the CRC calculation.

• The μPD72852 continues to assert Receive to CTL until the packet is finally transmitted.

• Idle is asserted to CTL, indicating completion of the packet transmission.

Figure 4-8. Receive Timing

PHY CTL0,CTL1 (Binary) — — — 00 / 10 — — — 10 / 10 / 10 / 10 — — — 10 / 00 / 00 — — —

PHY D0-D7 (Hex) — — — 00 / FF — — — FF / SP / D0 / D1 — — — D_n / 00 / 00 — — —

The packet transfer rate of the serial bus depends on the topology of the bus. The μPD72852 checks if the node can receive at the faster transfer rate. At this time, DATA_PREFIX → DATA_END is transmitted to the μPD72852.

www.DataSheet4U.com After DATA_PREFIX is transmitted to the Link, Receive from the serial bus is completed, asserting Idle.

Table 4-14 shows the speed code encoding.

Table 4-14. Speed Encoding

D0-D7		Data rate
Transmitted	Observed	
00000000	00xxxxxx	S100
01000000	0100xxxx	S200
01010000	01010000	S400
11111111	11xxxxxx	Data Prefix

5. CABLE PHY PACKET

The node on the serial bus transmits and receives the PHY packet to control the bus.

The PHY packet is composed of 2 quadlets (64-bit); the second quadlet (32-bit) contains the inverse value of the first quadlet.

The PHY packet is transmitted at a transfer rate of S100. All of the PHY packets received from the serial bus are transmitted to the Link.

Though the PHY packet from the μPD72852 is transmitted to the Link, the PHY packet which was transmitted from the Link of the node is not transmitted to the Link.

There are four types of PHY packets, as follows:

• Self_ID packet
• Link-on packet
• PHY configuration packet
• Extended PHY packet

The Self_ID packet transmitted automatically by the μPD72852 is also transmitted to the Link of a local node.

The μPD72852 PHY packet Receive from the serial bus operates similar to the PHY packet transmitted by the Link (when the packet transmission to the Link is executed).

5.1 Self_ID Packet

During the Self_ID phase of the initialization or when the Ping packet responds, the μPD72852 transmits the Self_ID packet.
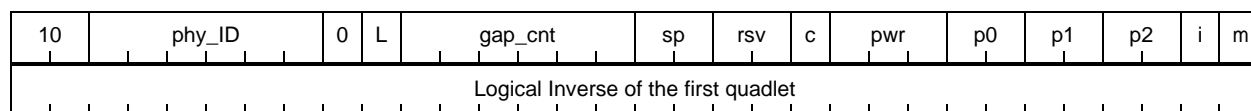
Figure 5-1. Self_ID Packet Format

10	phy_ID	0	L	gap_cnt	sp	rsv	c	pwr	p0	p1	p2	i	m
Logical Inverse of the first quadlet													

Table 5-1. Self_ID Packet

Field	Description
phy_ID	Physical ID of the node.
L	Logical product of Link_active and LPS in the PHY register.
gap_cnt	Gap_count value in the PHY register.
sp	Physpeed 10 (corresponds to 98.304, 196.608, 393.216 Mbps).
c	C bit values in the PHY register.
pwr	pwr value in the PHY register. 000: The node does not need the power supply. No power repeat. 001: Obtains power supply for the node. Can supply 15W or more. 010: Obtains power supply for the node. Can supply 30W or more. 011: Obtains power supply for the node. Can supply 45W or more. 100: The node consumes 3W maximum power. 110: The node consumes 3W maximum power. At least 3W are necessary to enable Link. 111: The node consumes 3W maximum power. At least 7W are necessary to enable Link.
i	It shows that the node issued Bus Reset and the bus was reset.
m	Read as 0.
rsv	Read as 00.

5.2 Link-on Packet

The μPD72852 outputs the Link-on signal of 6.144 MHz from the pin LKON when receiving the Link-on packet.

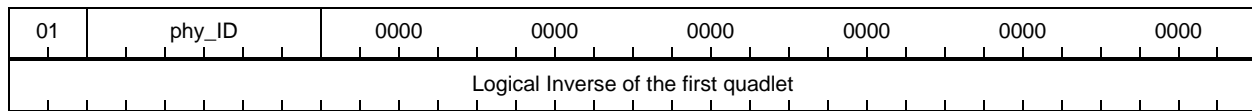**Figure 5-2. Link-on Packet Format**

01	phy_ID	0000	0000	0000	0000	0000	0000
Logical Inverse of the first quadlet							

Table 5-2. Link-on Packet

Field	Description
phy_ID	Physical_ID of the destination of the Link-on packet

5.3 PHY Configuration Packet

Use the PHY configuration packet to set the gap count for the bus.

Figure 5-3. PHY Configuration Packet Format

00	root_ID	R	T	gap_cnt	0000	0000	0000	0000
Logical Inverse of the first quadlet								
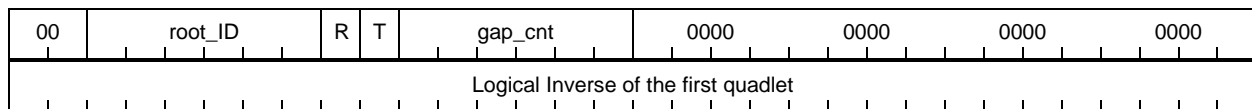
Table 5-3. PHY Configuration Packet

Field	Description
root_ID	Sets the Physical_ID node as root contender (for the next reset).
R	When this bit is set to 1 and the Phyisical_ID of the node corresponds to the rootID of this packet, the μPD72852 sets the force_root bit. The force_root bit is cleared if there is discrepancy.
T	If this bit is 1, the gap_cnt value of this packet is used as the gap_count value. The gap_count value must not be cleared by the following bus reset, set the gap_count_reset_disable flag in the μPD72852 to TRUE.
gap_cnt	When this packet is received, the gap count is set to this value. While it remains effective for the next bus reset, it will be cleared by the second bus reset to 3FH.

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Remark Applying 0 to both R,T, regards the following packets as extended PHY packets, the PHY configuration is not recognized.

5.4 Extended PHY Packet

An extended PHY packet is defined when both the R (in the PHY configuration packet) and T bits are transmitted as 0. The extended PHY packet does not influence the force_root_bit and the gap_count bit on any node.

Following are the types of extended PHY packets:

• Ping packet
• Remote access packet
• Remote reply packet
• Remote command packet
• Remote confirmation packet
• Resume packet

5.4.1 Ping Packet

When the μPD72852 receives the Ping packet, it will transmit the Self_ID packet within the RESPONSE_TIME.
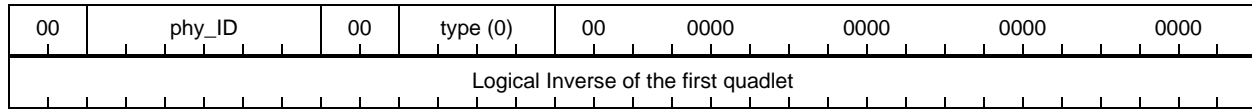
Figure 5-4. Ping Packet Format

00	phy_ID	00	type (0)	00	0000	0000	0000	0000
Logical Inverse of the first quadlet								

Table 5-4. Ping Packet

Field	Description
phy_ID	Physical ID of the destination node of the Ping packet
type	Indicates that there is a Ping packet with a value of 0

5.4.2 Remote Access Packet

The Remote access packet reads information in the PHY register of another node. The PHY specified by the Remote access packet transmits the value in the register using the Remote Reply packet.

Figure 5-5. Remote Access Packet Format

00	phy_ID	00	type	page	port	reg	reserved
Logical Inverse of the first quadlet							
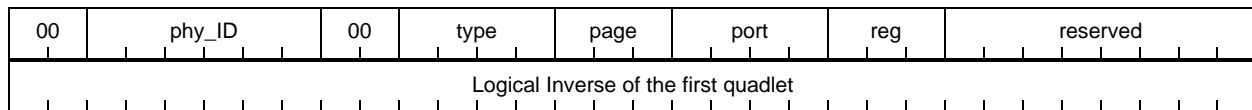
Table 5-5. Remote Access Packet

Field	Description
phy_ID	Physical ID of the destination node of the Remote access packet
type	1 = read register (base register), 5 = read register (page register)
page	Specifies the page of the PHY register
port	Specifies the register of each port in the PHY register
reg	Specifies the address when reading the base register. In case of the Page and port registers, specifies the address with 1000+reg.

5.4.3 Remote Reply Packet

The *µ*PD72852 transmits the value in the register by using the Remote reply packet as a response to the Remote access packet.
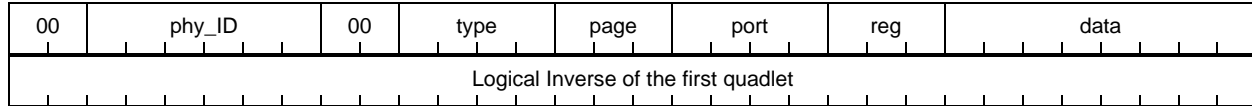
Figure 5-6. Remote Reply Packet Format

00	phy_ID	00	type	page	port	reg	data
Logical Inverse of the first quadlet							

Table 5-6. Remote Reply Packet

Field	Description
phy_ID	Physical ID of the node (Node's original packet transmit)
type	3 = register read (base register), 7 = read register (page register)
page	Used when specifying the page of the PHY register
port	Used to specify the register of each port in the PHY register
reg	Specifies the address when reading the base register. In case of the Page and port registers, specify the address with 1000+reg.
data	Contents of the specified register

5.4.4 Remote Command Packet

Use the Remote command packet to operate the function of the port of the PHY of another node.

Figure 5-7. Remote Command Packet Format

00	phy_ID	00	type(8)	000	port	0000	0000	cmnd
Logical Inverse of the first quadlet								
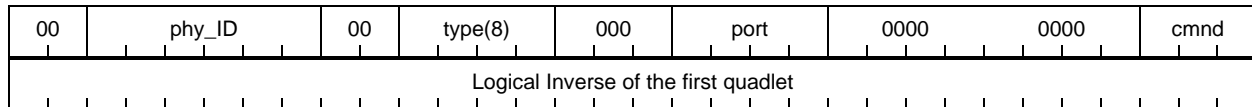
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Table 5-7. Remote Command Packet

Field	Description
phy_ID	Physical ID of the destination packet
type	Extended PHY packet type; set to 8 for Remote command packet
port	Port of the PHY of the operating node
cmnd	Command 0: NOP 1: Disables the port after transmission of the TX_DISABLE_NOTIFY 2: Suspend initiator 4: Clears to 0 the Fault bit of the port 5: Enables the port 6: Resumes the port

5.4.5 Remote Confirmation Packet

The μPD72852 transmits the Remote confirmation when the Remote command packet is received, responding whether cmnd can be executed.
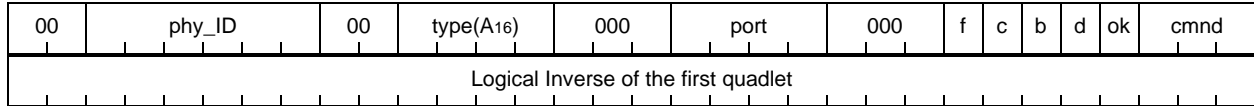
Figure 5-8. Remote Confirmation Packet Format

00	phy_ID	00	type(A16)	000	port	000	f	c	b	d	ok	cmnd
Logical Inverse of the first quadlet												

Table 5-8. Remote Confirmation Packet

Field	Description
phy_ID	Physical ID of the node (node's original packet transmit)
type	Extended PHY packet type; set to A16 for Remote confirmation packet
port	Port set from the Remote command packet
f	Fault bit value of the PHY register of this port
c	Connected bit value of the PHY register of this port
b	Bias bit value of the PHY register of this port
d	Disable bit value of the PHY register of this port
ok	1 indicates executing; otherwise it is 0
cmnd	Specifies the command value with the Remote command packet

5.4.6 Resume Packet

When the μPD72852 receives the Resume packet, all of the ports that were suspended resume the connection. The Resume packet does the broadcast.

Figure 5-9. Resume Packet Format

00	phy_ID	00	type (F16)	00	0000	0000	0000	0000
Logical Inverse of the first quadlet								
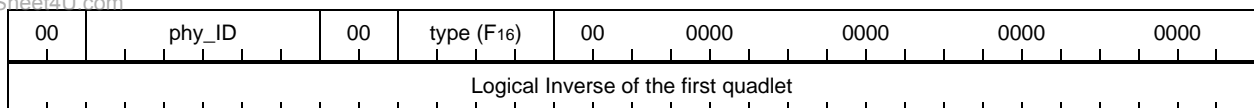
Table 5-9. Resume Packet

Field	Description
phy_ID	Physical ID of the original packet transmit
type	Extended PHY packet type; set to F16 for Resume packet

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DDm}		−0.5 to +4.6	V
Input voltage	V_{IN}		−0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}		−0.5 to V_{DD}+0.5	V
Storage temperature	T_{stg}		−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	Source power node	3.0	3.3	3.6	V
		Non-source power node	2.7[Note]	3.0	3.6	V
Operating temperature	T_A		0.0		70.0	°C
Power dissipation	P_D				440	mW

Note For a node does not source power.

DC Characteristics

Common

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply current	I_{DD}	Note 1		68		mA
		Note 2		60		mA
		Note 3		41		mA
		Note 4		31		mA
		Note 5		115		μA

Notes 1. Transmit maximum packet (all ports transmitting maximum size isochronous packet - 4096 bytes, sent on every isochronous interval, S400, data value of CCCCCCCCH), V_{DD} = 3.3 V, T_A = 25°C

2. Repeat typical packet (receiving on one port DV packets on every isochronous interval, S100, and transmitting on the other port), V_{DD} = 3.3 V, T_A = 25°C

3. Idle (one port receiving and one port transmitting cycle starts), V_{DD} = 3.3 V, T_A = 25°C

4. 1 port receiving cycle start packet only, V_{DD} = 3.3 V, T_A = 25°C

5. Suspend mode, V_{DD} = 3.3 V, T_A = 25°C

★ **PHY/Link Interface**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	CTL0, CTL1, D0-D7, LKON, SCLK, I_{OH} = −9 mA, V_{DD} > 3 V	V_{DD}−0.45			V
		CTL0, CTL1, D0-D7, LKON, SCLK, I_{OH} = −4 mA, V_{DD} = 2.7 V	V_{DD}−0.4			V
Low-level output voltage	V_{OL}	CTL0, CTL1, D0-D7, LKON, SCLK, I_{OH} = +9 mA, V_{DD} > 3 V			0.4	V
		CTL0, CTL1, D0-D7, LKON, SCLK, I_{OH} = +4 mA, V_{DD} = 2.7 V			0.4	V
High-level input voltage	V_{IH}	LPS, SPD, DIRECT, PC0-PC2, SUS/RES, CMC	0.7V_{DD}			V
Low-level input voltage	V_{IL}	LPS, SPD, DIRECT, PC0-PC2, SUS/RES, CMC			0.2V_{DD}	V
High-level input voltage (schmitt)	V_{IHS}	CTL0, CTL1, D0-D7, LREQ, V_{DD} > 3 V	0.456V_{DD} +0.3		0.456V_{DD} +0.9	V
Low-level input voltage (schmitt)	V_{ILS}	CTL0, CTL1, D0-D7, LREQ, V_{DD} > 3 V	0.456V_{DD} −0.9		0.456V_{DD} −0.3	V
High-level input current	I_{IH}	CTL0, CTL1, D0-D7, V_I = V_{DD}, DIRECT = 0 V	−10			μA
		LPS, SPD, DIRECT, PC0-PC2, SUS/RES, CMC, V_I = V_{DD}	−10			μA
Low-level input current	I_{IL}	CTL0, CTL1, D0-D7, LKON, SCLK, V_I = 0 V, DIRECT = 0 V			10	μA
		LPS, SPD, DIRECT, PC0-PC2, SUS/RES, CMC, V_I = 0 V			10	μA

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Cable Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential input voltage	V_{ID}	Cable input, 100 Mbps operation	142		260	mV
		Cable input, 200 Mbps operation	132		260	mV
		Cable input, 400 Mbps operation	118		260	mV
TpB common mode input voltage	V_{ICM}	100 Mbps speed signaling off	1.165		2.515	V
		200 Mbps speed signaling	0.935		2.515	V
		400 Mbps speed signaling	0.523		2.515	V
Differential output voltage	V_{OD}	Cable output (Test load 55Ω)	172.0		265.0	mV
TpA common mode output voltage	V_{OCM}	100 Mbps speed signaling off	1.665		2.015	V
		200 Mbps speed signaling	1.438		2.015	V
		400 Mbps speed signaling	1.030		2.015	V
TpA common mode output current	I_{CM}	100 Mbps speed signaling off	−0.81		+0.44	mA
		200 Mbps speed signaling	−4.84		−2.53	mA
		400 Mbps speed signaling	−12.40		−8.10	mA
Power status threshold voltage	V_{TH}	CPS			7.5	V
TpBias output voltage	V_{TPBIAS}		1.665		2.015	V

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AC Characteristics

PHY/Link Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D, CTL, LREQ setup time	t_{SU}		5			ns
D, CTL, LREQ hold time	t_{HD}		0			ns
D, CTL output timing	t_D		0.5		9	ns
SCLK cycle time	t_{SCLK}		20			ns
SCLK high level time	t_{SCLKH}		9		11	ns
SCLK low level time	t_{SCLKL}		9		11	ns
LKON cycle time	t_{LINKON}		160			ns

Link Interface Timing (SCLK, LKON)

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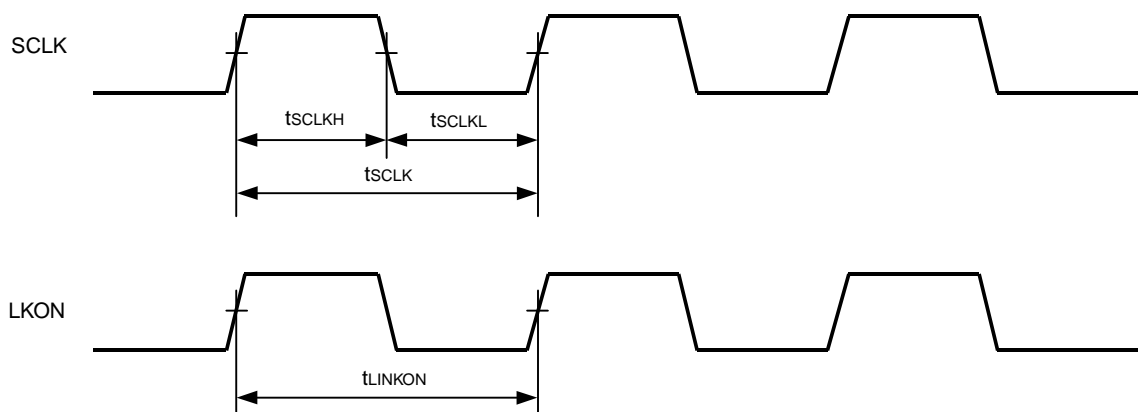
Link Interface Timing (CTL, D)
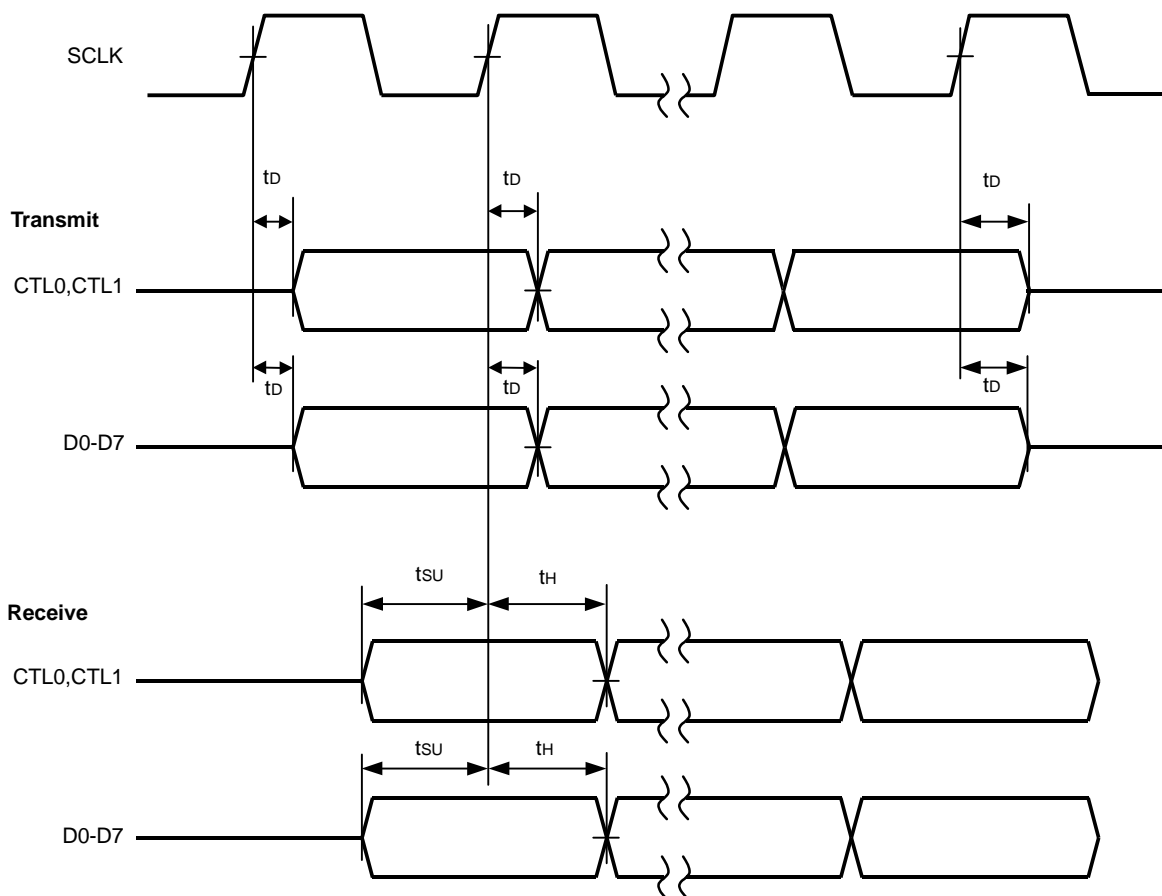
Link Interface Timing (LREQ)

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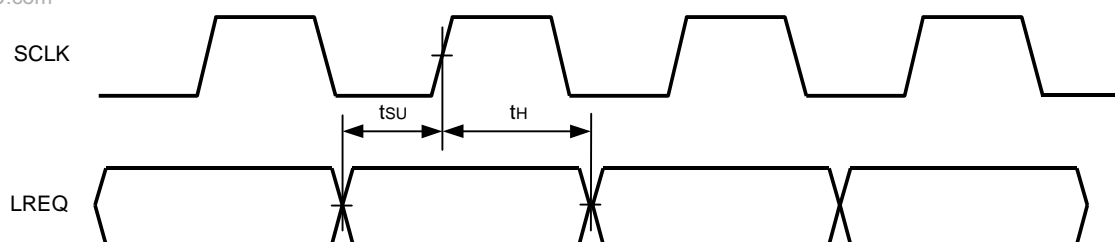
Cable Interface

Parameter	Symbol	Condition	Speed	MIN.	TYP.	MAX.	Unit
TpA, TpB transfer jitter	t_{JITTER}	Between TpA and TpB				±0.15	ns
TpA strobe, TpB data transfer	t_{SKEW}	Between TpA and TpB				±0.10	ns
TPA, TPB rise time/fall time	t_R/t_F	10% to 90%, via 55Ω and 10 pF	S100	0.5		3.2	ns
			S200	0.5		2.2	ns
			S400	0.5		1.2	ns

7. APPLICATION CIRCUIT EXAMPLE

• **IEEE1394 Interface**
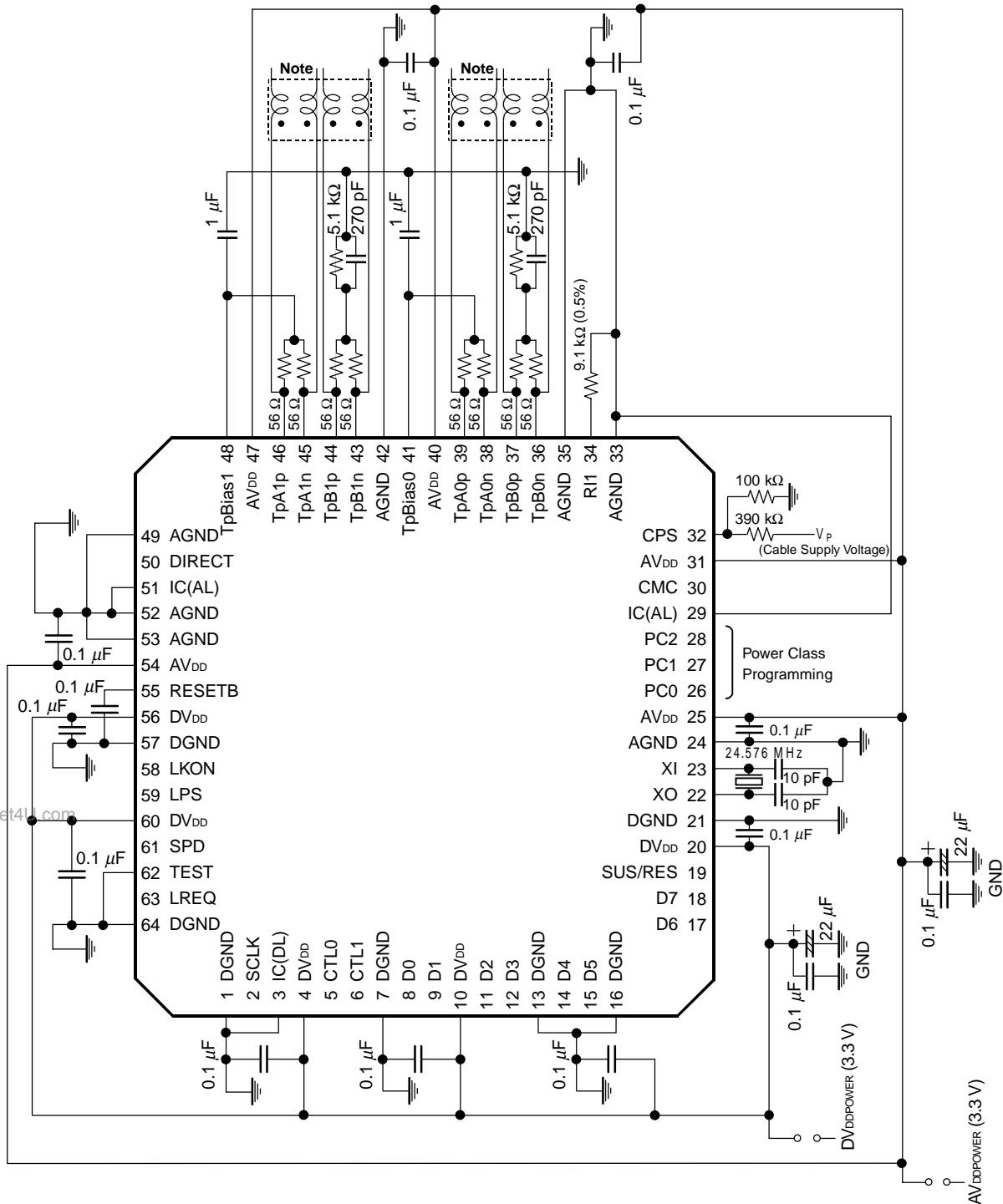
Note Common mode choke.
   Recommendation : TOKO   Part No.944CM-0004 (TYPE B4W)
                  : MURATA   Part No.PLP31DN161SL4

8. PACKAGE DRAWING

64-PIN PLASTIC LQFP (10x10)

detail of lead end

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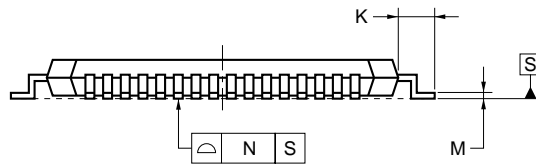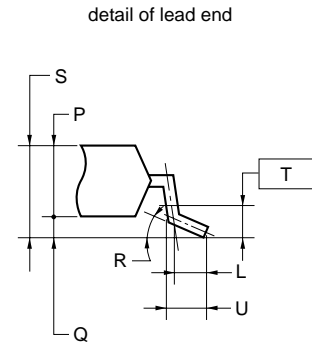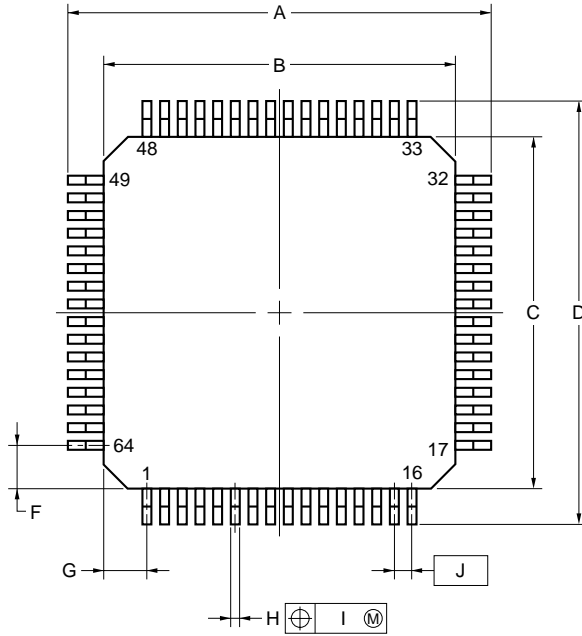
ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.1±0.05
R	$3°^{+4°}_{-3°}$
S	1.5±0.10
T	0.25
U	0.6±0.15

S64GB-50-8EU-1

9. RECOMMENDED SOLDERING CONDITIONS

The μPD72852 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 9-1. Surface Mounting Type Soldering Conditions

μ**PD72852GB-8EU: 64-pin plastic LQFP (10 x 10)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher). Count: three times or less Exposure limit: 3 days**Note** (after that prebake at 125°C for 10 hours)	IR35-103-3
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**
Note:
Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**
Note:
No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**
Note:
Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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④ **PAY ATTENTION TO CHARGING WITH STATIC ELECTRICITY OF THE DEVICE OR THE SURFACE OF THE DEVICE PACKAGE**
Note:
In case the handling of this product and the production manufacturing process, please use the ionizer for this device to eliminate static electricity.

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