SURFACE-MOUNT
PNP POWER TRANSISTORS

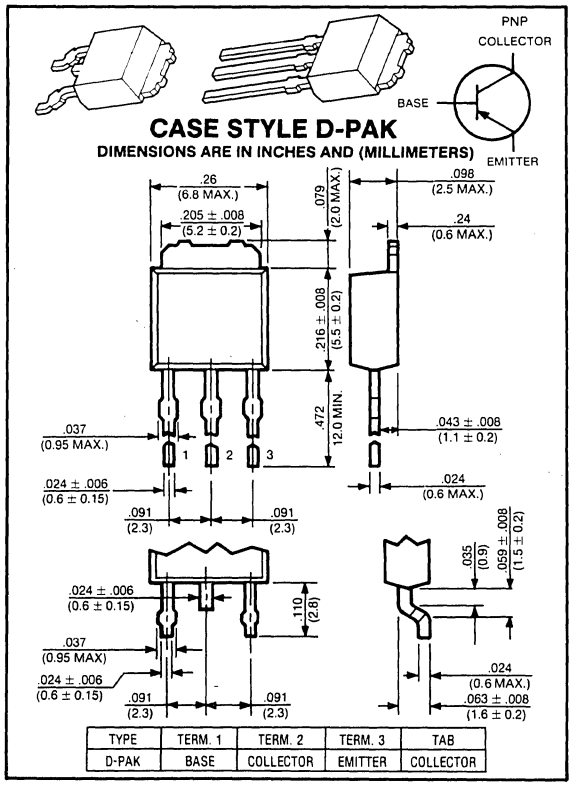
D73F5T1,2

-50 VOLTS
-5 AMP, 20 WATTS

Designed for high current switching applications.

Features:

- Low Collector Saturation Voltage
  : $V_{CE(sat)}$ = -0.4V (Max.) (at I_C = 3A)
- High Speed Switching Time : t_{stg} = 1.0μs (Typ.)
- Complementary to D72F5T1,2
- Suffix "2" designates lead formed version
- See page 840 for mounting and handling considerations.



TYPE	TERM. 1	TERM. 2	TERM. 3	TAB
D-PAK	BASE	COLLECTOR	EMITTER	COLLECTOR

maximum ratings (T_A = 25°C) (unless otherwise specified)

RATING	SYMBOL	D73F5T1,2	UNITS
Collector-Emitter Voltage	V_{CEO}	-50	Volts
Collector-Base Voltage	V_{CBO}	-60	Volts
Emitter Base Voltage	V_{EBO}	-5	Volts
Collector Current — Continuous	I_C	-5	A
Base Current — Continuous	I_B	-1	A
Total Power Dissipation @ T_C = 25°C @ T_C = 25°C	P_D	1.0 20	Watts
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C

thermal characteristics[1]

Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L	235	°C

(1) See page 841 for thermal considerations.

electrical characteristics (T_A = 25° C) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
off characteristics					
Collector-Emitter Breakdown Voltage (I_C = 10mA, I_B = 0)	$V_{(BR)CEO}$	-50	—	—	Volts
Collector Cutoff Current (V_{CB} = 50V, I_E = 0)	I_{CBO}	—	—	-1	μA
Emitter Cutoff Current (V_{EB} = 5V, I_C = 0)	I_{EBO}	—	—	-1	μA
second breakdown					
Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 11			
on characteristics					
DC Current Gain[2] (I_C = -1A, V_{CE} = -1V)	h_{FE}	70	—	240	—
(I_C = -3A, V_{CE} = -1V)	h_{FE}	30	—	—	
Collector-Emitter Saturation Voltage (I_C = -3A, I_B = -0.15A)	$V_{CE(sat)}$	—	-0.2	-0.4	V
Base-Emitter Saturation Voltage (I_C = -3A, I_B = -0.15A)	$V_{BE(sat)}$	—	-0.9	-1.2	Volts
switching characteristics					
Turn-on Time	V_{CC} = -30V	t_{on}	—	0.1	—	μs
Storage Time	$-I_{B1} = I_{B2}$ = 0.15A	t_{stg}	—	1.0	—	
Fall Time	Duty Cycle ≦ 1%	t_f	—	0.1	—	

(2) See page 43 for h_{FE} ranges.

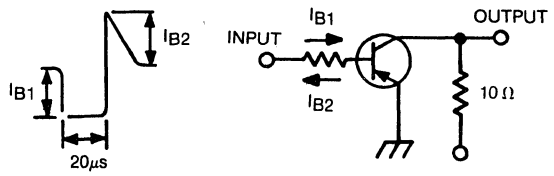


FIG. 1 SWITCHING TIME TEST CIRCUIT

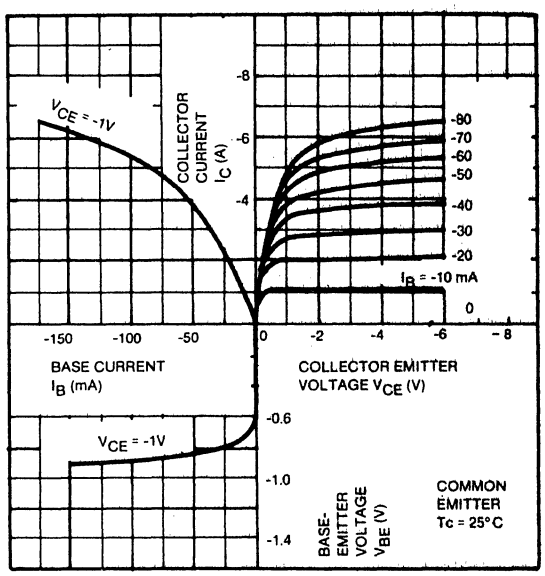


FIG. 2 STATIC CHARACTERISTICS

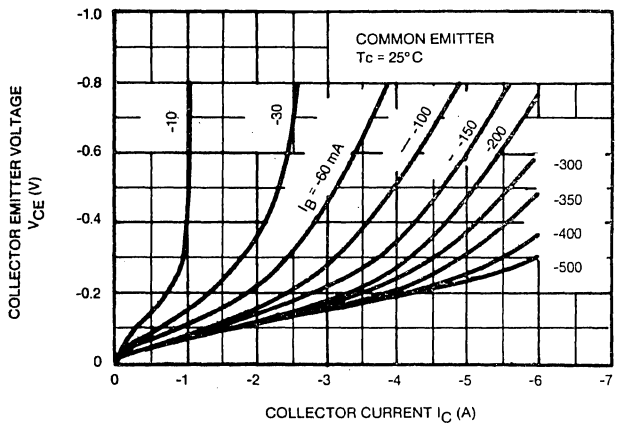


FIG. 3 V_{CE} - I_C

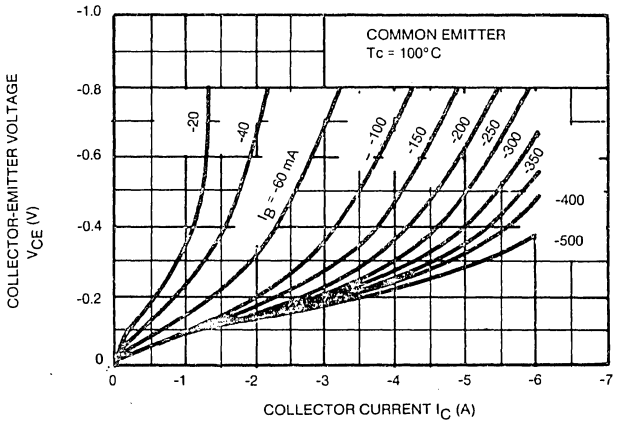


FIG. 4 V_{CE} - I_C

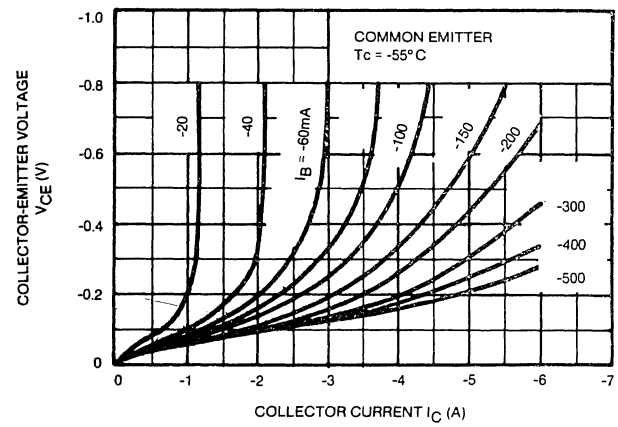


FIG. 5 V_{CE} - I_C

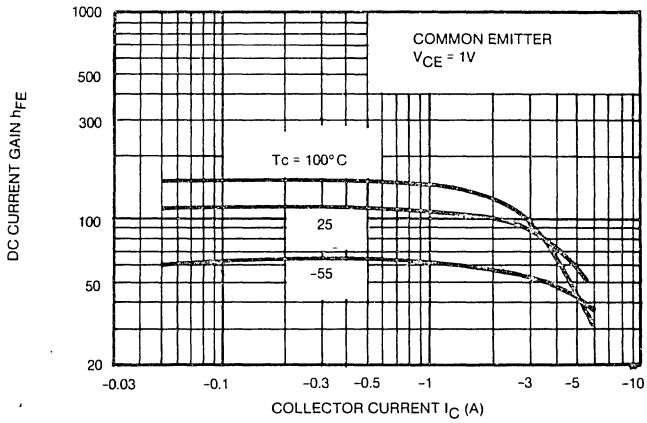


FIG. 6 h_{FE} - I_C

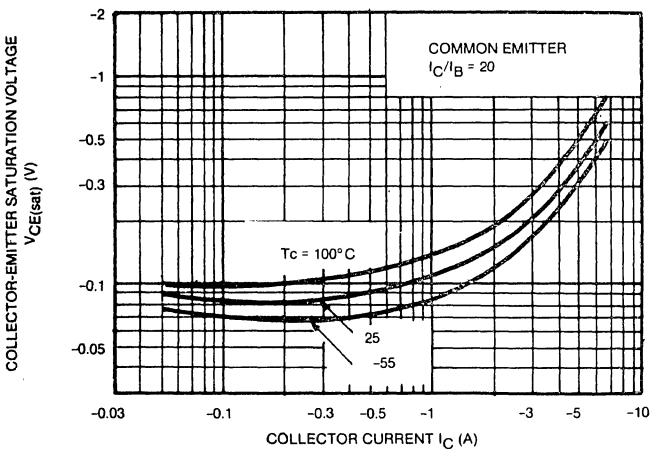


FIG. 7 $V_{CE(sat)}$ - I_C

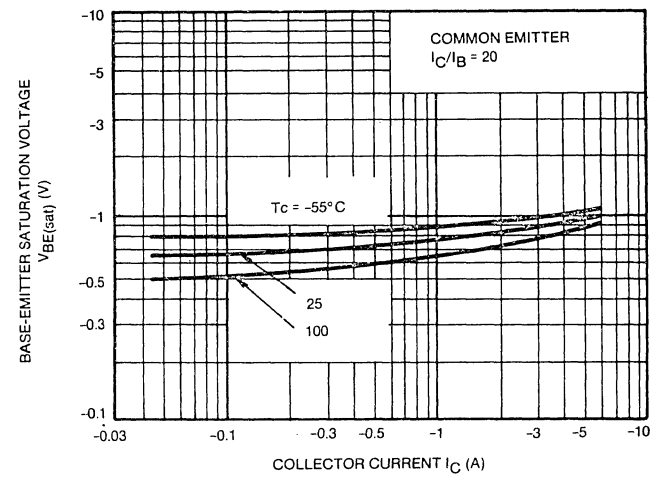


FIG. 8 $V_{BE(sat)}$ - I_C

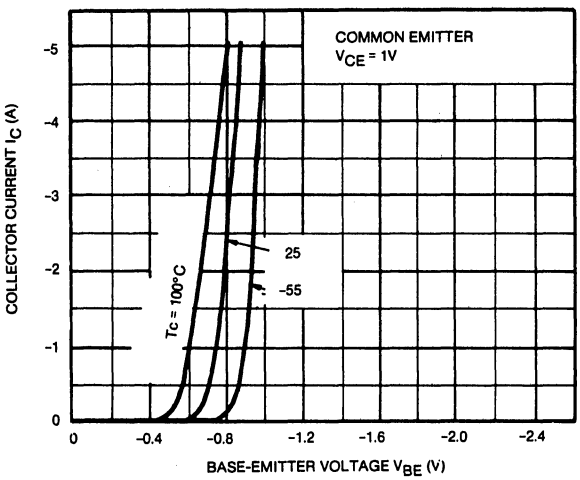


FIG. 9 I_C - V_{BE}

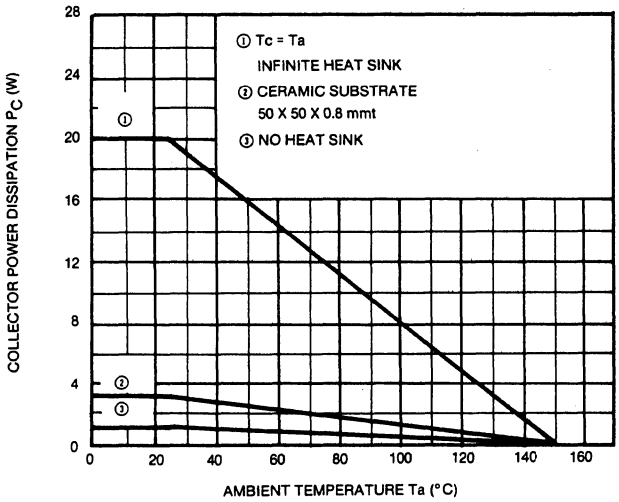


FIG. 10 P_C - Ta

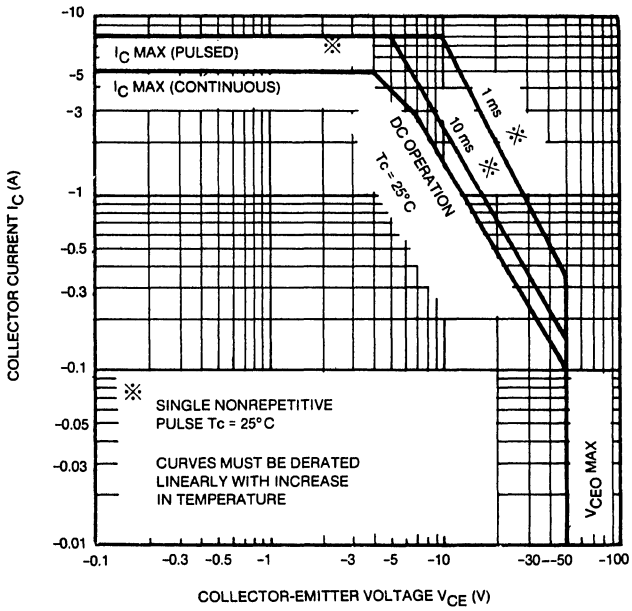


FIG. 11 SAFE OPERATING AREA