NEC
NEC Electronics Inc.

μPD7500H/H-E 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS FOR μPD7500-SERIES EVALUATION

Description

The μPD7500H and μPD7500H-E are single-chip microcomputers created as ROM-less evaluation chips for 4-bit single-chip microcomputers in the μPD7500 series. They are used with the appropriate Evakit development tool to emulate device operation of the μPD7500 series. The μPD7500H and μPD7500H-E incorporate a 4-bit parallel ALU, a data memory (RAM), a bus interface, I/O ports, an 8-bit serial interface, an 8-bit programmable timer/event counter, and vectored interrupt functions integrated into a single-chip design.

External memory may be a 2764 or any other type that interfaces an 8085-type bus.

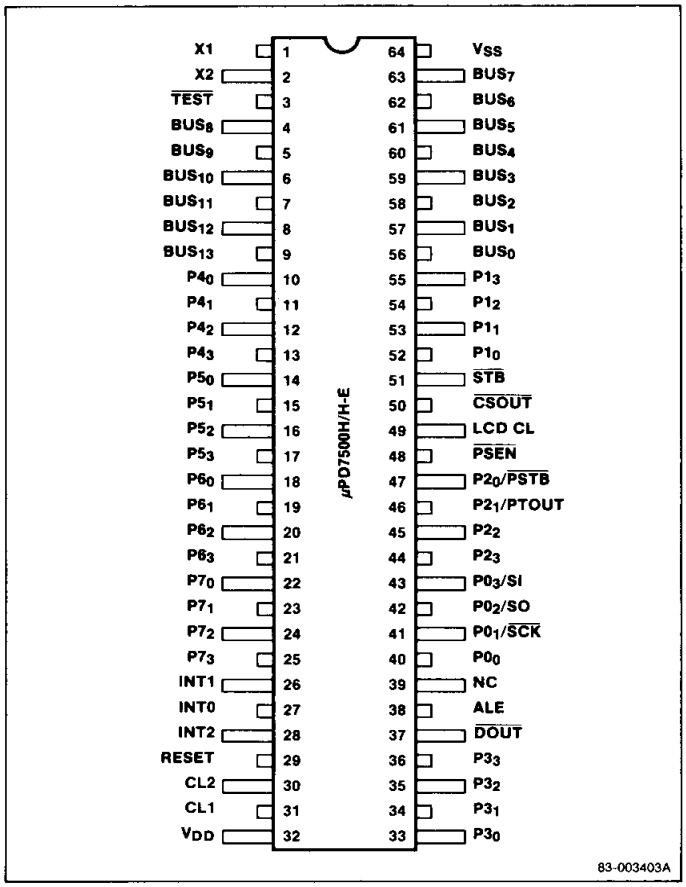
Features

- ☐ μPD7500 series evaluation chip
- ☐ 4-bit microcomputer
- ☐ Two instruction sets:
  - — Set A: 110 instructions
  - — Set B: 70 instructions
- ☐ Instruction cycles:
  - — μPD7500H: RC oscillator = 5 μs/400 kHz
    External clock = 2.86 μs/700 kHz
  - — μPD7500H-E: RC oscillator = 10 μs/200 kHz
    External clock = 10 μs/200 kHz
- ☐ External program memory: 8192 words x 8 bits
- ☐ Internal data memory (RAM): 256 words x 4 bits
- ☐ Three vectored interrupts (INT0, INT1, INT2)
- ☐ Two internal interrupts (INTS, INTT)
- ☐ 8-bit interval timer/event counter
- ☐ 8-bit serial interface
- ☐ Three types of serial clocks
- ☐ 8243 I/O expander interface
- ☐ Power-down functions using standby (STOP/HALT) mode
- ☐ Built-in RC oscillator for system clock (external drive also possible)
- ☐ Built-in crystal oscillator for count clock (external drive also possible)
- ☐ LCD regulating clock output (LCD CL)
- ☐ Low power consumption CMOS
- ☐ Single +5 V ±10% power supply

Ordering Information

Part Number	Package Type	Maximum Frequency of Operation
μPD7500HG-36	64-pin plastic QUIP	700 kHz
μPD7500H-EG-36	64-pin plastic QUIP	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2	X2, X1	Crystal clock/external event input port n
3	$\overline{TEST}$	Factory test pin (connect to V_{SS})
4-9, 56-63	BUS_0-BUS_{13}	External data bus connected to external program memory
10-13	$P4_0$-$P4_3$	4-bit input/latched three-state output port 4
14-17	$P5_0$-$P5_3$	4-bit input/latched three-state output port 5
18-21	$P6_0$-$P6_3$	4-bit input/latched three-state output port 6
22-25	$P7_0$-$P7_3$	4-bit input/latched three-state output port 7
26	INT1	External interrupt INT1
27	INT0	External interrupt INT0
28	INT2	External interrupt INT2
29	RESET	RESET input
30, 31	CL1, CL2	System clock input
32	V_{DD}	Positive power supply
33-36	$P3_0$-$P3_3$	4-bit input/latched three-state output port 3
37	$\overline{DOUT}$	Data output
38	ALE	Address latch enable
39	NC	No connection
40-43	$P0_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input port 0, serial I/O interface
44-47	$P2_0/\overline{PSTB}$ $P2_1$/PTOUT $P2_2$, $P2_3$	4-bit latched three-state output port 2
48	$\overline{PSEN}$	Program store enable
49	LCD CL	Display timing pulse
50	$\overline{CSOUT}$	Chip select output
51	$\overline{STB}$	Strobe output
52-55	$P1_0$-$P1_3$	4-bit input/three-state output port 1
64	V_{SS}	Ground

Pin Functions

BUS_0-BUS_{13} [Data Bus]

External data bus connected to external program memory.

$P0_0$, $P0_1/\overline{SCK}$, $P0_2$/SO, $P0_3$/SI [Port 0/Serial Interface]

4-bit input port 0/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface, under control of the serial mode select register. The serial input SI , serial output SO , and the serial clock $\overline{SCK}$ (synchronizes data transfer) make up the 8-bit serial I/O interface.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port 1. Data output from port 1 is strobed in synchronization with a $P2_0/\overline{PSTB}$ pulse.

$P2_0/\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port 2 . Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer-out F/F signal .

$P3_0$-$P3_3$ [Port 3]

4-bit input/latched three-state output port 3.

$P4_0$-$P4_3$ [Port 4]

4-bit input/latched three-state output port 4. Also performs 8-bit parallel I/O with port 5.

$P5_0$-$P5_3$ [Port 5]

4-bit input/latched three-state output port 5. Also performs 8-bit parallel I/O with port 4.

$P6_0$-$P6_3$ [Port 6]

4-bit input/latched three-state output port 6. Individual lines can be configured as inputs or outputs under control of the port 6 mode select register.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port 7.

INT0 [Interrupt 0]

External interrupt INT0 . This is a rising edge-triggered interrupt.

INT1 [Interrupt 1]

External interrupt INT1 . This is a rising edge-triggered interrupt.

INT2 [Interrupt 2]

External interrupt INT2 . This is a rising edge-triggered interrupt.

CL1, CL2 [Clock Inputs]

System clock input. Connect 62-kΩ resistor across CL1 and CL2, and connect 33-pF capacitor from CL1 to V_{SS}. Alternatively, you may connect an external clock source to CL1 and leave CL2 open.

X2, X1 [Crystal Inputs]

Crystal clock/external event input port n. A crystal oscillator circuit is connected to input X1 and output X2 for crystal clock operation. Alternatively, external event pulses are connected to input X1 and output X2 is left open.

$\overline{DOUT}$ [Data Output]

Data output.

ALE [Address Latch Enable]

Address latch enable .

$\overline{PSEN}$ [Program Store Enable]

Program store enable.

LCD CL [Display Timing]

Display timing pulse .

$\overline{CSOUT}$ [Chip Select Output]

Chip select output. Connected to μPD82C43.

$\overline{STB}$ [Strobe Output]

Strobe output. Connected to μPD82C43.

$\overline{TEST}$ [Test Pin]

Factory test pin (connect to V_{SS}).

RESET [Reset]

RESET input . RC circuit or pulse initializes μPD7500H after power up.

NC [No Connection]

No connection.

V_{DD} [Power Supply]

Positive power supply. Apply single voltage in the range 4.5 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Evaluation Chip Selection for Emulation

Table 1 lists which evaluation chip should be used with the Evakits to emulate the appropriate speed of each device in the μPD7500 series.

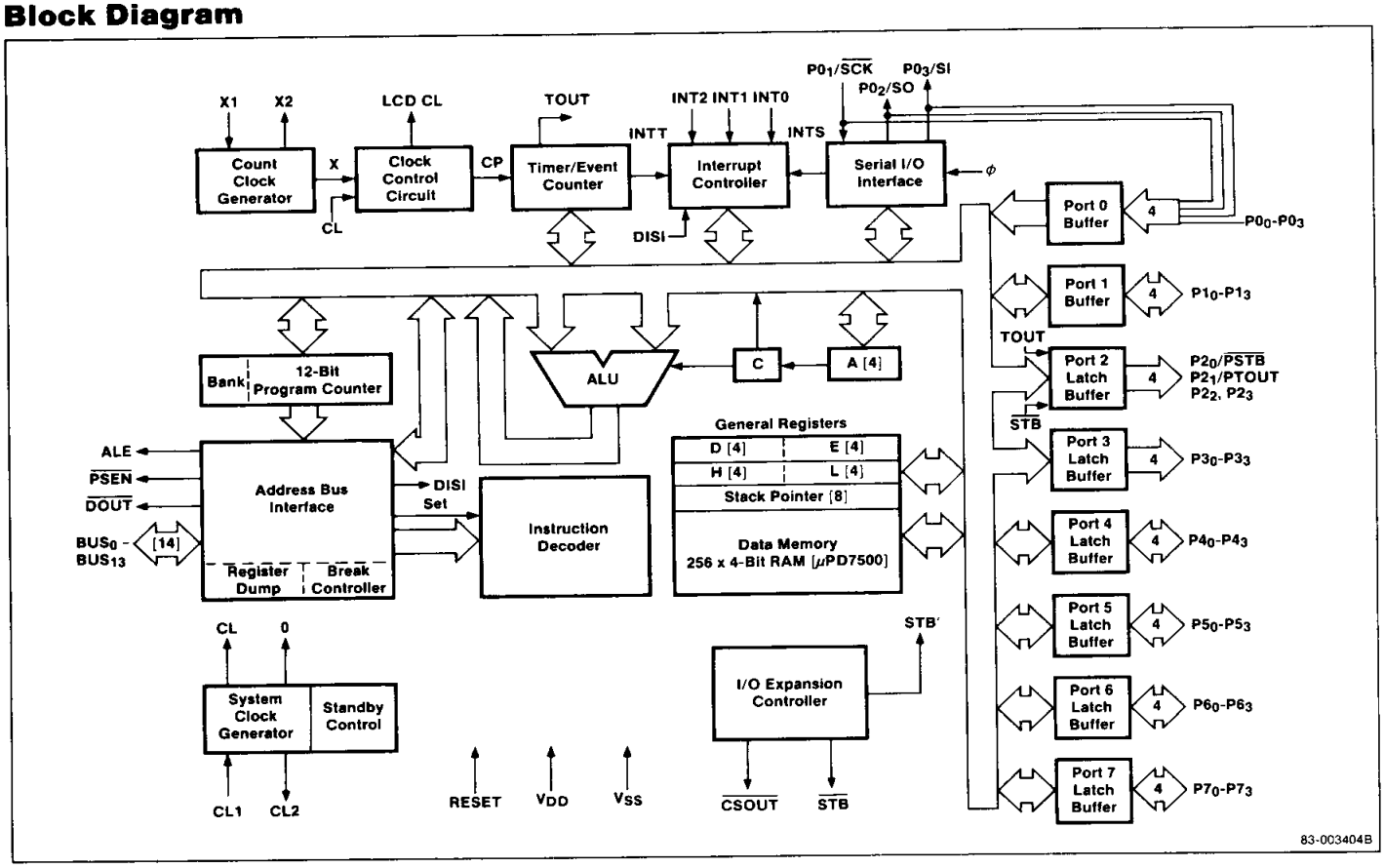
Table 1. Evaluation Chip Selection

μPD7500H	μPD7500H-E
μPD7507H	μPD7501
μPD7508H	μPD7502
μPD7514	μPD7503
μPD7516H (Note 1)	μPD7506
μPD7519H (Note 1)	μPD7507
μPD7527A	μPD7507S
μPD7528A	μPD7508
μPD7533	μPD7508A
μPD7537A	μPD7519
μPD7538A	
μPD7554	
μPD7556	
μPD7564	
μPD7566	

Note:

(1) Up to 5.5 MHz during emulation.

Block Diagram



See figures 1 through 7 for additional block diagram details.

Figure	Title
1	Data Memory Map
2	Program Memory Map
3	Timer/Event Counter
4	Serial Interface
5	Interrupt Control
6	Clock Control
7	Interface at Input/Output Ports

Figure 1. Data Memory Map

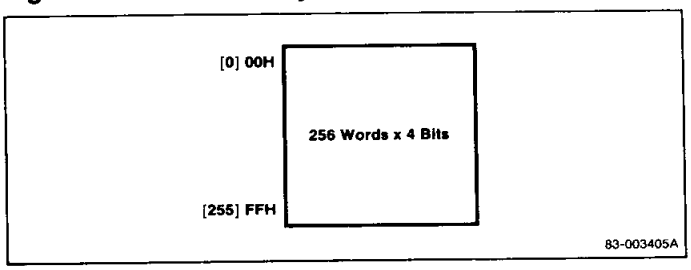


Figure 2. Program Memory Map

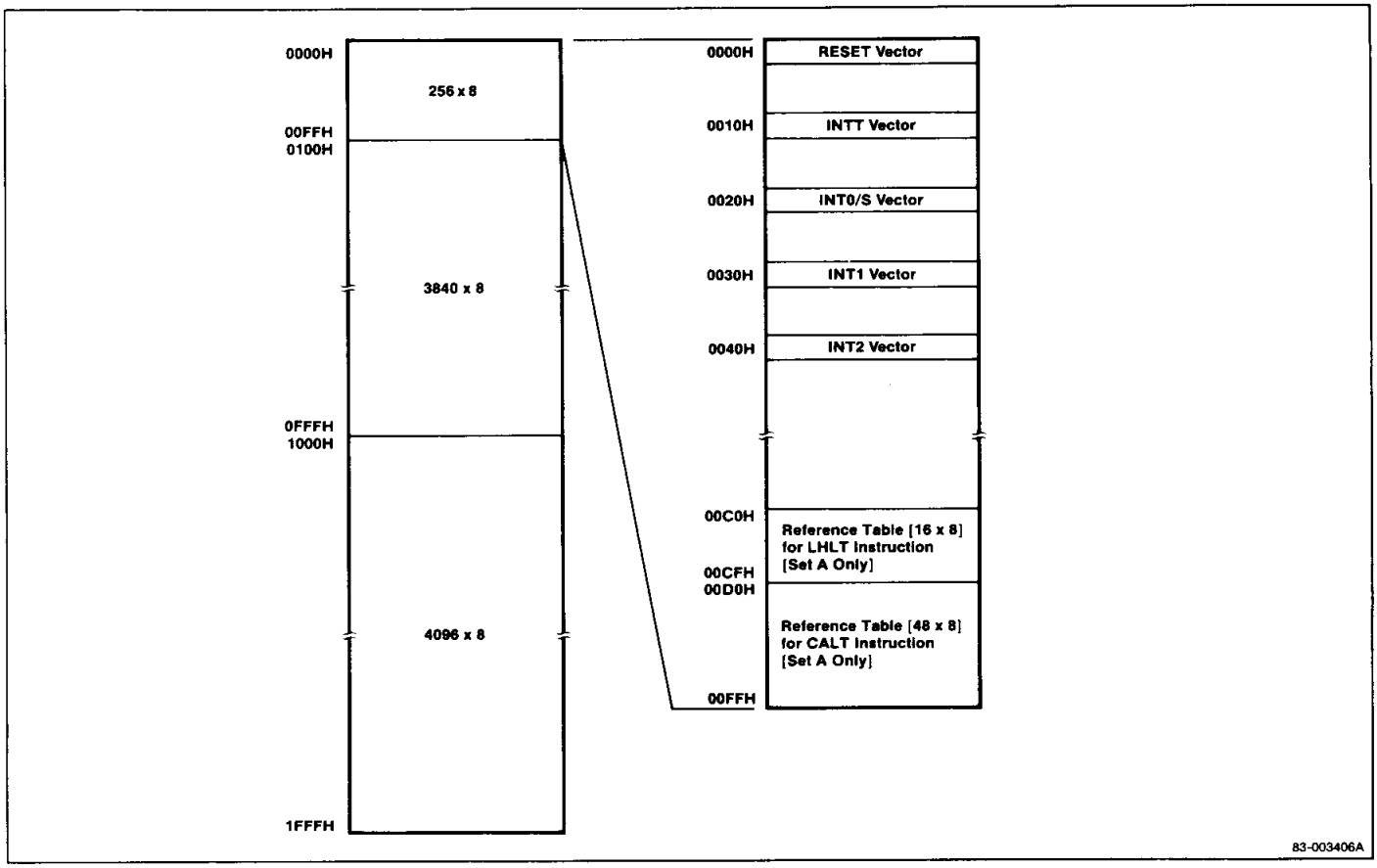


Figure 3. Timer/Event Counter

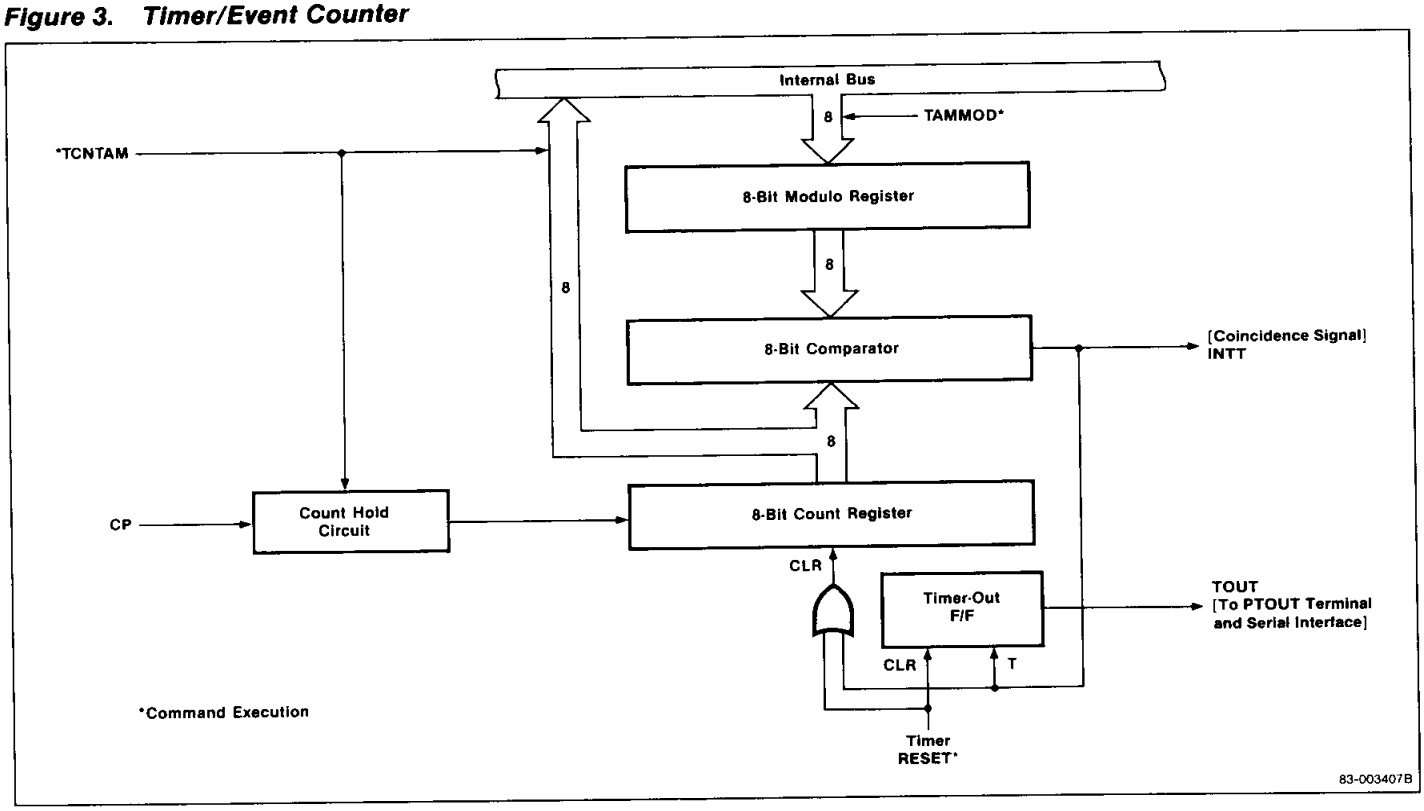


Figure 4. Serial Interface

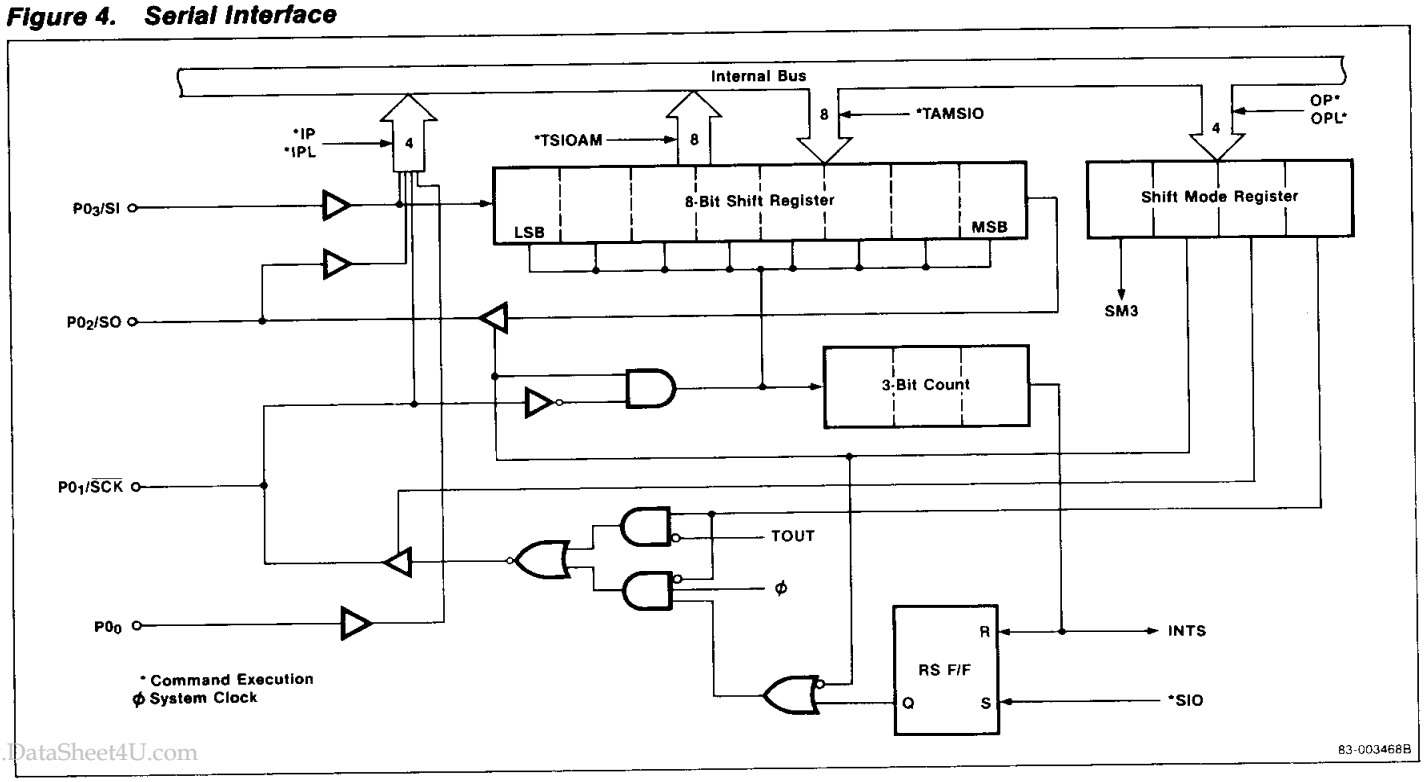


Figure 5. Interrupt Control

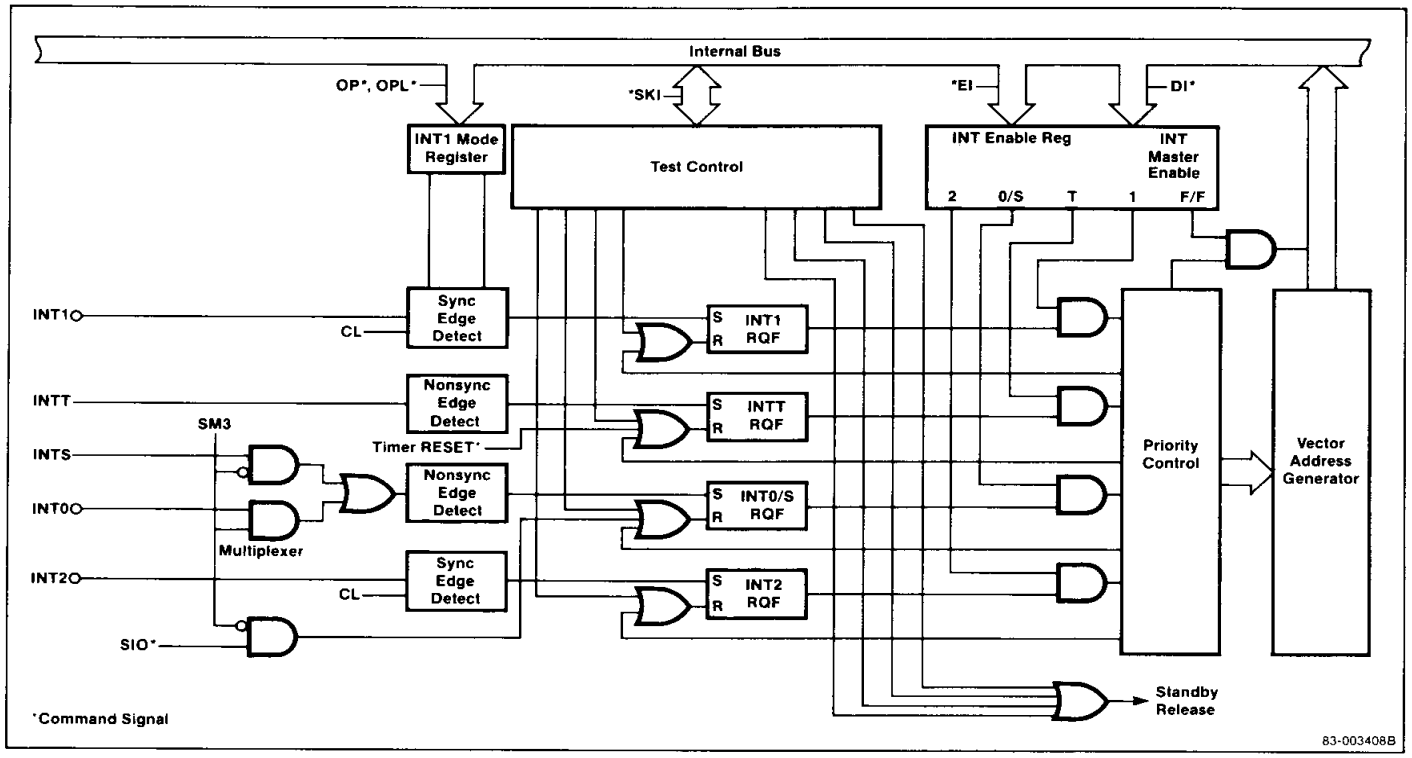


Figure 6. Clock Control

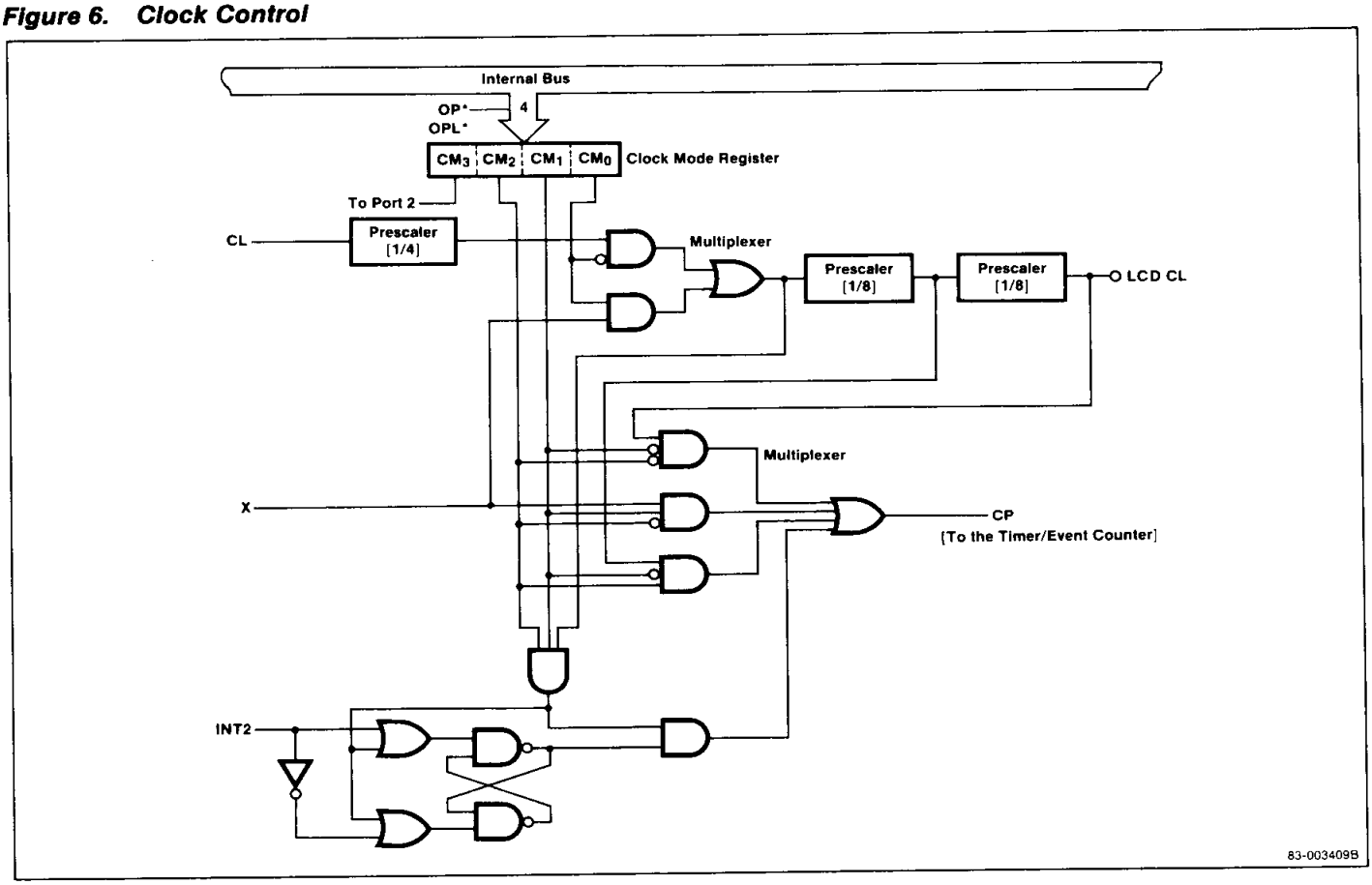
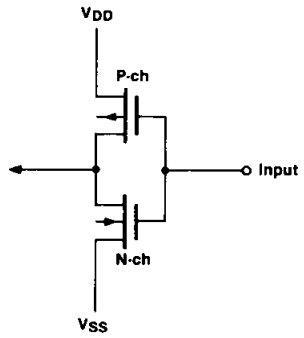
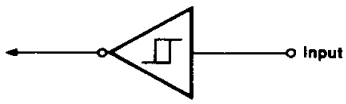


Figure 7. Interface at Input/Output Ports

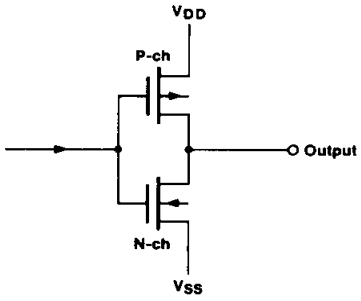
Type A
TEST, $P0_0$



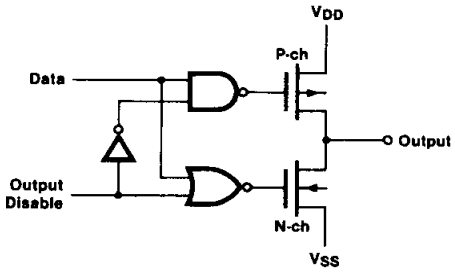
Type B
INT0, INT1, INT2, RESET, $P0_3$/SI



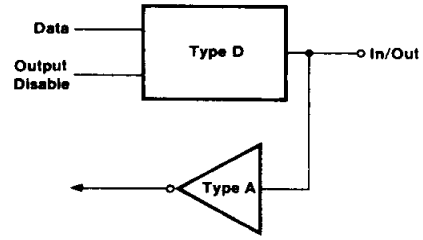
Type C
BUS_8, BUS_9 $\overline{DOUT}$, ALE, $\overline{PSEN}$, LCD CL, $\overline{CSOUT}$, $\overline{STB}$



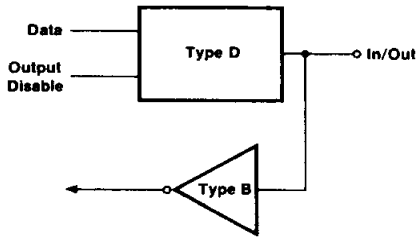
Type D
$P3_0$-$P3_3$, $P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$



Type E
BUS_0-BUS_7, BUS_{10}-BUS_{13}, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P7_0$-$P7_3$, $P0_2$/SO, $P1_0$-$P1_3$



Type F
$P0_1$/$\overline{SCK}$



83-003410C

Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	
μPD7500H	0 to +40°C
μPD7500H-E	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current (total, all output ports)	
I_{OH}	−20 mA
I_{OL}	50 mA

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

μPD7500H: $T_A = 0$ to +40°C, $V_{DD} = 5$ V ±5%
μPD7500H-E: $T_A = -10$ to +70°C, $V_{DD} = 5$ V ±10%

		Limits							
		μPD7500H			μPD7500H-E				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	0.7 V_{DD}		V_{DD}	V	All inputs other than CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
Input low voltage	V_{IL1}	0		0.3 V_{DD}	0		0.3 V_{DD}	V	All inputs other than CL1, X1
	V_{IL2}	0		0.5	0		0.5	V	CL1, X1
Input leakage current, high	I_{LIH1}			3			3	μA	All inputs other than CL1, X1
	I_{LIH2}			10			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3			−3	μA	All inputs other than CL1, X1
	I_{LIL2}			−10			−10	μA	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V_{DD} − 1.0			V	$I_{OH} = 1.0$ mA
Output voltage, low	V_{OL}			0.4			0.4	V	$I_{OL} = 1.6$ mA
Output leakage current, high	I_{LOH}		3			3		μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}		−3			−3		μA	$V_O = 0$ V
Supply current	I_{DD1}		4			3		mA	Normal operation, all output pins open, no BUS conflicts
	I_{DD2}	2	20		2	20		μA	Stop mode, X1 = 0 V

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V, f = 1 MHz

		Limits							
		μPD7500H			μPD7500H-E				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15			15	pF	Unmeasured pins returned to V_{SS}
Output capacitance	C_O			15			15	pF	
I/O capacitance	C_{IO}			15			15	pF	

AC Characteristics

μPD7500H: T_A = 0 to 40°C, V_{DD} = 5 V ±5%
μPD7500H-E: T_A = −10 to +70°C, V_{DD} = 5 V ±10%

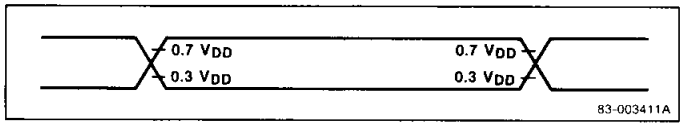
Parameter	Symbol	Limits μPD7500H Min	Typ	Max	Limits μPD7500H-E Min	Typ	Max	Unit	Test Conditions
Clock Operation									
System clock oscillation frequency	f_ϕ	300	400	500	160	200	250	kHz	C = 33 pF ±5%; μPD7500H: R = 33 kΩ ±2%; μPD7500H-E: R = 62 kΩ ±2%
		10		700	10		410	kHz	CL1 = external clock
CL1 input rise time	t_{CR}			0.2			0.2	μs	
CL1 input fall time	t_{CF}			0.2			0.2	μs	
CL1 input clock width (high)	t_{CH}	0.7			1.2			μs	
CL1 input clock width (low)	t_{CL}	0.7			1.2			μs	
Count clock oscillation frequency (X1, X2)	f_{XX}	25	32	50	25	32	50	kHz	Crystal oscillation
Count clock input frequency (X1)	f_X	0		700	0		410	kHz	
X1 input rise time	f_{XR}			0.2			0.2	μs	
X1 input fall time	f_{XF}			0.2			0.2	μs	
X1 input clock width (high)	t_{XH}	0.7			1.2			μs	
X1 input clock width (low)	t_{XL}	0.7			1.2			μs	
Bus I/O Operation									
ALE pulse width (high)	t_{LH}	400			600			ns	
Address setup time to ALE ↓	t_{AL}	100			200			ns	
Address hold time to ALE ↓	t_{LA}	80			80			ns	
Output data setup time to $\overline{DOUT}$ ↑	t_{DDO}	200			200			ns	
Output data hold time after $\overline{DOUT}$ ↑	t_{DOD}	80			80			ns	
$\overline{DOUT}$ pulse width (low)	t_{DOL}	400			600			ns	
ALE → data input valid time	t_{LDV}			600			700	ns	
Address → data input valid time	t_{ADV}			700			900	ns	
$\overline{PSEN}$ pulse width (low)	t_{PSL}	700			1000			ns	
$\overline{PSEN}$ → data input valid time	t_{PSDV}			300			600	ns	
$\overline{PSEN}$ → data float	t_{PSDF}	0			0			ns	

AC Characteristics (cont)

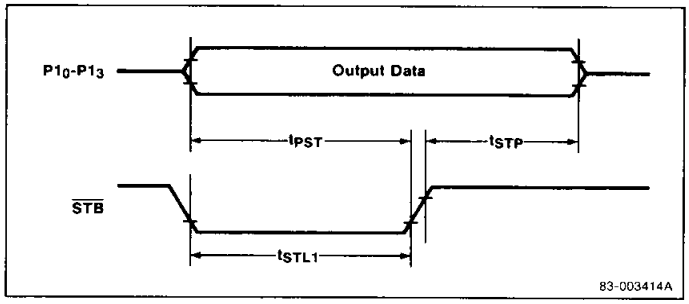
Parameter	Symbol	Limits μPD7500H Min	Typ	Max	Limits μPD7500H-E Min	Typ	Max	Unit	Test Conditions
Port I/O Operation									
Port 1 output setup time to $\overline{STB}\uparrow$	t_{PST}	200			200			ns	Port output mode
Port 1 output hold time after $\overline{STB}\uparrow$	t_{STP}	80			80			ns	
$\overline{STB}$ pulse width (low)	t_{STL1}	400			600			ns	
Output data setup time to $\overline{STB}\uparrow$	t_{DST}	300			300			ns	I/O expander mode
Output data hold time after $\overline{STB}\uparrow$	t_{STD}	80			80			ns	
$\overline{STB}\downarrow\rightarrow$ input data valid time	t_{STDV}			850			850	ns	
$\overline{STB}\downarrow\rightarrow$ input data float time	t_{STDF}	0			0			ns	
Control setup time to $\overline{STB}\downarrow$	t_{CST}	200			200			ns	
Control hold time after $\overline{STB}\downarrow$	t_{STC}	80			80			ns	
$\overline{STB}$ pulse width (low)	t_{STL2}	700			1000			ns	
$\overline{CSOUT}$ setup time to $\overline{STB}\downarrow$	t_{CSST}	200			200			ns	
$\overline{CSOUT}$ hold time after $\overline{STB}\downarrow$	t_{STCS}	80			80			ns	
Serial Interface Operation									
$\overline{SCK}$ cycle time	t_{KCY}	2.5			3.0			μs	Input
		2.86			4.9			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.1			1.3			μs	Input
		1.3			2.2			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	1.1			1.3			μs	Input
		1.3			2.2			μs	Output
SI setup time to $\overline{SCK}\uparrow$	t_{SIK}	300			300			ns	
SI hold time after $\overline{SCK}\uparrow$	t_{KSI}	450			450			ns	
SO output delay after $\overline{SCK}\uparrow$	t_{SKO}			500			850	ns	
Other Operations									
INT0 pulse width, high	t_{I0H}	10			10			μs	
INT0 pulse width, low	t_{I0L}	10			10			μs	
INT1 pulse width, high	t_{I1H}	$2/f_\phi$			$2/f_\phi$			μs	
INT1 pulse width, low	t_{I1L}	$2/f_\phi$			$2/f_\phi$			μs	
INT2 pulse width, high	t_{I2H}	$2/f_\phi$			$2/f_\phi$			μs	
INT2 pulse width, low	t_{I2L}	$2/f_\phi$			$2/f_\phi$			μs	
RESET pulse width, high	t_{RSH}	10			10			μs	
RESET pulse width, low	t_{RSL}	10			10			μs	

Timing Waveforms

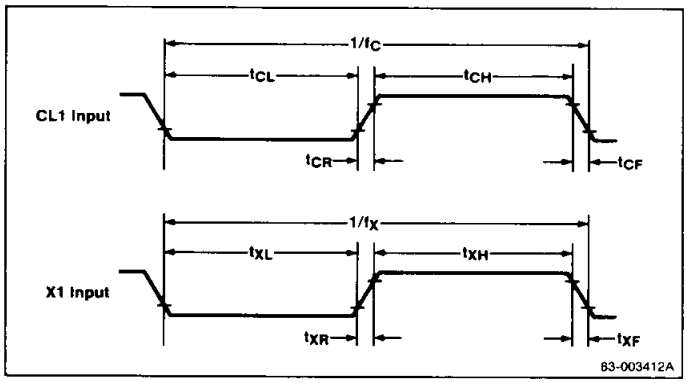
AC Test Input



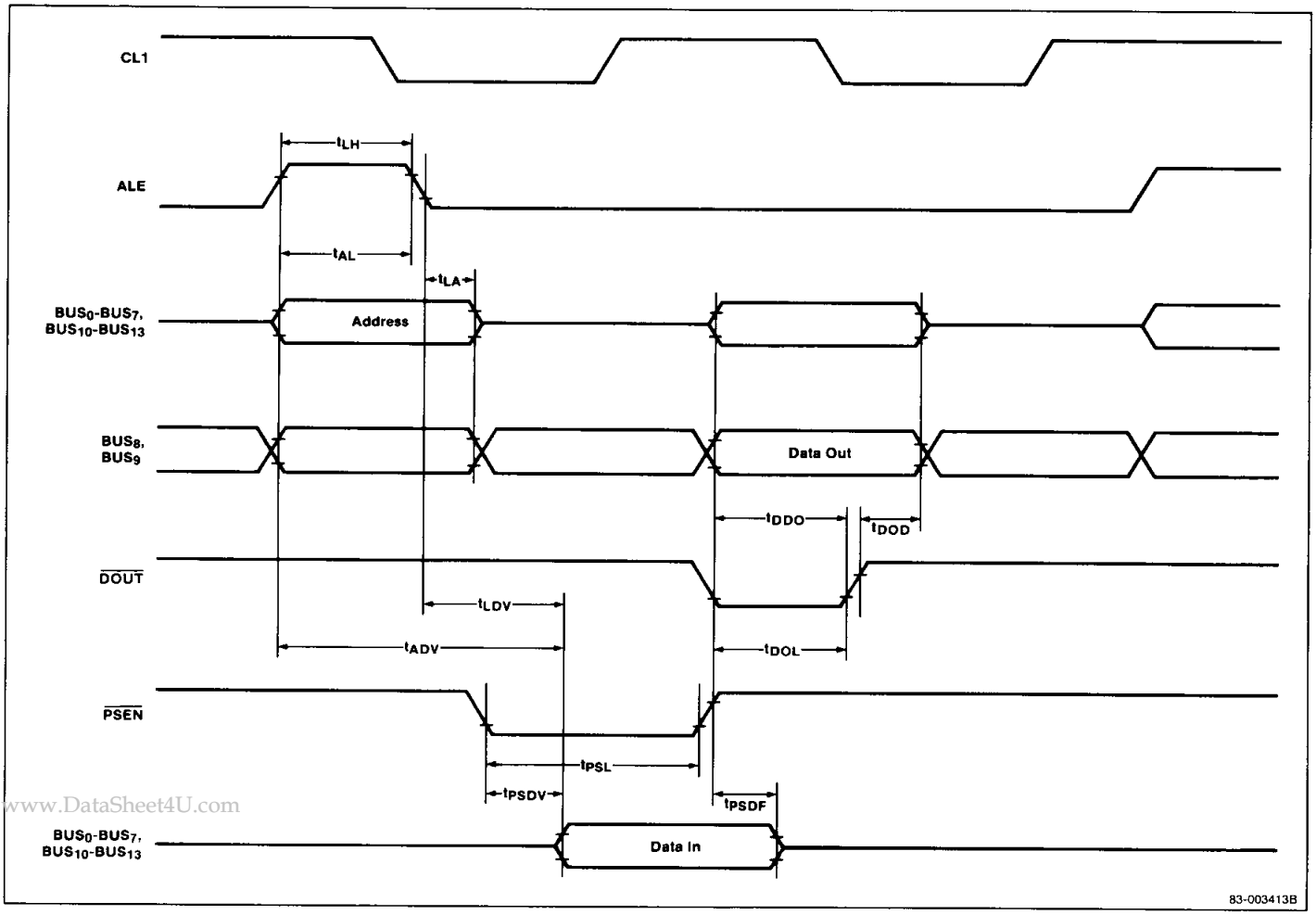
Strobe Output Timing



Clock Timing

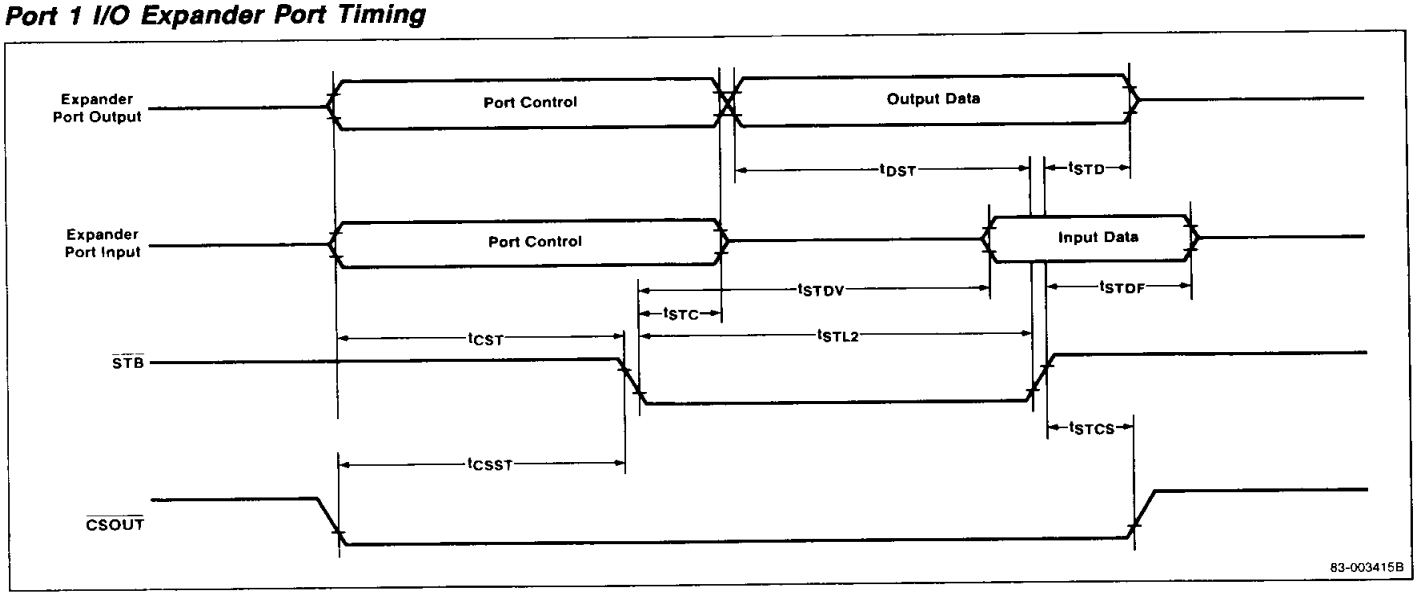


Bus I/O Timing

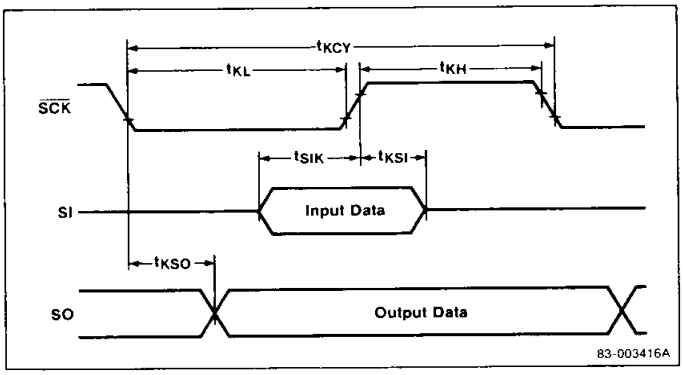


Timing Waveforms (cont)

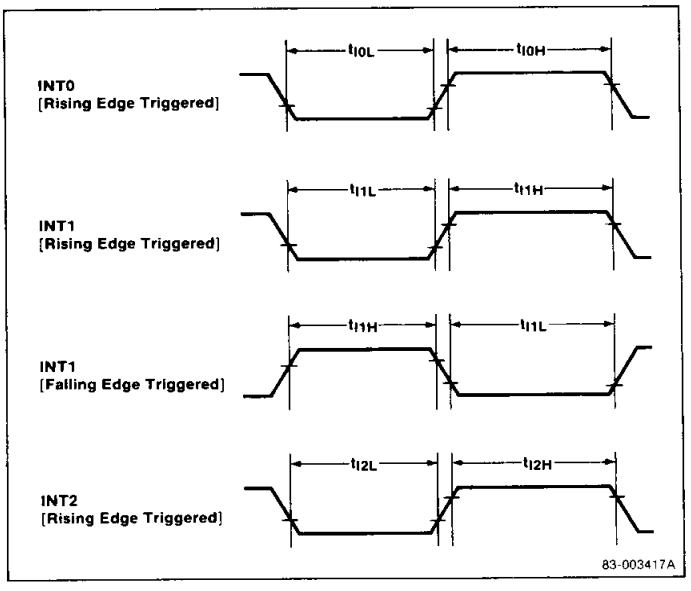
Port 1 I/O Expander Port Timing



Serial Interface Timing



Interrupt Input Timing



RESET Input Timing