Description

The μPD751xx/P1xx is a family of high-performance single-chip CMOS microcomputers containing CPU, ROM, RAM, I/O ports, comparator, interval timer, two timer/counters, vectored interrupts, and a serial interface.

The instruction set allows the user to manipulate RAM data and I/O ports in 1-, 4-, and 8-bit units. The devices are ideally suited for controlling VCRs, telephones, and meters.

Both EPROM and OTP versions are available. See ordering information.

Features

- 136 instructions
  - Bit manipulation
  - 4-bit and 8-bit transfer, arithmetic, logical, comparison, and increment/decrement instructions
  - 1-byte relative branch
  - GETI instruction, to convert one 2-byte, one 3-byte, or two 1-byte instructions into a single 1-byte instruction
- Fast execution time
  (Main system clock @ 4.19 MHz)
  - High-speed cycle: 0.95 μs
  - Lower-voltage cycles: 1.91 and 15.3 μs
- Program ROM
  - μPD75104/104A: 4096 bytes
  - μPD75106: 6016 bytes
  - μPD75108/108A/P108: 8064 bytes
  - μPD75112: 12160 bytes
  - μPD75116/P116: 16256 bytes
- Data memory (RAM)
  - μPD75104/104A/106: 320 x 4 bits
  - Others: 512 x 4 bits
  - Allows operation on 1, 4, or 8 bits
- Bit sequential buffer
  - 16-bit, bit manipulation memory
- Four banks of eight 4-bit registers
- Accumulators
  - 1-bit (CY)
  - 4-bit (A)
  - 8-bit (XA)
- 58 I/O lines
  - All outputs directly drive LEDs (I_{sink} = 15 mA rms)
  - 12 N-channel open-drain, can withstand 12 V
  - 44 I/O lines
  - 14 input-only lines
- 4-input programmable threshold comparator
- Three timers
  - One 8-bit basic interval timer
  - Two 8-bit timer/event counters
- 8-bit serial interface
  - Data transfer can be full duplex or receive only, and can be MSB or LSB first
- Vectored interrupts
  - Two-level nesting
  - Three external interrupts
  - Four internal interrupts
  - Two inputs which generate an interrupt request
- Standby modes
  - HALT mode: stops CPU only
  - STOP mode: stops main system clock
- Power-on-reset and power-on flag
  (always provided with μPD75P108, never on μPD75P116, and available on the others as a mask option)
- Mask option port pull-up resistors
  (not available on μPD75P108/P116)
- Operates with oscillator or ceramic resonator
- CMOS operation, with V_{DD} from 2.7 to 6.0 V
- Low operating current (@5 V and 4.19 MHz)
  - Normal operation: 3.0 mA typical
  - HALT mode: 0.5 mA typical
  - STOP mode: 0.1 μA typical
- Programmable versions
  - OTP & EPROM: μPD75P108
  - OTP: μPD75P116
  - OTP, low voltage: μPD75P108B (Note)

Note: Low voltage target spec of 2.7 to 6.0 V operation. Contact your local NEC Sales Office for latest information; none of the electrical specifications in this data sheet directly apply to this part.

Ordering Information

Part Number	Package Type	ROM
μPD75104CW-xxx	64-pin plastic SDIP (750 mil)	Mask ROM
μPD75104G-xxx-1B	64-pin plastic QFP (resin thickness = 2.05 mm; pitch = 1.0 mm)	Mask ROM
μPD75104GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	Mask ROM
μPD75104AGC-xxx-AB8	64-pin plastic QFP (resin thickness = 2.55 mm; pitch = 0.8 mm)	Mask ROM
μPD75106CW-xxx	64-pin plastic SDIP (750 mil)	Mask ROM
μPD75106G-xxx-1B	64-pin plastic QFP (resin thickness = 2.05 mm; pitch = 1.0 mm)	Mask ROM
μPD75106GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	Mask ROM
μPD75108CW-xxx	64-pin plastic SDIP (750 mil)	Mask ROM
μPD75108G-xxx-1B	64-pin plastic QFP (resin thickness = 2.05 mm; pitch = 1.0 mm)	Mask ROM
μPD75108GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	Mask ROM
μPD75108AG-xxx-22	64-pin plastic QFP (resin thickness = 1.5 mm; pitch = 0.8 mm)	Mask ROM
μPD75108AGC-xxx-AB8	64-pin plastic QFP (resin thickness = 2.55 mm; pitch = 0.8 mm)	Mask ROM
μPD75P108CW	64-pin plastic SDIP (750 mil)	OTP
μPD75P108DW	64-pin shrink CERDIP (w/ 350-mil window)	EPROM
μPD75P108G-1B	64-pin plastic QFP (resin thickness = 2.05 mm; pitch = 1.0 mm)	OTP
μPD75P108BCW (Note 2)	64-pin plastic SDIP	Low voltage OTP
μPD75P108BGF-3BE (Note 2)	64-pin plastic QFP	Low voltage OTP
μPD75112CW-xxx	64-pin plastic SDIP (750 mil)	Mask ROM
μPD75112GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	Mask ROM
μPD75116CW-xxx	64-pin plastic SDIP (750 mil)	Mask ROM
μPD75116GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	Mask ROM
μPD75P116CW-xxx	64-pin plastic SDIP (750 mil)	OTP
μPD75P116GF-xxx-3BE	64-pin plastic QFP (resin thickness = 2.7 mm; pitch = 1.0 mm)	OTP

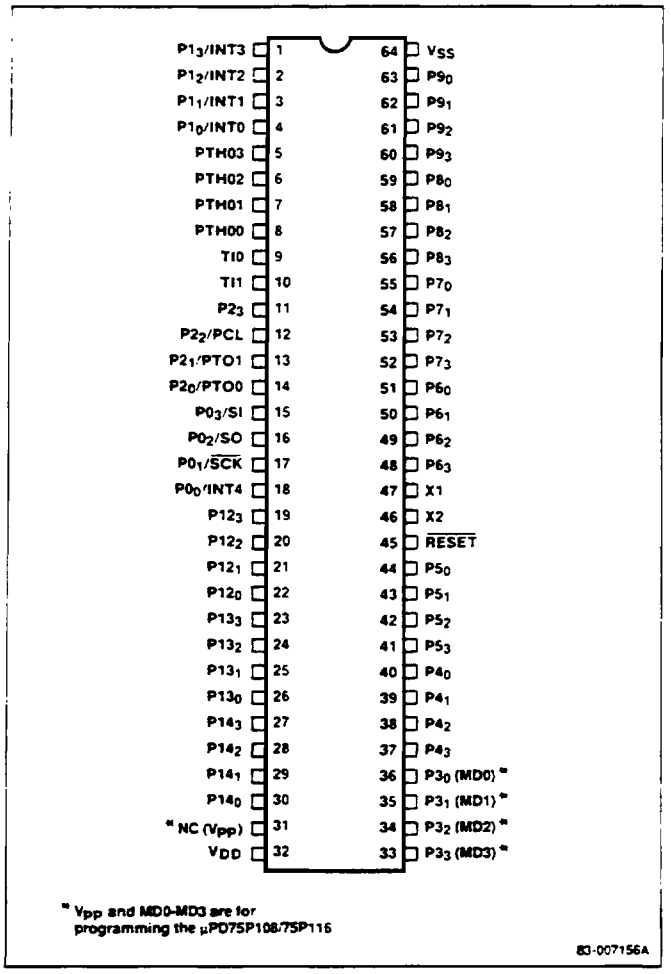
Notes:

(1) xxx indicates ROM code suffix.

(2) Contact your local NEC sales office for latest information.

Pin Configurations

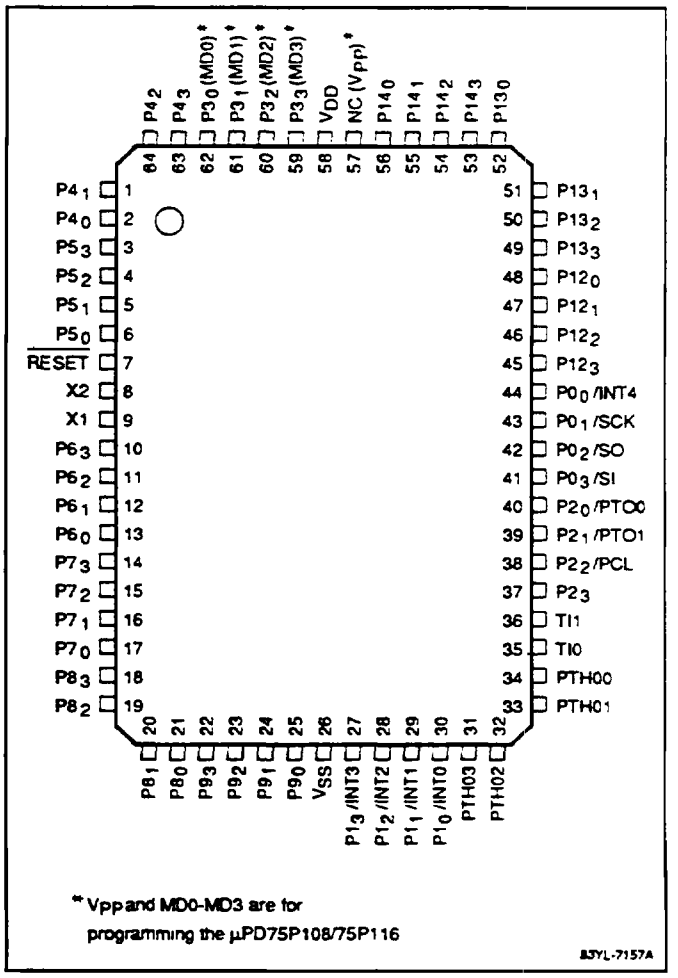
64-Pin Plastic SDIP and 64-Pin Ceramic SDIP w/Window



* Vpp and MD0-MD3 are for programming the μPD75P108/75P116

80-007156A

64-Pin Plastic QFP (All Parts Except μPD75104A/108A)

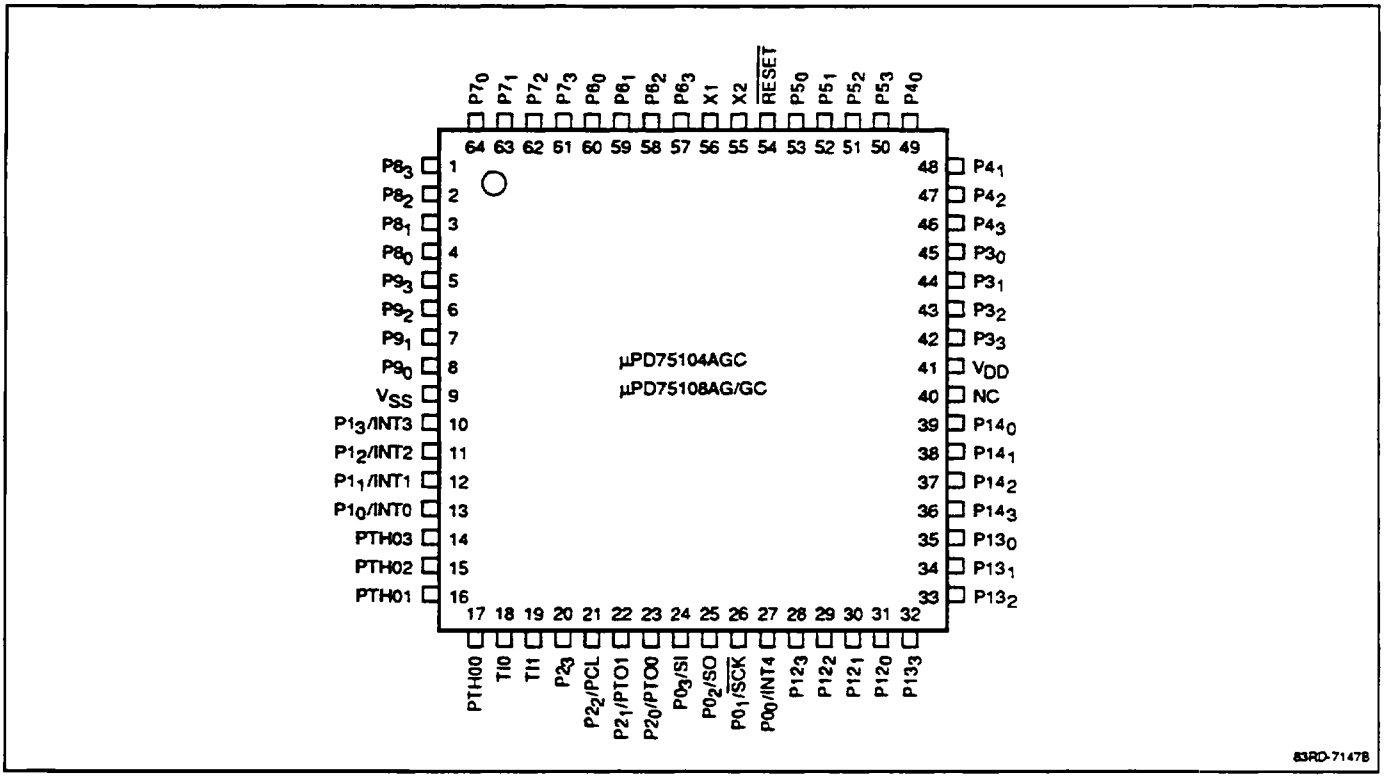


* Vpp and MD0-MD3 are for programming the μPD75P108/75P116

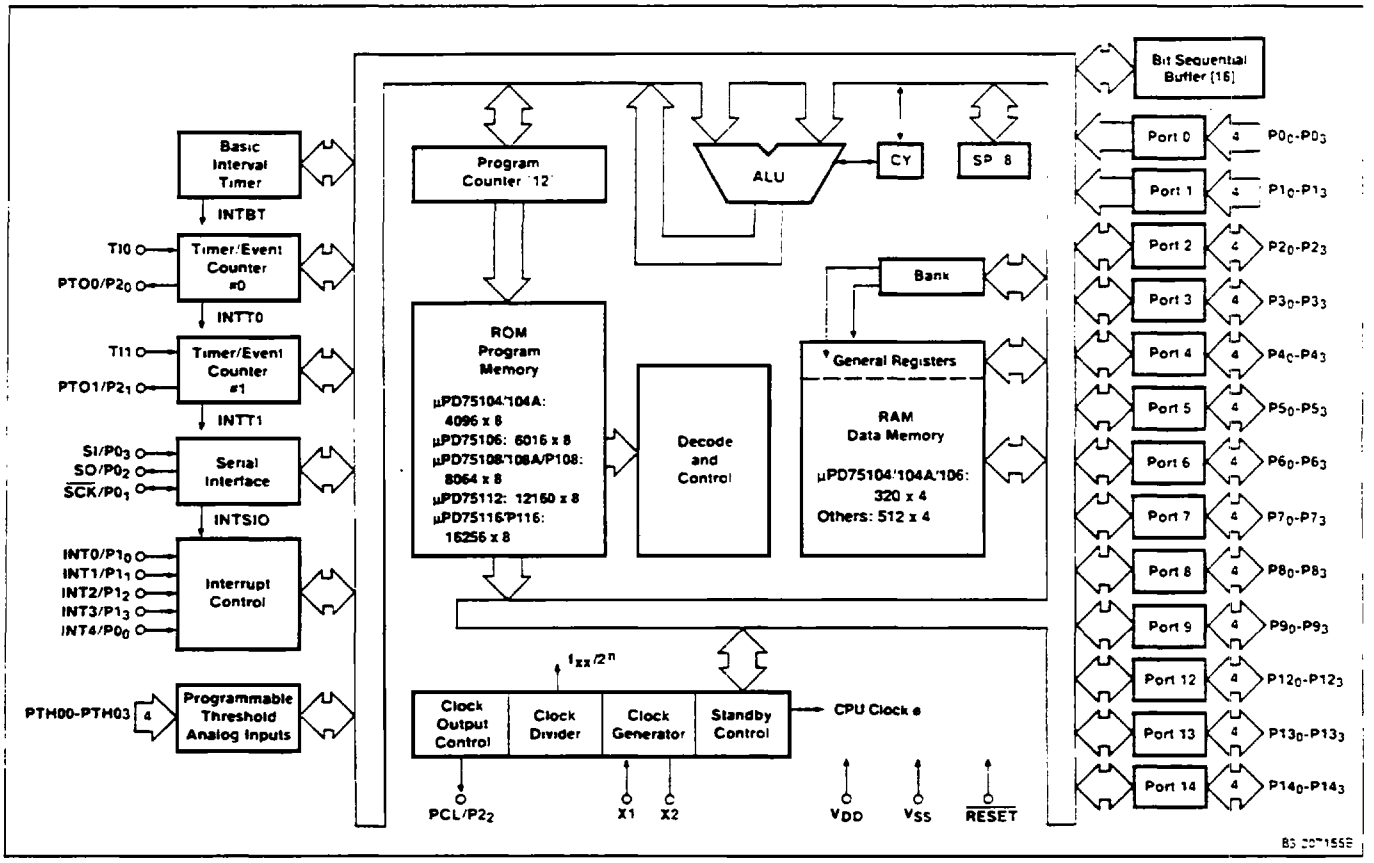
83YL-7157A

Pin Configurations (cont)

64-Pin Plastic QFP (μPD75104A/108A only)



Block Diagram



Pin Identification

Symbol	Function
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/SCK	Port 0 input; serial clock
$P0_2$/SO	Port 0 input; serial out
$P0_3$/SI	Port 0 input; serial in
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/INT3	Port 1 input; interrupt 3
$P2_0$/PTO0	Port 2 I/O; timer/event counter 0
$P2_1$/PTO1	Port 2 I/O; timer/event counter 1
$P2_2$/PCL	Port 2 I/O; clock output
$P2_3$	Port 2 I/O
$P3_0$/MD0	Port 3 I/O; programming mode select 0 (μPD75P108/P116)
$P3_1$/MD1	Port 3 I/O; programming mode select 1 (μPD75P108/P116)
$P3_2$/MD2	Port 3 I/O; programming mode select 2 (μPD75P108/P116)
$P3_3$/MD3	Port 3 I/O; programming mode select 3 (μPD75P108/ P116)
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$-$P6_3$	Port 6 I/O
$P7_0$-$P7_3$	Port 7 I/O
$P8_0$-$P8_3$	Port 8 I/O
$P9_0$-$P9_3$	Port 9 I/O
$P12_0$-$P12_3$	Port 12 I/O
$P13_0$-$P13_3$	Port 13 I/O
$P14_0$-$P14_3$	Port 14 I/O
PTH00-PTH03	4-bit programmable threshold comparator analog input port
$\overline{\text{RESET}}$	Reset input
TI0/TI1	Event timer/counter external input
V_{DD}	Positive power supply
V_{SS}	Ground
X1, X2	Main clock inputs
NC/V_{PP}	No connection; programming pin for μPD75P108/P116

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{\text{SCK}}$, $P0_2$/SO, $P0_3$/SI

These pins can be used as the 4-bit input port 0. $P0_0$ can be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface; SI is the serial input, SO is the serial output, and $\overline{\text{SCK}}$ is the serial clock. Reset causes these pins to default to the Port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/INT3

These pins can be used as 4-bit input port 1. They can also be used, respectively, for edge-triggered interrupts INT0, INT1, INT2, and INT3. INT0 and INT1 are triggered by rising or falling edges, while INT2 and INT3 respond to rising edges only and generate an interrupt request but not an interrupt. Reset causes these pins to default to the Port 1 input mode. Individual pull-up resistors can be provided by mask option in the μPD75104A/108A.

$P2_0$/PTO0, $P2_1$/PTO1, $P2_2$/PCL, $P2_3$

These pins can be used as 4-bit I/O port 2. This port has latched outputs, and can directly drive LEDs. PTO0 and PTO1 are the timer/event counter output pins; PCL is the clock output pin. Reset causes these pins to default to the Port 2 input mode.

$P3_0$/MD0, $P3_1$/MD1, $P3_2$/MD2, $P3_3$/MD3

These pins are used for I/O Port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. $P3_0$-$P3_3$ are used as the programming mode select pins for the μPD75P108/P116 during EPROM/OTP programming and verification. A reset signal causes this port to default to the input mode.

$P4_0$-$P4_3$, $P5_0$-$P5_3$

Port 4 and Port 5 are identical 4-bit I/O ports which can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode. Individual pull-up resistors are available as a mask option in the μPD75104A/108A.

$P6_0$-$P6_3$, $P7_0$-$P7_3$

Port 6 and Port 7 are 4-bit I/O ports; port 6 is I/O bit programmable. These ports may be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode. Individual pull-up resistors are available as a mask option in the μPD75104A/108A

$P8_0$-$P9_3$, $P9_0$-$P9_3$

Port 8 and Port 9 are identical 4-bit I/O ports which can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. A reset signal causes these ports to default to the input mode. Individual pull-up resistors are available as a mask option in the μPD75104A/108A

$P12_0$-$P12_3$, $P13_0$-$P13_3$

Port 12 and Port 13 are identical 4-bit I/O ports which can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. Outputs are N-channel open drain, and can withstand up to 12 volts; pull-up resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode.

$P14_0$-$P14_3$

Port 14 is a 4-bit I/O port. Latched outputs will directly drive LEDs. Outputs are N-channel open drain, and can withstand up to 12 volts; pull-up resistor mask options are available for this port. A reset signal causes the port to default to the input mode.

PTH00-PTH03

4-channel comparator with 4-bit resolution and on-chip resistor ladder.

TI0, TI1

External event input for the timer/event counters. Each pin can also act as an edge-triggered vectored interrupt and a 1-bit input port.

NC/V_{PP}

This pin may be left unconnected when using the μPD751xx. For the μPD75P108/P116, this pin is used as the programming voltage input during the EPROM write/verify cycles. When the devices are not being programmed, this pin should be connected to V_{DD}. Pin must be connected to V_{DD} if the same circuit board is used for both programmable and nonprogrammable devices.

X1, X2

These pins are the system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$

This is the reset input, and it is active low.

V_{DD}

The system positive power supply pin.

V_{SS}

System ground.

Product Comparison

Item	μPD75104/104A	μPD75106	μPD75108/108A	μPD75P108	μPD75112	μPD75116	μPD75P116
Program memory	Mask ROM 000H–FFFH 4096 x 8 bits	Mask ROM 000H–177FH 6016 x 8 bits	Mask ROM 000H–1F7FH 8064 x 8 bits	EPROM/OTP 000H–1FFFH 8192 x 8 bits	Mask ROM 000H–2F7FH 12160 x 8 bits	Mask ROM 000H–3F7FH 16256 x 8 bits	OTP 000H–3FFFH 16384 x 8 bits
Data memory	320 x 4 bits Bank 0: 256 x 4 Bank 1: 64 x 4	320 x 4 bits Bank 0: 256 x 4 Bank 1: 64 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4	512 x 4 bits Bank 0: 256 x 4 Bank 1: 256 x 4
Instruction set	The BR !addr instruction is not provided in the μPD75104/104A.						
Port lines	CMOS I/O lines: 32 12 open-drain outputs with 12 V breakdown. These outputs can have pull-up resistors as a mask option, except for programmable parts. (Note 1) Lines which directly drive LEDs: 44 Total number of lines: 52 (44 I/O and 8 input-only)						

Product Comparison

Item	μPD75104/104A	μPD75106	μPD75108/108A	μPD75P108	μPD75112	μPD75116	μPD75P116
Power-on-reset circuit and power-on flag	Mask option	Mask option	Mask option	Internally provided	Mask option	Mask option	Not included
Operating voltage range	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 10%	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 10%
Package	See ordering information for a complete list of packages						

Notes:

(1) The μPD75104/104A have 24 additional I/O port lines and 4 more input-only lines with mask option programmable pull-up resistors.

ADDRESS SPACES AND MEMORY MAPS

The 75X architecture has two separate address spaces, one for program memory (ROM), and another for data memory (RAM).

Program Memory (ROM)

The ROM is addressed by the program counter. The size of the program counter is 12, 13, or 14 bits; its size depends on which member of the family is being used, as does the amount of ROM present. The ROM contains program object code, interrupt vector table, a GETI instruction reference table, and table data. Table data can be obtained using the table reference instruction, MOVT.

Figure 1 shows the addressing range which can be made using a branch instruction or subroutine call instruction. In addition, the BR PCDE and BR PCXA instructions can be used for a branch where only the low 8 bits of the PC are changed. The program memory addresses are,

μPD75104/104A: 000H to FFFH
μPD75106: 0000H to 177FH
μPD75108/108A: 0000H to 1F7FH
μPD75P108: 0000H to 1FFFH
μPD75112: 0000H to 2F7FH
μPD75116: 0000H to 3F7FH
μPD75P116: 0000H to 3FFFH

All locations of ROM except 000H and 0001H can be used as program memory. However, if interrupts or GETI instructions are used, the locations corresponding to those functions cannot be used. Addresses are normally reserved as follows:

0000H to 0001H: This address area contains the program start address when a $\overline{\text{RESET}}$ is applied, and is also used for setting the values of RBE and MBE. Program execution can be started from any address after a $\overline{\text{RESET}}$.

002H to 000BH: This area is used for interrupt vector addresses and for setting the value of RBE and MBE. Interrupts can start from any location except where noted.

0020H to 007FH: This is the table area for GETI instructions. The GETI instruction is used to access 1, 2 or 3-byte instructions using one byte of program memory. This is useful in compacting code.

Program Counter (PC)

This is a 12/13/14-bit binary counter that contains the address of the current program memory location. The μPD75104/104A contain a 12-bit PC, the μPD75106/108/108A/P108 have a 13-bit PC, and the μPD75112/116/P116 have a 14-bit PC.

When an instruction is executed, the PC is automatically incremented by the number of bytes of the current instruction. When a branch instruction (BR, BRCB) is executed, the contents of the immediate data or register pair indicating the new address are loaded into some or all the bits of the PC. When a subroutine call instruction (CALL, CALLF) is executed or an interrupt is generated, the PC is incremented to point to the next instruction, and this information is saved on the stack. During an interrupt, the program status word (PSW) is

also automatically saved on the stack. The address to be jumped to by the CALL or interrupt is then loaded into the PC.

When a return instruction (RET, RETS, or RETI) is executed, the contents of the stack are restored to the PC.

Data Memory (RAM)

The data memory contains three memory banks, 0, 1, and 15. The RAM memory map is shown in figure 2. The memory consists of general purpose static RAM, general purpose registers, and peripheral control registers. Memory banks are accessed by using the MBE (memory bank enable) bit and by programming the BS (bank select) register. If MBE = 0, the lower 128 nibbles of memory bank 0 and the upper 128 nibbles of memory bank 15 are accessed. If MBE = 1, the upper four bits in the BS register will specify the memory bank. The values are 0H for memory bank 0, 1H for memory bank 1, and FH for memory bank 15. Memory bank 0 contains 256 nibbles, while memory bank 1 contains either 64 or 256 nibbles depending on which member of the μPD751XX/P1XX family is being used. Although the memory is organized in nibbles, the 75X architecture allows the data to be manipulated in bytes, nibbles and individual bits.

The data memory is used for storing processed data, general purpose registers, and as a stack for subroutine or interrupt service. Because of its static nature, the RAM will retain its data when the chip is in the STOP mode, provided V_{DD} is at least 2 volts.

The on-chip peripheral control registers and ports reside in the upper 128 nibbles of bank 15. Bank 15 addresses which are not assigned to a register are not available as random memory except for the 16-bit sequential buffer. Also, the lower 128 nibbles of bank 15 do not contain RAM.

There are four general-purpose register banks in RAM Bank 0, beginning at address 00H. Each bank contains eight 4-bit registers, (B, C, D, E, H, L, X, A), which may be used together to form four 8-bit registers. Register bank selection is accomplished by using the two low-order bits of the BS register and the RBE (register bank enable) bit. A register bank is selected by setting RBE to 1 and programming BS to be 0H-3H for register banks 0-3, respectively. If RBE = 0, the chip defaults to bank 0. Registers which are not used for any other purpose may be used as general purpose RAM.

Each register can be used either in a 4-bit configuration or in a 8-bit configuration when paired with one of the others (BC, DE, HL, XA). There is also a "DL" pair available. DL and pairs DE and HL can be used as data pointers. For 8-bit manipulation, besides BC, DE, HL, and XA, register pairs BC', DE', HL', and XA' are provided. If memory bank 0 is selected and BC' is referenced, BC' is register BC in memory bank 1. If bank 1 is selected and BC' is referenced, BC' is register BC in bank 0.The same concept is true for register banks 2 and 3

Figure 1. Program Memory Map

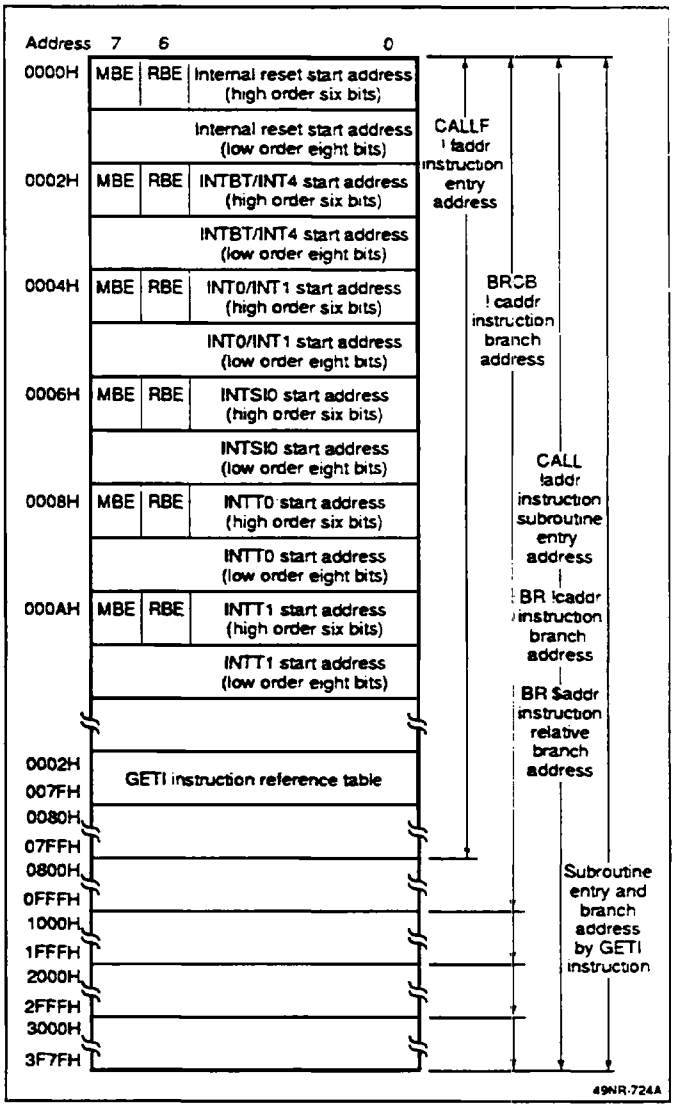


Figure 2. Data Memory Map (μPD75104/104A/106)

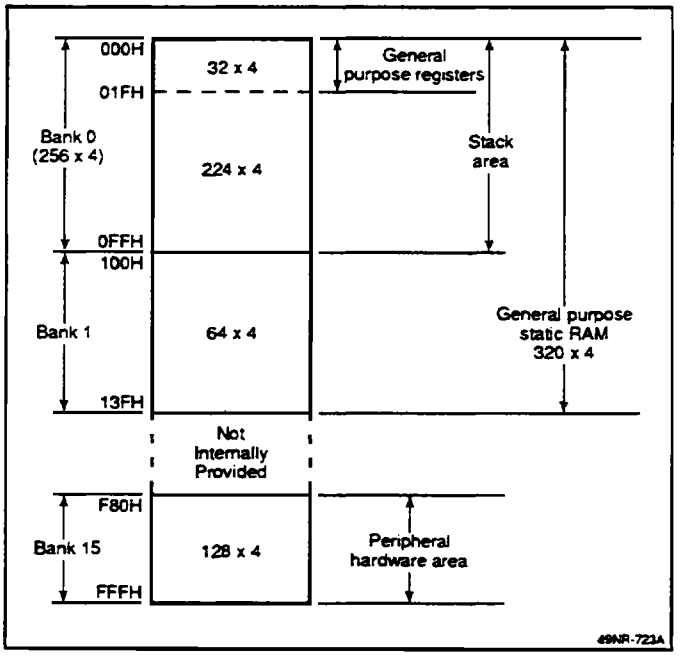


Figure 2a. Data Memory Map (μPD75108 to μPD75116)

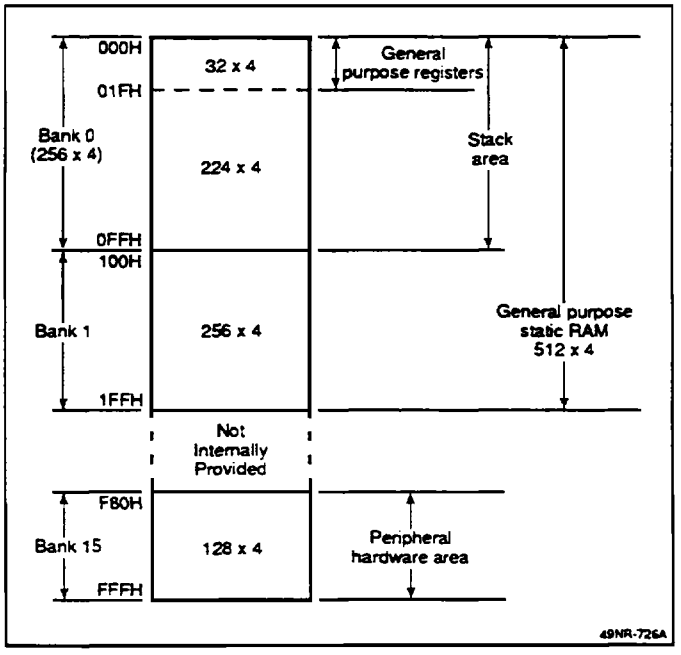
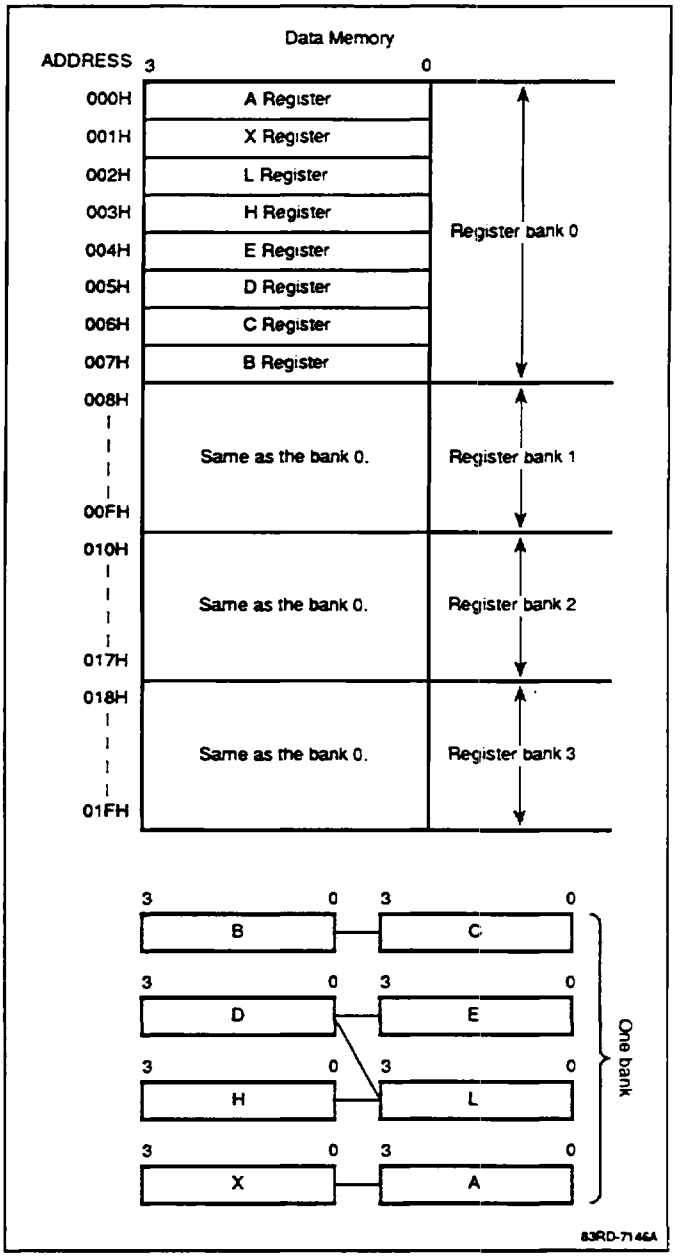


Figure 3. General Purpose Register Configurations



Addressing Modes

The μPD751xx/P1xx is able to address data memory and ports as individual bits, nibbles, or bytes. The addressing modes are as follows:

1-bit direct data memory
4-bit direct data memory
4-bit register indirect (@rpa)
8-bit direct data memory
8-bit register indirect (@HL)

See table 1 for data memory addressing and table 2 for peripheral control register addressing.

Table 1. Data Memory Addressing Modes

Addressing Mode	Representation Format	How the Address is Created
1-bit direct addressing	mem.bit	If MBE = 0, the memory bank is Bank 0 for addresses 00H-7FH, and Bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the four bits of the MBS. The bit to be manipulated is specified in mem.bit
4-bit direct addressing	mem	If MBE = 0, the memory bank is Bank 0 for addresses 00H-7FH, and Bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the four bits of the MBS. The bit to be manipulated is specified in mem.
8-bit direct addressing	mem (must be an even address)	If MBE = 0, the memory bank is Bank 0 for addresses 00H-7FH, and Bank 15 for addresses 80H-FFH. If MBE = 1, the memory bank is selected by the four bits of the MBS. The bit to be manipulated is specified in mem.
4-bit register indirect addressing	@HL, @HL+, @HL–	The memory bank is selected by the four bits of the MBS, and the location within the memory bank is contained in register HL. @HL+ : After addressing the L register automatically increments. @HL– : After addressing, the L register automatically decrements.
	@DE	The memory bank is always Bank 0, and the location within the memory bank is contained in register DE
	@DL	The memory bank is always Bank 0, and the location within the memory bank is contained in register DL
8-bit register indirect addressing	@HL (must be an even address)	The memory bank is selected by the four bits of the MBS, and the location within the memory bank is contained in register HL.
Bit manipulation addressing	fmem.bit	The memory bank is Bank 15, and the location is fmem, where fmem = FB0H- FBFH for interrupts fmem = FF0H-FFFH I/O ports The actual bit is specified in fmem.bit
	pmem.@L (where pmem= FC0H to FFFH)	The memory location is independent of MBE and MBS. The upper 10 address bits of the location are contained in the ten high order bits of pmem and the two lower address bits are contained in the two upper bits of register L. The bit to be manipulated is specified by the two LSBs of register L.
	@H + mem.bit	The memory bank is selected by the four bits of the MBS, and the location is determined by the following: The four upper bits are the contents of register H The four lower bits are mem. The actual bit is specified in mem.bit.
Stack addressing		The memory bank is always Bank 0, and the location is indicated by the stack pointer (SP)

MBE: memory bank enable bit
MB: memory bank
MBS: memory bank select register
mem: a location within a memory bank
mem.bit: a bit at a specified memory location.
fmem and pmem are specialized cases of mem.

Table 2. Addressing Modes During Peripheral Hardware Operation

Manipulation	Addressing Mode	Applicable Hardware
1-bit	With MBE = 0 (or MBE = 1 and MBS = 15) direct addressing (address in mem.bit)	All hardware where bit manipulation can be performed
	Direct addressing regardless of how MBE and MBS are set. (address in fmem.bit)	IST0, IST1, MBE, RBE IExxx, IRQxxx, PORTn (n=0 to 3)
	Indirect addressing regardless of how MBE and MBS are set. (address in pmem. @L)	BSBn.x PORTn
4-bit	With MBE = 0 (or MBE = 1 and MBS = 15) direct addressing (address in mem.bit)	All hardware where 4-bit manipulation can be performed
	With MBE = 1 and MBS = 15, register indirect addressing (address in @HL)	
8-bit	With MBE= 0 (or MBE = 1 and MBS = 15) direct addressing (address in mem); mem must be an even address	All hardware where 8-bit manipulation can be performed
	With MBE = 1 and MBS = 15, register indirect addressing (address in @HL); L register must contain an even number	

INSTRUCTIONS

The μPD751xx/P1xx provides a powerful set of 136 instructions.

Instruction Timing

The minimum instruction execution time is 0.95 μs with a 4.19 MHz clock. The PCC register can be used to program the CPU's minimum instruction cycle time to 0.95, 1.91, or 15.3 μs; all three speeds presuppose a 4.19 MHz crystal. Reducing the CPU clock speed will reduce the microprocessor's power consumption.

Instruction Set

The instruction set contains the following features:

- Versatile bit manipulation instructions
- Efficient 4-bit manipulation instructions
- 8-bit instructions
- GETI instruction to reduce program size
- Vertically stored instructions and base correction instructions
- Table reference instructions
- 1-byte relative branch instructions

The instruction set is unusually powerful for a 4-bit microcomputer. It consists of the full 75X instruction set. It contains instructions that operate on 1-bit, 4-bit, and 8-bit data. It contains 8-bit instructions generically equivalent to virtually every 4-bit instruction type. Specifically, the instruction set contains the following 8-bit instruction types:

- Arithmetic: ADD W/CARRY, ADD W/SKIP, SUB W/BORROW, SUB W/SKIP
- Logical: AND, OR, XOR
- Comparison: SKE (skip if equal)
- Transfer: MOV, MOVT, XCH, IN, OUT, PUSH, POP, BR, CALL
- Manipulation: INC W/SKIP, DEC W/SKIP

In addition, some of the 4-bit ports may be paired together to function as one 8-bit port. The combination of 8-bit ports and 8-bit instructions allows IN and OUT instructions to move full bytes of data at a time.

Organization. Tables 3 and 4 define the instruction set symbols and operand formats, found in the instruction set.

Clock Cycles. One machine cycle equals one CPU Clock Cycle ϕ. The PCC selects one of four available CPU cycle speeds.

Skip Cycles. S equals the number of extra machine cycles required for skip operation when executing a skip instruction:

- S = 0; no skip
- S = 1; one- or two-byte instruction or GETI instruction is skipped
- S = 2; three-byte instruction is skipped (BR !addr, CALL !addr)

Table 3. Instruction Set Symbols

The devices use the following symbol definitions:

Symbol	Definition
A	A register; 4-bit accumulator
B	B register; 4-bit register
C	C register; 4-bit register
D	D register; 4-bit register
E	E register; 4-bit register
H	H register; 4-bit register
L	L register; 4-bit register
X	X register; 4-bit register
XA	XA register pair; 8-bit accumulator
BC	BC register pair; 8-bit register
DE	DE register pair; 8-bit register
DL	DL register pair; 8-bit register
HL	HL register pair; 8-bit register
XA'	XA' register pair; 8-bit register
BC'	BC' register pair; 8-bit register
DE'	DE' register pair; 8-bit register
HL'	HL' register pair; 8-bit register
PC	Program counter
SP	Stack pointer
CY	Carry flag; bit accumulator
PSW	Program status word
MBE	Memory bank enable flag
RBE	Register bank enable flag
PORTn	Port n (n = 0-9, 12-14)
IME	Interrupt master enable
IPS	Interrupt priority selection register
IExxx	Interrupt enable flag
RBS	Register bank selection register
MBS	Memory bank selection register
PCC	Clock processor control register
.	Separation between address and bit
(xx)	The contents addressed by xx
xxH	Hexadecimal data

Operation Representation Format and Description Method

An operand is entered in the operand field of each instruction according to the format of the instruction (see assembler specifications). When two or more en tries are indicated in the description method, one should be selected. Capital letters and symbols must be entered exactly as shown. For immediate data, a proper numeric value or label should be entered as shown in table 4.

Table 4. Operand Formats

Symbol	Description
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC' DE', HL'
rp'1	BC, DE, HL, XA', BC' DE', HL'
rpa	HL, HL+, HL-, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem (Note 1)	8-bit immediate data or label
bit	2-bit immediate data or label
fmem	FB0H-FBFH, FF0H-FFFH immediate data or label
pmem	FC0H-FFFH immediate data or label
addr, caddr	μPD75104: 000H-FFFH immediate data or label
	μPD75106: 000H-177FH immediate data or label
	μPD75108: 000H-1F7FH immediate data or label μPD75P108: 000H-1FFFH immediate data or label
	μPD75112: 000H-2F7FH immediate data or label
	μPD75116: 000H-3F7F immediate data or label μPD75P116: 000H-3FFFH immediate data or label.
faddr	11-bit immediate data or label
taddr	20H-7EH immediate data (where bit 0 = 0) or label
PORTn	Port 0-Port 9, Port 12-Port 14
IExxx	IEBT, IESIO, IET0, IET1, IE0-IE4
RBn	RB0-RB3
MBn	MB0, MB1, MB15

Notes:

(1) Memory address must be an even number in 8-bit processing.

String Instructions

The μPD751xx/P1xx family has the following two types of string effect instructions:

(1) MOV A, #n4 or MOV XA, #n8
(2) MOV HL, #n8

String effect means to place the same type instructions in consecutive addresses. For example;

A0: MOV A, #0
A1: MOV A, #1
XA7: MOV XA, #07

If the first execution address is A0, the two subsequent instructions are treated as NOP instructions during program execution; if the first execution address is A1, the instruction that follows is treated as an NOP instruction during program execution. This means that only the first string instruction is valid, with the following string instructions being treated as NOP instructions during program execution.

The string instructions increase efficiency when setting constants into an accumulator (A register or XA register-pair) or into a data pointer (HL register pair).

Instruction Set

Mnemonic	Operand	Bytes	Machine Cycle	Operation	Skip Condition
Transfer					
MOV	A, #n4	1	1	A ← n4	String A
	reg1, #n4	2	2	reg1 ← n4	
	XA, #n8	2	2	XA ← n8	String A
	HL, #n8	2	2	HL ← n8	String B
	rp2, #n8	2	2	rp2 ← n8	
	A, @HL	1	1	A ← (HL)	
	A, @HL+	1	2+S	A ← (HL), then L←L+1	L = 0
	A, @HL–	1	2+S	A ← (HL), then L←L–1	L = FH
	A, @rpa1	1	1	A ← (rpa1)	
	XA, @HL	2	2	XA ← (HL)	
	@HL, A	1	1	(HL) ← A	
	@HL, XA	2	2	(HL) ← XA	
	A, mem	2	2	A ← (mem)	
	XA, mem	2	2	XA ← (mem)	
	mem, A	2	2	(mem) ← A	
	mem, XA	2	2	(mem) ← XA	
	A, reg1	2	2	A ← (reg1)	
	XA, rp'	2	2	XA ← rp'	
	reg1, A	2	2	reg1 ← A	
	rp'1, XA	2	2	rp'1 ← XA	
XCH	A, @HL	1	1	A ↔ (HL)	
	A, @HL+	1	2+S	A ↔ (HL), then L←L+1	L = 0
	A, @HL–	1	2+S	A ↔ (HL), then L←L–1	L = FH
	A, @rpa1	1	1	A ↔ (rpa1)	
	XA, @HL	2	2	XA ↔ (HL)	
	A, mem	2	2	A ↔ (mem)	
	XA, mem	2	2	XA ↔ (mem)	
	A, reg1	1	1	A ↔ (reg1)	
	XA, rp'	2	2	XA ↔ rp'	
MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8}+DE)_{ROM}$	
	XA, @PCXA	1	3	XA ← $(PC_{13-8}+XA)_{ROM}$	

Instruction Set (cont)

Mnemonic	Operand	Bytes	Machine Cycle	Operation	Skip Condition
Transfer (cont)					
MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	
	CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0}))	
	CY, @H+ *mem.bit*	2	2	CY ← (H+ mem_{3-0}.bit)	
	fmem.bit, CY	2	2	(fmem.bit) ← CY	
	pmem.@L, CY	2	2	($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) ← CY	
	@H+ mem.bit, CY	2	2	(H+ mem_{3-0}.bit) ← CY	
Arithmetic					
ADDS	A, #n4	1	1+S	A ← A+ n4	Carry
	XA, #n8	2	2+S	XA ← XA+ n8	Carry
	A, @HL	1	1+S	A ← A+ (HL)	Carry
	XA, rp'	2	2+S	XA ← XA+ rp'	Carry
	rp'1, XA	2	2+S	rp'1 ← rp'1 + XA	Carry
ADDC	A, @HL	1	1	A, CY ← A+ (HL)+ CY	
	XA, rp'	2	2	XA, CY ← XA+ rp'+ CY	
	rp'1, XA	2	2	rp'1, CY ← rp'1 + XA+ CY	
SUBS	A, @HL	1	1+S	A ← A–(HL)	Borrow
	XA, rp'	2	2+S	XA ← XA–rp'	Borrow
	rp'1, XA	2	2+S	rp'1 ← rp'1–XA	Borrow
SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	
	XA, rp'	2	2	XA, CY ← XA–rp'–CY	
	rp'1, XA	2	2	rp'1, CY ← rp'1–XA–CY	
AND	A, #n4	2	2	A←A ∧ n4	
	A, @HL	1	1	A←A ∧ (HL)	
	XA, rp'	2	2	XA ← XA ∧ rp'	
	rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA	
OR	A, #n4	2	2	A ← A ∨ n4	
	A, @HL	1	1	A ←A ∨ (HL)	
	XA, rp'	2	2	XA ← XA ∨ rp'	
	rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA	
XOR	A, #n4	2	2	A ← A XOR n4	
	A, @HL	1	1	A ← A XOR (HL)	
	XA, rp'	2	2	XA ← XA XOR rp'	
	rp'1, XA	2	2	rp'1 ← rp'1 XOR XA	
Accumulator Manipulation					
RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n	
NOT	A	2	2	A ← $\overline{A}$	

Instruction Set (cont)

Mnemonic	Operand	Bytes	Machine Cycle	Operation	Skip Condition
Increment/decrement					
INCS	reg	1	1+S	reg ← reg+1	reg = 0
	rp1	1	1+S	rp1 ← rp1+1	rp1 = 00H
	@HL	2	2+S	(HL) ← (HL)+1	(HL) = 0
	mem	2	2+S	(mem) ← (mem)+1	(mem) = 0
DECS	reg	1	1+S	reg ← reg−1	reg = FH
	rp'	2	2+S	rp' ← rp'−1	rp' = FFH
Comparison					
SKE	reg, #n4	2	2+S	skip if reg = n4	reg = n4
	@HL, #n4	2	2+S	skip if (HL) = n4	(HL) = n4
	A, @HL	1	1+S	skip if A = (HL)	A = (HL)
	XA, @HL	2	2+S	skip if XA = (HL)	XA = (HL)
	A, reg	2	2+S	skip if A = reg	A = reg
	XA, rp'	2	2+S	skip if XA = rp'	XA = rp'
Carry Flag Manipulation					
SET1	CY	1	1	CY ← 1	
CLR1	CY	1	1	CY ← 0	
SKT	CY	1	1+S	skip if CY = 1	CY = 1
NOT1	CY	1	1	CY ← $\overline{CY}$	
Memory Bit Manipulation					
SET1	mem.bit	2	2	(mem.bit) ← 1	
	fmem.bit	2	2	(fmem.bit) ← 1	
	pmem.@L	2	2	($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) ← 1	
	@H+ mem.bit	2	2	(H + mem_{3-0}.bit) ← 1	
CLR1	mem.bit	2	2	(mem.bit) ← 0	
	fmem.bit	2	2	(fmem.bit) ← 0	
	pmem.@L	2	2	($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) ← 0	
	@H+ mem.bit	2	2	(H + mem_{3-0}.bit) ← 0	
SKT	mem.bit	2	2+S	skip if (mem.bit) = 1	(mem.bit) = 1
	fmem.bit	2	2+S	skip if (fmem.bit) = 1	(fmem.bit) = 1
	pmem.@L	2	2+S	skip if ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) = 1	(pmem.@L = 1)
	@H+ mem.bit	2	2+S	skip if (H+ mem_{3-0}.bit) = 1	(@H+ mem.bit) = 1
SKF	mem.bit	2	2+S	skip if (mem.bit) = 0	(mem.bit) = 0
	fmem.bit	2	2+S	skip if (fmem.bit) = 0	(fmem.bit) = 0
	pmem.@L	2	2+S	skip if ($pmem_{7-2}$+ L_{3-2}.bit(L_{1-0})) = 0	(pmem.@L = 0)
	@H+ mem.bit	2	2+S	skip if (H+ mem_{3-0}.bit) = 0	(@H+ mem.bit) = 0

Instruction Set (cont)

Mnemonic	Operand	Bytes	Machine Cycle	Operation	Skip Condition
Memory Bit Manipulation (cont)					
SKTCLR	fmem.bit	2	2+S	skip if (fmem.bit) = 1 and clear	(fmem.bit) = 1
	pmem.@L	2	2+S	skip if ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) = 1 and clear	(pmem.@L = 1)
	@H+ mem.bit	2	2+S	skip if (H+mem_{3-0}.bit) = 1 and clear	(@H+ mem.bit) = 1
AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	
	CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	
	CY, @H+ mem.bit	2	2	CY ← CY ∧ (H+mem_{3-0}.bit)	
OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	
	CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	
	CY, @H+ mem.bit	2	2	CY ← CY ∨ (H+mem_{3-0}.bit)	
XOR1	CY, fmem.bit	2	2	CY ← CY **XOR** (fmem.bit)	
	CY, pmem.@L	2	2	CY ← CY **XOR** ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	
	CY, @H+ mem.bit	2	2	CY ← CY **XOR** (H+mem_{3-0}.bit)	
Branch					
BR (Note 1)	addr	–	–	PC_{13-0} ← addr	
	!addr (Note 1)	3	3	PC_{13-0} ← addr	
	$addr	1	2	PC_{13-0} ← addr	
BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13,12}$+$caddr_{11-0}$	
BR	PCDE	2	3	PC_{13-0} ← PC_{13-8}+DE	
	PCXA	2	3	PC_{13-0} ← PC_{13-8}+XA	
Subroutine Stack Control					
CALL	!addr	3	3	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← (MBE, RBE, $PC_{13,12}$) PC_{13-0} ← addr, SP ← (SP–4)	
CALLF	!faddr	2	2	(SP–4)(SP–1)(SP–2) ← PC_{11-0} (SP–3) ← (MBE, RBE, $PC_{13,12}$) PC_{13-0} ← 00, faddr, SP ← (SP–4)	
RET		1	3	(MBE, RBE, $PC_{13,12}$) ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← (SP+4)	
RETS		1	3+S	(MBE, RBE, $PC_{13,12}$) ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← (SP+4), then skip unconditionally	Unconditional
RETI		1	3	($PC_{13,12}$) ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← (SP+6)	
PUSH	rp	1	1	(SP–1)(SP–2) ← rp, SP ← (SP–2)	
	BS	2	2	(SP–1) ← MBS, (SP–2) ← RBS, SP ← (SP–2)	
POP	rp	1	1	rp ← (SP+1)(SP), SP ← (SP+2)	
	BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← (SP+2)	

Instruction Set (cont)

Mnemonic	Operand	Bytes	Machine Cycle	Operation	Skip Condition
Interrupt Control					
EI		2	2	IME ← 1	
	IExxx	2	2	IExxx ← 1	
DI		2	2	IME ← 0	
	IExxx	2	2	IExxx ← 0	
Input/Output (Note 2)					
IN	A, $PORT_n$	2	2	A ← $PORT_n$; (n = 0 to 9, 12-14)	
	XA, $PORT_n$	2	2	XA ← $PORT_{n+1}$, $PORT_n$; (n = 4, 6, 8, 12)	
OUT	$PORT_n$, A	2	2	$PORT_n$ ← A; (n = 2 to 9, 12-14)	
	$PORT_n$, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA; (n = 4, 6, 8, 12)	
CPU Control					
HALT		2	2	Set HALT mode (PCC.2 ← 1)	
STOP		2	2	Set STOP mode (PCC.3 ← 1)	
NOP		1	1	No operation	
Special					
SEL	RB_n	2	2	RBS ← n; (n = 0-3)	
	MB_n	2	2	MBS ← n; (n = 0, 1, 15)	
GETI	taddr	1	3	When the table is specified by the TBR instruction, PC_{11-0} ← $(taddr)_{3-0}$ + (taddr+1) When the table is specified by the TCALL instruction (SP-4)(SP-1)(SP-2) ← PC_{11-0}; (SP-3) ← (MBE, RBE, $PC_{13,12}$); PC_{13-0} ← $(taddr)_{5-0}$ + (taddr+1); SP ← SP-4 When the table is specified by any other instructions, the (taddr), (taddr+1) instructions are executed. (Note 3)	Depends on the referenced instruction

Notes:

(1) Appropriate instructions are selected from BR !addr, BRCB !caddr, and BR $addr by the assembler. (BR !addr is not available on the μPD75104/104A)

(2) When executing the IN/OUT instruction, either MBE must be reset to 0, or MBE and MBS must be set to 1 and 15, respectively.

(3) TBR and TCALL are pseudoinstructions used only to specify these tables.

Table 5. Digital Port Features

Port Number	Type	Operational Features	Comments
Port 0	4-bit input	Can be read or tested at any time regardless of the functional mode of the shared pins.	Pins are also used for SI, SO, $\overline{SCK}$, and INT4.
Port 1	4-bit input	Can be read or tested at any time regardless of the functional mode of the shared pins.	Pins also used for INT0-INT3. On the μPD75104A/108A, internal pull-up resistors are available for each line as a mask option.
Port 3 Port 6	4-bit I/O	Can be set for input or output mode in 1-bit units.	On the μPD75104A/108A, internal pull-up resistors are available for each line of port 6 as a mask option.
Port 2 (Note 1)	4-bit I/O	Can be set for input or output mode in 4-bit units.	Pins are also used for PTO0, PTO1, and PCL.
Port 4 Port 5 Port 7 Port 8 Port 9 (Note 1)	4-bit I/O	Can be set for input or output mode in 4-bit units. Ports 4-5, 6-7, and 8-9 can be paired together to enable 8-bit data transfers.	On the μPD75104A/108A, internal pull-up resistors are available for each line as a mask option.
Port 12 Port 13 Port 14 (Notes 1, 2)	4-bit I/O	Can be set for input or output mode in 4-bit units; Ports 12 and 13 can be paired to form a single 8-bit I/O port.	Except for μPD75P108/P116, internal pull-up resistors are available for each line as a mask option.

Notes:

(1) Ports 2-9 and 12-14 can directly drive LEDs. Total current must not exceed 200 mA (peak).

(2) The output stage of ports 12-14 contains an N-channel open-drain transistor capable of withstanding 12 V.

Input/Output Ports

There are thirteen 4-bit ports; some are I/O ports and some are input only. Figure 4 shows the structure of the ports and table 5 lists the features. Figure 4 also shows the structure of inputs and outputs of the other pins.

Clock Generator

The clock generator (figure 5) uses the crystal inputs X1 and X2 as a time base to provide clocks for the μPD751xx/P1xx . The generator consists of an oscillator, frequency dividers, multiplexers, and two control registers, (PCC and CLOM). By programming PCC and CLOM, frequencies derived from the crystal are supplied to the CPU, the interval timer, the timer/event counter, the serial interface, and the output pin, PCL.

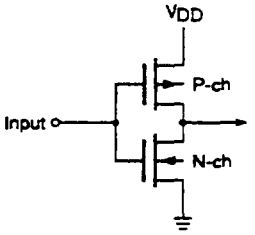
The PCC register controls the HALT and STOP logic and can also be used to set the CPU to operate at one of three speeds. The CLOM register controls the output clock PCL.

Basic Interval Timer

The basic interval timer (figure 6) is used to provide continuous real-time interrupts. It consists of a multiplexer, an 8-bit free-running counter, and a 4-bit control register (BTM). Each time the counter reaches FFH it causes an interrupt, overflows to 00H and continues to count. The BTM register is used to select one of four clock inputs to the counter as well as clear the counter and its interrupt request. The counter can generate 250 ms interrupts with a 4.19 MHz crystal and also provides oscillator stabilization time when the chip comes out of the STOP mode.

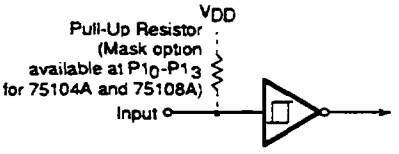
Figure 4. I/O Circuits

Type A
(for Type E)



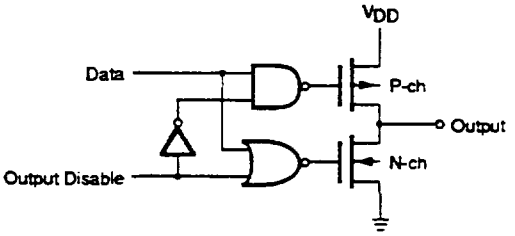
CMOS standard input buffer

Type B
($P0_0$, $P0_3$, $P1_0$-$P1_3$, TI0, TI1, RESET)



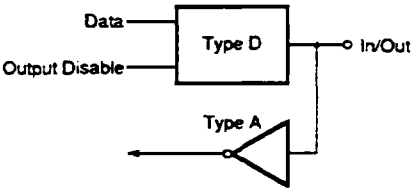
Schmitt trigger input with
hysteresis characteristic.

Type D
(For Type E, F)



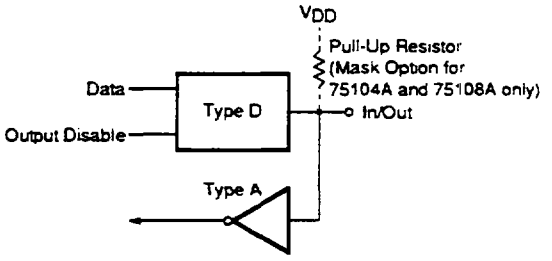
Push-pull output where output can be placed in high impedance. P and N channels are turned off.

Type E
($P0_2$, $P2_0$-$P2_3$, $P3_0$-$P3_3$)



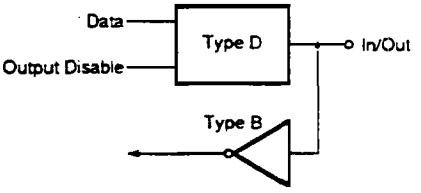
Input/Output circuit composed of a Type D push-pull output and a Type A input buffer.

Type E-A
($P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P7_0$-$P7_3$, $P8_0$-$P8_3$, $P9_0$-$P9_3$)



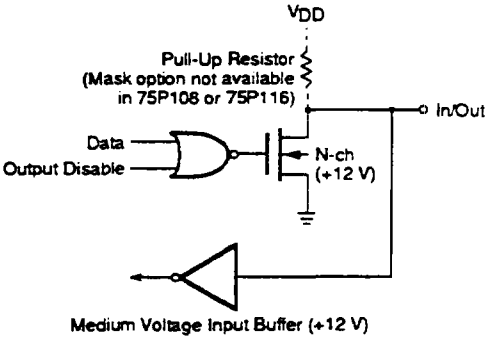
Input/output circuit composed of a Type D push-pull output and a Type A input buffer.

Type F
($P0_1$)



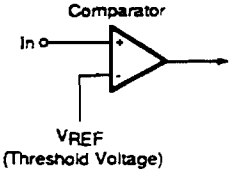
Input/output circuit composed of a Type D push-pull output and a Type B Schmitt trigger input.

Type M-A
($P12_0$-$P12_3$, $P13_0$-$P13_3$, $P14_0$-$P14_3$)



Medium Voltage Input Buffer (+12 V)

Type N
($PTH0_0$-$PTH0_3$)



49NR-725B

Figure 5. Clock Generator

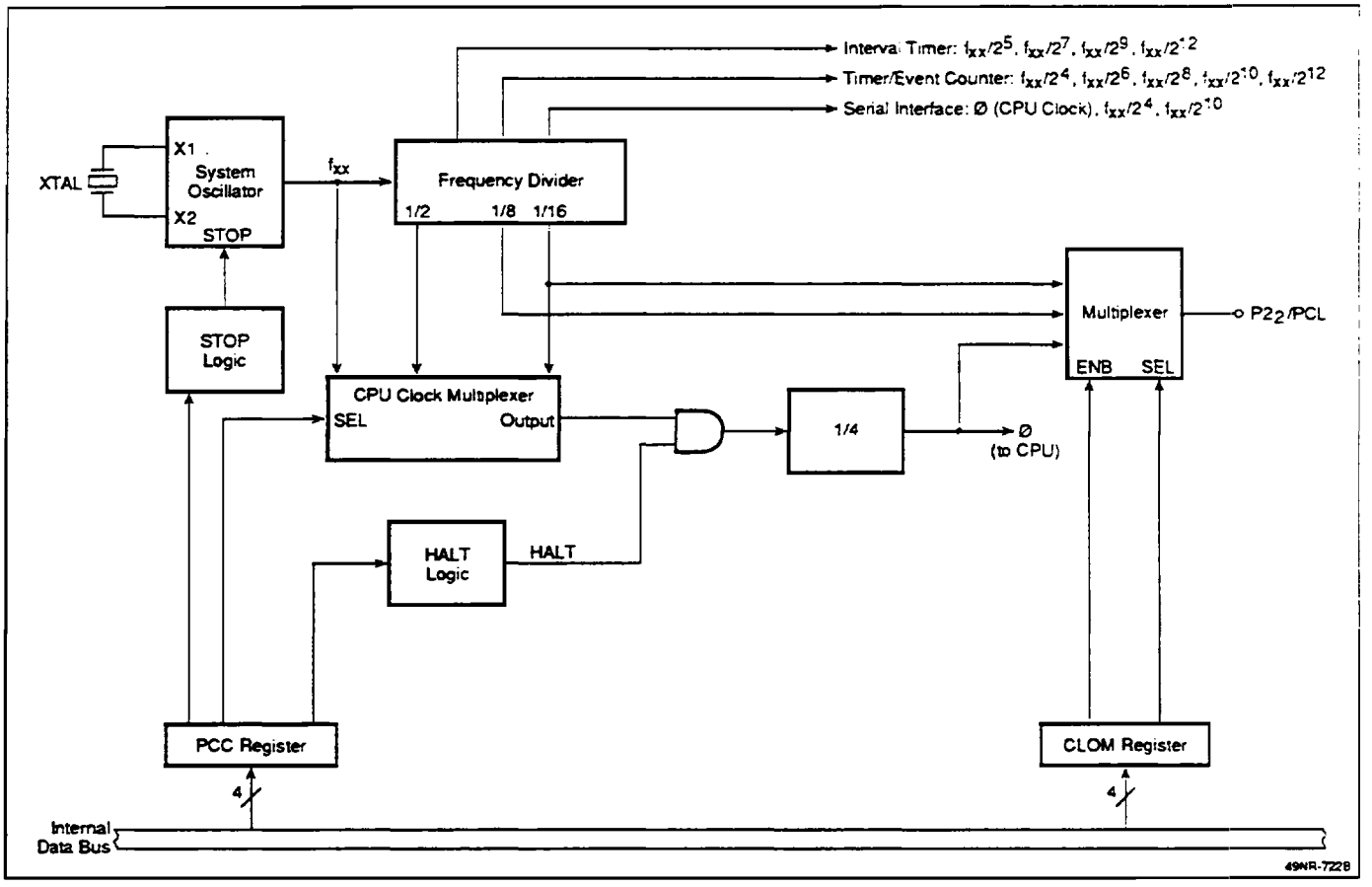
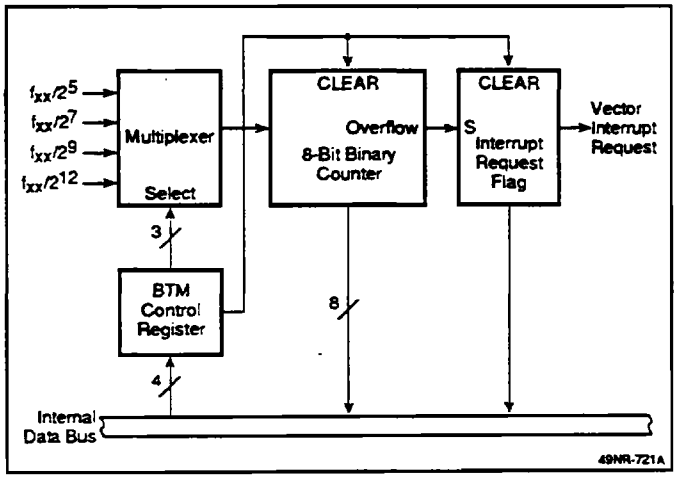


Figure 6. Basic Interval Timer



Timer/Event Counters

Each of the two timer/event counters (figure 7) consists of an 8-bit modulo register, 8-bit comparator, 8-bit count register, clock multiplexer, mode control register, and a TOUT flip flop. There is also some control logic so that the timer's TOUT flip flop can be sent to port 2.

The two timers differ only by the clock selection to the count register. Timer 0 has an $f_{xx}/16$ clock input, and Timer 1 has an $f_{xx}/4096$ clock input. TI0 and TI1 can also be used as external clock inputs to count events.

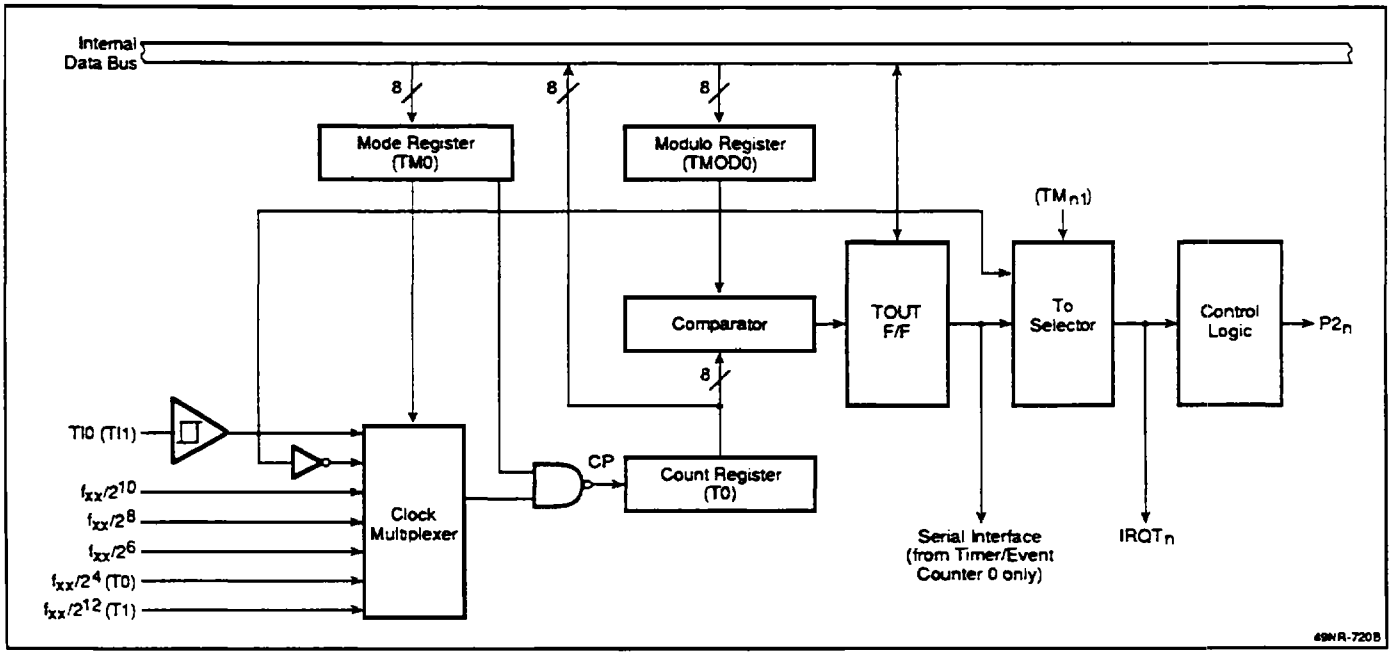
An 8-bit value is loaded into the modulo register, and a count register clock is selected by the clock multiplexer, via control register TM0 (or TM1 for counter 1). The count register is incremented each time it receives a CP pulse. When the value in the count register is equal to the count in the modulo register, the comparator generates a signal which toggles the TOUT flip flop and causes the count register to be reset to 00H. The count register will continue to count up unless stopped. Each time TOUT changes state it causes an interrupt. This signal can also be used as a clock for the serial interface.

Serial Interface

The 8-bit serial interface (figure 8) allows the μPD751xx/P1xx to communicate with other NEC or NEC-like serial interfaces. It consists of an 8-bit shift register, 3-bit counter, clock multiplexer, and control register SIOM. The three-wire interface consists of the serial data in (SI), serial data out (SO), and serial shift clock ($\overline{SCK}$).

The 8-bit shift register is loaded with a byte of data, and when bit 3 of SIOM is set, 8 clock pulses are generated. These pulses shift data out the SO line and data in from the SI line, thus, communicating in full duplex. Each time bit 3 of SIOM is set, a burst of eight clock pulses is generated and eight bits of data will be sent. Data may be sent either LSB or MSB first. The interface may also be set to receive data only; in this case SO is in the high-impedance state. One of four internal clocks or an external clock may be used to clock the data.

Figure 7. Timer/Event Counter



Comparator Port

The four-input comparator port (figure 9) contains a resistor ladder with 4-bit resolution, a 4-1 multiplexer, a comparator, a 1-4 demultiplexer, and an input result register, PTH0. This port is controlled by the 8-bit PTHM register and operates in a sequential manner. When bit 7 of the PTHM starts the comparator, the comparator reads and converts input PTH3, then the others in order, ending with PTH0. Then the PTH0 register may be read to get the results.

The user may select a slow or fast conversion time. With a 4.19 MHz crystal, total time required to convert all four inputs is 258 μs and 32.3 μs, respectively.

Bit Sequential Buffer

The bit sequential buffer is 16 bits of general-purpose RAM located in the upper half of memory bank 15, and is the only general-purpose RAM in this area. All other locations in this bank contain either the on-chip peripheral control registers or are unused addresses. A typical application of this buffer might be to store data for the next serial output or to store data from a serial input. It could also be used to store data which is to be sent from a port. This area can be bit, nibble, or byte manipulated.

Interrupts

The μPD751xx/P1xx family interrupts (figure 10) are all vectored; there are five external and four internal interrupts. Table 4 gives a summary of the interrupts. The hardware provides two levels of interrupt nesting; interrupt priorities can be changed via register IPS. Inputs INT2 and INT3 will detect rising edges and generate an interrupt request flag which is testable. Neither INT2 nor INT3 will cause an interrupt, but they can be used to release the STANDBY mode.

Figure 8. Serial Interface Block Diagram

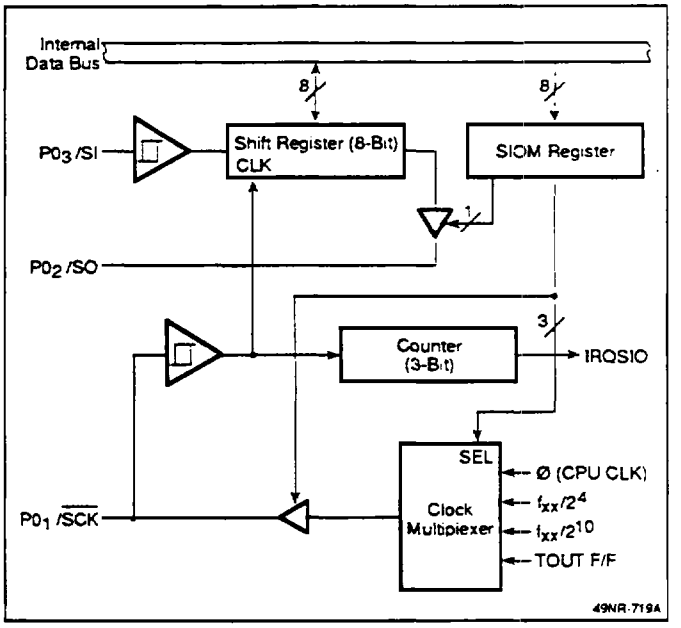


Figure 9. Comparator Port

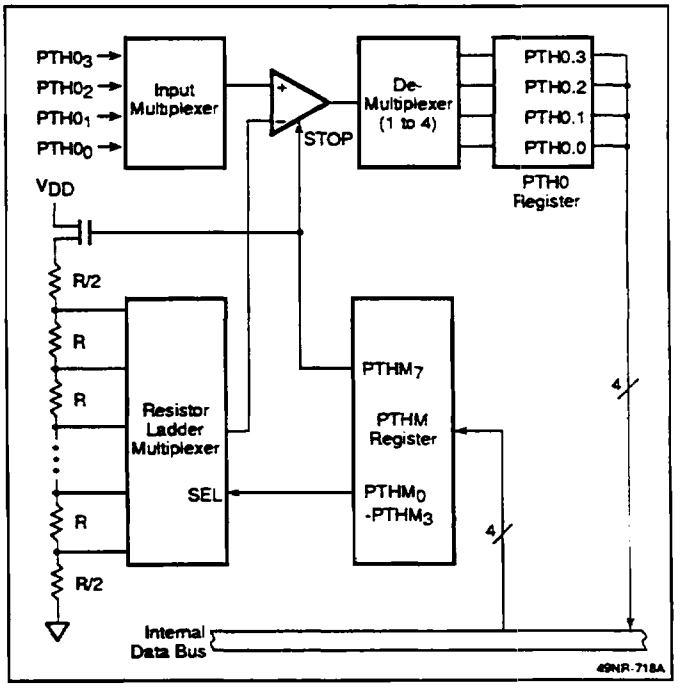
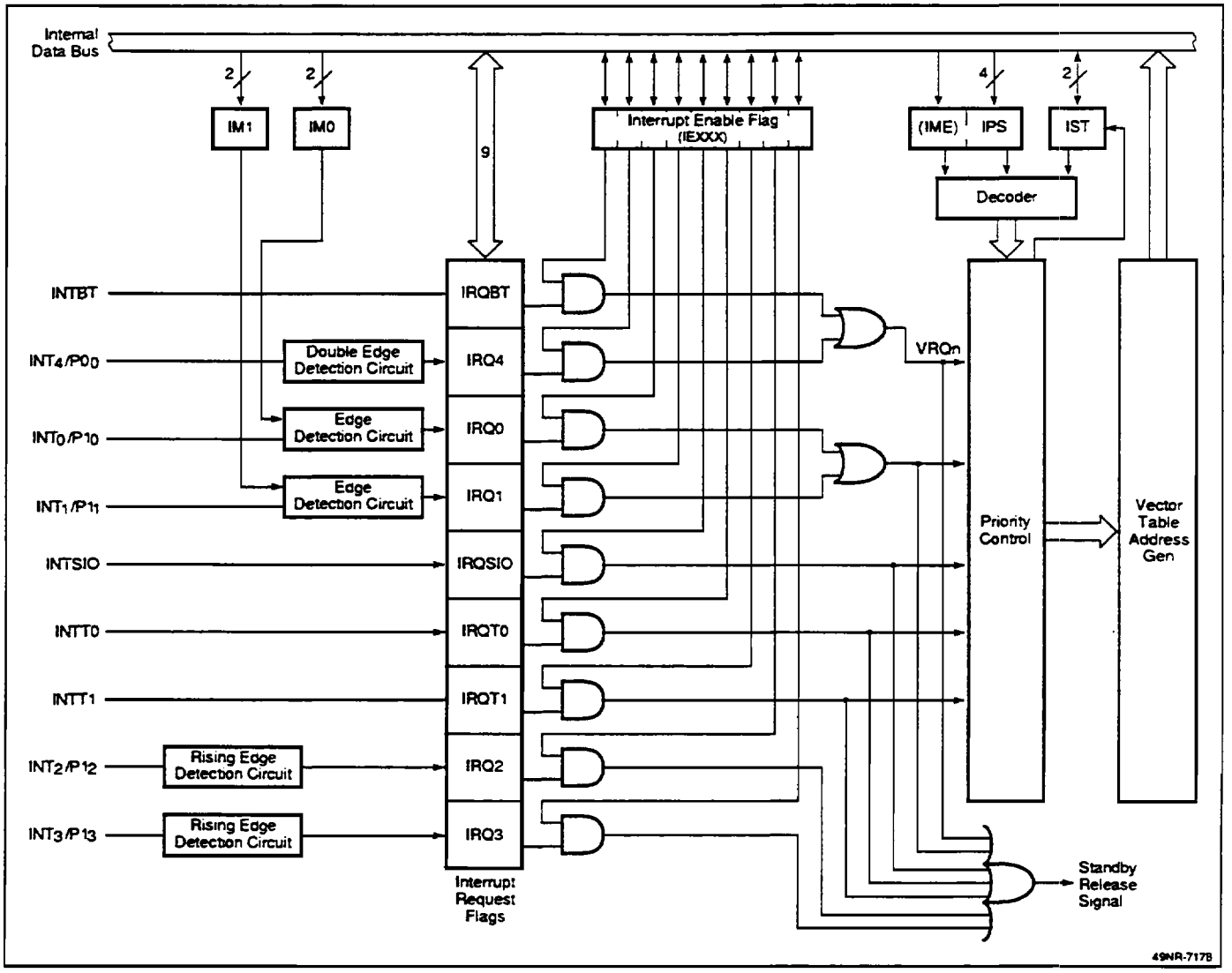


Figure 10. Interrupt Controller Block Diagram



Standby Modes

The standby mode is summarized in table 7 and consists of three submodes, HALT, STOP, and Data Retention.

HALT mode. The HALT mode is entered by executing the HALT instruction. In this mode, the clock to the CPU is shut off (thus stopping the CPU), while all other parts of the chip remain fully functional.

STOP mode. The STOP mode is entered by executing the STOP instruction. In this mode, the chip's main system oscillator is shut off, thereby stopping all portions of the chip.

The HALT and STOP modes are released by a $\overline{\text{RESET}}$ or by any interrupt request.

Data Retention mode. This mode may be entered after entering the STOP mode. Here, supply voltage V_{DD} may be lowered to 2 volts to further reduce power consumption. The contents of the RAM and registers are retained. This mode is released by first raising V_{DD} to the proper operating range, then releasing the STOP mode.

Table 6. Interrupt Sources

Interrupt Source	Operation and Source	Internal/ External	Interrupt Priority	Vectored Interrupt Request Signal (Vector Table Address)
INTBT	Reference time interval signal from basic interval timer	Internal	1	VRQ1 (002H)
INT4	Both rising and falling edge detection	External		
INT0	Selection of rising or falling edge detection	External	2	VRQ2 (0004H)
INT1	Selection of rising or falling edge detection	External		
INTSIO	Serial data transfer completion signal	Internal	3	VRQ3 (0006H)
INTT0	Coincidence signal between timer/counter 0, or edge detection of TI0 input	Internal/External	4	VRQ4 (0008H)
INTT1	Coincidence signal between timer/counter 1, or edge detection of TI1 input	Internal/External	5	VRQ5 (000AH)
INT2	Rising edge detection	External	Testable input signals (IRQ2 and IRQ3 are set)	
INT3	Rising edge detection	External		

Table 7. Standby Mode Operation

Item	STOP Mode	HALT Mode
Setting the mode	STOP Instruction	HALT Instruction
Clock oscillator	The main system clock oscillator is stopped	Only CPU clock ϕ is stopped (oscillation continues)
Basic interval timer	Operation stopped	Can Operate (IRQBT is set by reference time interval)
Serial interface	Can operate only when external $\overline{SCK}$ input is selected for serial clock. (Note 1)	Can operate if other than CPU clock ϕ is specified as serial clock
Timer/event counter	Can operate only when TIn (n = 0, 1) pin input is selected for count clock	Can operate
Clock output circuit	Stops operation	Can operate if other than CPU clock ϕ is specified
CPU	Operation stopped	Operation stopped
Retained data	Contents of all registers (general registers, flags, mode registers, and output latches) and contents of data memory retained	
Release signal	Interrupt request signal (enabled with interrupt enable flag) from operating hardware or $\overline{RESET}$	

Notes:

(1) Can also operate with TI0 selected as the serial clock, but only when Timer/Event Counter 0 is operated with an external TI0 input.

RESET and the Reset Generator

The power-on-reset (POR) generator (figure 11) is always present in the μPD75P108, not present in the μPD75P116, and available by mask option in the mask ROM devices.

The POR circuit generates a one-shot pulse by detecting the supply voltage rising edge. Use of this pulse is determined by mask option:

(1) Both SWA and SWB are ON.
When the power supply rising edge is detected, the internal reset signal ($\overline{RES}$) is generated and the power-on flag (PONF) is set at the same time.

(2) SWA only is ON.
When the power supply rising edge is detected, PONF is set. ($\overline{RES}$ is not generated automatically.)

(3) Both SWA and SWB are OFF.
The power-on reset generator and and power-on flag are disabled. $\overline{RES}$ is generated only by the $\overline{RESET}$ input.

Figure 11. Power-On-Reset Signal Generator and PONF

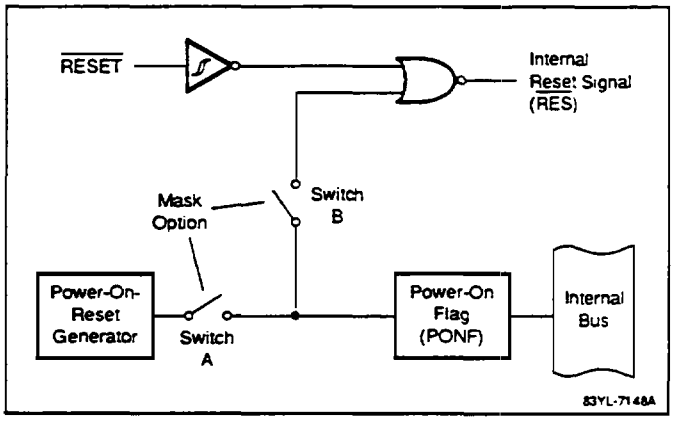


Table 8. State of the Device after Reset

Hardware		$\overline{RESET}$ Inputted During Standby Mode	$\overline{RESET}$ Inputted During Normal Operation or Power-on
Program counter (PC)		*The six low-order bits of program memory address 000H are loaded into PC13–PC8. The contents of address 0001H are loaded into PC7–PC0.*	
PSW	Carry flag (CY)	Held	Undefined
	Skip flags (SK0, SK1, SK2)	0	0
	Interrupt status flags (IST0, IST1)	0	0
	Bank enable flags (MBE, RBE)	Bit 6 of program memory address 000H is loaded into RBE and bit 7 into MBE.	
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held (Note 1)	Undefined
General purpose registers (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection registers (MBS, RBS)		0, 0	0, 0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter (n= 0, 1)	Counter (Tn)	0	0
	Modulo register (TMODn)	FFH	FFH
	Mode register (TMn)	0	0
	TOEn, TOFn	0, 0	0, 0
Serial interface	Shift register (SIO)	Held	Undefined
	Mode register (SIOM)	0	0

Table 8. State of the Device after Reset (cont)

Hardware		$\overline{\text{RESET}}$ Inputted During Standby Mode	$\overline{\text{RESET}}$ Inputted During Normal Operation or Power-on
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt function	Interrupt request flags (IRQxxx)	Reset to 0	Reset to 0
	Interrupt enable flags (IExxx)	0	0
	Priority selection register (IPS)	0	0
	INT0, and INT1 mode registers (IM0, IM1)	0, 0	0, 0
Digital ports	Output buffers	Off	Off
	Output latches	Cleared (to 0)	Cleared (to 0)
	Input/output mode registers (PMGA, PMGB, PMGC)	0	0
Bit sequential buffer		0	0
Analog port	PTH00-03 input latches	Undefined	Undefined
	Mode register (PTHM)	0	0
Power-on flag (PONF)		Undefined	1, Undefined (Note 2)
Bit sequential buffer (BSB0-3)		0	0

Notes:

(1) Addresses 0F8H to 0FDH are undefined after RESET.

(2) This value is 1 upon power-on-reset and undefined during normal operation.

EPROM Write/Verify

The μPD75P108 contains 8192 bytes of EPROM, while the μPD75P116 has 16256 bytes. Table 9 shows the pin functions during the Write/Verify cycles. Note that it is not necessary to enter an address, since the address is updated by pulsing the clock pins. When V_{DD} = 6 V and V_{PP} = 21 V in the μPD75P108 (or V_{PP} = 12.5 V in the μPD75P116) are applied, the EPROM is placed in the write/verify mode. The operation is selected by the MD0–MD3 pins, as shown in table 10.

Table 9. EPROM Write/Verify Pin Functions

Pin Name	Function
X1, X2	After a write/verify write, the X1, and X2 clock pins are pulsed. (Note that these pins are also pulsed during a read.)
MD0–MD3	These are the operation mode selection pins.
$P4_0$–$P4_3$ (four low-order bits) $P5_0$–$P5_3$ (four high-order bits)	8-bit data input/output pins for write/verify
V_{DD}	Supply voltage. Normally 5 volts; 6 volts is applied during write/verify
V_{PP}	Normally 5 volts; V_{PP} = 21 V in the μPD75P108 (or V_{PP} = 12.5 V in the μPD75P116) during write/verify

Notes:

(1) A cover should be placed over the UV erase window. The OTP devices do not have windows, thus the EPROM contents cannot be erased.

Caution

Apart from their normal functions, The $P0_0$/INT4 and $\overline{RESET}$ pins are used to test the internal operation of the programmable devices. The test mode is entered by applying a voltage greater than V_{DD} to either of these pins.

For this reason, care must be taken to limit the voltage applied to these two pins. For example, it is conceivable that even during normal operation enough spurious noise may be present to set the chip into the test mode. If this happens, further normal operation is impossible. Consequently, it is important that interwiring noise be suppressed as much as possible. If this is inconvenient, anti-noise measures, like those shown in figure 12, should be implemented.

The write/verify mode is entered by applying 6 volts to V_{DD} and V_{PP} = 21 V in the μPD75P108 (or V_{PP} = 12.5 V in the μPD75P116). Mode is determined by the setting of the MD0-MD3 pins; all other pins are tied to ground by pulldown resistors.

Figure 12. Noise Reduction Techniques

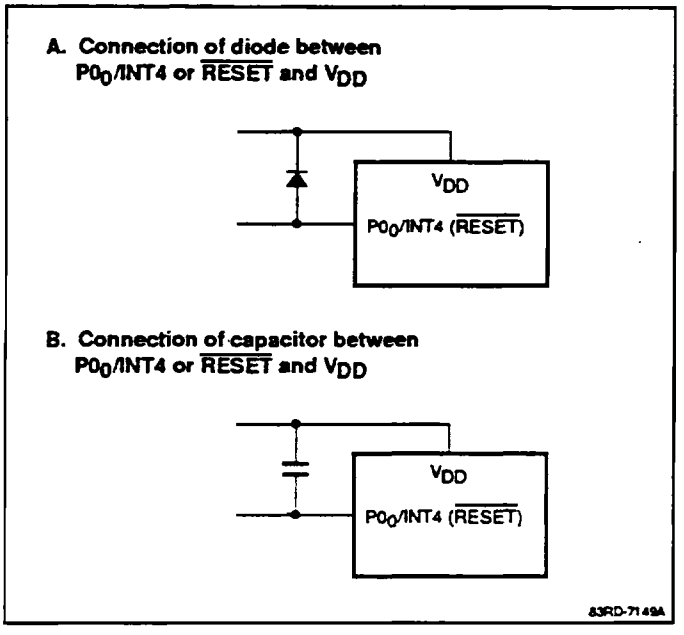


Table 10. Write/Verify Operation

V_{PP} = 21 V in the μPD75P108, V_{PP} = 12.5 in the μPD75P116, V_{DD} = +6.0 V

Operation Mode Specification				
MD0	**MD1**	**MD2**	**MD3**	**Operation Mode**
1	0	1	0	Clear program memory address
0	1	1	1	Write mode
0	0	1	1	Verify mode
1	X	1	1	Program inhibit

Notes:

(1) X = Don't care.

EPROM Write/Verify Procedure

EPROMs can be written at high speed using the follow ing procedure:

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply 5 volts to the V_{DD} and V_{PP} pins.

(3) Wait for 10 μs.

(4) Select the *clear program memory address* mode.

(5) For the μPD75P108, supply 6 volts to V_{DD} and 21.0 volts to V_{PP}. For the μPD75P116, supply 6 volts to V_{DD}, and 12.5 volts to V_{PP}.

(6) Select the *program inhibit* mode.

(7) Write data in the 1 ms write mode.

(8) Select the *program inhibit* mode.

(9) Select the *verify* mode. If the data is correct, proceed to step 10. If not, repeat steps 7, 8, and 9.

(10) Perform one additional write with an MD0 pulse width equal in ms to the number of *writes* performed in step 7, times 1 ms.

(11) Select the *program inhibit* mode.

(12) Apply four pulses to the X1 pin to increment the program memory address by one.

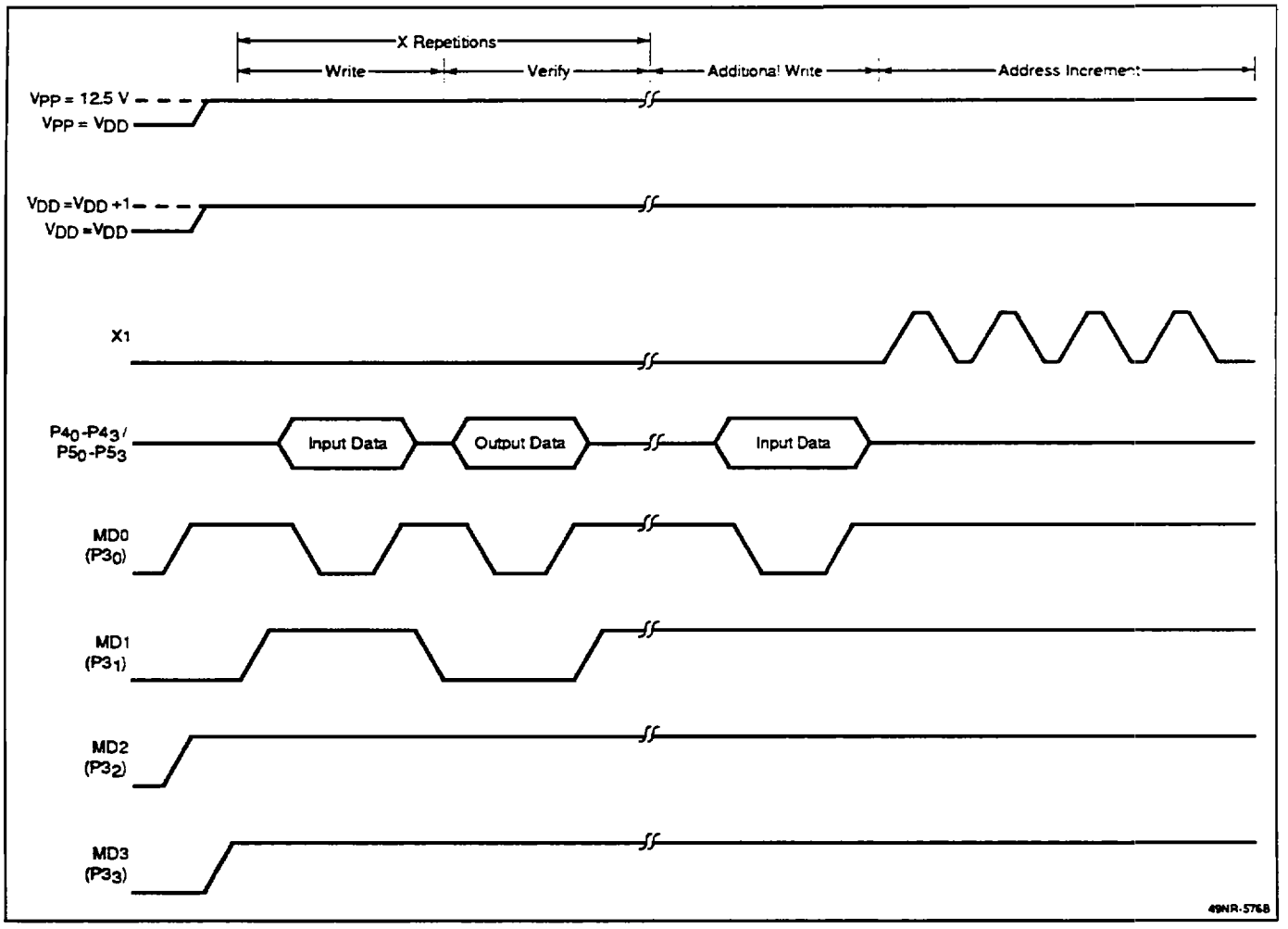
(13) Repeat steps 7-12 until the end address is reached.

(14) Select the *clear program memory address* mode.

(15) Return the V_{DD} and V_{PP} pins back to + 5 volts.

(16) Turn off the power.

Figure 13. EPROM Write/Verify Cycle Timing



EPROM Read Procedure

The EPROM contents can be read by using the following procedure:

(1) Pull unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply 5 volts to the V_{DD} and V_{PP} pins.

(3) Wait for 10 μs.

(4) Select the *clear program memory address* mode.

(5) For the μPD75P108, supply 6 volts to V_{DD} and 21.0 volts to V_{PP}. For the μPD75P116, supply 6 volts to V_{DD}, and 12.5 volts to V_{PP}.

(6) Select the *program inhibit* mode.

(7) Select the *verify* mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.

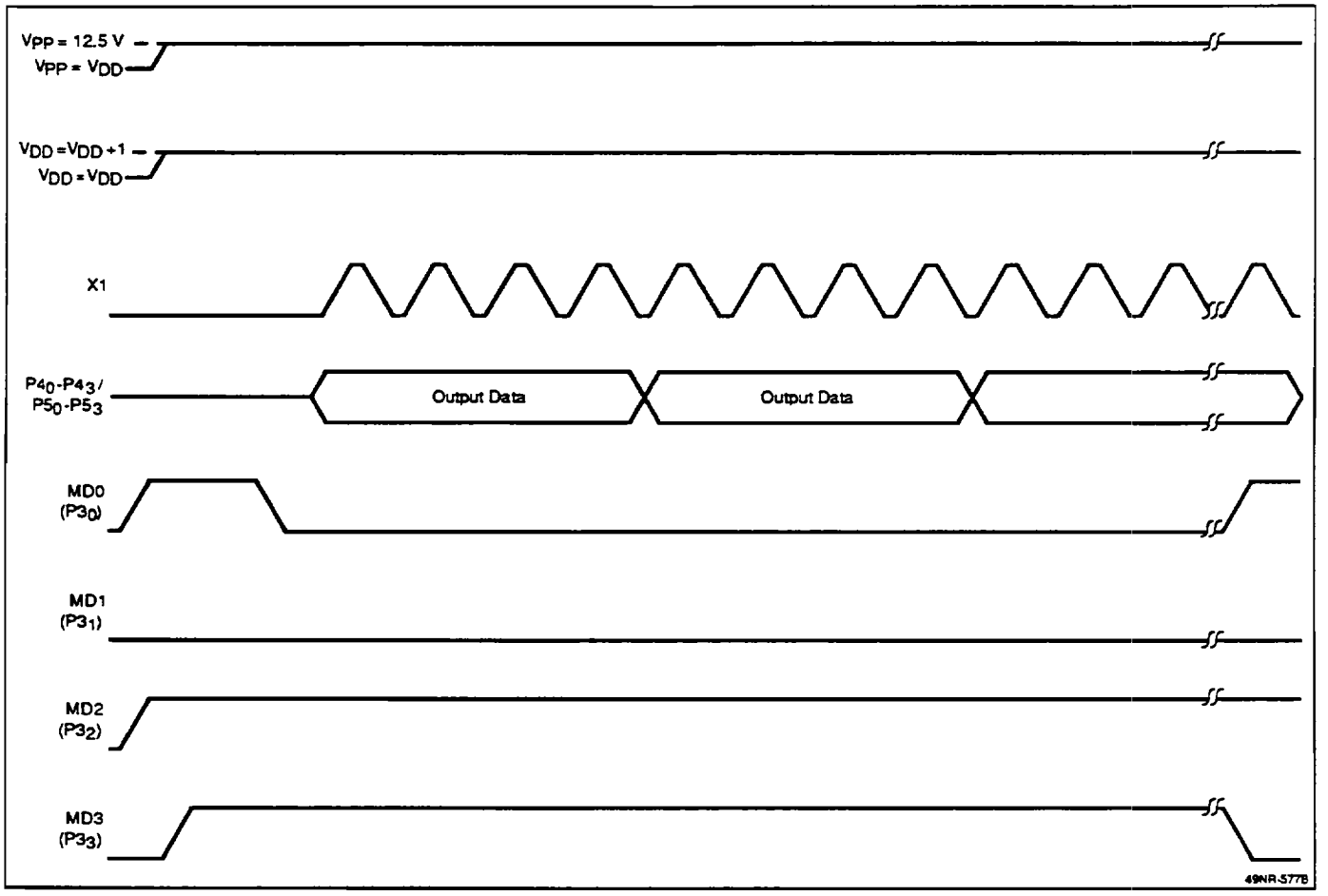
(8) Select the *program inhibit* mode.

(9) Select the *clear program memory address* mode.

(10) Return the V_{DD} and V_{PP} pins to + 5 volts.

(11) Turn off the power.

Figure 14. EPROM Read Cycle Timing



Program Memory Erase (μPD75P108DW only)

The μPD75P108DW allows the programmed data contents to be erased by light rays whose wavelength is shorter than about 400 nm. The programmed data contents may also be erased if the uncovered window is exposed to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the window with an opaque film. NEC provides quality-tested shading film with each UV EPROM shipment.

For normal EPROM erase, place the device under an ultraviolet light source (254 nm). The minimum amount of radiation exposure required to erase the μPD75P108DW completely is 15 Ws/cm^2 (ultraviolet ray strength times erase time). This corresponds to about 15 to 20 minutes when using a UV lamp of 12 V_{PP} μW/cm^2. However, the erase time may be prolonged if the UV lamp is old or if the device window is dirty. The distance between the light source and the window should be 2.5 cm or less.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (μPD751xx)

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_{I1} (ports 12-14)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 12-14; internal pull-up resistor)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 12-14; open drain)	−0.3 to +13 V (Note 1)
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH} (Single pin)	−15 mA
High-level output current, I_{OH} (Total of all pins)	−30 mA
Low-level output current, I_{OL} (Single pin)	30 mA pk
	15 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 0, 2–4, 12–14)	100 mA pk
	60 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 5–9)	100 mA pk
	60 mA rms (Note 2)
Operating temperature, t_{OPT}	−40 to + 85°C
Storage temperature, t_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Notes:

(1) When applying more than 10 V to ports 12, 13, or 14, the external pull-up resistor must be at least 50 kΩ.

(2) rms value = pk x (duty cycle)$^{1/2}$.

Capacitance (μPD751xx)

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}	15	pF	
I/O capacitance	C_{IO}	15	pF	

Oscillator Characteristics (All devices)

μPD751xx: T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V
μPD75P108: T_A = −10 to +85°C; V_{DD} = 4.5 to 5.5 V
μPD75P116: T_A = −40 to +85°C; V_{DD} = 4.5 to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 15A)	Oscillation frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	After V_{DD} reaches oscillation voltage
Crystal resonator (Figure 15A)	Oscillation frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	Oscillation stabilization time (Note 2)				10 (Note 3)	ms	V_{DD} = 4.5 to 6.0 V
					30 (Note 3)	ms	
External clock (Figure 15B)	X1 input frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	X1 input high/low level width	t_{XH}, t_{XL}	100		250	ns	

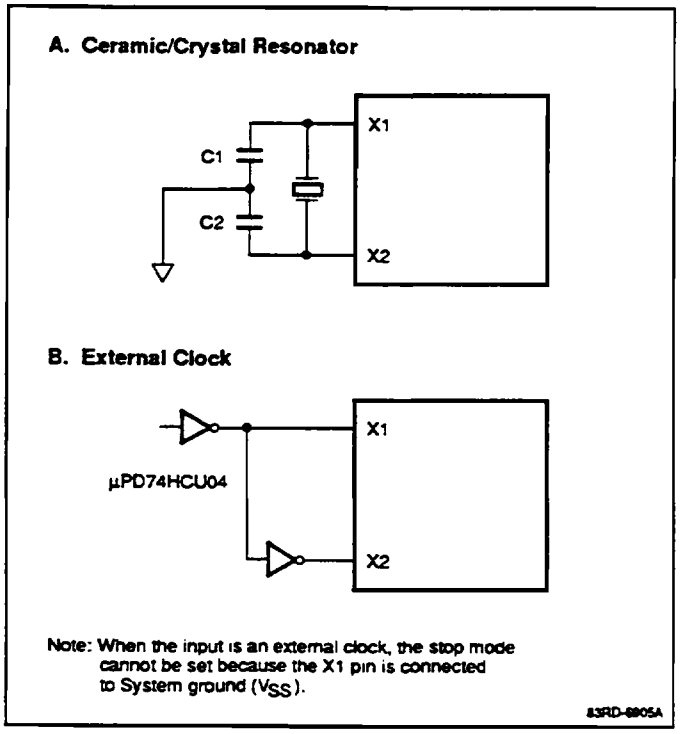
Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage is applied or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's spec sheets.

Figure 15. System Clock Configurations



Recommended Ceramic Resonators (μPD751xx)

Manufacturer	Part Number	C1 (pF)	C2 (pF)	Remarks
Murata	CSA 2.00MG	30	30	V_{DD} = 2.7 to 6.0 V
	CSA 4.19MG	30	30	V_{DD} = 3.0 to 6.0 V
	CSA 4.19MGU	30	30	V_{DD} = 2.7 to 6.0 V
	CST 4.19T (Note 1)	—	—	V_{DD} = 3.0 to 6.0 V
Kyocera	KBR-2.0MS	100	100	V_{DD} = 3.0 to 6.0 V
	KBR-4.0MS	33	33	
	KBR-4.19MS	33	33	
	KBR-4.9152M	33	33	

Notes:

(3) C1 and C2 are contained in the oscillator

Recommended Crystal Resonator (μPD751xx)

Manufacturer	Frequency (MHz)	Part Number (note 1)	C1 (pF)	C2 (pF)	Remarks
Kinseki	4.19	HC-49/U	22	22	V_{DD} = 2.7 to 6.0 V

Notes:

(1) Equivalent series resistance of crystal must be less than 80 Ω

Comparator Characteristics (All devices)

μPD751xx: V_{DD} = 4.5 to 6.0 V; T_A = −40 to +85°C
μPD75P108: T_A = −10 to +85°C; V_{DD} = 4.5 to 5.5 V
μPD75P116: T_A = −40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Comparison accuracy	V_{ACOMP}			±100	mV	
Threshold voltage	V_{TH}	0		V_{DD}	V	
PTH input voltage	V_{IPTH}	0		V_{DD}	V	
Comparator consumption current	I_{COMP}		1		mA	Set PTHM7 to 1

DC Characteristics (μPD751xx)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Except ports 0, 1, 12-14, TI0, TI1, $\overline{RESET}$, X1, X2
	V_{IH2}	$0.8V_{DD}$		V_{DD}	V	Ports 0, 1, TI0, TI1 and $\overline{RESET}$
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 12-14; built-in pull-up resistor
		$0.7V_{DD}$		12	V	Ports 12-14; open drain
	V_{IH4}	V_{DD}−0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		$0.3V_{DD}$	V	Except ports 0, 1, TI0, TI1, $\overline{RESET}$, X1, X2
	V_{IL2}	0		$0.2V_{DD}$	V	Ports 0, 1, TI0, TI1 and $\overline{RESET}$
	V_{IL3}	0		0.4	V	X1, X2
High-level output voltage	V_{OH}	V_{DD}−1.0			V	V_{DD} = 4.5 to 6.0 V; I_{OH} = −1 mA
		V_{DD}−0.5			V	V_{DD} = 2.7 to 6.0 V; I_{OH} = −100 μA
Low-level output voltage	V_{OL}		0.35	2.0	V	Ports 0, 2-9; V_{DD} = 4.5 to 6.0 V; I_{OL} = 15 mA
			0.35	2.0	V	Ports 12-14; V_{DD} = 4.5 to 6.0 V; I_{OL} = 10 mA
				0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and ports 12-14; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 12-14 (with open drain); V_{IN} = 12 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	Other than Ports 12-14; V_{OUT} = V_{DD}
	I_{LOH2}			20	μA	Ports 12-14 (open drain); V_{OUT} = 12 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Internal pull-up resistor	R_L	15	40	70	kΩ	Ports 12-14; V_{DD} = 5.0 V ± 10%
		10		80	kΩ	Ports 12-14
Supply current (Note 1)	I_{DD1}		3	9	mA	V_{DD} = 5 V ± 10% (Notes 2, 3)
			0.55	1.5	mA	V_{DD} = 3 V ± 10% (Notes 3, 4)
	I_{DD2}		600	1800	μA	HALT mode; V_{DD} = 5 V ± 10% (Note 3)
			200	600	μA	HALT mode; V_{DD} = 3 V ± 10% (Note 3)
	I_{DD3}		0.1	10	μA	STOP mode; V_{DD} = 3 V ± 10%

Notes:

(1) Does not include pull-up resistor current, current through the power-on-reset circuit, or comparator current.

(2) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

(3) f_{XX} = 4.19 MHz; C1 = C2 = 22 pF.

(4) When operated in the low-speed mode with the PCC set to 0000.

Figure 16. DC Characteristics (μPD751xx)

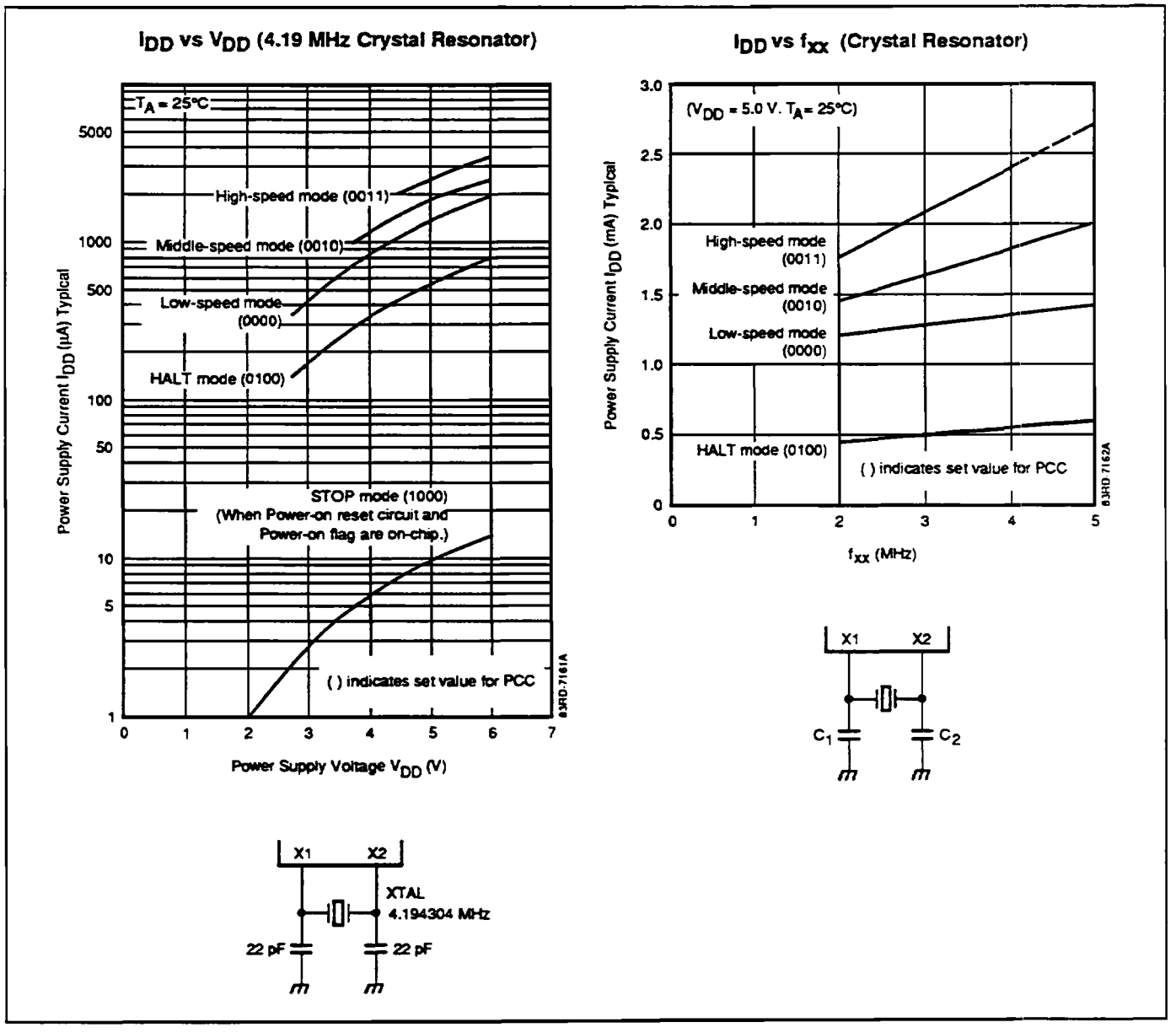
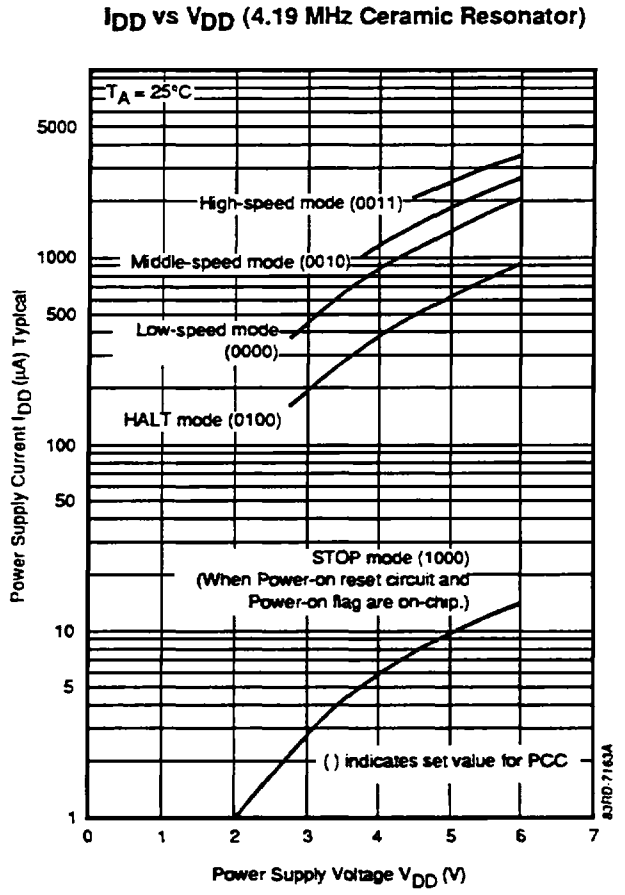
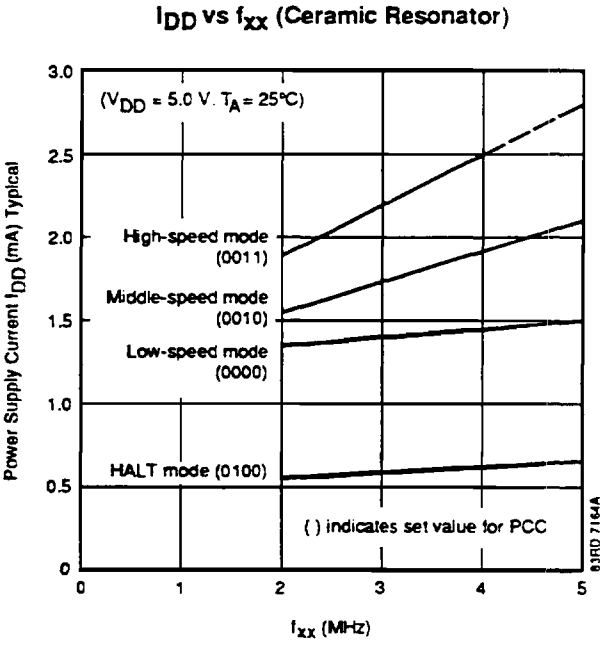
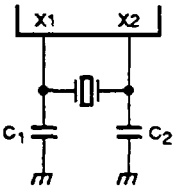


Figure 16. DC Characteristics (μPD751xx) (cont)







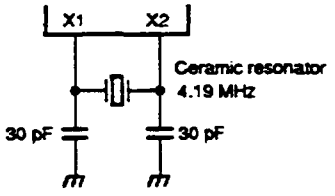


Figure 16. DC Characteristics (μPD751xx) (cont)

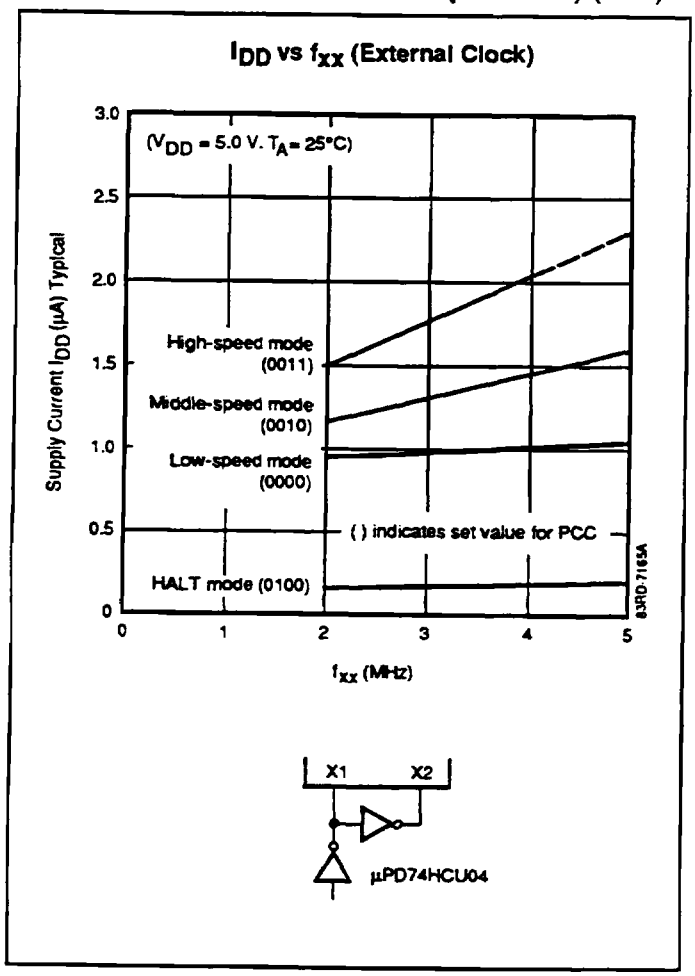
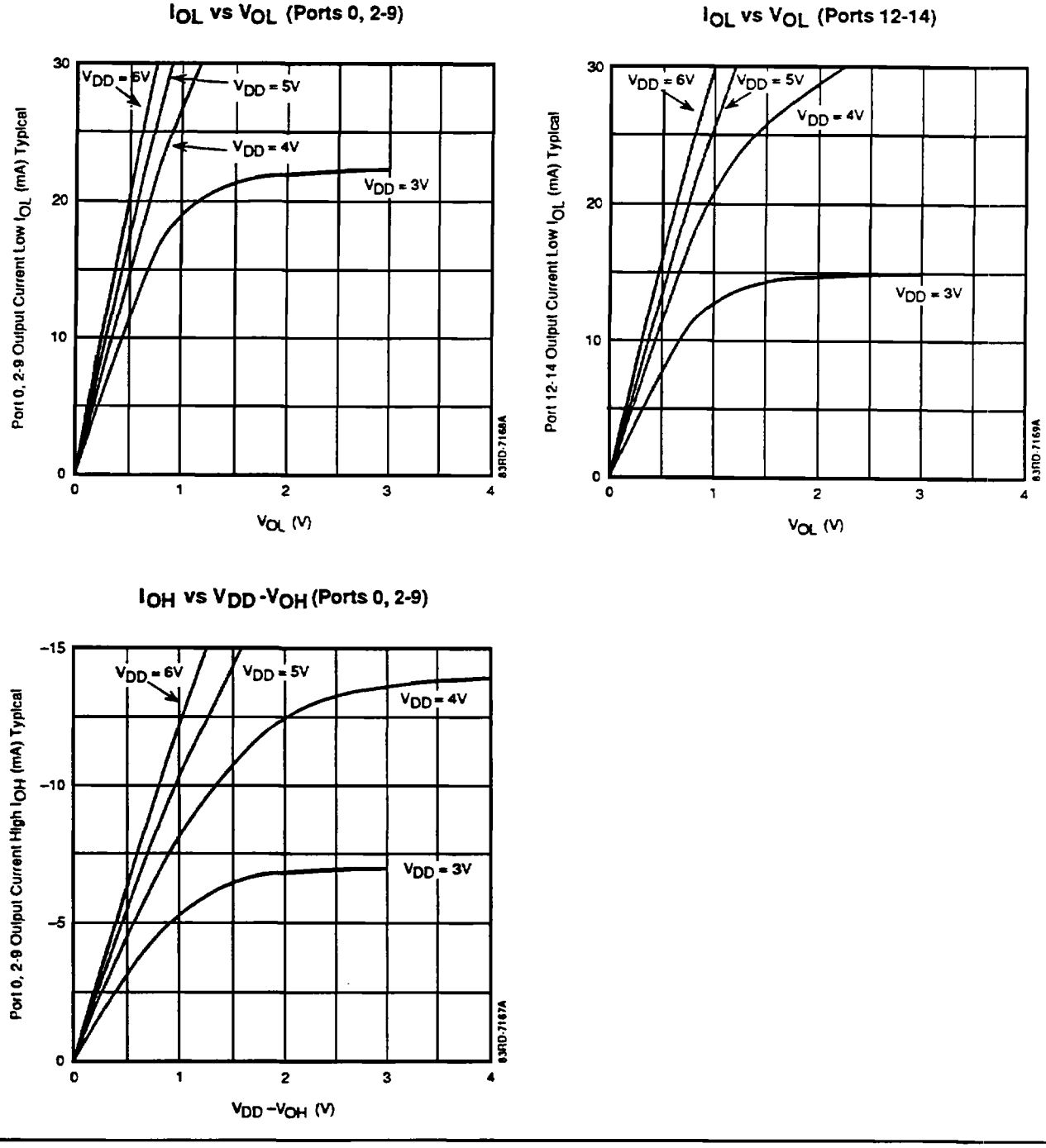


Figure 16. DC Characteristics (μPD751xx) (cont)



Power-on-Reset Circuit Characteristics (All devices exept μPD75P116...notes 3, 4)

μPD751xx: T_A = −40 to +85°C
μPD75P108: T_A = −10 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power-on reset voltage, high	V_{DDH}	4.5		V_{DD} max	V	μPD751xx: V_{DD} max = 6.0 V μPD75P108: V_{DD} max = 5.5 V
Power-on reset voltage, low	V_{DDL}	0		0.2	V	
Power supply voltage rise time	t_r	10		(Note 1)	μs	
Power supply voltage off time	t_{off}	1			s	
POR circuit consumption circuit ; μPD75108 only (Note 2)	I_{DDPR}		10	100	μA	V_{DD} = 5 V ± 10%
			2	20	μA	V_{DD} = 2.5 V

Notes:

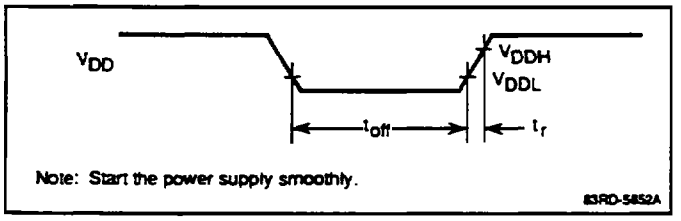
(1) $2^{17}/f_{xx}$ (31.3 ms at f_{xx} = 4.19 MHz)

(2) Current consumed when POR circuit or power-on flag is provided internally.

(3) Power supply voltage must be raised smoothly. See "Power-On-Reset" timing diagram.

(4) Power-on-reset circuit is available as a mask option on on all μPD751xx devices, is always provided with the μPD75P108, and not available on the μPD75P116.

Power-On-Reset Timing



AC Characteristics (μPD751xx)

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY}	0.95		32	μs	V_{DD} = 4.5 to 6.0 V
		3.8		32	μs	V_{DD} = 2.7 to 6.0 V
TI0, TI1 input frequency	f_{TI}	0		1	MHz	V_{DD} = 4.5 to 6.0 V
		0		275	kHz	V_{DD} = 2.7 to 6.0 V
TI0, TI1 input high- and low-level width	t_{TIH}, t_{TIL}	0.48			μs	V_{DD} = 4.5 to 6.0 V
		1.8			μs	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input; V_{DD} = 4.5 to 6.0 V
		0.95			μs	Output; V_{DD} = 4.5 to 6.0 V
		3.2			μs	Input; V_{DD} = 2.7 to 6.0 V
		3.8			μs	Output; V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high and low level width	t_{KH}, t_{KL}	0.4			μs	Input; V_{DD} = 4.5 to 6.0 V
		$0.5\ t_{KCY}-50$			ns	Output; V_{DD} = 4.5 to 6.0 V
		1.6			μs	Input; V_{DD} = 2.7 to 6.0 V
		$0.5\ t_{KCY}-150$			ns	Output; V_{DD} = 2.7 to 6.0 V

AC Characteristics (μPD751xx) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SI vs $\overline{SCK}$ ↑ setup time	t_{SIK}	100			ns	
SI vs $\overline{SCK}$ ↑ hold time	t_{KSI}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO}			300	ns	V_{DD} = 4.5 to 6.0 V
				1000	ns	V_{DD} = 2.7 to 6.0 V
INT0-INT4 high- and low-level width	t_{INTH}, t_{INTL}	5			μs	
$\overline{RESET}$ low level width	t_{RSL}	5			μs	

Notes:

(1) Cycle time (minimum instruction execution time is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC). See figure 17.

Figure 17. Guaranteed Operating Range (μPD751xx)

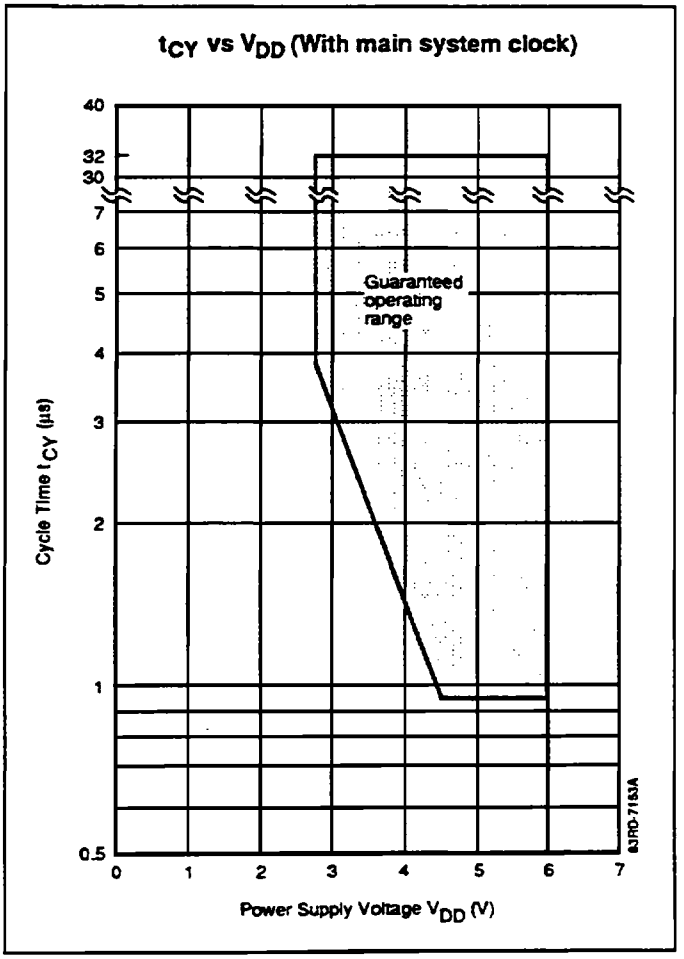


Figure 18. AC Timing Measurement Points (except Ports 0, 1, TI0, TI1, X1, X2, and $\overline{RESET}$)

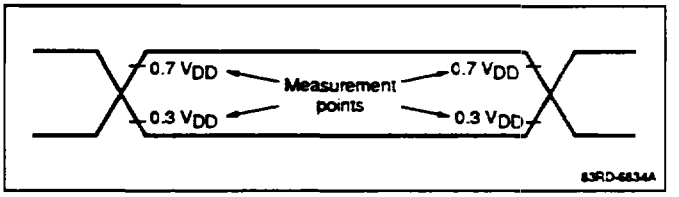


Figure 18A. Clock Timing Measurement Points

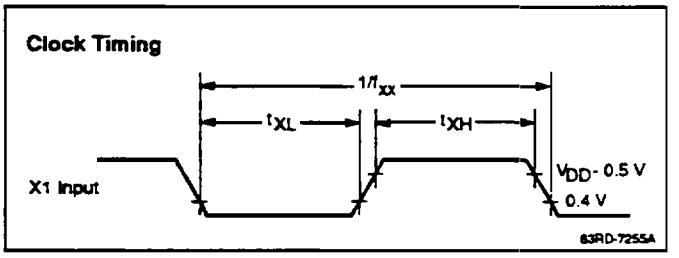


Figure 18B. TI Timing

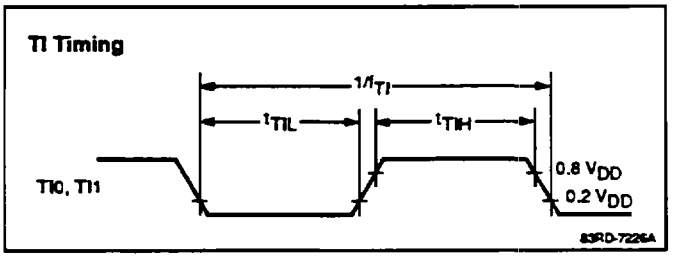


Figure 18C. Serial Transfer Timing

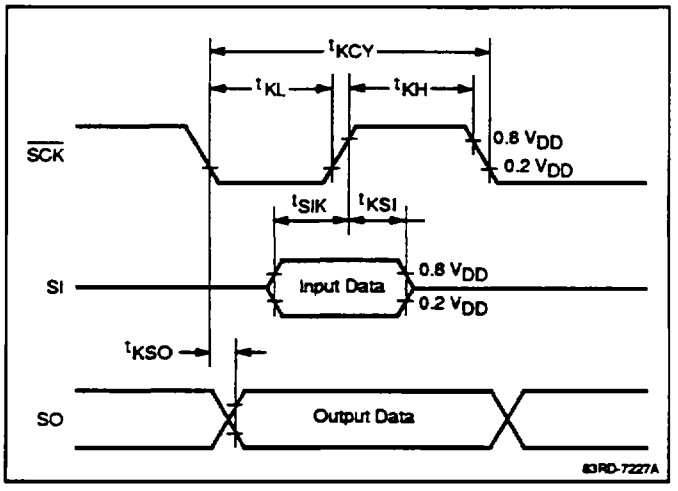


Figure 18D. Interrupt Input Timing

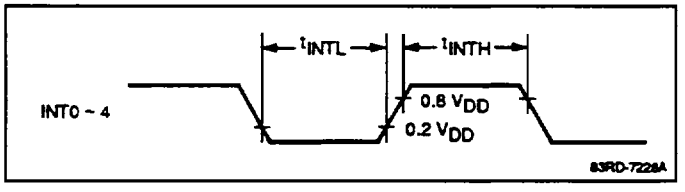


Figure 18E. RESET Input Timing

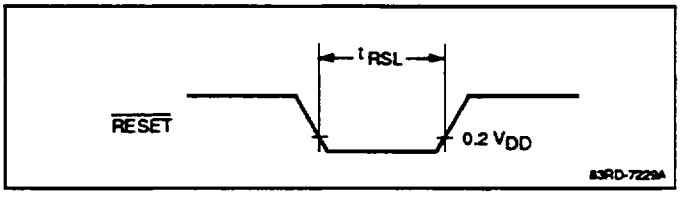
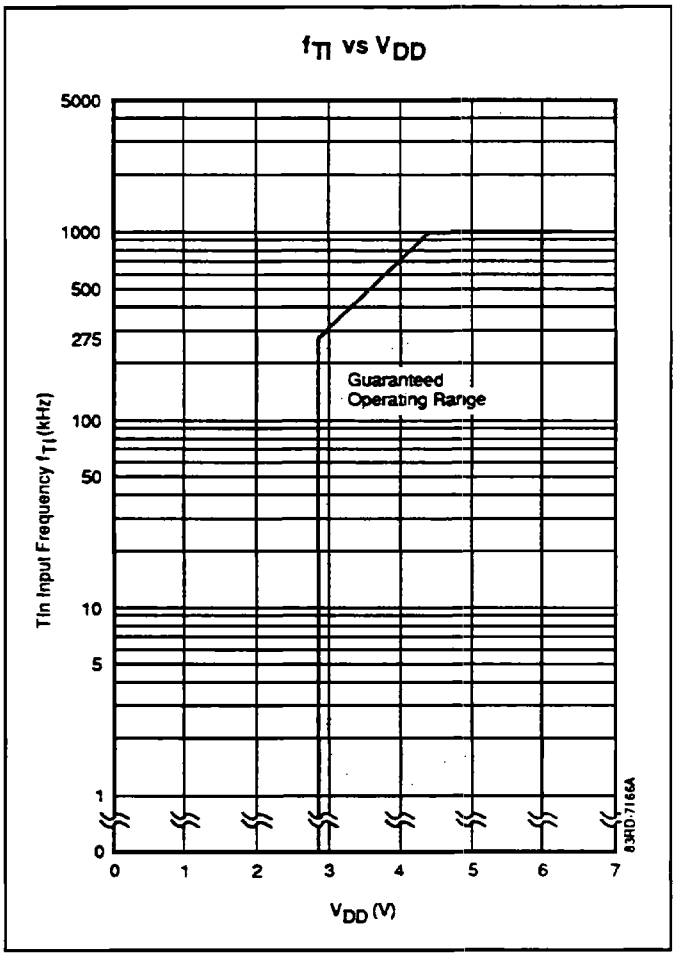


Figure 18F. f_{TI} vs V_{DD}



Data Memory STOP Mode, Low Voltage Data Retention Characteristics (μPD751xx)

T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		6.0	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		$2^{17}/f_{XX}$		s	Release by $\overline{\text{RESET}}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

(1) Excludes current in the pull-up resistors, power-on-reset circuit, and comparator

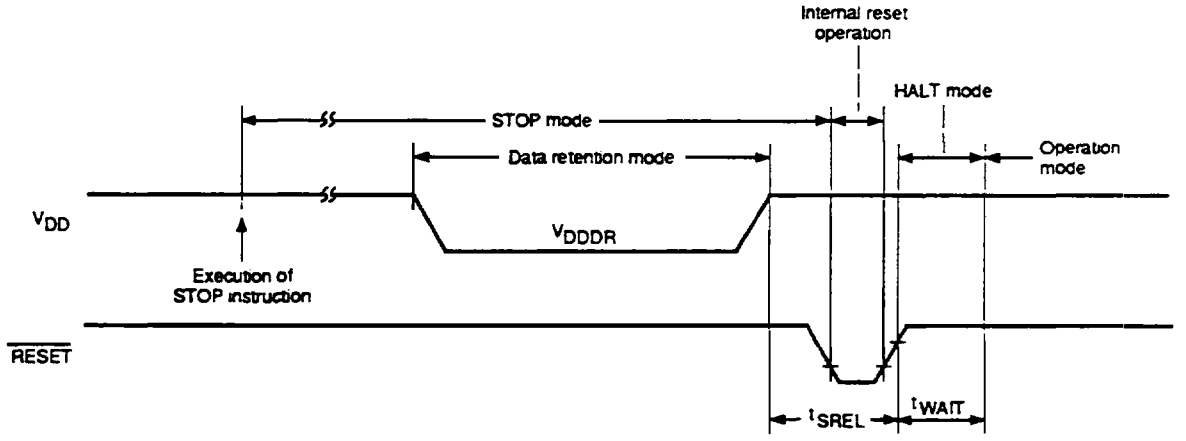
(2) Consult the manufacturer's resonator or crystal spec sheet for this value

(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the the basic interval timer mode register (BTM) according to the following table: .

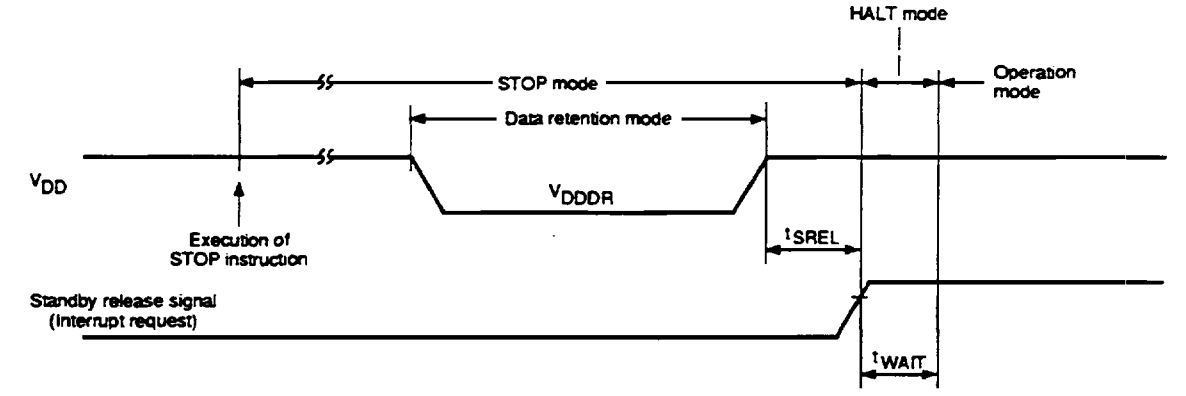
BTM3	BTM2	BTM1	BTM0	WAIT time (f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (Approx 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx 1.95 ms)

Figure 19. Data Retention Timing

A. STOP mode is released by $\overline{\text{RESET}}$ input



B. STOP mode is released by interrupt signal



83RD-64568

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (μPD75P1xx)

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Operating voltage, V_{PP} (μPD75P108)	−0.3 to +22 V
Operating voltage, V_{PP} (μPD75P116)	−0.3 to +13.5 V
Input voltage, V_{I1} (other than ports 12-14)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (ports 12-14)	−0.3 to +13 V (Note 1)
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH} (Single pin)	−15 mA
High-level output current, I_{OH} (Total of all pins)	−30 mA
Low-level output current, I_{OL} (Single pin)	30 mA pk 15 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 0, 2–4, 12–14)	100 mA pk 36 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 5–9)	100 mA pk 36 mA rms (Note 2)
Operating temperature, t_{OPT}: μPD75P108	−10 to + 85°C
Operating temperature, t_{OPT}: μPD75P116	−40 to + 85°C
Storage temperature, t_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Notes:

(1) When applying more than 10 V to ports 12, 13, or 14, the external pull-up resistor must be at least 50 kΩ.

(2) rms value = pk x (duty cycle)$^{1/2}$.

Capacitance (μPD75P1xx)

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}	15	pF	
I/O capacitance	C_{IO}	15	pF	

DC Characteristics (μPD75P1xx)

μPD75P108: T_A = −10 to +85°C; V_{DD} = 4.5 to 5.5 V

μPD75P116: T_A = −40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except ports 0, 1, 12-14, TI0, TI1, X1, X2, and $\overline{\text{RESET}}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, TI0, TI1 and $\overline{\text{RESET}}$
	V_{IH3}	0.7 V_{DD}		12	V	Ports 12-14; open drain
	V_{IH4}	V_{DD}−0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Except ports 0, 1, TI0, TI1, X1, X2, and $\overline{\text{RESET}}$
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, TI0, TI1 and $\overline{\text{RESET}}$
	V_{IL3}	0		0.4	V	X1, X2
High-level output voltage	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Low-level output voltage	V_{OL}		0.55	2.0	V	Ports 0, 2-9; I_{OL}= 15 mA
			0.35	2.0	V	Ports 12-14; I_{OL}= 10 mA
				0.4	V	I_{OL} = 1.6 mA
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and ports 12-14; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 12-14; V_{IN} = 12 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2; V_{IN} = 0 V

DC Characteristics (μPD75P1xx) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level output leakage current	I_{LOH1}			3	μA	All output pins except ports 12-14; $V_{OUT} = V_{DD}$
	I_{LOH2}			20	μA	Ports 12-14; V_{OUT} = 12 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Supply current (Note 1)	I_{DD1}		5	10	mA	V_{DD} = 5 V ± 10%; (Notes 2, 3)
	I_{DD2}		500	1500	μA	HALT Mode (Notes 2, 4); V_{DD} = 5V ±5%
	I_{DD3}		0.5	20	μA	μPD75P116: STOP Mode; V_{DD} = 5V ±5% (Note 5)
			30	100	μA	μPD75P108: STOP Mode ; V_{DD} = 5 V ±5% (Note 5)

Notes:

(1) Does not include comparator and includes current in the power-on-reset circuit.

(2) 4.19 MHz crystal oscillator; C1 = C2 = 22 pF.

(3) Value during high-speed operation and the processor control clock (PCC) is set to 0011.

(4) Value when the processor control clock (PCC) is set to 0100, and CPU is in HALT mode.

(5) I_{DD3} is less for the μPD75P116 because it does not contain the power-on-reset and power-on flag circuitry.

AC Characteristics (μPD75P1xx)

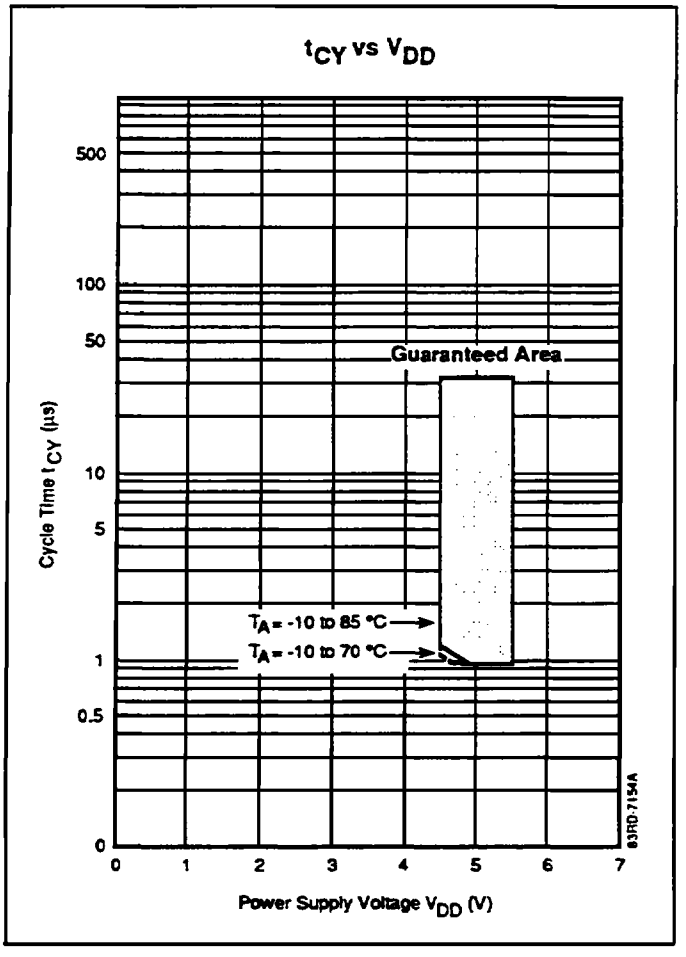
μPD75P108: T_A = −10 to +85°C; V_{DD} = 4.5 to 5.5 V
μPD75P116: T_A = −40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY}	0.95		32	μs	V_{DD} = 5 V ± 5%
		1.1		32	μs	V_{DD} = 5 V ± 10%
TI0, TI1 input frequency	f_{TI}	0		1	MHz	
TI0, TI1 input high-and low-level width	t_{TIH}, t_{TIL}	0.48			μs	
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input
		0.95			μs	Output
$\overline{SCK}$ high-and low-level width	t_{KH}, t_{KL}	0.4			μs	Input
		0.5 t_{KCY}−50			ns	Output
SI vs. $\overline{SCK}$ ↑ setup time	t_{SIK}	100			ns	
SI vs. $\overline{SCK}$ ↑ hold time	t_{KSI}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO}			300	ns	
INT0-4 high- and low-level width	t_{INTH}, t_{INTL}	5			μs	
$\overline{RESET}$ low level width	t_{RSL}	5			μs	

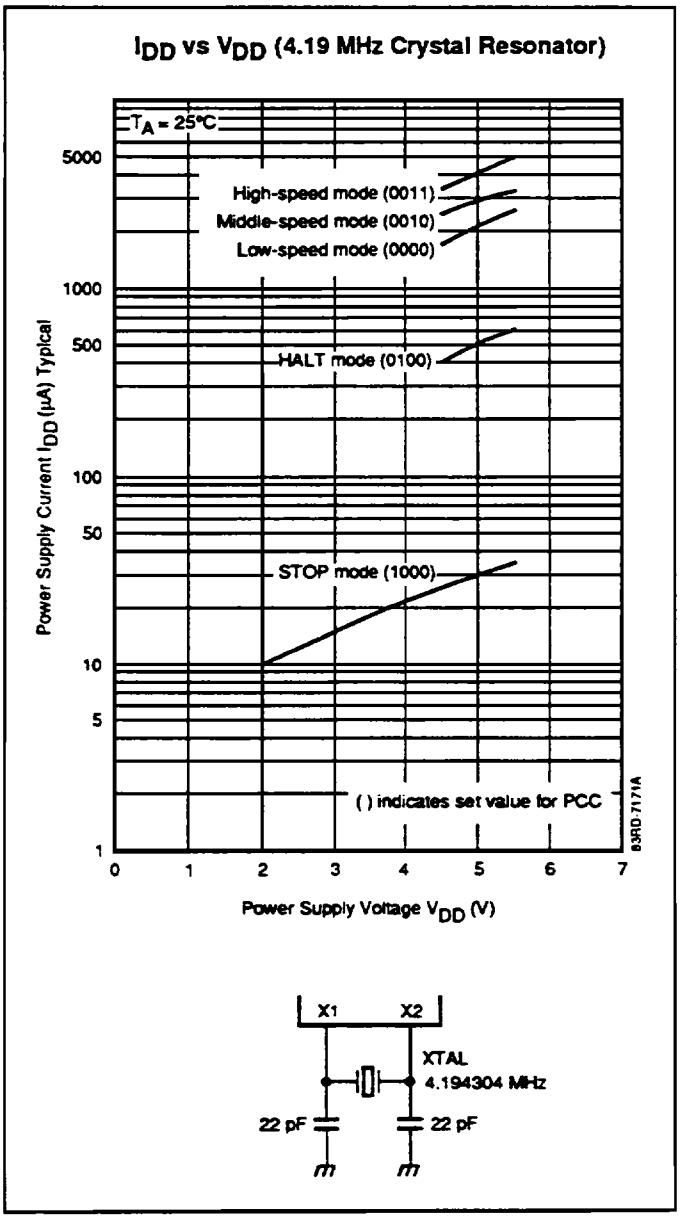
Notes:

(1) Cycle time is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC). See figure 20.

Figure 20. Guaranteed Operating Range (μPD75P1xx)

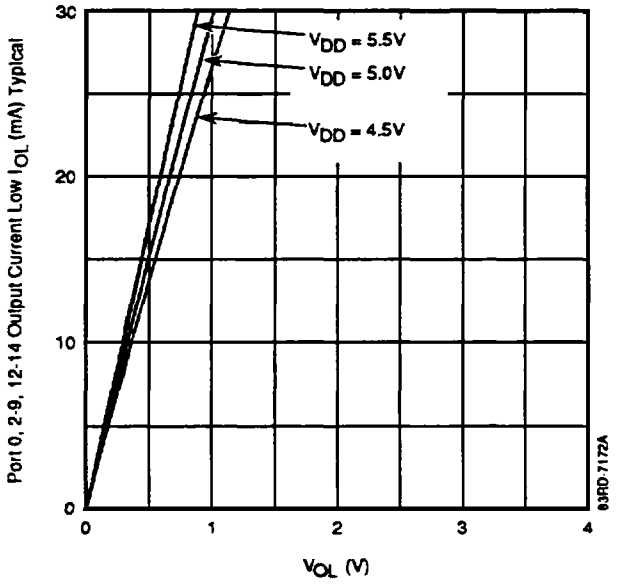


DC Characteristics (μPD75PIxx)

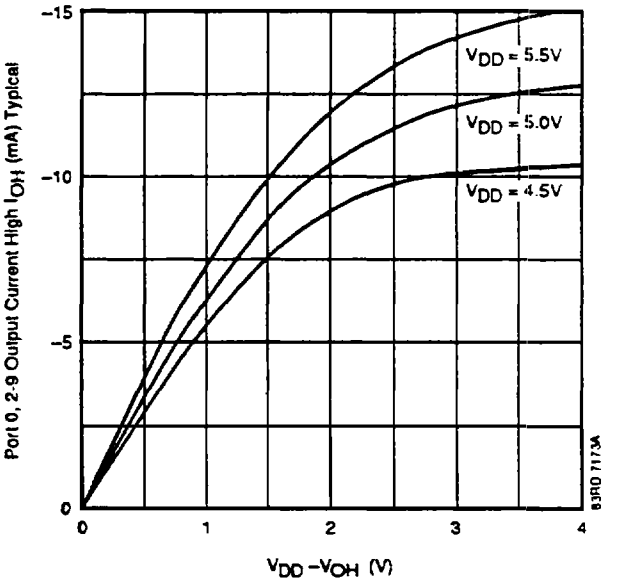


DC Characteristics (μPD75PIxx) (cont)

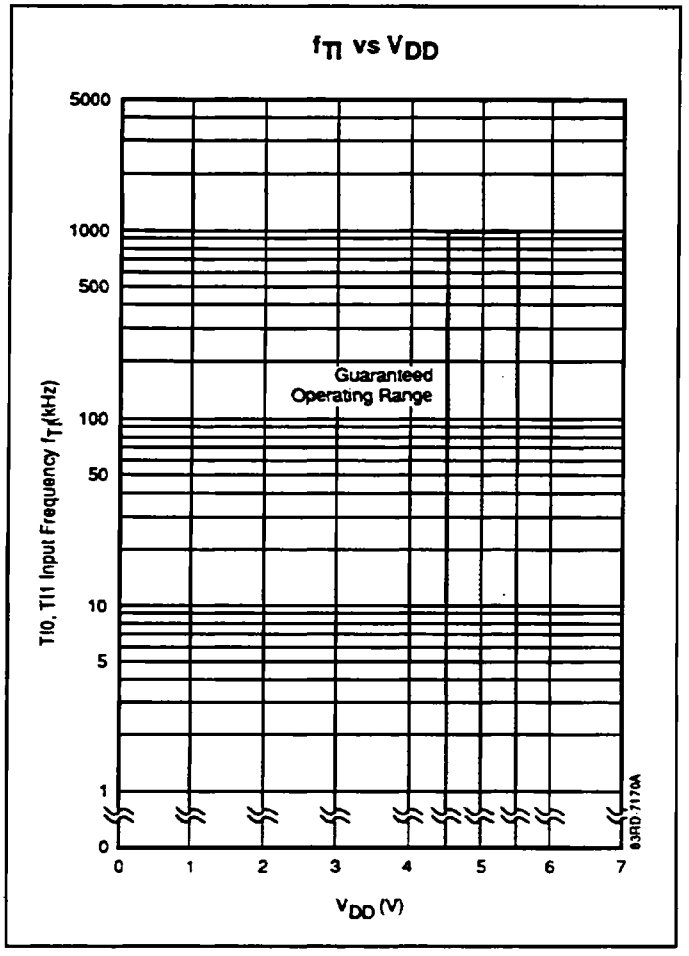
I_{OL} vs V_{OL} (Ports 0, 2-9, 12-14)



I_{OH} vs V_{DD}-V_{OH} (Ports 0, 2-9)



DC Characteristics (μPD75PIxx) (cont)



Data Memory STOP Mode Low Voltage Data Retention Characteristics (μPD75P1xx)

μPD75P108: T_A = −10 to +85°C; V_{DD} = 4.5 to 5.5 V
μPD75P116: T_A = −40 to +85°C; V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		5.5	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	μPD75P116; V_{DDDR} = 2.0 V (Note 4)
			15	40	μA	μPD75P108; V_{DDDR} = 2.0 V (Note 4)
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		$2^{17}/f_{XX}$		s	Release by $\overline{RESET}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

(1) Includes current in the power-on-reset circuit, but excludes current in the comparator circuit.

(2) Consult the manufacturer's resonator or crystal specification for this value.

(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time (f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (Approx 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx 1.95 ms)

(4) I_{DDDR} is less for the μPD75P116 because it does not contain the power-on-reset or power-on flag circuitry

DC Programming Characteristics (μPD75P1xx)

μPD75P108: V_{DD} = 6.0 ± 0.25 V; V_{PP} = 21.0 ± 0.5 V; V_{SS} = 0 V; T_A = 25°C
μPD75P116: V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V; T_A = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	All except X1, X2
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		$0.3V_{DD}$	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed +22.0 V (μPD75P108) or +13.5 V (μPD75P116), including overshoot.

(2) V_{DD} must be applied before V_{PP}, and should be removed after V_{PP} is removed.

AC Programming Characteristics (μPD75P1xx)

μPD75P108: V_{DD} = 6.0 ± 0.25 V; V_{PP} = 21.0 ± 0.5 V; V_{SS} = 0 V; T_A = 25°C
μPD75P116: V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V; T_A = 25°C

Parameter	Symbol	(Note 1)	Min	Max	Unit	Conditions
Address setup time to MD0 ↓ (Note 2)	t_{AS}	t_{AS}	2		μs	
MD1 to MD0 ↓ setup	t_{M1S}	t_{OES}	2		μs	
Data to MD0 ↓ setup	t_{DS}	t_{DS}	2		μs	
Address hold from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2		μs	
Data hold from MD0 ↑	t_{DH}	t_{DH}	2		μs	
Data output float from MD0 ↑ delay	t_{DF}	t_{DF}	0	130	ns	
V_{PP} Setup to MD3 ↑	t_{VPS}	t_{VPS}	2		μs	
V_{DD} Setup to MD3 ↑	t_{VDS}	t_{VCS}	2		μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95	21	ms	
MD0 setup to MD1 ↑	t_{MOS}	t_{CES}	2		μs	
Data output from MD0 ↓ delay	t_{DV}	t_{DV}		1	μs	MD0 = MD1 = V_{IL}
MD1 hold to MD0 ↑	t_{M1H}	t_{OEH}	2		μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 recovery from MD0 ↓	t_{M1R}	t_{OR}	2		μs	$t_{M1H} + t_{M1R} \geq 50$ μs
Program counter reset	t_{PCR}	–	10		μs	
X1 input high/low level width	t_{XH}, t_{XL}	–	0.125		μs	
X1 input frequency	f_{XX}	–		4.19	MHz	
Initial mode set	t_I	–	2		μs	
MD3 setup to MD1 ↑	t_{M3S}	–	2		μs	
MD3 hold to MD1 ↓	t_{M3H}	–	2		μs	
MD3 setup to MD0 ↓	t_{M3SR}	–	2		μs	During program read cycle
Address to data output delay time (Note 2)	t_{DAD}	t_{ACC}	2		μs	
Address to data output hold time (Note 2)	t_{HAD}	t_{OH}	0	130	ns	
MD3 output hold from MD0 ↑	t_{M3HR}	–	2		μs	
Data output from MD3 ↓ float delay time	t_{DFR}	–	2		μs	

Notes:

(1) These symbols correspond to these of the μPD27C256 EPROM.

(2) The internal address signal is incremented by one by the rising edge of the fourth X1 pulse.The address is not connected to an external pin.

Figure 21. EPROM Program Memory Write/Verify Timing

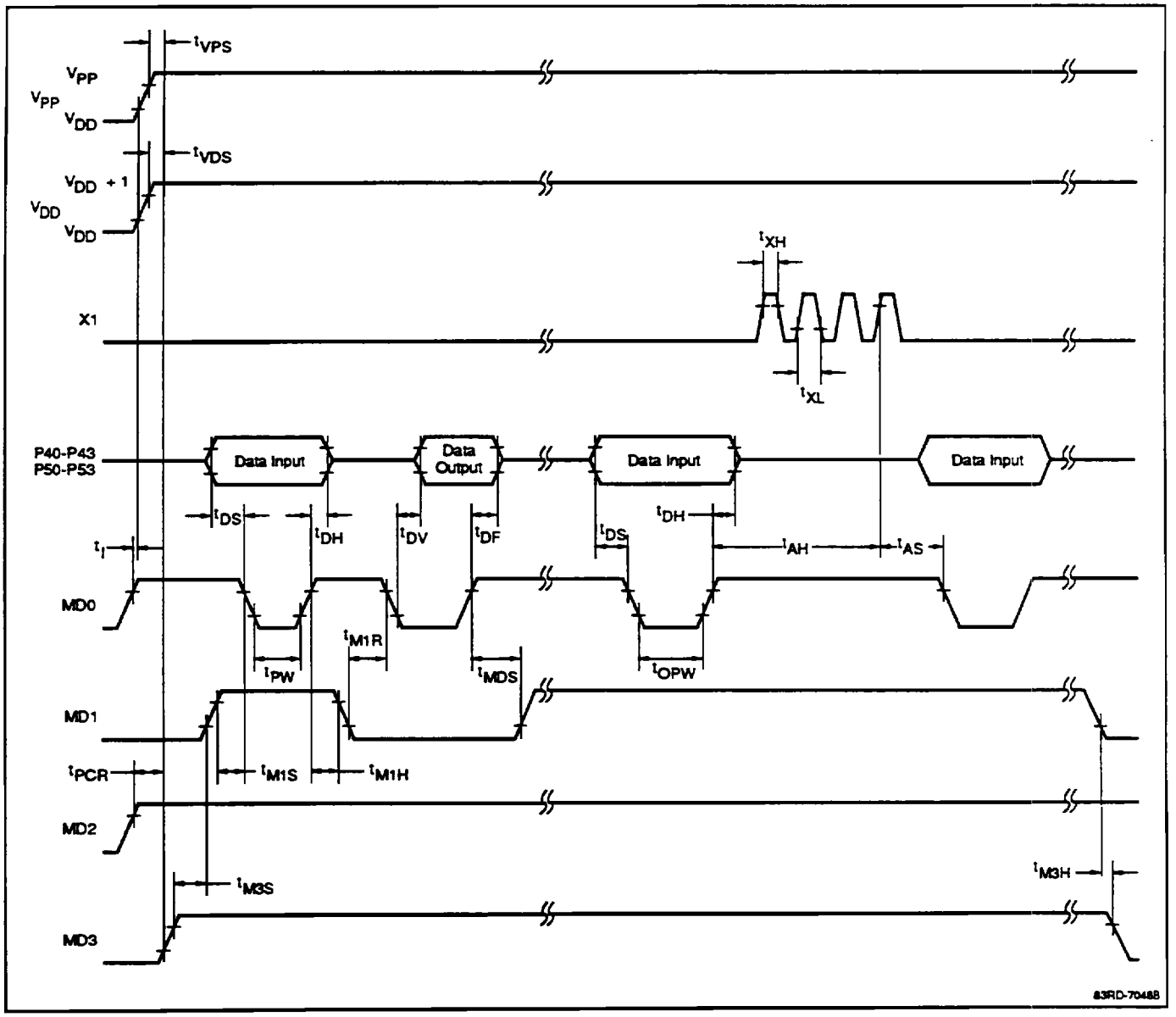


Figure 22. EPROM Program Memory Read Timing