



NPN POWER TRANSISTOR ARRAY

D76FY2T

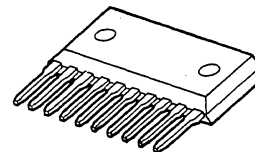
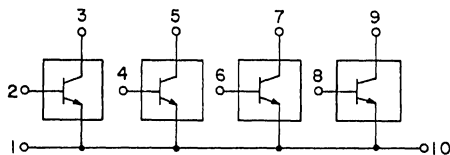
80 VOLTS
2 AMP, 4.0 WATTS

Designed for switching applications, solenoid drive applications.

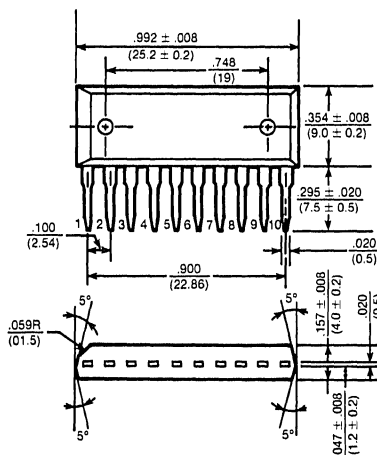
Features:

- Epoxy single-inline package (10 pin)
- High DC current gain: $h_{FE} = 500$ (Min.) ($I_C = 400\text{mA}$)
- Low saturation voltage:
 $V_{CE(sat)} = 0.5\text{V}$ (Max.) ($I_C = 300\text{mA}$)

ARRAY CONFIGURATION



CASE STYLE SIP-10 PIN
DIMENSIONS ARE IN INCHES AND (MILLIMETERS)



maximum ratings ($T_A = 25^\circ\text{C}$) (unless otherwise specified)

RATING	SYMBOL	D76FY2T	UNITS
Collector-Emitter Voltage	V_{CEO}	80	Volts
Collector-Base Voltage	V_{CBO}	80	Volts
Emitter Base Voltage	V_{EBO}	7	Volts
Collector Current — Continuous	I_C	2	A
Base Current — Continuous	I_B	0.5	A
Collector Power Dissipation	P_D	4.0	Watts
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

thermal characteristics

Thermal Resistance, Junction to Ambient	$\Sigma R_{\theta JA}$	31.3	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	260	$^\circ\text{C}$

electrical characteristics ($T_A = 25^\circ\text{C}$) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
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off characteristics

Collector-Emitter Breakdown Voltage ($I_C = 10\text{mA}$, $I_B = 0$)	$V_{BR(CEO)}$	80	—	—	Volts
Collector Cutoff Current ($V_{CB} = 80\text{V}$, $I_E = 0$)	I_{CBO}	—	—	1	μA
Emitter Cutoff Current ($V_{EB} = 7\text{V}$, $I_C = 0$)	I_{EBO}	—	—	1	μA

on characteristics

DC Current Gain ($I_C = 400\text{mA}$, $V_{CE} = 1\text{V}$)	h_{FE}	500	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 300\text{mA}$, $I_B = 1\text{mA}$)	$V_{CE(sat)}$	—	0.3	0.5	Volts
Base-Emitter Saturation Voltage ($I_C = 300\text{mA}$, $I_B = 1\text{mA}$)	$V_{BE(sat)}$	—	—	1.1	Volts

switching characteristics

Turn-on Time	$V_{CC} = 30\text{V}$ $I_{B1} = -I_{B2} = 1\text{mA}$ Duty Cycle $\leq 1\%$	t_{on}	—	2.0	—	μs
Storage Time		t_{stg}	—	5.0	—	
Fall Time		t_f	—	2.0	—	

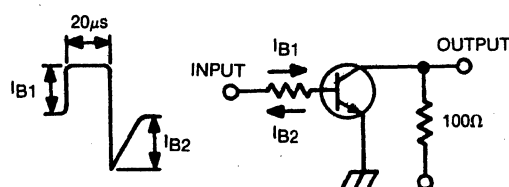


FIG. 1 SWITCHING TIME TEST CIRCUIT

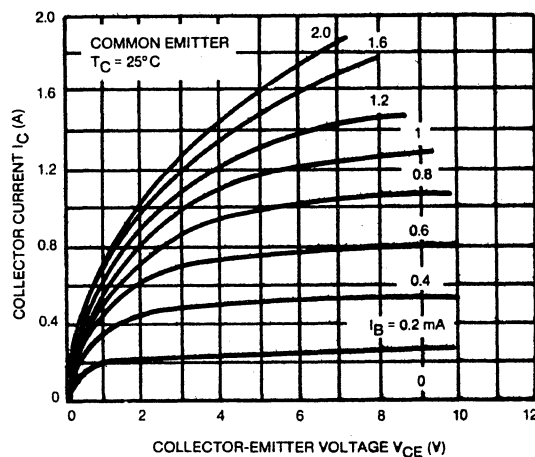


FIG. 2 $I_C - V_{CE}$

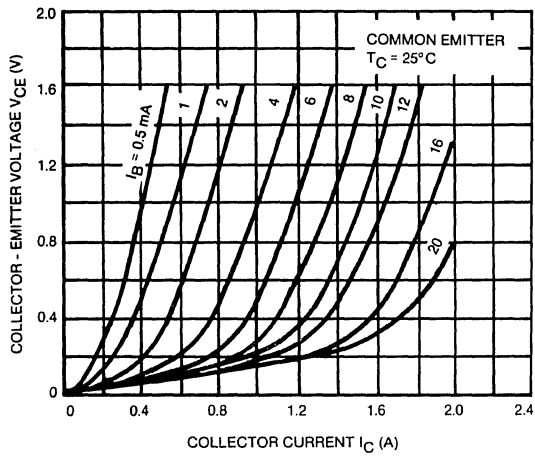


FIG. 3 $V_{CE} - I_C$

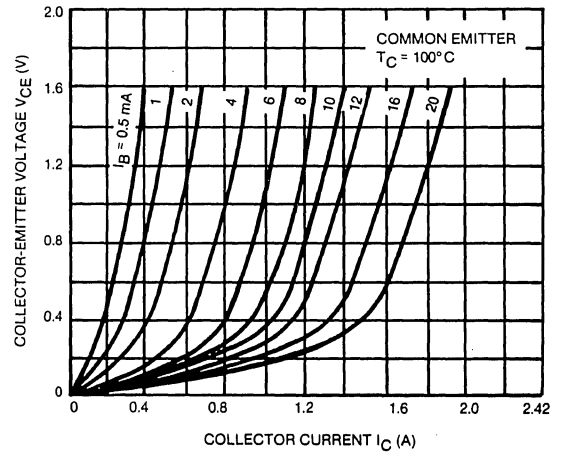


FIG. 4 $V_{CE} - I_C$

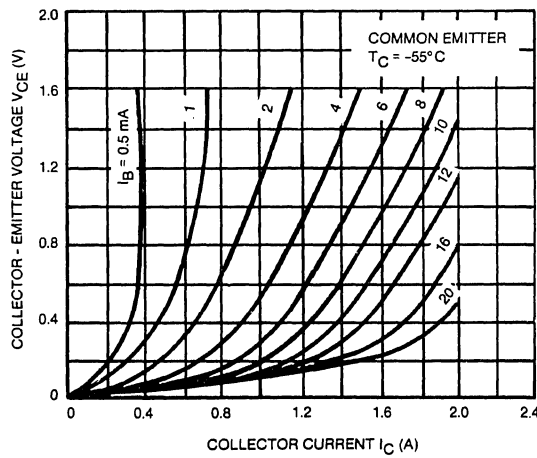


FIG. 5 $V_{CE} - I_C$

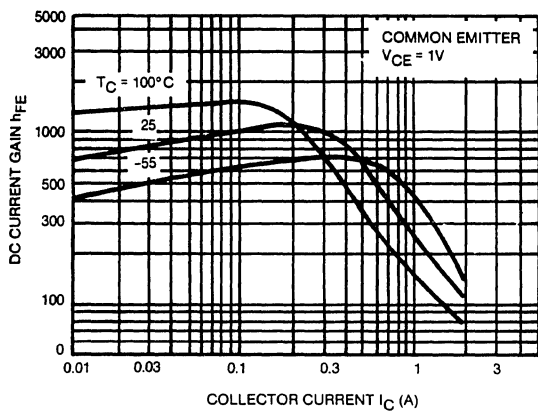


FIG. 6 $h_{FE} - I_C$

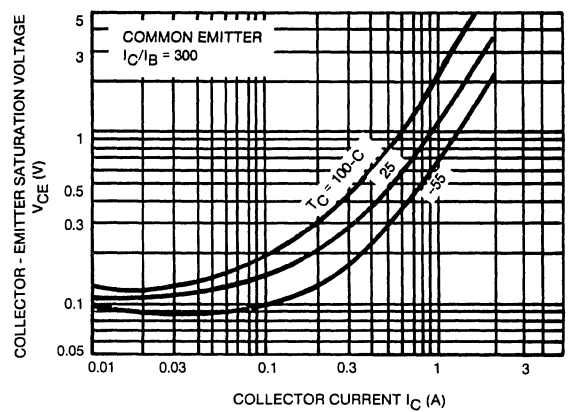


FIG. 7 $V_{CE}(\text{sat}) - I_C$

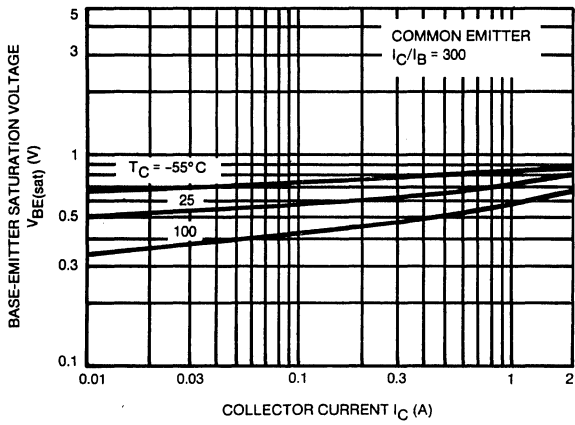


FIG. 8 $V_{BE(sat)} - I_C$

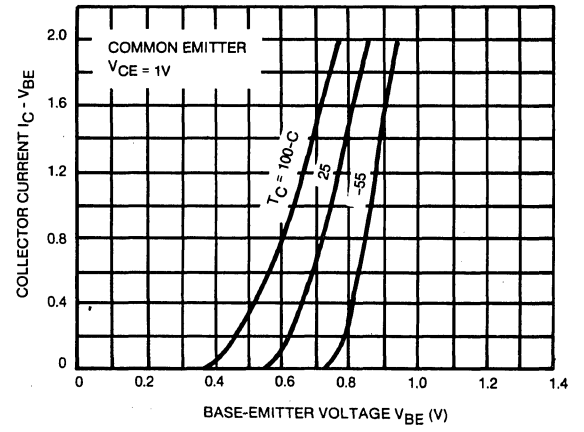


FIG. 9 $I_C - V_{BE}$