DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD780021A, 780022A, 780023A, 780024A
780021AY, 780022AY, 780023AY, 780024AY

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780021A, 780022A, 780023A, and 780024A are members of the μPD780024A Subseries of the 78K/0 Series. Only selected functions of the existing μPD78054 Subseries are provided, and the serial interface is enhanced.

The μPD780021AY, 780022AY, 780023AY, and 780024AY are the μPD780024A Subseries with a multimaster supporting I^2C bus interface, which makes them suitable for AV equipment.

Flash memory versions, the μPD78F0034A, 78F0034B, 78F0034AY, and 78F0034BY, that can operate in the same power supply voltage range as the mask ROM versions, and various development tools, are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780024A, 780034A, 780024AY, 780034AY
Subseries User's Manual: U14046E
78K/0 Series Instructions User's Manual: U12326E

FEATURES

- Internal ROM and RAM

Part Number \ Item	Program Memory (Internal ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD780021A, 780021AY	8 KB	512 bytes	• 64-pin plastic SDIP (19.05 mm (750))
μPD780022A, 780022AY	16 KB		• 64-pin plastic QFP (14 x 14) • 64-pin plastic LQFP (14 x 14)
μPD780023A, 780023AY	24 KB	1024 bytes	• 64-pin plastic TQFP (12 x 12)
μPD780024A, 780024AY	32 KB		• 64-pin plastic LQFP (10 x 10) • 73-pin plastic FBGA (9 x 9)

- External memory expansion space: 64 KB
- Minimum instruction execution time
  - Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A: 0.166 μs (f_X = 12 MHz, V_{DD} = 4.5 to 5.5 V)
  - μPD780021AY, 780022AY, 780023AY, 780024AY and conventional products of μPD780021A, 780022A, 780023A, 780024A: 0.238 μs (f_X = 8.38 MHz, V_{DD} = 4.0 to 5.5 V)
- I/O ports: 51 (N-ch open-drain (5 V withstanding voltage): 4)
- 8-bit resolution A/D converter: 8 channels (AV_{DD} = 1.8 to 5.5 V)
- Serial interface: 3 channels
  - μPD780021A, 780022A, 780023A, 780024A: UART mode, 3-wire serial I/O mode (2 channels)
  - μPD780021AY, 780022AY, 780023AY, 780024AY: UART mode, 3-wire serial I/O mode, I^2C bus mode
- Timer: 5 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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Printed in Japan

The mark ★ shows major revised points.

APPLICATIONS

Telephones, household electrical appliances, pagers, AV equipment, car audios, office automation equipment, etc.

ORDERING INFORMATION (1/2)

(1) μPD780024A Subseries

	Part Number	Package
	μPD780021ACW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780021AGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780021AGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780021AGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780021AGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780021AF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780022ACW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780022AGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780022AGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780022AGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780022AGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780022AF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780023ACW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780023AGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780023AGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780023AGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780023AGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780023AF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780024ACW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780024AGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780024AGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780024AGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780024AGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780024AF1-×××-CN3	73-pin plastic FBGA (9 x 9)

Remark ××× indicates ROM code suffix.

ORDERING INFORMATION (2/2)

(2) μPD780024AY Subseries

	Part Number	Package
	μPD780021AYCW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780021AYGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780021AYGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780021AYGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780021AYGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780021AYF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780022AYCW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780022AYGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780022AYGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780022AYGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780022AYGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780022AYF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780023AYCW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780023AYGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780023AYGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780023AYGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780023AYGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780023AYF1-×××-CN3	73-pin plastic FBGA (9 x 9)
	μPD780024AYCW-×××	64-pin plastic SDIP (19.05 mm (750))
	μPD780024AYGC-×××-AB8	64-pin plastic QFP (14 x 14)
★	μPD780024AYGC-×××-8BS	64-pin plastic LQFP (14 x 14)
	μPD780024AYGK-×××-9ET	64-pin plastic TQFP (12 x 12)
★	μPD780024AYGB-×××-8EU	64-pin plastic LQFP (10 x 10)
★	μPD780024AYF1-×××-CN3	73-pin plastic FBGA (9 x 9)

Remark ××× indicates ROM code suffix.

★ EXPANDED-SPECIFICATION PRODUCTS AND CONVENTIONAL PRODUCTS

The expanded-specification product and conventional product refer to the following products.

Expanded-specification product: μPD780021A, 780022A, 780023A, 780024A for which orders were received after December 1, 2001.
(Products with a rank[Note] other than K, E, P, X)

Conventional product: Products other than the above expanded specification products.
(Products with rank[Note] K, E, P, X)
μPD780021AY, 780022AY, 780023AY, 780024AY

Note The rank is indicated by the 5th digit from the left in the lot number marked on the package.

Lot number ○○ ○○ △ ××××

Year code | Week code | Rank | NEC Electronics control code

Expanded-specification products and conventional products differ in the power supply voltage range and operating frequency ratings.

Power Supply Voltage (V_{DD})	Guaranteed Operating Speed (Operating Frequency)	
	Conventional Products	Expanded-Specification Products
4.5 to 5.5 V	8.38 MHz (0.238 μs)	12 MHz (0.166 μs)
4.0 to 5.5 V	8.38 MHz (0.238 μs)	8.38 MHz (0.238 μs)
3.0 to 5.5 V	5 MHz (0.4 μs)	8.38 MHz (0.238 μs)
2.7 to 5.5 V	5 MHz (0.4 μs)	5 MHz (0.4 μs)
1.8 to 5.5 V	1.25 MHz (1.6 μs)	1.25 MHz (1.6 μs)

Remark The parenthesized values indicates the minimum instruction execution time.

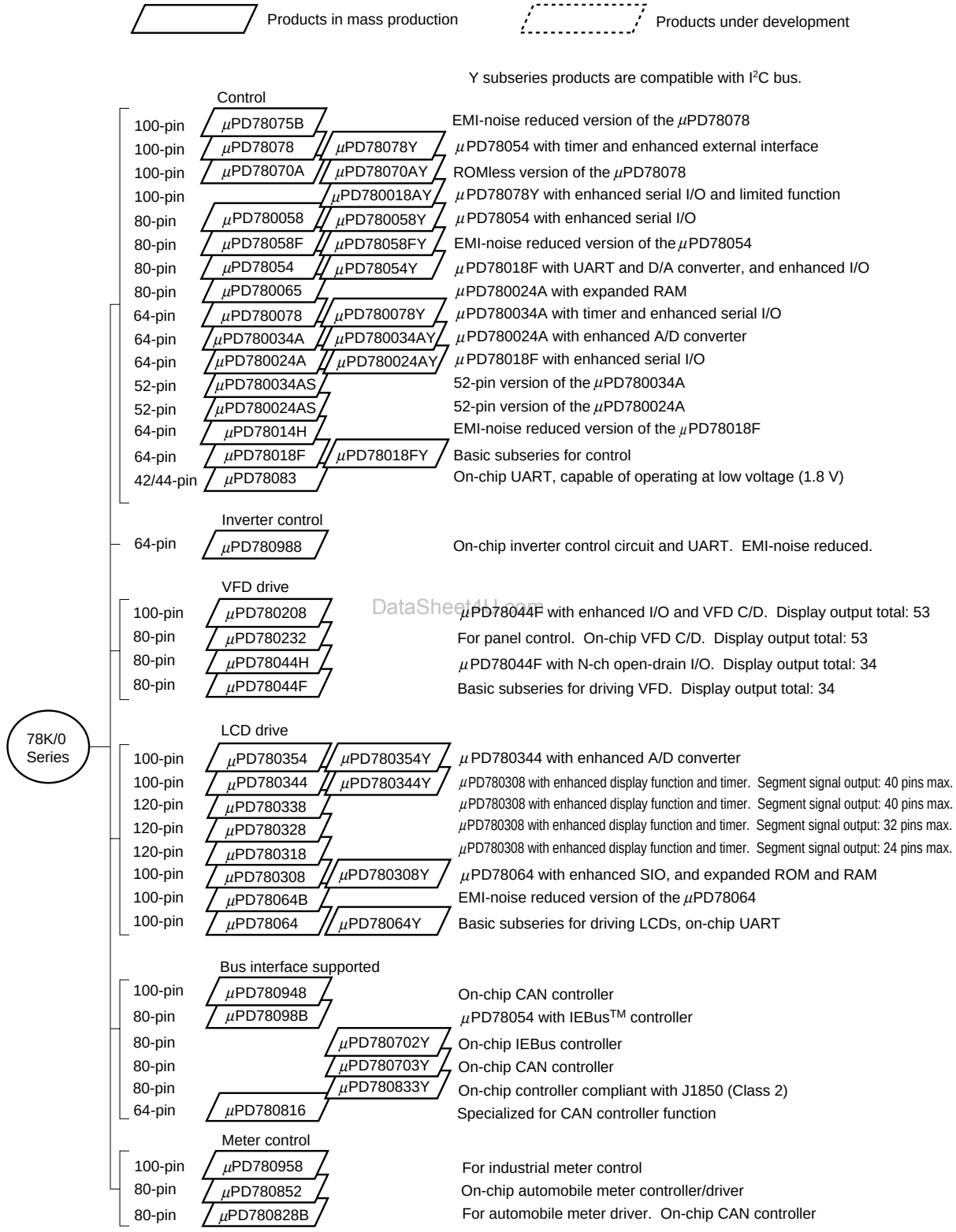
★ CORRESPONDENCE BETWEEN MASK ROM PRODUCTS AND FLASH MEMORY PRODUCTS

Mask ROM Products	Flash Memory Products
Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A	μPD78F0034B
Conventional products of μPD780021A, 780022A, 780023A, 780024A	μPD78F0034A
μPD780021AY, 780022AY, 780023AY, 780024AY	μPD78F0034AY, 78F0034BY

Remark The μPD78F0034A and 78F0034B differ in the operating frequency ratings and communication mode of flash memory programming. The μPD78F0034AY and 78F0034BY only differ in the communication mode of flash memory programming. Refer to the data sheet of the products.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are same.

The major functional differences among the subseries are listed below.

- Non-Y subseries

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD780034AS						–	4 ch			39		–
	μPD780024AS						4 ch	–					
	μPD78014H						8 ch			2 ch	53		√
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780354	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	3 ch (UART: 1 ch)	66	1.8 V	–
	μPD780344						8 ch	–					
	μPD780338	48 K to 60 K	3 ch	2 ch			–	10 ch	1 ch	2 ch (UART: 1 ch)	54		
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash-board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K									59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

- **Y subseries**

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch, I^2C: 1 ch)	88	1.8 V	√
	μPD78070AY	–									61	2.7 V	
	μPD780018AY	48 K to 60 K							–	3 ch (I^2C: 1 ch)	88		
	μPD780058Y	24 K to 60 K	2 ch						2 ch	3 ch (time-division UART: 1 ch, I^2C: 1 ch)	68	1.8 V	
	μPD78058FY	48 K to 60 K								3 ch (UART: 1 ch, I^2C: 1 ch)	69	2.7 V	
	μPD78054Y	16 K to 60 K										2.0 V	
	μPD780078Y	48 K to 60 K		2 ch			–	8 ch	–	4 ch (UART: 2 ch, I^2C: 1 ch)	52	1.8 V	
	μPD780034AY	8 K to 32 K		1 ch						3 ch (UART: 1 ch, I^2C: 1 ch)	51		
	μPD780024AY						8 ch	–					
	μPD78018FY	8 K to 60 K								2 ch (I^2C: 1 ch)	53		
LCD drive	μPD780354Y	24 K to 32 K	4 ch	1 ch	1 ch	1 ch	–	8 ch	–	4 ch (UART: 1 ch, I^2C: 1 ch)	66	1.8 V	–
	μPD780344Y						8 ch	–					
	μPD780308Y	48 K to 60 K	2 ch							3 ch (time-division UART: 1 ch, I^2C: 1 ch)	57	2.0 V	
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I^2C: 1 ch)			
Bus interface supported	μPD780701Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	–	–	4 ch (UART: 1 ch, I^2C: 1 ch)	67	3.5 V	–
	μPD780703Y												
	μPD780833Y										65	4.5 V	

Remark The functions of non-Y subseries and Y subseries products are the same, except for the serial interface.

OVERVIEW OF FUNCTIONS (1/2)

Item \ Part Number		μPD780021A μPD780021AY	μPD780022A μPD780022AY	μPD780023A μPD780023AY	μPD780024A μPD780024AY
Internal memory	ROM	8 KB	16 KB	24 KB	32 KB
	High-speed RAM	512 bytes		1024 bytes	
Memory space		64 KB			
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
★ Minimum instruction execution time		On-chip minimum instruction execution time cycle variable function			
	When main system clock selected	• Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A: 0.166 μs/0.333 μs/0.666 μs/1.33 μs/2.66 μs (@12 MHz, V_{DD} = 4.5 to 5.5 V operation) • μPD780021AY, 780022AY, 780023AY, 780024AY and conventional products of μPD780021A, 780022A, 780023A, 780024A: 0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@8.38 MHz, V_{DD} = 4.0 to 5.5 V operation)			
	When subsystem clock selected	122 μs (@ 32.768 kHz operation)			
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.			
I/O ports		Total: 51 • CMOS input: 8 • CMOS I/O: 39 • N-ch open-drain I/O (5 V withstanding voltage): 4			
A/D converter		• 8-bit resolution × 8 channels • Low-voltage operation available: AV_{DD} = 1.8 to 5.5 V			
Serial interface		• μPD780021A, 780022A, 780023A, 780024A UART mode: 1 channel 3-wire serial I/O mode: 2 channels • μPD780021AY, 780022AY, 780023AY, 780024AY UART mode: 1 channel 3-wire serial I/O mode: 1 channel I^2C bus mode (multimaster supporting): 1 channel			
Timers		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel			
Timer outputs		3 (8-bit PWM output capable: 2)			

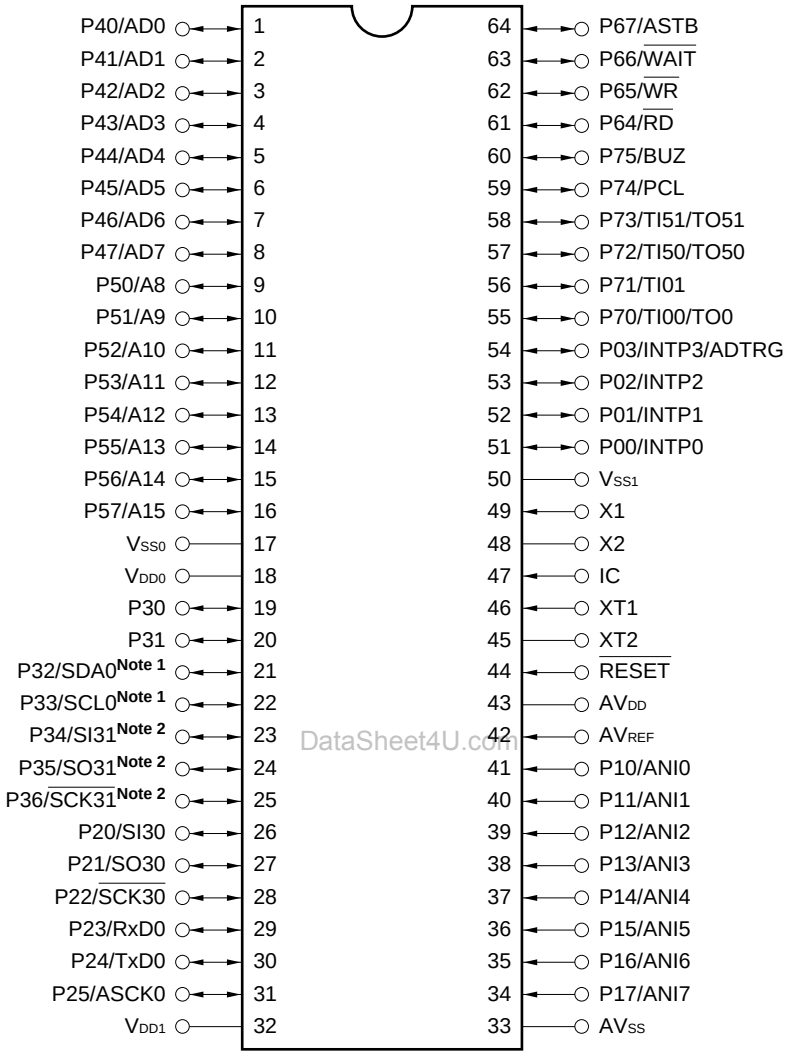
OVERVIEW OF FUNCTIONS (2/2)

Item \ Part Number		μPD780021A μPD780021AY	μPD780022A μPD780022AY	μPD780023A μPD780023AY	μPD780024A μPD780024AY
★ Clock output		• Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A: 93.75 kHz, 187.5 kHz, 375 kHz, 750 kHz, 1.25 MHz, 3 MHz, 6 MHz, 12 MHz (@12MHz operation with main system clock) 32.768 kHz (@ 32.768 kHz operation with subsystem clock) • μPD780021AY, 780022AY, 780023AY, 780024AY and conventional products of μPD780021A, 780022A, 780023A, 780024A: 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38 MHz operation with main system clock) 32.768 kHz (@ 32.768 kHz operation with subsystem clock)			
★ Buzzer output		• Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A: 1.46 kHz, 2.93 kHz, 5.86 kHz, 11.7 kHz (@ 12 MHz operation with main system clock) • μPD780021AY, 780022AY, 780023AY, 780024AY and conventional products of μPD780021A, 780022A, 780023A, 780024A: 1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38 MHz operation with main system clock)			
Vectored interrupt sources	Maskable	Internal: 13, external: 5			
	Non-maskable	Internal: 1			
	Software	1			
Power supply voltage		V_{DD} = 1.8 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85°C			
Package		• 64-pin plastic SDIP (19.05 mm (750)) • 64-pin plastic QFP (14 x 14) ★ • 64-pin plastic LQFP (14 x 14) • 64-pin plastic TQFP (12 x 12) ★ • 64-pin plastic LQFP (10 x 10) ★ • 73-pin plastic FBGA (9 x 9)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic SDIP (19.05 mm (750))**



Notes 1. SDA0 and SCL0 are incorporated only in the μPD780024AY Subseries.

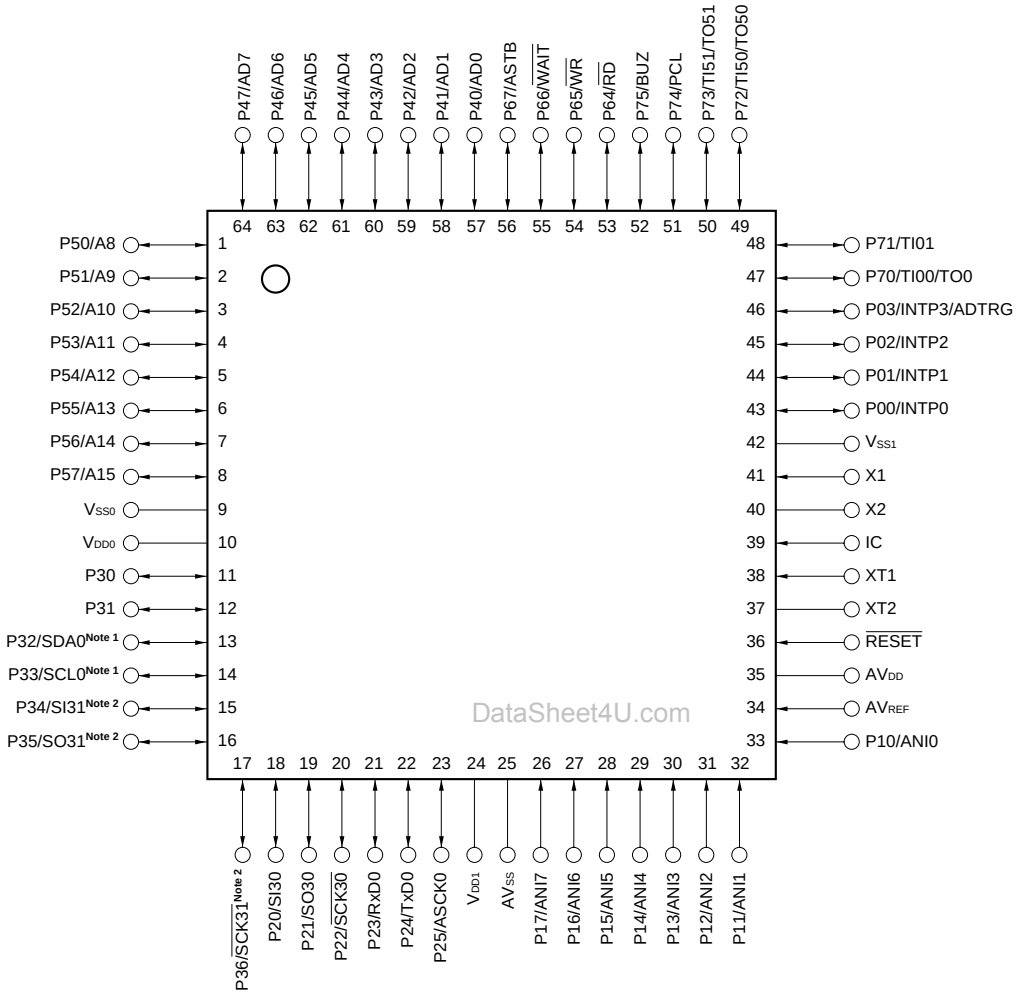
2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD780024A Subseries.

Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, and 780024AY are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

- **64-pin plastic QFP (14 x 14)**
- ★ **64-pin plastic LQFP (14 x 14)**
- **64-pin plastic TQFP (12 x 12)**
- ★ **64-Pin plastic LQFP (10 x 10)**



Notes 1. SDA0 and SCL0 are incorporated only in the μPD780024AY Subseries.

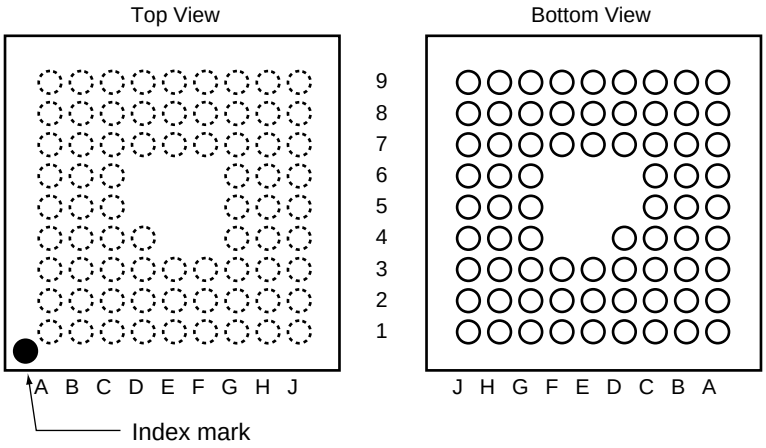
2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD780024A Subseries.

Cautions 1. Connect the IC (Internally Connected) pin directory to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, and 780024AY are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

★ • **73-pin plastic FBGA (9 x 9)**



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	NC	C1	P52/A10	E1	P57/A15	G1	P33/SCL0Note 1	J1	NC
A2	P46/AD6	C2	P53/A11	E2	V_{DD0}	G2	P32/SDA0Note 1	J2	P36/$\overline{SCK31}$Note 2
A3	P44/AD4	C3	P45/AD5	E3	P54/A12	G3	P20/SI30	J3	NC
A4	P41/AD1	C4	P42/AD2	E4	–	G4	P21/SO30	J4	P25/ASCK0
A5	P67/ASTB	C5	P64/$\overline{RD}$	E5	–	G5	P24/TxD0	J5	NC
A6	P65/$\overline{WR}$	C6	P73/TI51/TO51	E6	–	G6	V_{DD1}	J6	P17/ANI7
A7	P74/PCL	C7	P03/INTP3/ADTRG	E7	P00/INTP0	G7	P16/ANI6	J7	P12/ANI2
A8	NC	C8	P01/INTP1	E8	XT1	G8	AV_{DD}	J8	P13/ANI3
A9	NC	C9	V_{SS1}	E9	X2	G9	NC	J9	NC
B1	P51/A9	D1	P55/A13	F1	P30	H1	P34/SI31Note 2		
B2	P47/AD7	D2	P56/A14	F2	P31	H2	P35/SO31Note 2		
B3	P43/AD3	D3	P50/A8	F3	V_{SS0}	H3	P23/RxD0		
B4	P40/AD0	D4	NC	F4	–	H4	P22/$\overline{SCK30}$		
B5	P66/$\overline{WAIT}$	D5	–	F5	–	H5	AV_{SS}		
B6	P75/BUZ	D6	–	F6	–	H6	P15/ANI5		
B7	P72/TI50/TO51	D7	P02/INTP2	F7	P14/ANI4	H7	P11/ANI1		
B8	P71/TI01	D8	IC	F8	$\overline{RESET}$	H8	P10/ANI0		
B9	P70/TI00/TO0	D9	X1	F9	XT2	H9	AV_{REF}		

Notes 1. SDA0 and SCL0 are incorporated only in the μPD780024AY Subseries.

2. SI31, SO31, and $\overline{SCK31}$ are incorporated only in the μPD780024A Subseries.

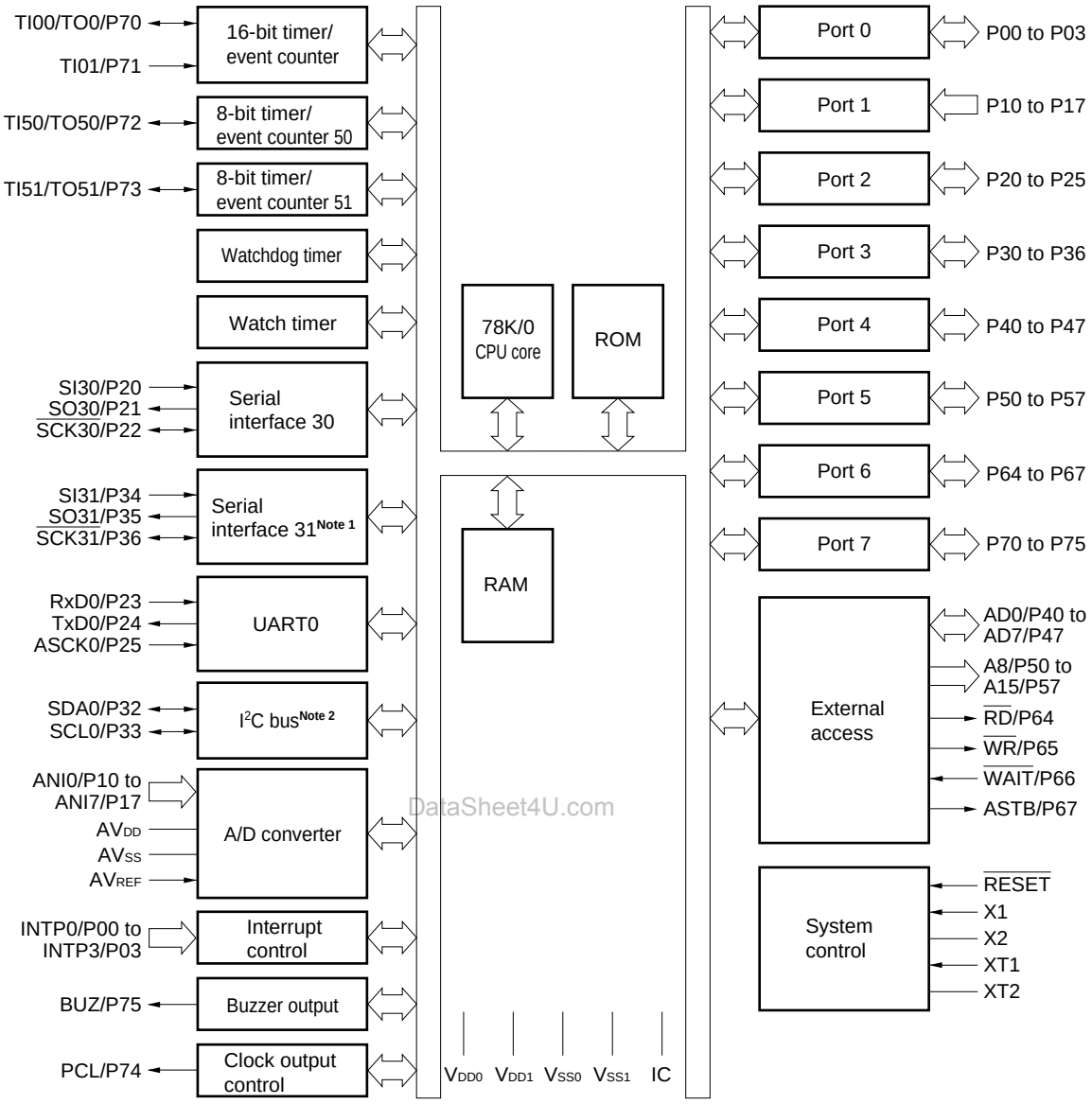
Cautions 1. Connect the IC (Internally Connected) pin directory to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, and 780024AY are used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15:	Address bus
AD0 to AD7:	Address/data bus
ADTRG:	AD trigger input
ANI0 to ANI7:	Analog input
ASCK0:	Asynchronous serial clock
ASTB:	Address strobe
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BUZ:	Buzzer clock
IC:	Internally connected
INTP0 to INTP3:	External interrupt input
★ NC:	No connection
P00 to P03:	Port 0
P10 to P17:	Port 1
P20 to P25:	Port 2
P30 to P36:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P64 to P67:	Port 6
P70 to P75:	Port 7
PCL:	Programmable clock
$\overline{RD}$:	Read strobe
$\overline{RESET}$:	Reset
RxD0:	Receive data
$\overline{SCK30}$, $\overline{SCK31}$, SCL0:	Serial clock
SDA0:	Serial data
SI30, SI31:	Serial input
SO30, SO31:	Serial output
TI00, TI01, TI50, TI51:	Timer input
TO0, TO50, TO51:	Timer output
TxD0:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{SS0}, V_{SS1}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write strobe
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM



Notes 1. Incorporated only in the μPD780024A Subseries.

2. Incorporated only in the μPD780024AY Subseries.

Remark The internal ROM and RAM capacities vary depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P02	I/O	Port 0 4-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.	Input	INTP0 to INTP2
P03				INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port	Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.	Input	SI30
P21				SO30
P22				$\overline{\text{SCK30}}$
P23				RxD0
P24				TxD0
P25				ASCK0
P30	I/O	Port 3 7-bit I/O port Input/output can be specified in 1-bit units.	N-ch open-drain I/O port An on-chip pull-up resistor can be specified by the mask option. LEDs can be driven directly.	Input	—
P31					
P32					SDA0Note 1
P33					SCL0Note 1
P34			An on-chip pull-up resistor can be used by setting software.		SI31Note 2
P35					SO31Note 2
P36					$\overline{\text{SCK31}}$Note 2
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.		Input	A8 to A15
P64	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

Notes 1. SDA0 and SCL0 are incorporated only in the μPD780024AY Subseries.

2. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD780024A Subseries.

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit I/O port Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00
INTP2				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input	Input	P20
SI31Note 1				P34
SO30	Output	Serial interface serial data output	Input	P21
SO31Note 1				P35
SDA0Note 2	I/O	Serial Interface serial data input/output	Input	P32
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output	Input	P22
$\overline{\text{SCK31}}$Note 1				P36
SCL0Note 2				P33
RxD0	Input	Serial data input for asynchronous serial interface	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P25
TI00	Input	External count clock input to 16-bit timer/event counter 0 Capture trigger input to capture register 01 (CR01) of 16-bit timer/event counter 0	Input	P70/TO0
TI01		Capture trigger input to capture register 00 (CR00) of 16-bit timer/event counter 0		P71
TI50		External count clock input to 8-bit timer/event counter 50		P72/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P73/TO51
TO0	Output	16-bit timer/event counter 0 output	Input	P70/TI00
TO50		8-bit timer/event counter 50 output (also used for 8-bit PWM output)	Input	P72/TI50
TO51		8-bit timer/event counter 51 output (also used for 8-bit PWM output)		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P74
BUZ	Output	Buzzer output	Input	P75
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for reading from external memory	Input	P64
$\overline{\text{WR}}$		Strobe signal output for writing to external memory		P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output that externally latches address information output to ports 4 and 5 to access external memory	Input	P67

Notes 1. SI31, SO31, and $\overline{\text{SCK31}}$ are incorporated only in the μPD780024A Subseries.

2. SDA0 and SCL0 are incorporated only in the μPD780024AY Subseries.

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage input	—	—
AV_{DD}	—	A/D converter analog power supply. Set potential to that of V_{DD0} or V_{DD1}	—	—
AV_{SS}	—	A/D converter ground potential. Set potential to that of V_{SS0} or V_{SS1}	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply for ports	—	—
V_{SS0}	—	Ground potential of ports	—	—
V_{DD1}	—	Positive power supply (except ports)	—	—
V_{SS1}	—	Ground potential (except ports)	—	—
IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	—	—
★ NC[Note]	—	Not internally connected. Leave open.	—	—

★ **Note** NC pins are incorporated only in the 73-pin plastic FBGA.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

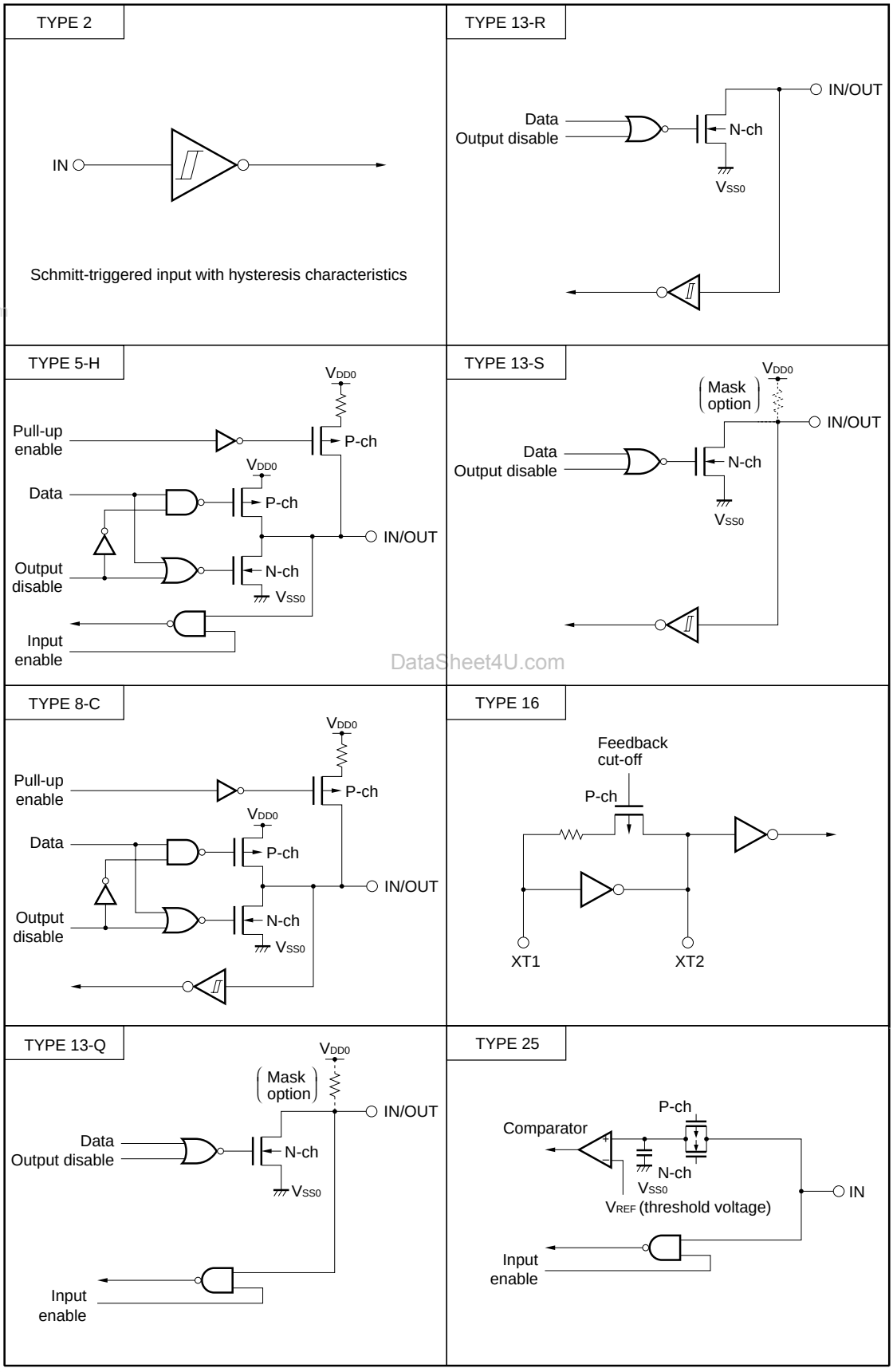
The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the I/O circuit configuration of each type, see Figure 3-1.

★ **Table 3-1. Types of Pin I/O Circuits**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-C	I/O	Input: Independently connect to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P03/INTP3/ADTRG			
P10/ANI0 to P17/ANI7	25	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.
P20/S130	8-C	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P21/SO30	5-H		
P22/$\overline{SCK30}$	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30, P31	13-Q		Input: Connect directly to V_{SS0} or V_{SS1}. Output: Leave open at low-level output.
P32, P33 (μPD780024A Subseries only)	13-S		
P32/SDA0 (μPD780024AY Subseries only)	13-R		
P33/SCL0 (μPD780024AY Subseries only)			
P34/SI31[Note]	8-C		Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P35/SO31[Note]	5-H		
P36/$\overline{SCK31}$[Note]	8-C		
P40/AD0 to P47/AD7	5-H		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P50/A8 to P57/A15			Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/TI00/TO0	8-C		
P71/TI01			
P72/TI50/TO50			
P73/TI51/TO51			
P74/PCL	5-H		
P75/BUZ			
$\overline{RESET}$	2	Input	—
XT1	16		Connect directly to V_{DD0} or V_{DD1}.
XT2		—	Leave open.
AV_{DD}	—		Connect to directly V_{DD0} or V_{DD1}.
AV_{REF}			Connect to directly V_{SS0} or V_{SS1}.
AV_{SS}			
IC			

Note SI31, SO31, and $\overline{SCK31}$ are incorporated only in the μPD780024A Subseries.

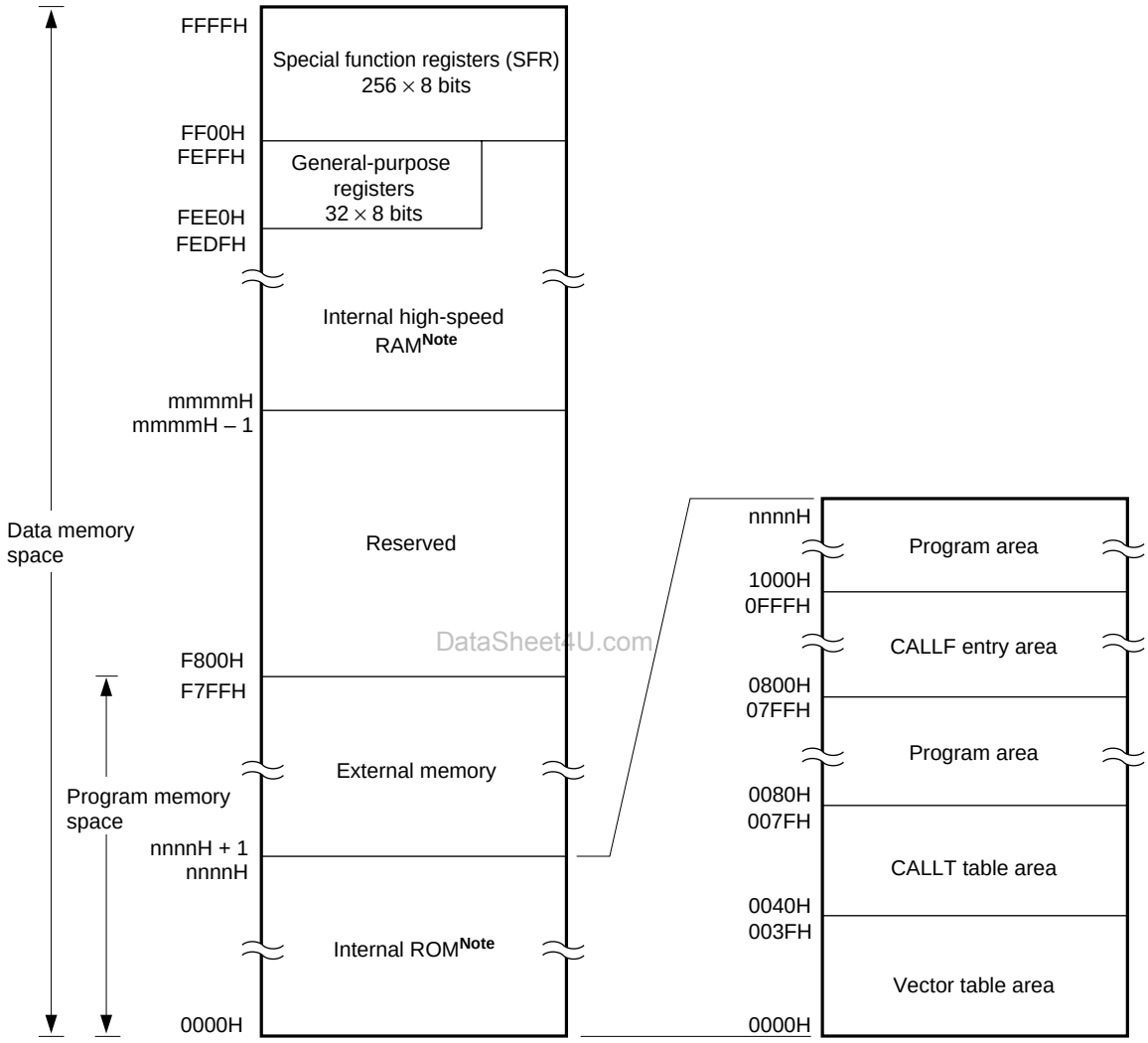
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, and 780024AY.

Figure 4-1. Memory Map



Note The internal ROM and internal high-speed RAM capacities vary depending on the product (see the following table).

Part Number	Last Address of Internal ROM nnnnH	Start Address of Internal High-Speed RAM mmmmH
μPD780021A, 780021AY	1FFFH	FD00H
μPD780022A, 780022AY	3FFFH	
μPD780023A, 780023AY	5FFFH	FB00H
μPD780024A, 780024AY	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (port 1): 8
- CMOS I/O (ports 0, 2, 4 to 7, P34 to P36): 39
- N-channel open-drain I/O (P30 to P33): 4

Total: 51

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.
Port 1	P10 to P17	Input-only port.
Port 2	P20 to P25	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.
Port 3	P30 to P33	N-channel open-drain I/O port. Input/output can be specified in 1-bit units. A pull-up resistor can be specified by mask option. LEDs can be driven directly.
	P34 to P36	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software. LEDs can be driven directly.
Port 6	P64 to P67	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.
Port 7	P70 to P75	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be used by setting software.

5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

★ • Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A

0.166 μs/0.333 μs/0.666 μs/1.33 μs/2.66 μs

(@12 MHz, V_{DD} = 4.5 to 5.5 V operation with main system clock)

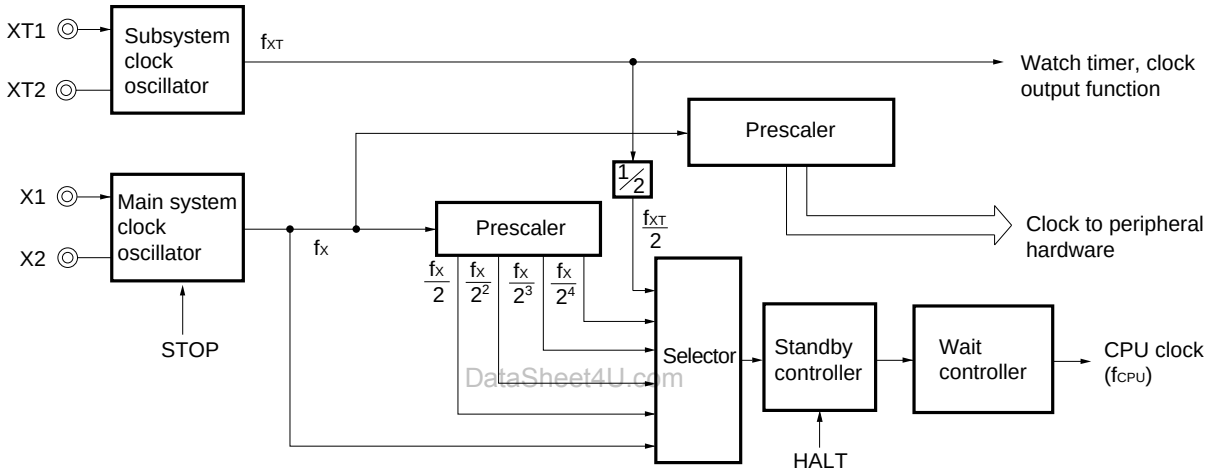
122 μs (@32.768 kHz, V_{DD} = 4.0 to 5.5 V operation with subsystem clock)

• μPD780021AY, 780022AY, 780023AY, 780024AY, and conventional products of μPD780021A, 780022A, 780023A, 780024A

0.238 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@8.38 MHz, V_{DD} = 4.0 to 5.5 V operation with main system clock)

122 μs (@32.768 kHz, V_{DD} = 4.0 to 5.5 V operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Counter

Five timer/counter channels are incorporated.

- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

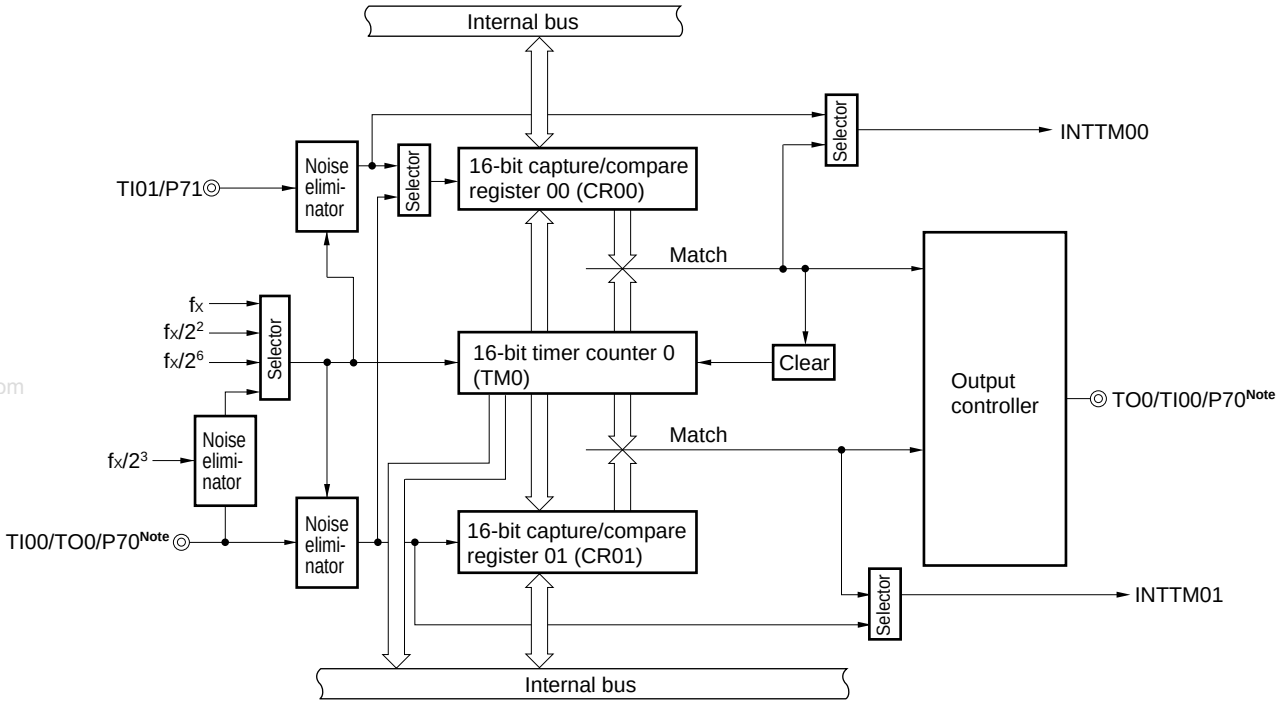
Table 5-2. Operations of Timer/Event Counter

	16-Bit Timer/ Event Counter 0	8-Bit Timer/ Event Counters 50, 51	Watch Timer	Watchdog Timer
Operation mode				
Interval timer	1 channel	2 channels	1 channel[Note 1]	1 channel[Note 2]
External event counter	1 channel	2 channels	—	—
Function				
Timer outputs	1	2	—	—
PPG outputs	1	—	—	—
PWM output	—	2	—	—
Pulse width measurement	2 inputs	—	—	—
Square wave outputs	1	2	—	—
Interrupt sources	2	2	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter 0



★ **Note** TI00 input and TO0 output cannot be used at the same time.

Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 50

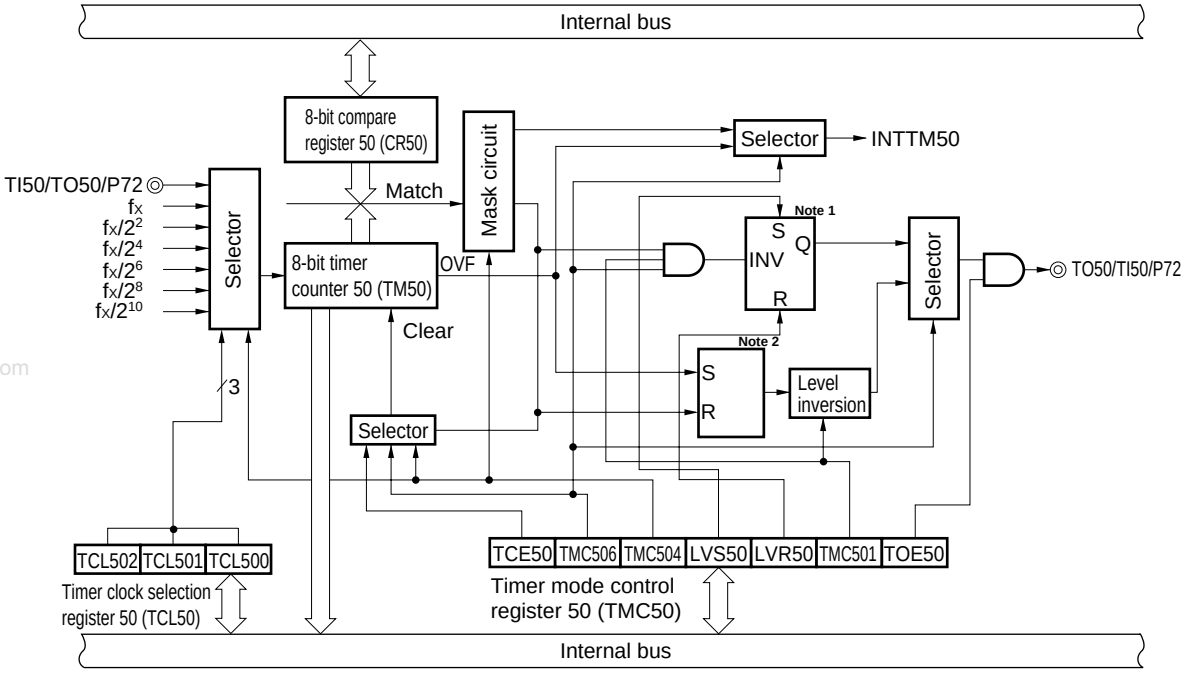
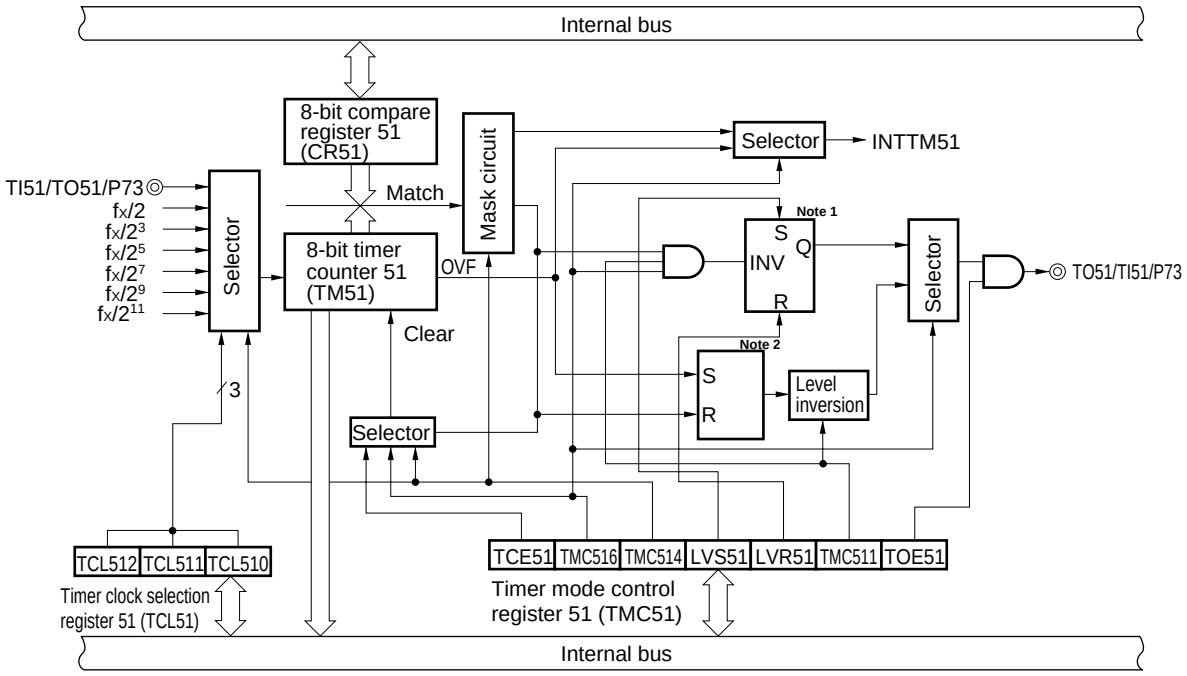


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 51



Notes 1. Timer output F/F

2. PWM output F/F

Figure 5-5. Watch Timer Block Diagram

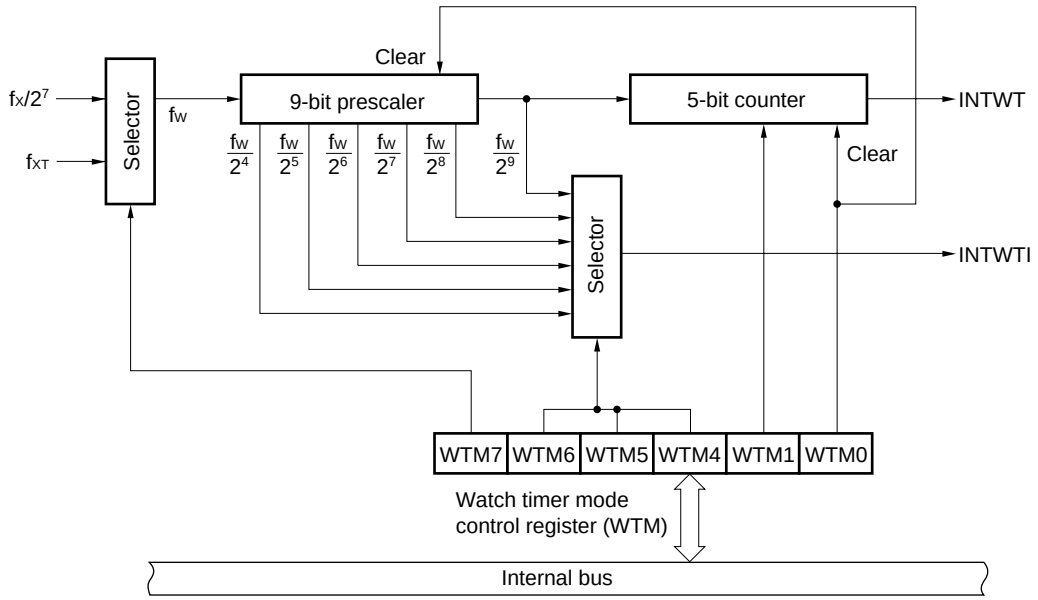
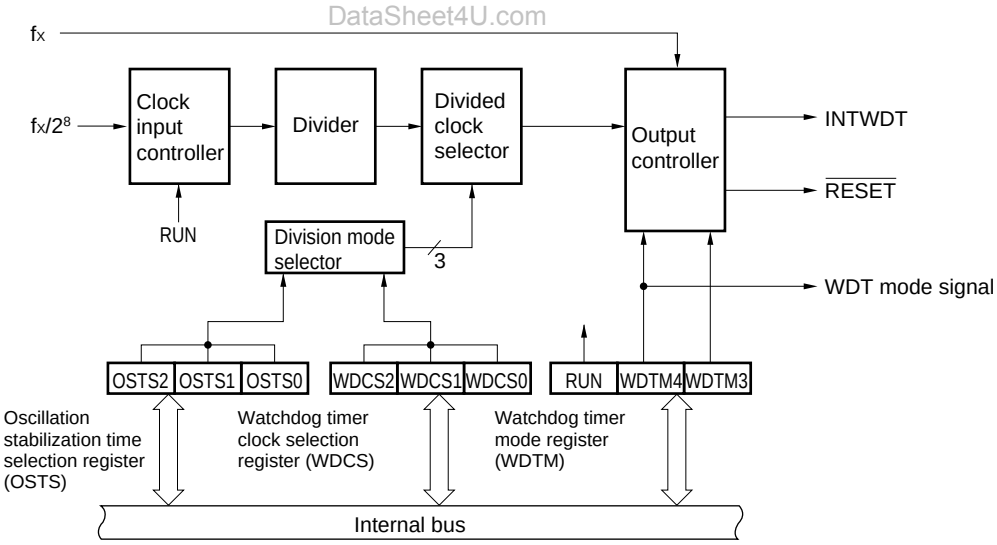


Figure 5-6. Watchdog Timer Block Diagram



5.4 Clock Output/Buzzer Output Controller

A clock output/buzzer output controller is incorporated.

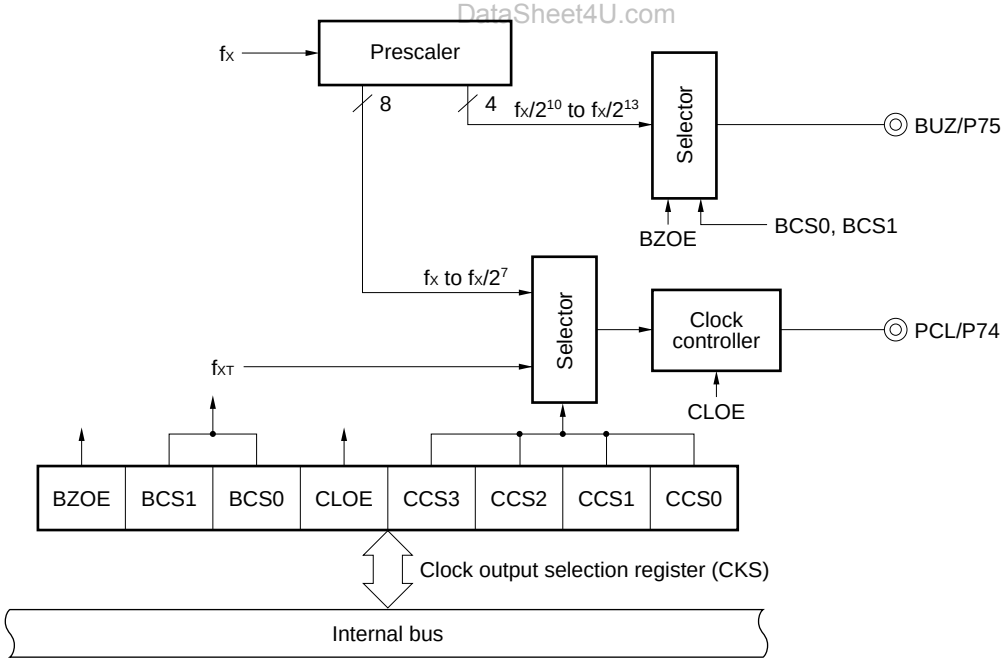
Clocks with the following frequencies can be output as clock output.

★ • **Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A**
  - 93.75 kHz/187.5 kHz/375 kHz/750 kHz/1.25 MHz/3 MHz/6 MHz/12 MHz (@12 MHz operation with main system clock)
  - 32.768 kHz (@32.768 kHz operation with subsystem clock)
- **μPD780021AY, 780022AY, 780023AY, 780024AY, and conventional products of μPD780021A, 780022A, 780023A, 780024A**
  - 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (@8.38 MHz operation with main system clock)
  - 32.768 kHz (@32.768 kHz operation with subsystem clock)

Clocks with the following frequencies can be output as buzzer output.

★ • **Expanded-specification products of μPD780021A, 780022A, 780023A, 780024A**
  1.46 kHz/2.93 kHz/5.86 kHz/11.7 kHz (@12 MHz operation with main system clock)
- **μPD780021AY, 780022AY, 780023AY, 780024AY, and conventional products of μPD780021A, 780022A, 780023A, 780024A**
  1.02 kHz/2.05 kHz/4.10 kHz/8.19 kHz (@8.38 MHz operation with subsystem clock)

Figure 5-7. Block Diagram of Clock Output/Buzzer Output Control Circuit



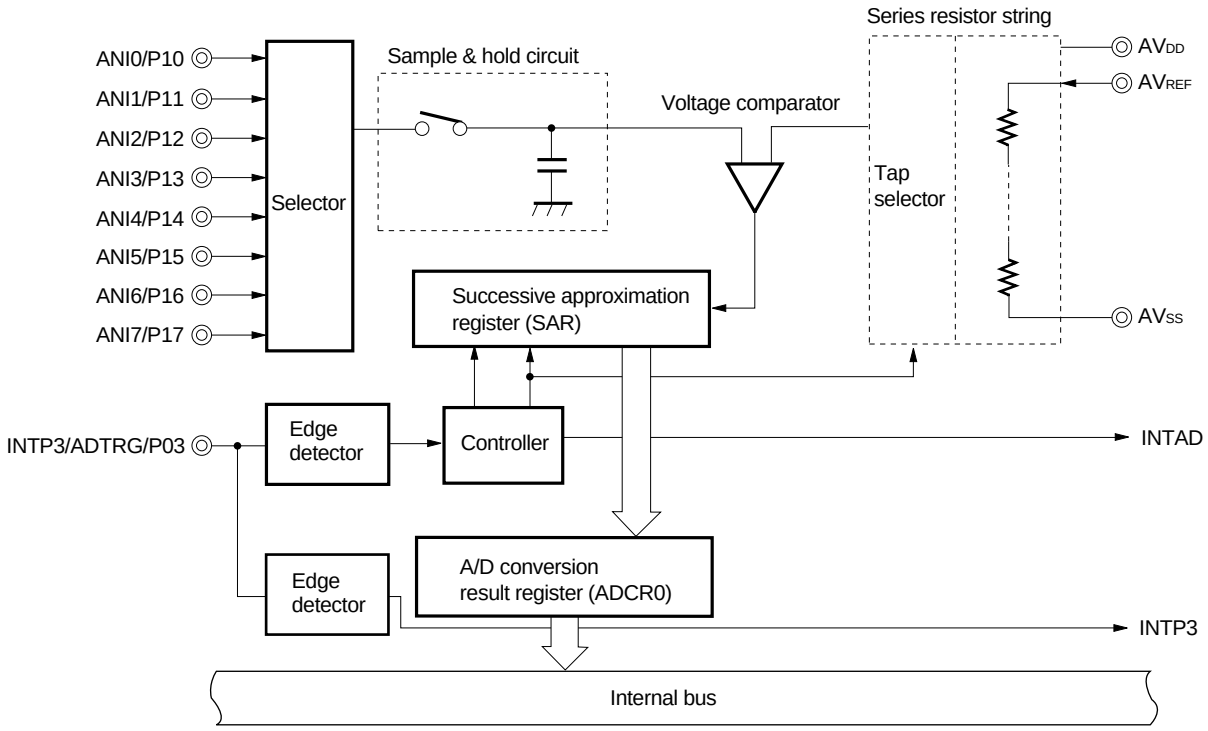
5.5 A/D Converter

An A/D converter consisting of eight 8-bit resolution channels is incorporated.

The following two A/D conversion operation startup methods are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram



5.6 Serial Interface

Three serial interface channels are incorporated.

- μPD780024A Subseries
  Serial interface UART0: 1 channel
  Serial interface SIO30, SIO31: 2 channels
- μPD780024AY Subseries
  Serial interface UART0: 1 channel
  Serial interface SIO30: 1 channel
  Serial interface IIC0 1 channel

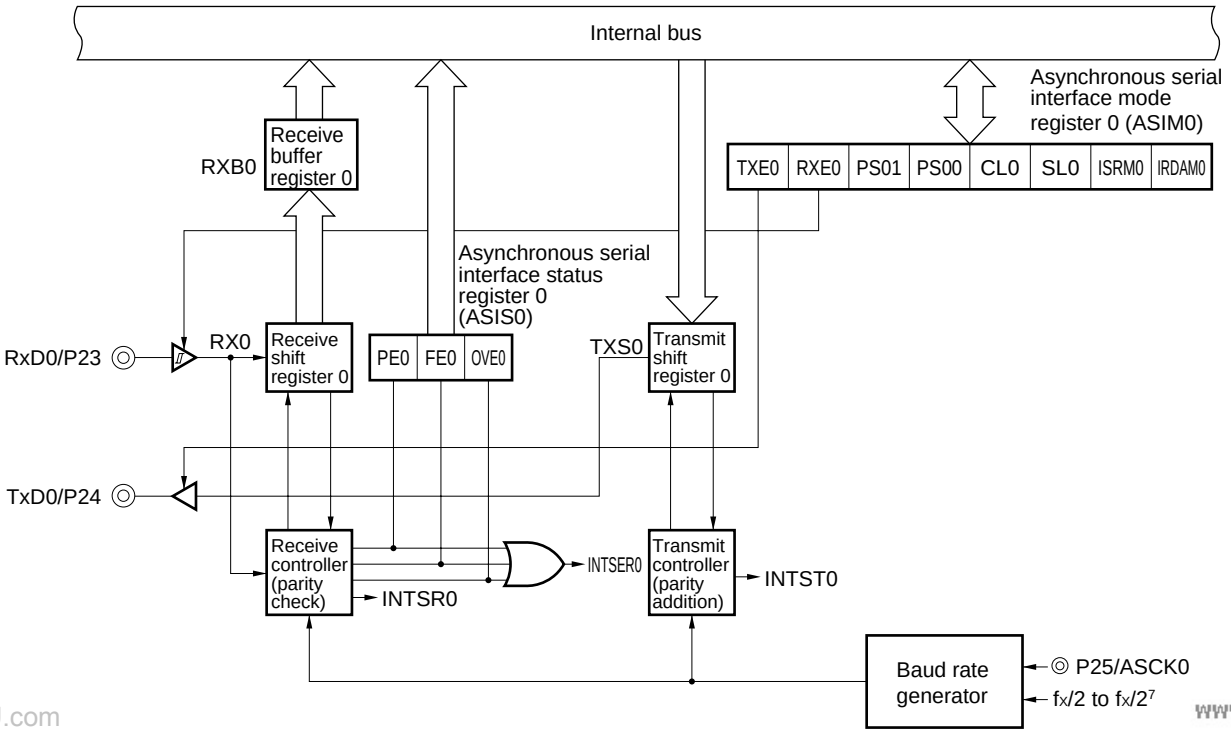
(1) Serial interface UART0

 Serial interface UART0 has two modes: asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**
  This mode enables full-duplex operation wherein one byte of data starting from the start bit is transmitted and received.
  The on-chip UART-dedicated baud-rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can also be defined by dividing the clock input to the ASCK0 pin.
  The UART-dedicated baud-rate generator can also be used to generate a MIDI-standard baud rate (31.25 kbps).

- **Infrared data transfer mode**
  This mode enables pulse output and pulse reception in data format.
  This mode can be used for office equipment applications such as personal computers.

Figure 5-9. Block Diagram of Serial Interface UART0



(2) Serial interface SIO3n

Serial interface SIO3n has one mode: 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

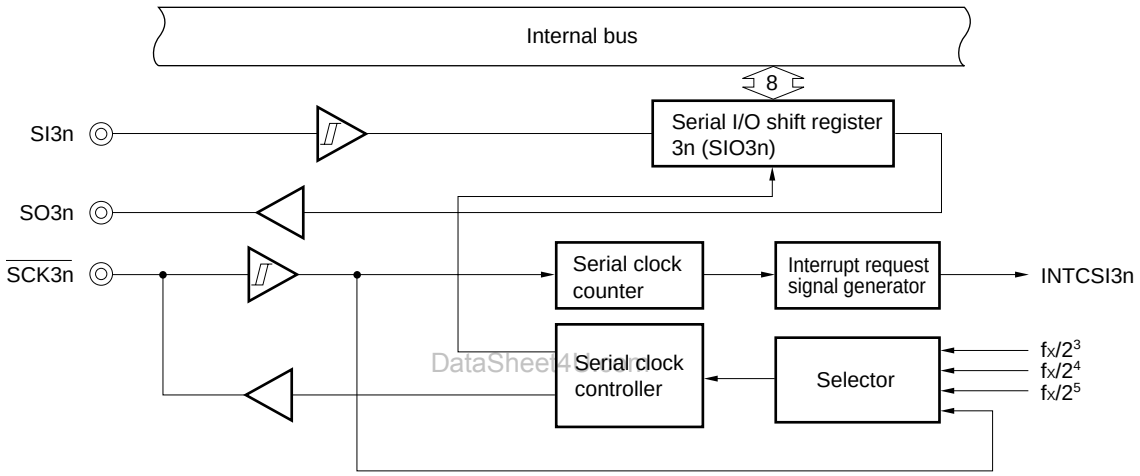
  This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{\text{SCK3n}}$), serial output line (SO3n), and serial input line (SI3n).

  Since simultaneous transmit and receive operations are enabled in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to peripheral I/O devices, and display controllers, etc., that include a clocked serial interface.

Figure 5-10. Block Diagram of Serial Interface SIO3n



Remark μPD780024A Subseries: n = 0, 1
μPD780024AY Subseries: n = 0

(3) Serial interface IIC0 (μPD780024AY Subseries only)

Serial interface IIC0 has one mode: I²C (Inter IC) bus mode (supporting multimaster).

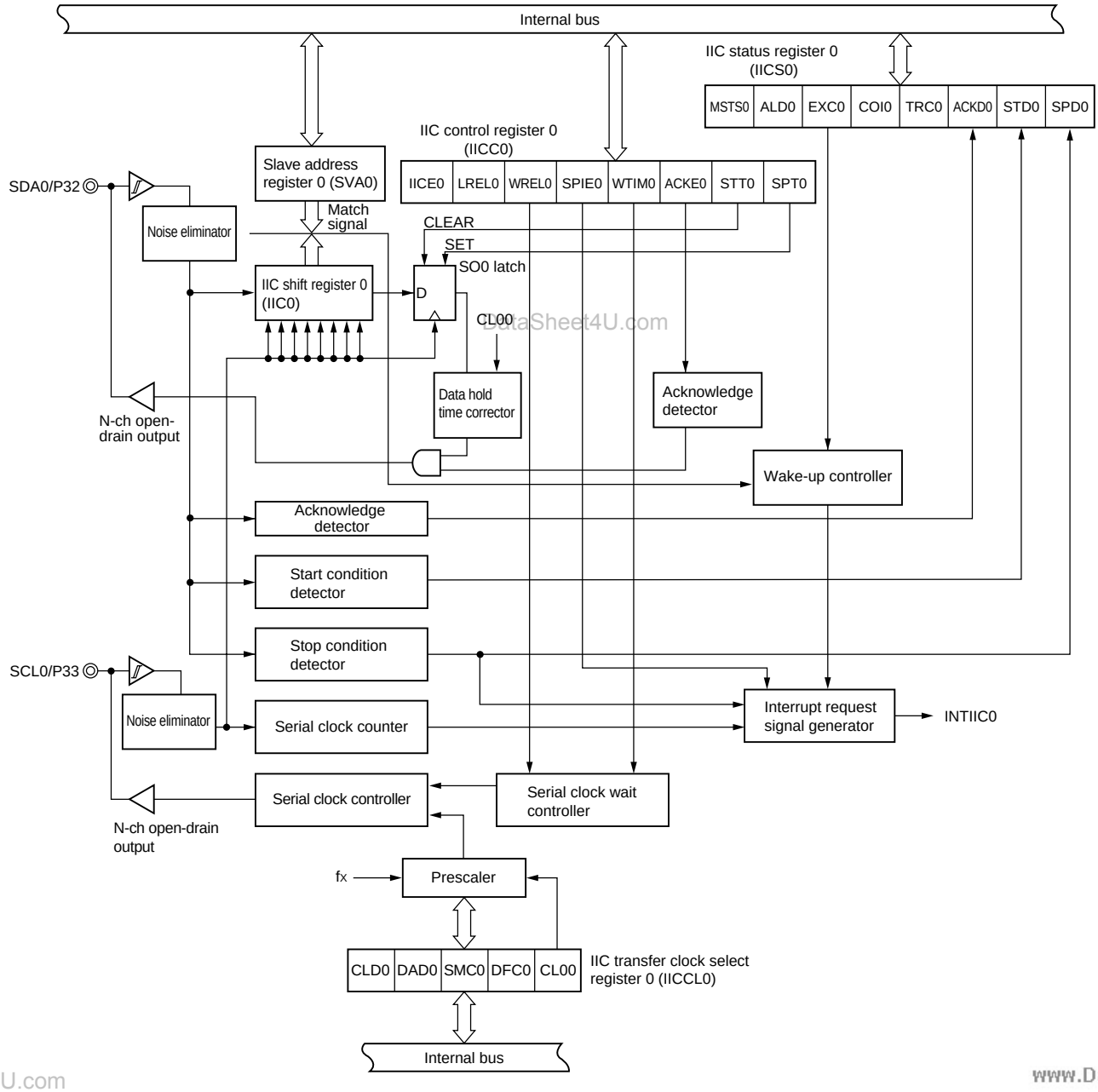
- **I²C bus mode (supporting multimaster)**

  This is an 8-bit data transfer mode using two lines: a serial clock line (SCL0) and a serial data bus line (SDA0).

  This mode complies with the I²C bus format, and can output a “start condition”, “data”, and a “stop condition” during transmission via the serial data bus. This data is automatically detected by hardware during reception.

  Since SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

Figure 5-11. Block Diagram of Serial Interface IIC0



6. INTERRUPT FUNCTIONS

A total of 20 interrupt sources are provided, divided into the following three types.

- Non-maskable: 1
- Maskable: 18
- Software: 1

Table 6-1. Interrupt Source List

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Serial interface UART0 reception error generation	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI30	End of serial interface SIO30 transfer		0014H	
	9	INTCSI31	End of serial interface SIO31 transfer [Only for μPD780024A Subseries]		0016H	
	10	INTIIC0	End of serial interface IIC0 transfer [Only for μPD780024AY Subseries]		0018H	
	11	INTWTI	Reference time interval signal from watch timer		001AH	
	12	INTTM00	Match between TM0 and CR00 (when CR00 is specified as compare register) Detection of TI01 valid edge (when CR00 is specified as capture register)		001CH	
	13	INTTM01	Match between TM0 and CR01 (when CR01 is specified as compare register) Detection of TI00 valid edge (when CR01 is specified as capture register)		001EH	
	14	INTTM50	Match between TM50 and CR50		0020H	
	15	INTTM51	Match between TM51 and CR51		0022H	
	16	INTAD0	End of A/D conversion		0024H	
	17	INTWT	Watch timer overflow		0026H	
	18	INTKR	Port 4 falling edge detection	External	0028H	(D)
Software	—	BRK	BRK instruction execution	—	003EH	(E)

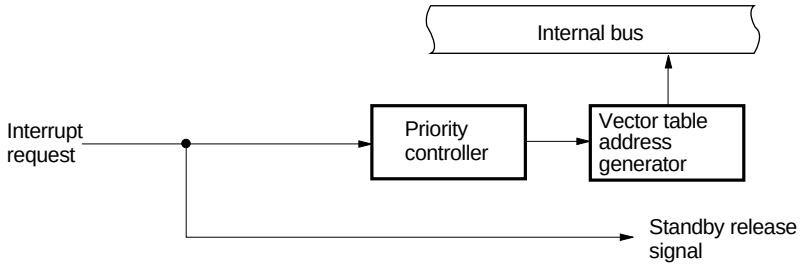
Notes 1. The default priority is the priority when several maskable interrupt requests are generated at the same time. 0 is the highest, and 18 is the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

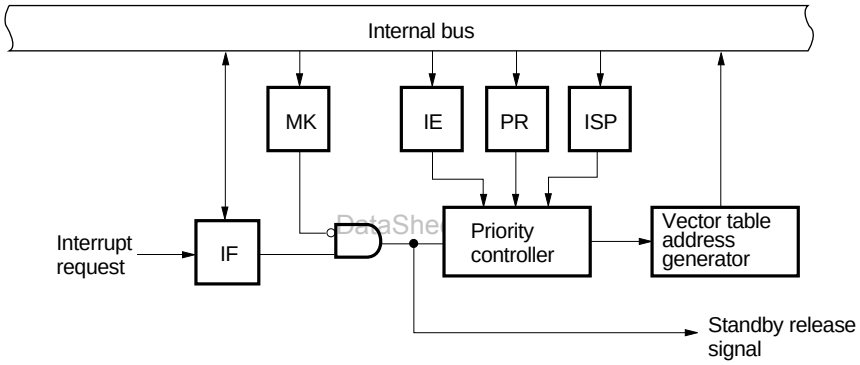
Remark The watchdog timer interrupt (INTWDT) can be selected from a non-maskable interrupt or a maskable interrupt (internal).

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP3)

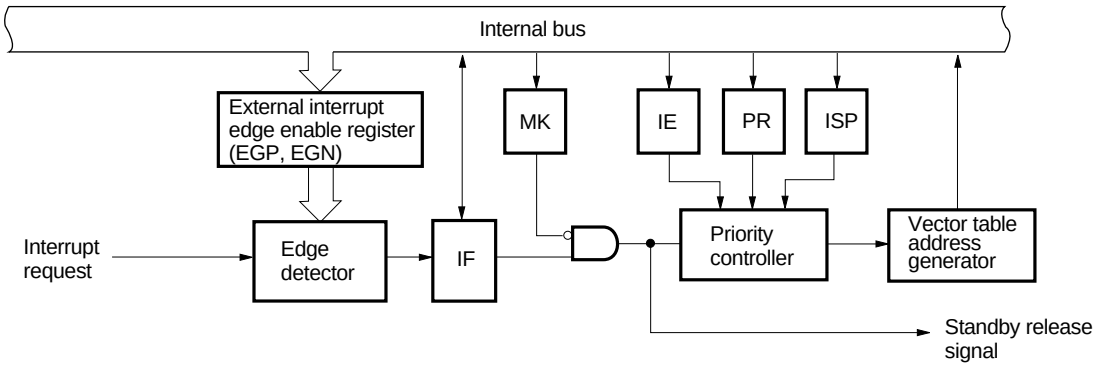
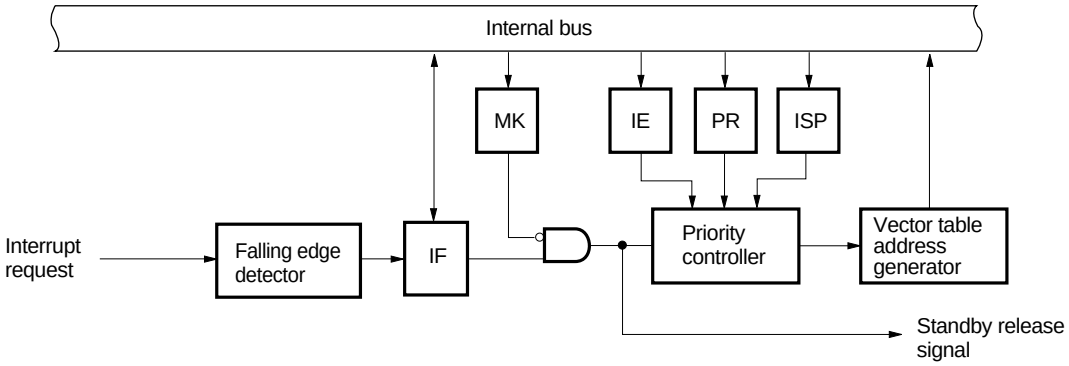
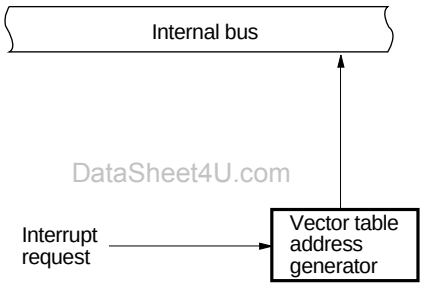


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)



(E) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

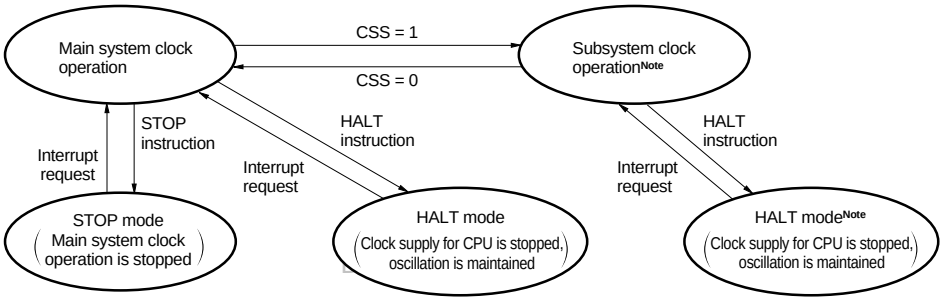
The external device expansion function is for connecting external devices to areas other than the internal ROM, RAM, and SFR areas. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

The following two standby modes are available for further reduction of system power consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average power consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption. This can be used only when the main system clock is operating (the subsystem clock oscillation cannot be stopped).

Figure 8-1. Standby Function



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC). The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer program loop time detection

10. MASK OPTION

Table 10-1 Pin Mask Option Selection

Subseries Name	Pins	Mask Option
μPD780024A Subseries	P30 to P33	An on-chip pull-up resistor can be specified in 1-bit units.
μPD780024AY Subseries	P30 and P31	

The mask option can be used to specify the connection of an on-chip pull-up resistor to P30 to P33[Note], in 1-bit units.

Note The μPD780024AY Subseries has P30 and P31 only.

11. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 12. ELECTRICAL SPECIFICATIONS

12.1 Expanded-Specification Products of μPD780021A, 780022A, 780023A, 780024A

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +6.5	V
	AV_{DD}				–0.3 to V_{DD} + 0.3[Note]	V
	AV_{REF}				–0.3 to V_{DD} + 0.3[Note]	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{\text{RESET}}$			–0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P30 to P33	N-ch open-drain	Without pull-up resistor	–0.3 to + 6.5	V
				With pull-up resistor	–0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}	P10 to P17		Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3[Note] and –0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin			–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75			–15	mA
		Total for P20 to P25, P30 to P36			–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75			20	mA
		Per pin for P30 to P33, P50 to P57			30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75			50	mA
		Total for P20 to P25			20	mA
		Total for P30 to P36			100	mA
		Total for P50 to P57			100	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note 6.5 V or below

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

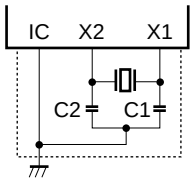
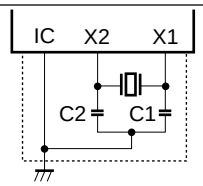
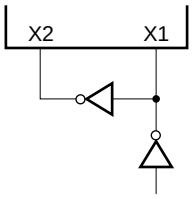
Remark Unless otherwise specified, the characteristic of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75			15	pF
			P30 to P33			20	pF

Remark Unless otherwise specified, the characteristic of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		Oscillation stabilization time[Note 2]	4.0 V ≤ V_{DD} ≤ 5.5 V			10	ms
			1.8 V ≤ V_{DD} < 4.0 V			30	
External clock		X1 input frequency (f_X)[Note 1]	4.5 V ≤ V_{DD} ≤ 5.5 V	1.0		12.0	MHz
			3.0 V ≤ V_{DD} < 4.5 V	1.0		8.38	
			1.8 V ≤ V_{DD} < 3.0 V	1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	4.5 V ≤ V_{DD} ≤ 5.5 V	38		500	ns
			3.0 V ≤ V_{DD} < 4.5 V	50		500	
			1.8 V ≤ V_{DD} < 3.0 V	85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

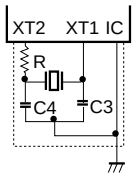
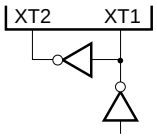
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	4.0 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 V ≤ V_{DD} < 4.0 V			10	
External clock		XT1 input frequency (f_{XT})Note 1		32		38.5	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		12		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Recommended Oscillator Constant

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSBFB1M00J58	1.00	100	100	2.2	1.8	5.5
	CSBLA1M00J58	1.00	100	100	2.2	1.8	5.5
	CSTCC2M00G56	2.00	On-chip	On-chip	0	1.8	5.5
	CSTLS2M00G56	2.00	On-chip	On-chip	0	1.8	5.5
	CSTCC3M58G53	3.58	On-chip	On-chip	0	1.8	5.5
	CSTLS3M58G53	3.58	On-chip	On-chip	0	1.8	5.5
	CSTCR4M00G53	4.00	On-chip	On-chip	0	1.8	5.5
	CSTLS4M00G53	4.00	On-chip	On-chip	0	1.8	5.5
	CSTCR4M19G53	4.19	On-chip	On-chip	0	1.8	5.5
	CSTLS4M19G53	4.19	On-chip	On-chip	0	1.8	5.5
	CSTCR4M91G53	4.91	On-chip	On-chip	0	1.8	5.5
	CSTLS4M91G53	4.91	On-chip	On-chip	0	1.8	5.5
	CSTCR5M00G53	5.00	On-chip	On-chip	0	1.8	5.5
	CSTLS5M00G53	5.00	On-chip	On-chip	0	1.8	5.5
	CSTCE8M00G52	8.00	On-chip	On-chip	0	3.0	5.5
	CSTLS8M00G53	8.00	On-chip	On-chip	0	3.0	5.5
	CSTCE8M38G52	8.38	On-chip	On-chip	0	3.0	5.5
	CSTLS8M38G53	8.38	On-chip	On-chip	0	3.0	5.5
	CSTCE10M0G52	10.00	On-chip	On-chip	0	4.5	5.5
	CSTLS10M0G53	10.00	On-chip	On-chip	0	4.5	5.5
	CSTCE12M0G52	12.00	On-chip	On-chip	0	4.5	5.5
	CSTLA12M0T55	12.00	On-chip	On-chip	0	4.5	5.5
TDK	CCR3.58MC3	3.58	On-chip	On-chip	0	1.8	5.5
	CCR4.19MC3	4.19	On-chip	On-chip	0	1.8	5.5
	CCR5.0MC3	5.00	On-chip	On-chip	0	1.8	5.5
	CCR8.0MC5	8.00	On-chip	On-chip	0	2.0	5.5
	CCR8.38MC5	8.38	On-chip	On-chip	0	2.0	5.5

Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD780024A Subseries within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		5.5	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		5.5	V
	V_{IH4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.15V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		1.8 V ≤ V_{DD} < 4.0 V, I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33[Note]			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33[Note]			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistance	R_1	V_{IN} = 0 V, P30, P31, P32, P33		15	30	90	kΩ
Software pull-up resistance	R_2	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Note When pull-up resistors are not connected to P30 to P33 (specified by the mask option).

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	12.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		8.5	17	mA
				When A/D converter is operating[Note 7]		9.5	19	mA
		8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		5.5	11	mA
				When A/D converter is operating[Note 7]		6.5	13	mA
			V_{DD} = 3.0 V + 10%[Notes 3, 6]	When A/D converter is stopped		3	6	mA
				When A/D converter is operating[Note 7]		4	8	mA
		5.00 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		2	4	mA
				When A/D converter is operating[Note 7]		3	6	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When A/D converter is stopped		0.4	1.5	mA
				When A/D converter is operating[Note 7]		1.4	4.2	mA
	I_{DD2}	12.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		2	4	mA
				When peripheral functions are operating			10	mA
		8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		1.1	2.2	mA
				When peripheral functions are operating			4.7	mA
			V_{DD} = 3.0 V + 10%[Notes 3, 6]	When peripheral functions are stopped		0.5	1	mA
				When peripheral functions are operating			4	mA
		5.00 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ±10%[Note 3]	When peripheral functions are stopped		0.35	0.7	mA
				When peripheral functions are operating			1.7	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When peripheral functions are stopped		0.15	0.4	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 5]		V_{DD} = 5.0 V ±10%		40	80	μA
				V_{DD} = 3.0 V ±10%		20	40	μA
				V_{DD} = 2.0 V ±10%		10	20	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 5]		V_{DD} = 5.0 V ±10%		30	60	μA
				V_{DD} = 3.0 V ±10%		6	18	μA
				V_{DD} = 2.0 V ±10%		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ±10%		0.1	30	μA
				V_{DD} = 3.0 V ±10%		0.05	10	μA
				V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}) (except the current through pull-up resistors of ports).

2. I_{DD1} includes the peripheral operation current.

3. When the processor clock control register (PCC) is set to 00H.

4. When PCC is set to 02H.

5. When main system clock operation is stopped.

6. The values show the specifications when V_{DD} = 3.0 to 3.3 V. The value in the TYP. column show the specifications when V_{DD} = 3.0 V.

7. Includes the current through the AV_{DD} pin.

AC Characteristics

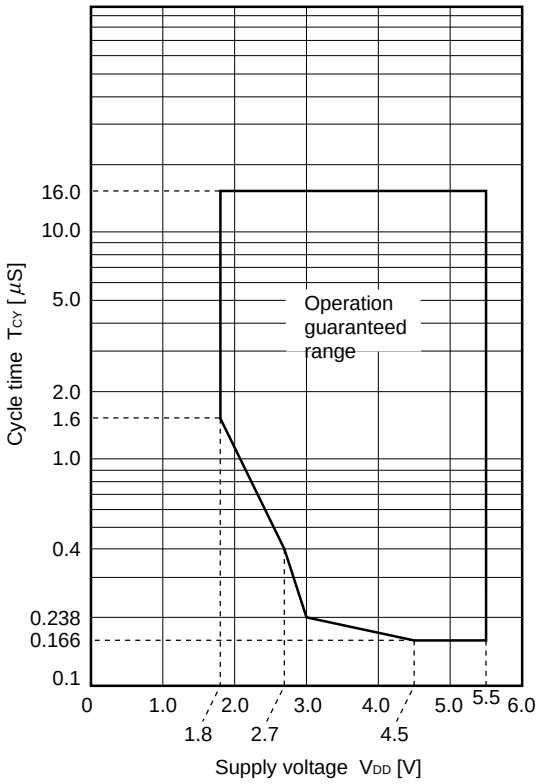
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.5 V ≤ V_{DD} ≤ 5.5 V	0.166		16	μs
			3.0 V ≤ V_{DD} ≤ 4.5 V	0.238		16	μs
			2.7 V ≤ V_{DD} ≤ 3.0 V	0.4		16	μs
			1.8 V ≤ V_{DD} ≤ 2.7 V	1.6		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	3.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 3.0 V		$2/f_{sam}$+0.2 Note 2			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note 2			μs
TI50, TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 5.5 V		0		4	MHz
		1.8 V ≤ V_{DD} < 2.7 V		0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		1.8			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
			1.8 V ≤ V_{DD} < 2.7 V	2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 5.5 V		10			μs
		1.8 V ≤ V_{DD} < 2.7 V		20			μs

Notes 1. Value when the external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of fsam = f_X, f_X/4, f_X/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes fsam = f_X/8.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3t_{CY}		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			(2 + 2n)t_{CY} – 54	ns
	t_{ADD2}			(3 + 2n)t_{CY} – 60	ns
Address output time from $\overline{RD}$↓	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(2 + 2n)t_{CY} – 87	ns
	t_{RDD2}			(3 + 2n)t_{CY} – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5 + 2n)t_{CY} – 33		ns
	t_{RDL2}		(2.5 + 2n)t_{CY} – 33		ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5 + n)t_{CY} + 10	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		(1.5 + 2n)t_{CY} – 15		ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{ASTWR}		2t_{CY} – 15		ns
Delay time from $\overline{RD}$↑ to ASTB↑ at external fetch	t_{RDAST}		0.8t_{CY} – 15	1.2t_{CY}	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		0.8t_{CY} – 15	1.2t_{CY} + 30	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		0.8t_{CY} – 15	1.2t_{CY} + 30	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{WTRD}		0.8t_{CY}	2.5t_{CY} + 25	ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{WTWR}		0.8t_{CY}	2.5t_{CY} + 25	ns

Caution T_{CY} can only be used when the MIN. value is 0.238 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.0 V)

(2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	200	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 30		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		10		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 30		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address at external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Caution T_{CY} can only be used when the MIN. value is 0.4 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V)

(3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	400	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		20		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 60		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address at external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Caution T_{CY} can only be used when the MIN. value is 1.6 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK3n}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V		666			ns
		3.0 V ≤ V_{DD} < 4.5 V		954			ns
		2.7 V ≤ V_{DD} < 3.0 V		1600			ns
		1.8 V ≤ V_{DD} < 2.7 V		3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH1}, t_{KL1}	3.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 50			ns
		1.8 V ≤ V_{DD} < 3.0 V		t_{KCY1}/2 – 100			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK1}	3.0 V ≤ V_{DD} ≤ 5.5 V		100			ns
		2.7 V ≤ V_{DD} < 3.0 V		150			ns
		1.8 V ≤ V_{DD} < 2.7 V		300			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI1}	4.5 V ≤ V_{DD} ≤ 5.5 V		300			ns
		1.8 V ≤ V_{DD} < 4.5 V		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO1}	C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V			200	ns
			1.8 V ≤ V_{DD} < 4.5 V			300	ns

Note C is the load capacitance of the $\overline{SCK3n}$ and SO3n output lines.

(b) 3-wire serial I/O mode ($\overline{SCK3n}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		666			ns
		3.0 V ≤ V_{DD} < 4.5 V		800			ns
		2.7 V ≤ V_{DD} < 3.0 V		1600			ns
		1.8 V ≤ V_{DD} < 2.7 V		3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		333			ns
		3.0 V ≤ V_{DD} < 4.5 V		400			ns
		2.7 V ≤ V_{DD} < 3.0 V		800			ns
		1.8 V ≤ V_{DD} < 2.7 V		1600			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK2}			100			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI2}	4.5 V ≤ V_{DD} ≤ 5.5 V		300			ns
		1.8 V ≤ V_{DD} < 4.5 V		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO2}	C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V			200	ns
			1.8 V ≤ V_{DD} < 4.5 V			300	ns

Note C is the load capacitance of the SO3n output line.

Remark n = 0, 1

(c) UART mode (dedicated baud-rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			187500	bps
		3.0 V ≤ V_{DD} < 4.5 V			131031	bps
		2.7 V ≤ V_{DD} < 3.0 V			78125	bps
		1.8 V ≤ V_{DD} < 2.7 V			39063	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
		1.8 V ≤ V_{DD} < 2.7 V			9766	bps

(e) UART mode (infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		131031	bps
Allowable bit rate error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/fbr[Note]	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

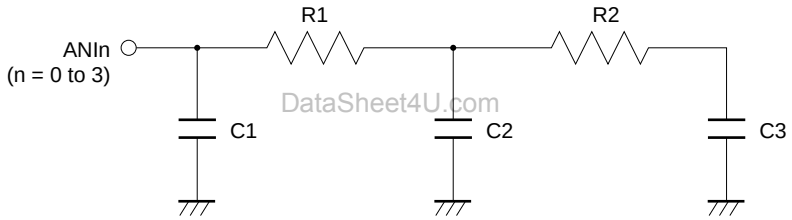
A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	12		96	μs
		4.0 V ≤ AV_{DD} < 4.5 V	14		96	μs
		2.7 V ≤ AV_{DD} < 4.0 V	17		96	μs
		1.8 V ≤ AV_{DD} < 2.7 V	28		96	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D converter not operating	20	40		kΩ

Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio (%FSR) to the full-scale value.

Remark The impedance of the analog input pins is shown below.

[Equivalent circuit]



[Parameter value]

(TYP.)

AV_{DD}	R1	R2	C1	C2	C3
2.7 V	12 kΩ	8.0 kΩ	3.0 pF	3.0 pF	2.0 pF
4.5 V	4 kΩ	2.7 kΩ	3.0 pF	1.4 pF	2.0 pF

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	Subsystem clock stop (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

12.2 μPD780021AY, 780022AY, 780023AY, 780024AY, and Conventional Products of μPD780021A, 780022A, 780023A,780024A

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +6.5	V
	AV_{DD}				–0.3 to V_{DD} + 0.3[Note]	V
	AV_{REF}				–0.3 to V_{DD} + 0.3[Note]	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, $\overline{RESET}$			–0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P30 to P33	N-ch open-drain	Without pull-up resistor	–0.3 to + 6.5	V
				With pull-up resistor	–0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}	P10 to P17		Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3[Note] and –0.3 to V_{DD} + 0.3[Note]	V
Output current, high	I_{OH}	Per pin			–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75			–15	mA
		Total for P20 to P25, P30 to P36			–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75			20	mA
		Per pin for P30 to P33, P50 to P57			30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75			50	mA
		Total for P20 to P25			20	mA
		Total for P30 to P36			100	mA
		Total for P50 to P57			100	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note 6.5 V or below

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

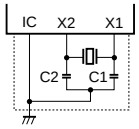
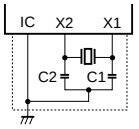
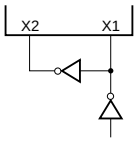
Remark Unless otherwise specified, the characteristic of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75			15	pF
			P30 to P33			20	pF

Remark Unless otherwise specified, the characteristic of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		Oscillation stabilization timeNote 2	4.0 V ≤ V_{DD} ≤ 5.5 V			10	ms
			1.8 V ≤ V_{DD} < 4.0 V			30	
External clock		X1 input frequency (f_X)Note 1	4.0 V ≤ V_{DD} ≤ 5.5 V	1.0		8.38	MHz
			1.8 V ≤ V_{DD} < 4.0 V	1.0		5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	4.0 V ≤ V_{DD} ≤ 5.5 V	50		500	ns
			1.8 V ≤ V_{DD} < 4.0 V	85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

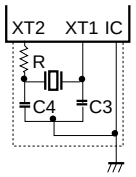
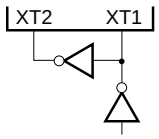
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	4.0 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.8 V ≤ V_{DD} < 4.0 V			10	
External clock		XT1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		12		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Recommended Oscillator Constant

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSBFB1M00J58	1.00	100	100	2.2	1.8	5.5
	CSBLA1M00J58	1.00	100	100	2.2	1.8	5.5
	CSTCC2M00G56	2.00	On-chip	On-chip	0	1.8	5.5
	CSTLS2M00G56	2.00	On-chip	On-chip	0	1.8	5.5
	CSTCC3M58G53	3.58	On-chip	On-chip	0	1.8	5.5
	CSTLS3M58G53	3.58	On-chip	On-chip	0	1.8	5.5
	CSTCR4M00G53	4.00	On-chip	On-chip	0	1.8	5.5
	CSTLS4M00G53	4.00	On-chip	On-chip	0	1.8	5.5
	CSTCR4M19G53	4.19	On-chip	On-chip	0	1.8	5.5
	CSTLS4M19G53	4.19	On-chip	On-chip	0	1.8	5.5
	CSTCR4M91G53	4.91	On-chip	On-chip	0	1.8	5.5
	CSTLS4M91G53	4.91	On-chip	On-chip	0	1.8	5.5
	CSTCR5M00G53	5.00	On-chip	On-chip	0	1.8	5.5
	CSTLS5M00G53	5.00	On-chip	On-chip	0	1.8	5.5
	CSTCE8M00G52	8.00	On-chip	On-chip	0	3.0	5.5
	CSTLS8M00G53	8.00	On-chip	On-chip	0	3.0	5.5
	CSTCE8M38G52	8.38	On-chip	On-chip	0	3.0	5.5
	CSTLS8M38G53	8.38	On-chip	On-chip	0	3.0	5.5
	CSTCE10M0G52	10.00	On-chip	On-chip	0	4.5	5.5
	CSTLS10M0G53	10.00	On-chip	On-chip	0	4.5	5.5
TDK	CCR3.58MC3	3.58	On-chip	On-chip	0	1.8	5.5
	CCR4.19MC3	4.19	On-chip	On-chip	0	1.8	5.5
	CCR5.0MC3	5.00	On-chip	On-chip	0	1.8	5.5
	CCR8.0MC5	8.00	On-chip	On-chip	0	2.0	5.5
	CCR8.38MC5	8.38	On-chip	On-chip	0	2.0	5.5

Caution The oscillator constant is a reference value based on evaluation in specific environments by the resonator manufacturer. If the oscillator characteristics need to be optimized in the actual application, request the resonator manufacturer for evaluation on the implementation circuit. Note that the oscillation voltage and oscillation frequency merely indicate the characteristics of the oscillator. Use the internal operation conditions of the μPD780024A, 780024AY Subseries within the specifications of the DC and AC characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		5.5	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8V_{DD}		5.5	V
	V_{IH4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.15V_{DD}	V
	V_{IL3}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.4	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL5}	XT1, XT2	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 4.0 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		1.8 V ≤ V_{DD} < 4.0 V, I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33Note 1			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33Note 1			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistance	R_1	V_{IN} = 0 V, P30, P31, P32Note 2, P33Note 2		15	30	90	kΩ
Software pull-up resistance	R_2	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

Notes 1. μPD780021A, 780022A, 780023A, 780024A: When pull-up resistors are not connected to P30 to P33 (specified by the mask option).

μPD780021AY, 780022AY, 780023AY, 780024AY: When pull-up resistors are not connected to P30 and P31 (specified by the mask option).

2. Only for the μPD780021A, 780022A, 780023A, and 780024A.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter is stopped		5.5	11	mA
				When A/D converter is operating[Note 6]		6.5	13	mA
		5.00 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter is stopped		2	4	mA
				When A/D converter is operating[Note 6]		3	6	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When A/D converter is stopped		0.4	1.5	mA
				When A/D converter is operating[Note 6]		1.4	4.2	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral functions are stopped		1.1	2.2	mA
				When peripheral functions are operating			4.7	mA
		5.00 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ±10%[Note 3]	When peripheral functions are stopped		0.35	0.7	mA
				When peripheral functions are operating			1.7	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When peripheral functions are stopped		0.15	0.4	mA
				When peripheral functions are operating			1.1	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 5]		V_{DD} = 5.0 V ±10%		40	80	μA
				V_{DD} = 3.0 V ±10%		20	40	μA
				V_{DD} = 2.0 V ±10%		10	20	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 5]		V_{DD} = 5.0 V ±10%		30	60	μA
				V_{DD} = 3.0 V ±10%		6	18	μA
				V_{DD} = 2.0 V ±10%		2	10	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ±10%		0.1	30	μA
				V_{DD} = 3.0 V ±10%		0.05	10	μA
				V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}) (except the current through pull-up resistors of ports).

2. I_{DD1} includes the peripheral operation current.

3. When the processor clock control register (PCC) is set to 00H.

4. When PCC is set to 02H.

5. When main system clock operation is stopped.

6. Includes the current through the AV_{DD} pin.

AC Characteristics

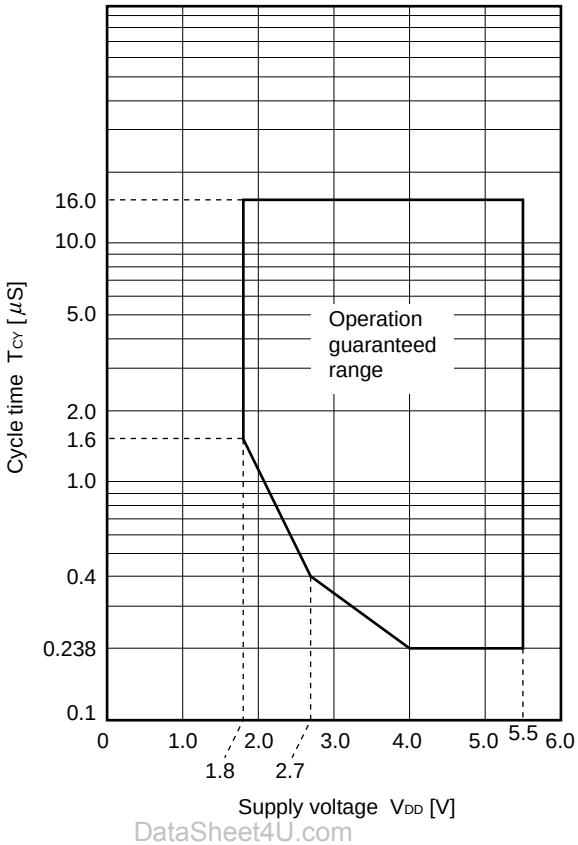
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.238		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
			1.8 V ≤ V_{DD} < 2.7 V	1.6		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	4.0 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}$+0.2 Note 2			μs
		1.8 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5 Note 2			μs
TI50, TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 5.5 V		0		4	MHz
		1.8 V ≤ V_{DD} < 2.7 V		0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}	2.7 V ≤ V_{DD} ≤ 5.5 V		100			ns
		1.8 V ≤ V_{DD} < 2.7 V		1.8			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3, P40 to P47	2.7 V ≤ V_{DD} ≤ 5.5 V	1			μs
			1.8 V ≤ V_{DD} < 2.7 V	2			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	2.7 V ≤ V_{DD} ≤ 5.5 V		10			μs
		1.8 V ≤ V_{DD} < 2.7 V		20			μs

Notes 1. Value when the external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of f_{sam} = f_X, f_X/4, f_X/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = f_X/8.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY}$ – 15		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Caution T_{CY} can only be used when the MIN. value is 0.238 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.0 V)

(2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3t_{CY}		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Input time from address to data	t_{ADD1}			(2 + 2n)t_{CY} – 108	ns
	t_{ADD2}			(3 + 2n)t_{CY} – 120	ns
Output time from $\overline{RD}$↓ to address	t_{RDAD}		0	200	ns
Input time from $\overline{RD}$↓ to data	t_{RDD1}			(2 + 2n)t_{CY} – 148	ns
	t_{RDD2}			(3 + 2n)t_{CY} – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5 + 2n)t_{CY} – 40		ns
	t_{RDL2}		(2.5 + 2n)t_{CY} – 40		ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 60	ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5 + 2n)t_{CY} + 10	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		(1.5 + 2n)t_{CY} – 30		ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{ASTRD}		10		ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{ASTWR}		2t_{CY} – 30		ns
Delay time from $\overline{RD}$↑ to ASTB↑ at external fetch	t_{RDAST}		0.8t_{CY} – 30	1.2t_{CY}	ns
Hold time from $\overline{RD}$↑ to address at external fetch	t_{RDADH}		0.8t_{CY} – 30	1.2t_{CY} + 60	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		20	120	ns
Hold time from $\overline{WR}$↑ to address	t_{WRADH}		0.8t_{CY} – 30	1.2t_{CY} + 60	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{WTRD}		0.5t_{CY}	2.5t_{CY} + 50	ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{WTWR}		0.5t_{CY}	2.5t_{CY} + 50	ns

Caution T_{CY} can only be used when the MIN. value is 0.4 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 2.7 V)

(3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3t_{CY}		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Input time from address to data	t_{ADD1}			(2 + 2n)t_{CY} – 233	ns
	t_{ADD2}			(3 + 2n)t_{CY} – 240	ns
Output time from $\overline{RD}$↓ to address	t_{RDAD}		0	400	ns
Input time from $\overline{RD}$↓ to data	t_{RDD1}			(2 + 2n)t_{CY} – 325	ns
	t_{RDD2}			(3 + 2n)t_{CY} – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5 + 2n)t_{CY} – 92		ns
	t_{RDL2}		(2.5 + 2n)t_{CY} – 92		ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 132	ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5 + 2n)t_{CY} + 10	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		(1.5 + 2n)t_{CY} – 60		ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{ASTRD}		20		ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{ASTWR}		2t_{CY} – 60		ns
Delay time from $\overline{RD}$↑ to ASTB↑ at external fetch	t_{RDAST}		0.8t_{CY} – 60	1.2t_{CY}	ns
Hold time from $\overline{RD}$↑ to address at external fetch	t_{RDADH}		0.8t_{CY} – 60	1.2t_{CY} + 120	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		40	240	ns
Hold time from $\overline{WR}$↑ to address	t_{WRADH}		0.8t_{CY} – 60	1.2t_{CY} + 120	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{WTRD}		0.5t_{CY}	2.5t_{CY} + 100	ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{WTWR}		0.5t_{CY}	2.5t_{CY} + 100	ns

Caution T_{CY} can only be used when the MIN. value is 1.6 μs.

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK3n}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 – 50			ns
		1.8 V ≤ V_{DD} < 4.0 V	t_{KCY1}/2 – 100			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	150			ns
		1.8 V ≤ V_{DD} < 2.7 V	300			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI1}		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK3n}$ and SO3n output lines.

(b) 3-wire serial I/O mode ($\overline{SCK3n}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
SI3n setup time (to $\overline{SCK3n}$↑)	t_{SIK2}		100			ns
SI3n hold time (from $\overline{SCK3n}$↑)	t_{KSI2}		400			ns
Delay time from $\overline{SCK3n}$↓ to SO3n output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO3n output line.

Remark Conventional products of μPD780021A, 780022A, 780023A, 780024A: n = 0 or 1
μPD780021AY, 780022AY, 780023AY, 780024AY: n = 0

(c) UART mode (dedicated baud-rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			131031	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps
		1.8 V ≤ V_{DD} < 2.7 V			39063	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
ASCK0 high-/low-level width	t_{KH3}, t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.0 V			19531	bps
		1.8 V ≤ V_{DD} < 2.7 V			9766	bps

(e) UART mode (infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		131031	bps
Allowable bit rate error		4.0 V ≤ V_{DD} ≤ 5.5 V		±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2	0.24/fbr[Note]	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X		μs

Note fbr: Specified baud rate

(f) I²C bus mode (μPD780021AY, 780022AY, 780023AY, 780024AY only)

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS-compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns
Capacitive load per bus line		Cb	—	400	—	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only the maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I²C bus is available in a standard mode I²C bus system. At this time, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I²C bus specification).

5. Cb: Total capacitance per bus line (unit: pF)

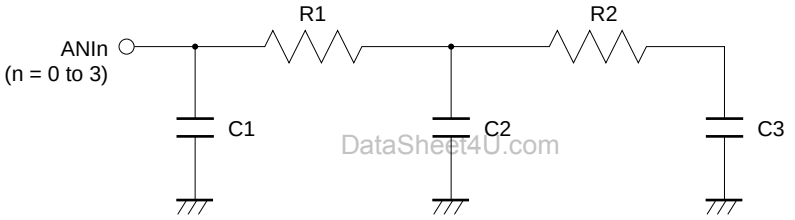
A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{DD} ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV_{DD} < 4.0 V	19		96	μs
		1.8 V ≤ AV_{DD} < 2.7 V	28		96	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D converter not operating	20	40		kΩ

Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio (%FSR) to the full-scale value.

Remark The impedance of the analog input pins is shown below.

[Equivalent circuit]



[Parameter value]

(TYP.)

AV_{DD}	R1	R2	C1	C2	C3
2.7 V	12 kΩ	8.0 kΩ	3.0 pF	3.0 pF	2.0 pF
4.5 V	4 kΩ	2.7 kΩ	3.0 pF	1.4 pF	2.0 pF

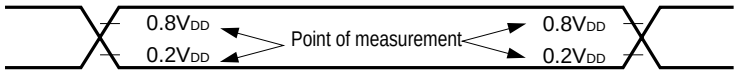
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	Subsystem clock stop (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization time	t_{WAIT}	Release by $\overline{RESET}$		2^{17}/fx		s
		Release by interrupt request		**Note**		s

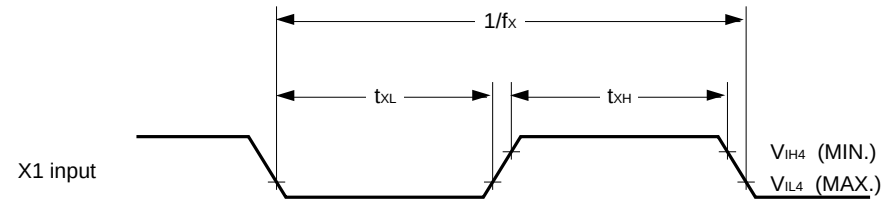
Note Selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

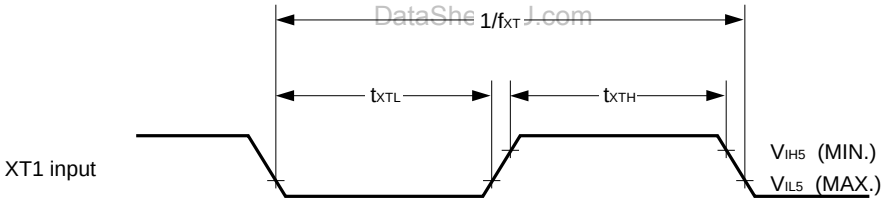
12.3 Timing Chart

AC Timing Test Points (excluding X1, XT1 inputs)

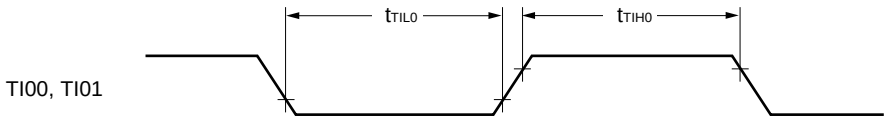


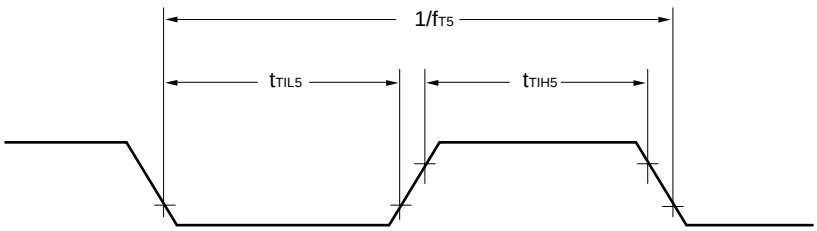
Clock Timing



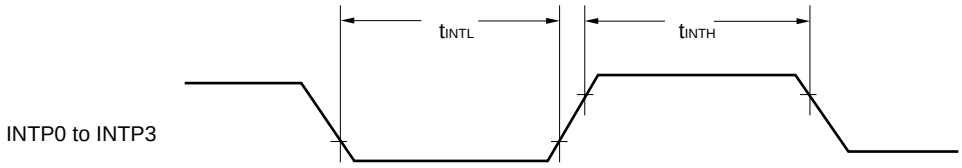


TI Timing

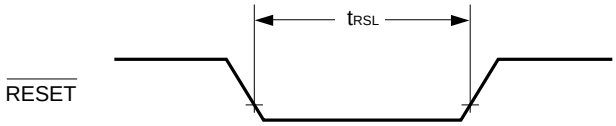




Interrupt Request Input Timing

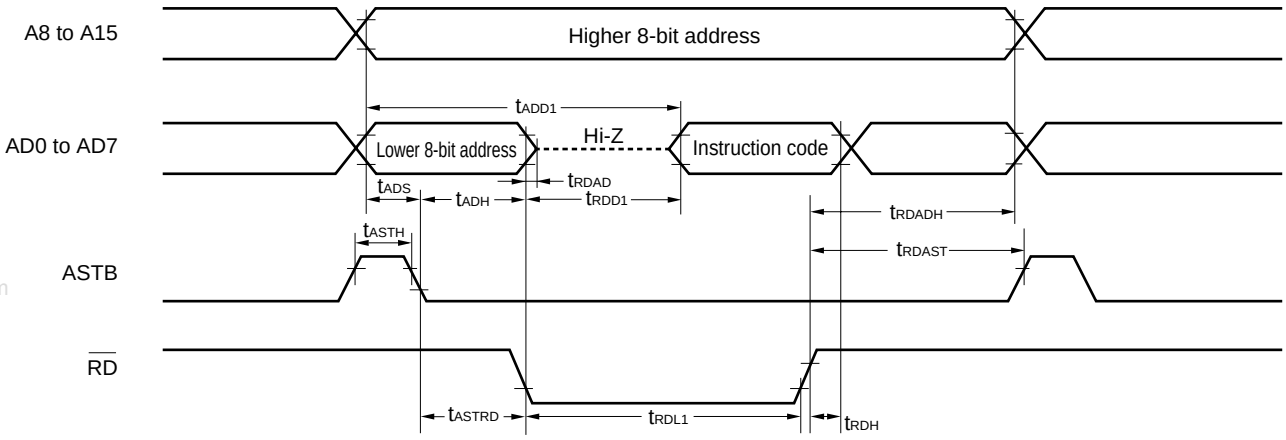


$\overline{\text{RESET}}$ Input Timing

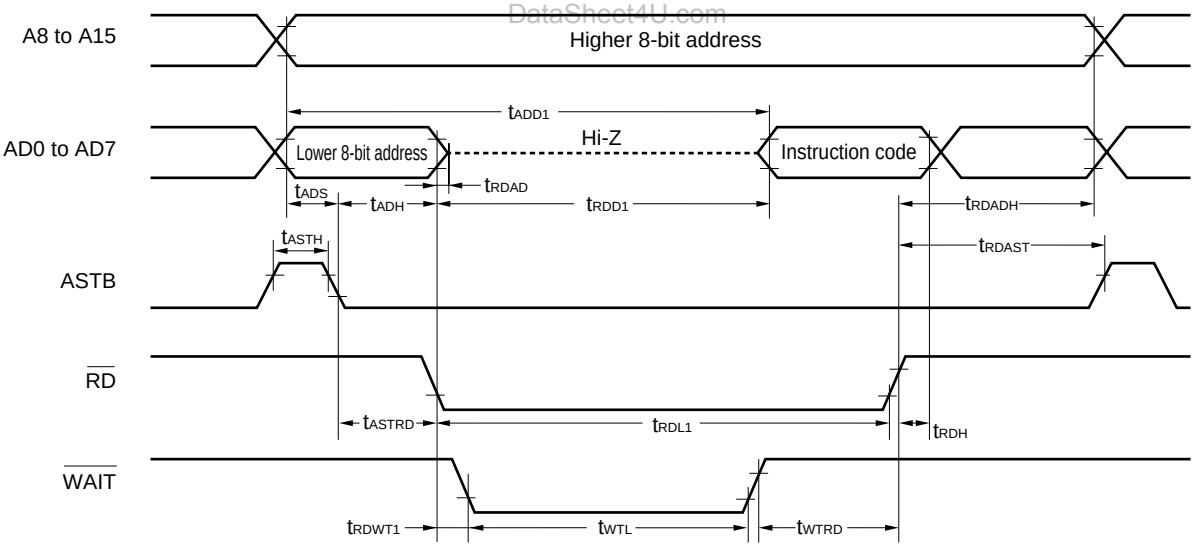


Read/Write Operation

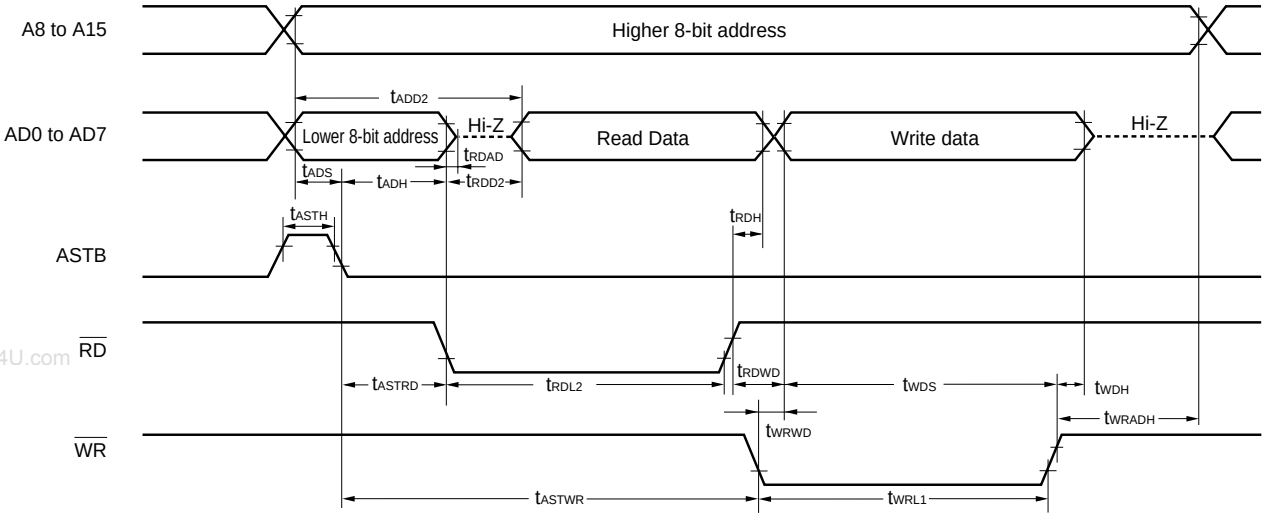
External fetch (no wait):



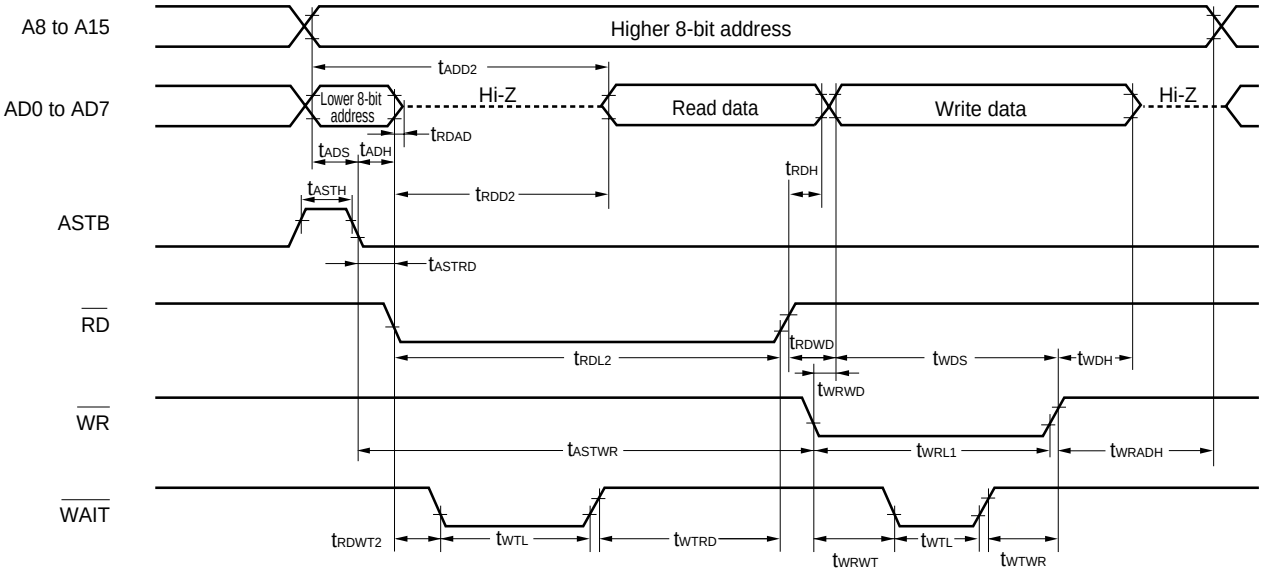
External fetch (wait insertion):



External data access (no wait):

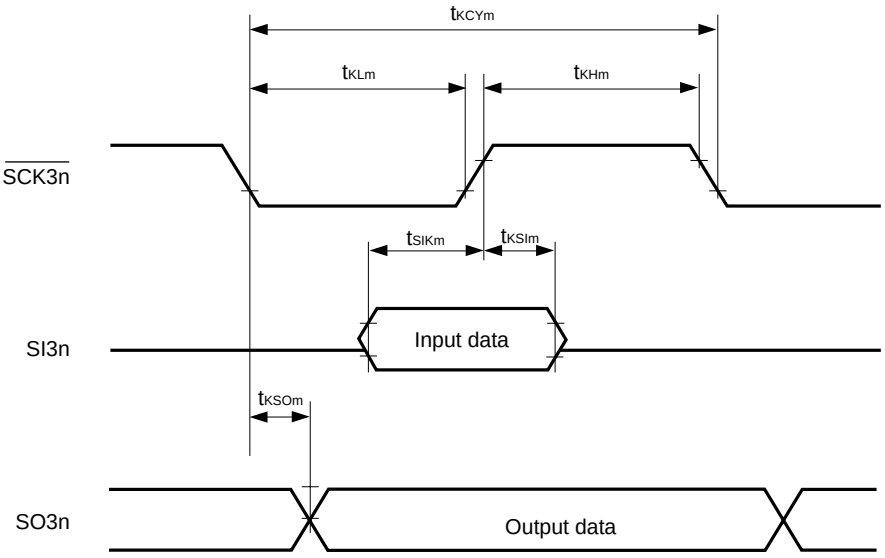


External data access (wait insertion):



Serial Transfer Timing

3-wire serial I/O mode:

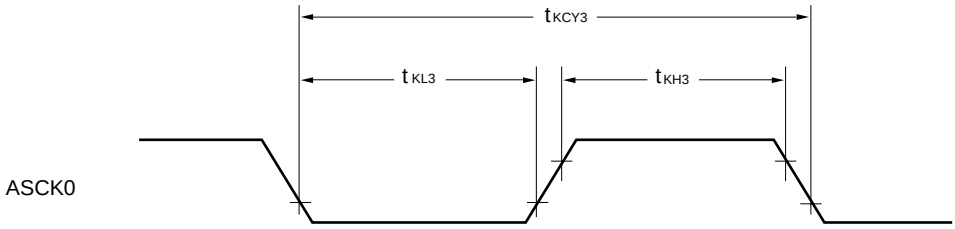


Remarks 1. m = 1, 2

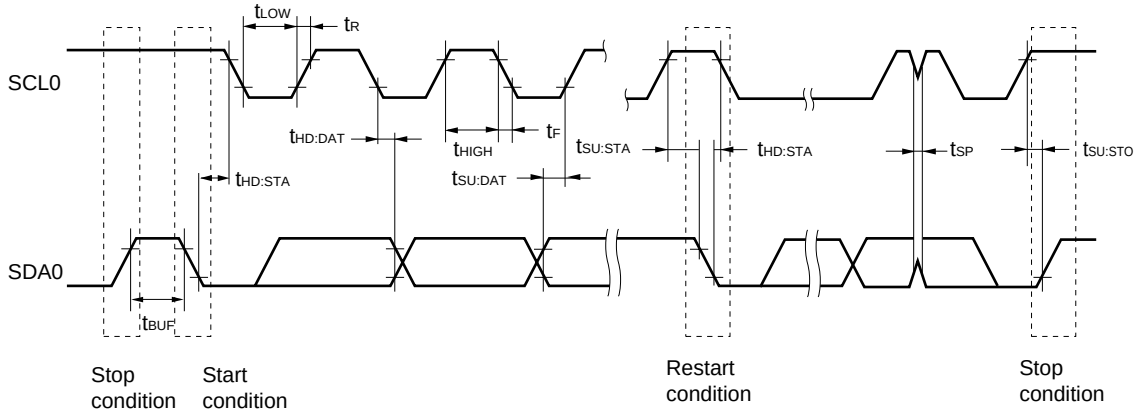
2. μPD780021A, 780022A, 780023A, 780024A: n = 0, 1

μPD780021AY, 780022AY, 780023AY, 780024AY: n = 0

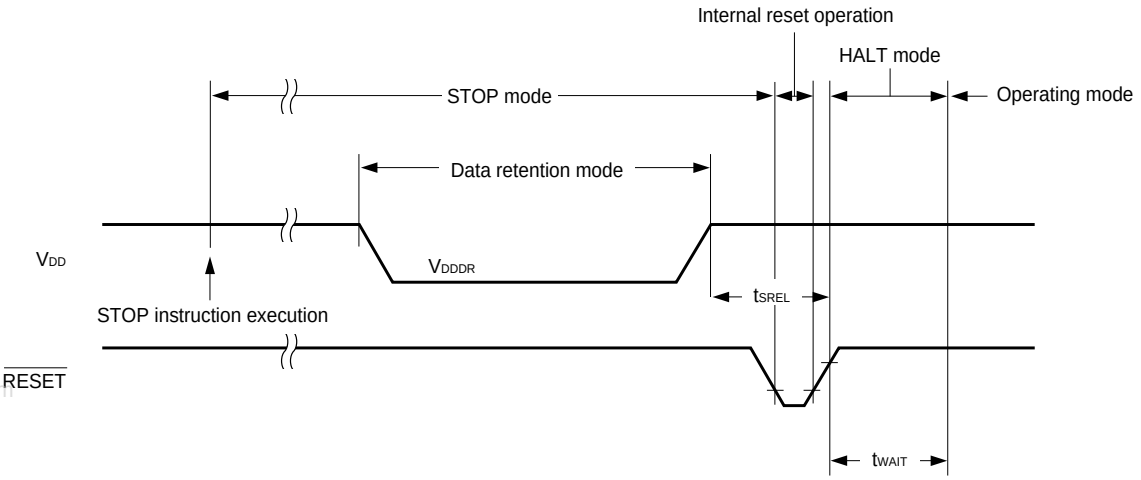
UART mode (external clock input):



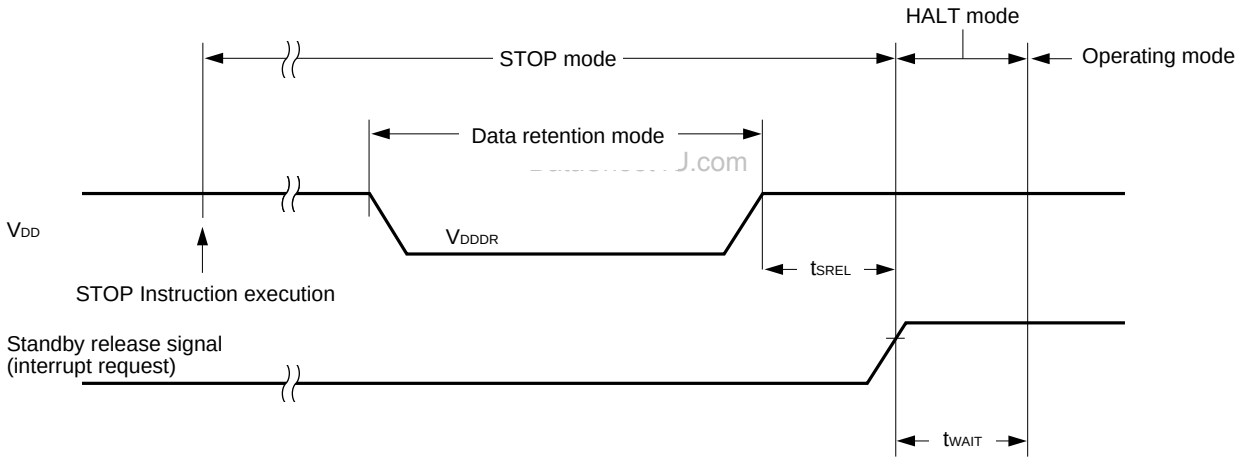
I²C bus mode (μPD780021AY, 780022AY, 780023AY, 780024AY only):



Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)

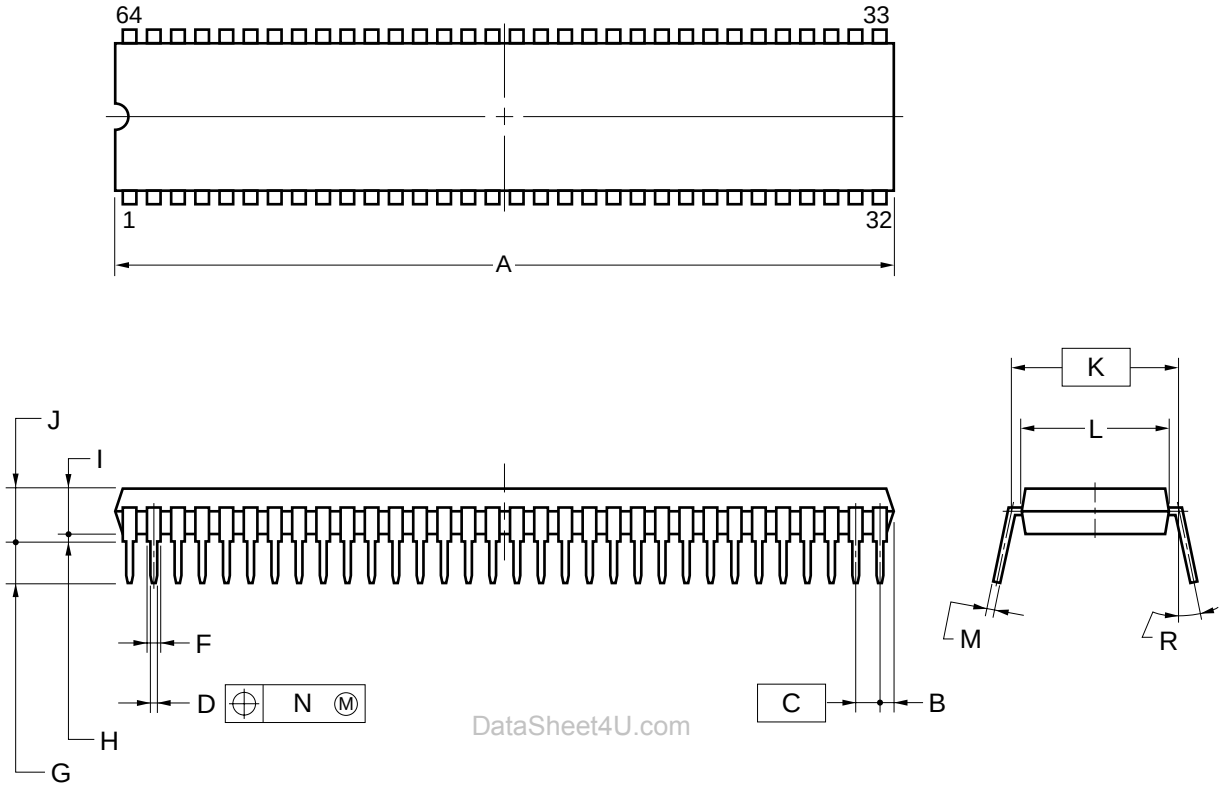


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



13. PACKAGE DRAWINGS

64-PIN PLASTIC SDIP (19.05mm(750))



NOTES

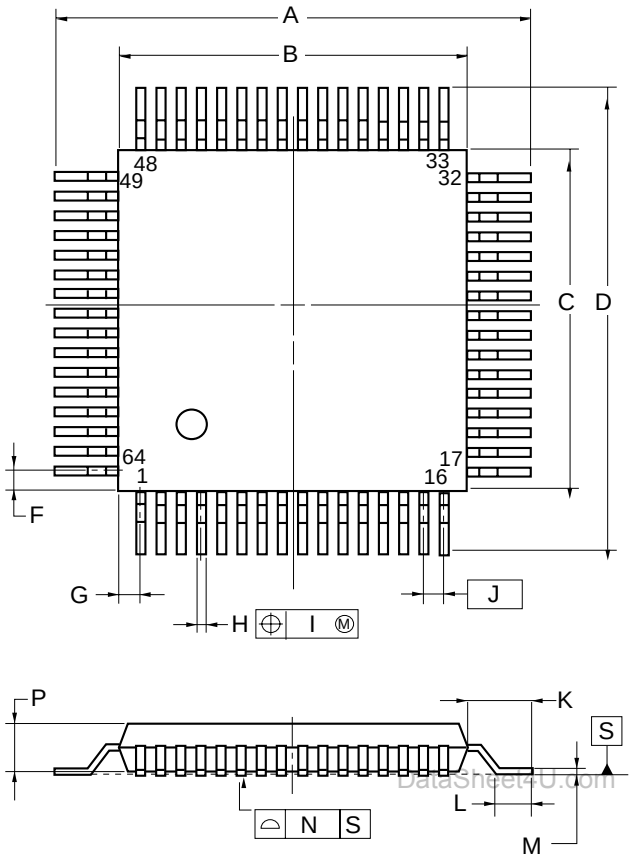
1. Each lead centerline is located within 0.17 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	$58.0^{+0.68}_{-0.20}$
B	1.78 MAX.
C	1.778 (T.P.)
D	0.50±0.10
F	0.9 MIN.
G	3.2±0.3
H	0.51 MIN.
I	$4.05^{+0.26}_{-0.20}$
J	5.08 MAX.
K	19.05 (T.P.)
L	17.0±0.2
M	$0.25^{+0.10}_{-0.05}$
N	0.17
R	0 ~ 15°

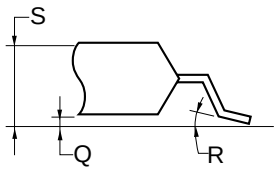
P64C-70-750A,C-4

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

64-PIN PLASTIC QFP (14x14)



detail of lead end



NOTE

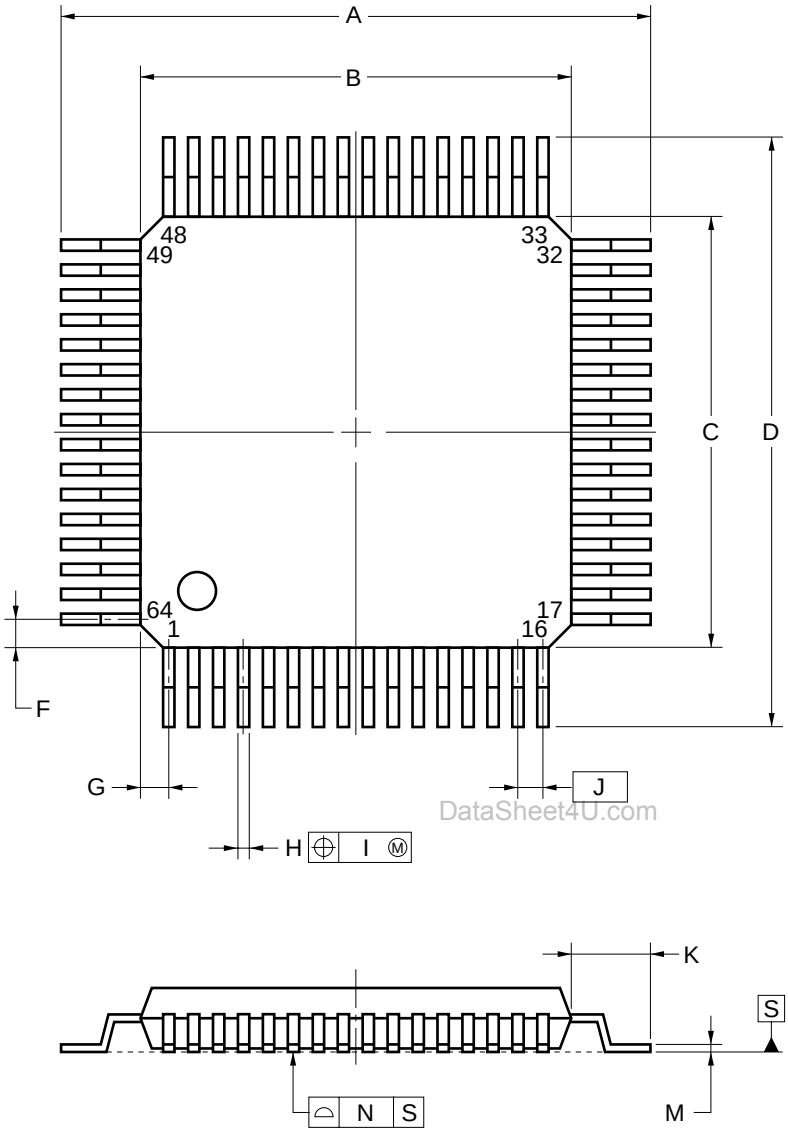
Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

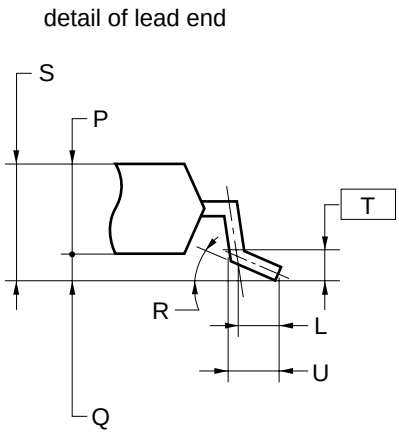
ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°± 5°
S	2.85 MAX.

P64GC-80-AB8-5

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

★ 64-PIN PLASTIC LQFP (14x14)





NOTE

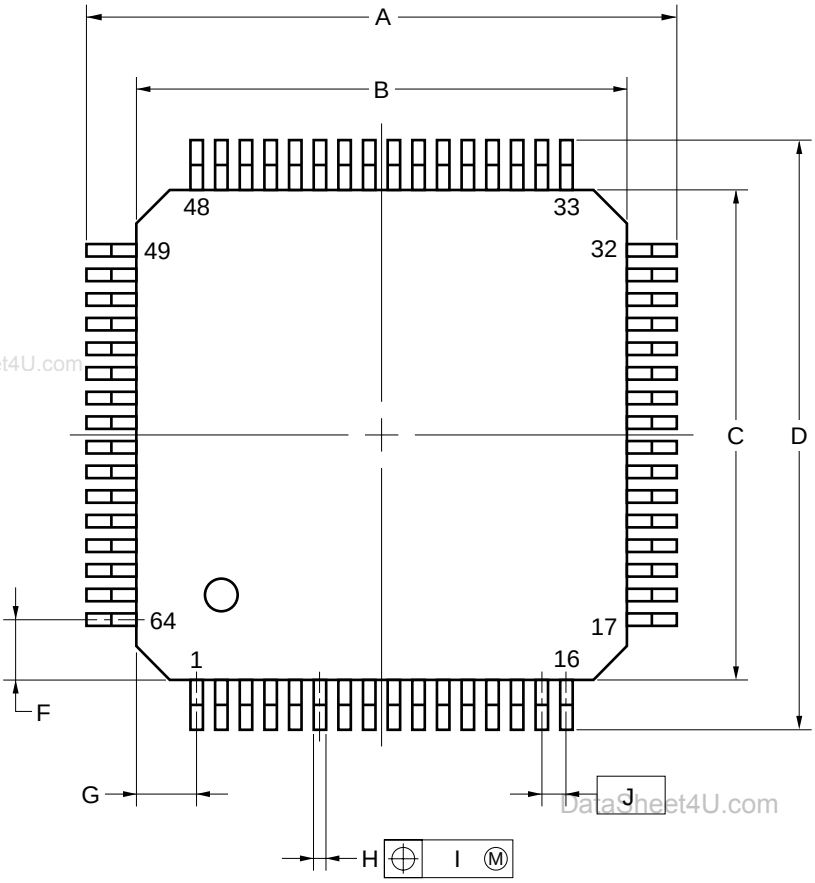
Each lead centerline is located within 0.20 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.2±0.2
B	14.0±0.2
C	14.0±0.2
D	17.2±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.20
J	0.8 (T.P.)
K	1.6±0.2
L	0.8
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.1
Q	0.127±0.075
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.
T	0.25
U	0.886±0.15

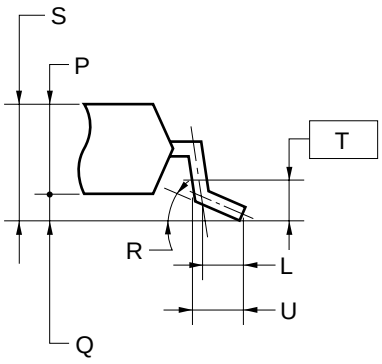
P64GC-80-8BS

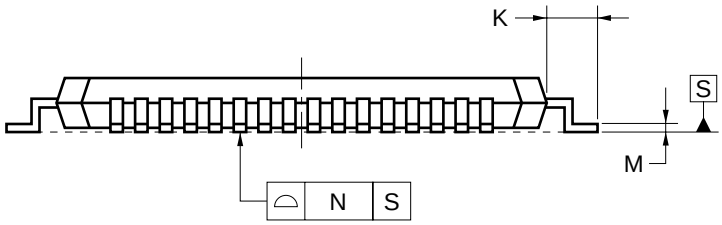
Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

64-PIN PLASTIC TQFP (12x12)



detail of lead end





NOTE

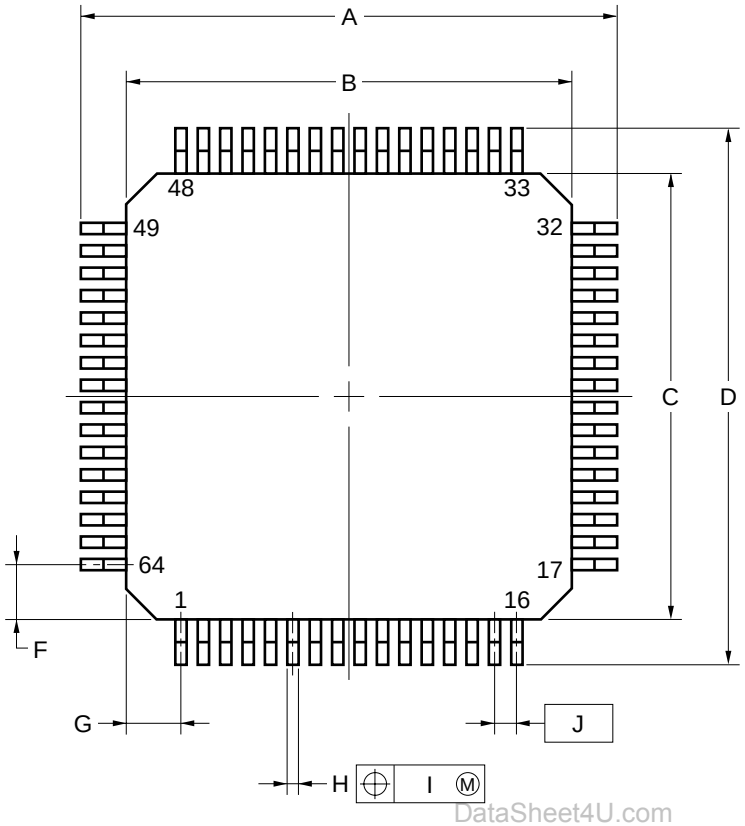
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

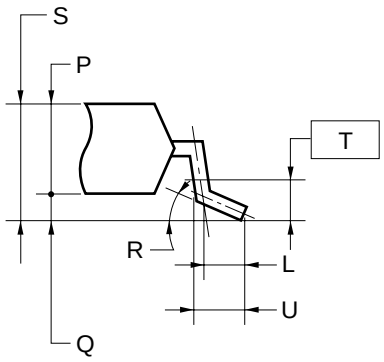
P64GK-65-9ET-3

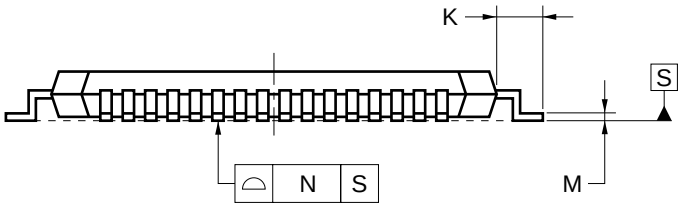
Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

★ 64-PIN PLASTIC LQFP (10x10)



detail of lead end



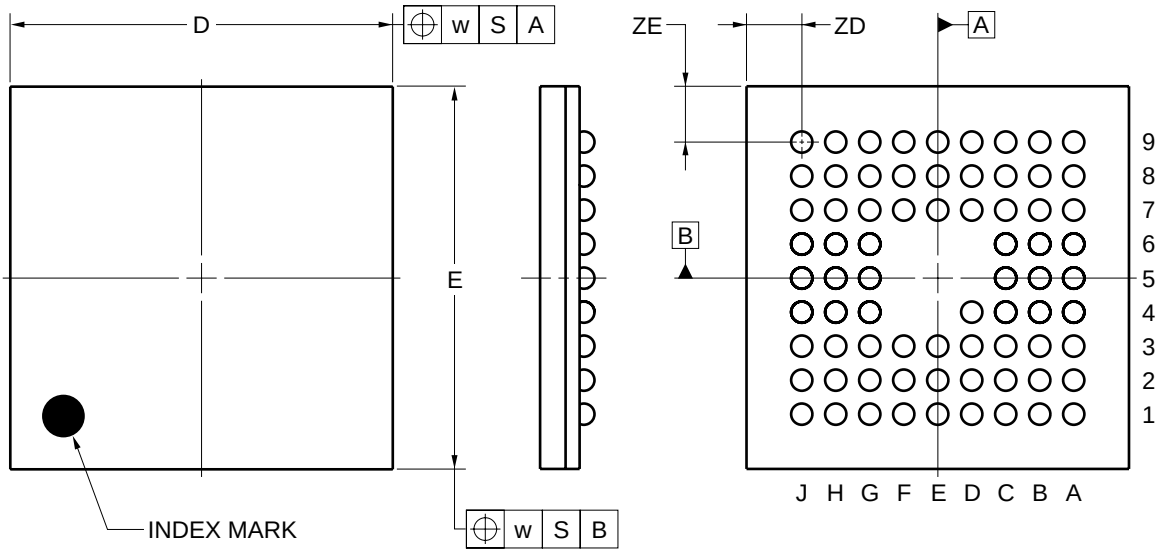


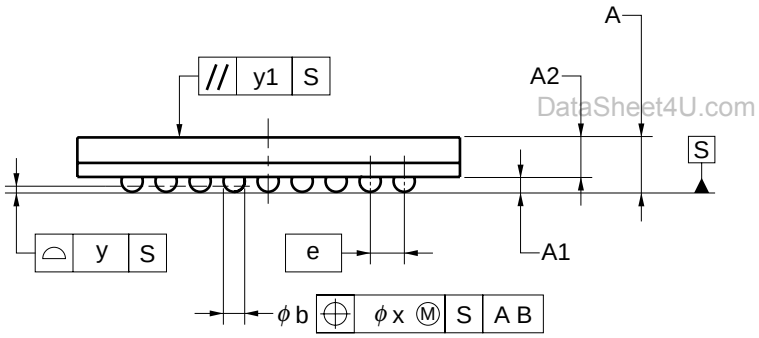
ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.10
T	0.25
U	0.6±0.15

S64GB-50-8EU-1

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

★ 73-PIN PLASTIC FBGA (9x9)





(UNIT:mm)

ITEM	DIMENSIONS
D	9.00±0.10
E	9.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.30
ZE	1.30

P73F1-80-CN3

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

14. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions (1/3)

(1) μPD780021AGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780022AGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780023AGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780024AGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780021AYGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780022AYGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780023AYGC-xxx-AB8: 64-pin plastic QFP (14 x 14)
μPD780024AYGC-xxx-AB8: 64-pin plastic QFP (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

★ **(2) μPD780021AGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)**
μPD780022AGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780023AGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780024AGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780021AYGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780022AYGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780023AYGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)
μPD780024AYGC-xxx-8BS: 64-pin plastic LQFP (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/3)

(3) μPD780021AGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780022AGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780023AGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780024AGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780021AYGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780022AYGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780023AYGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)
μPD780024AYGK-xxx-9ET: 64-pin plastic TQFP (12 x 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65%RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (3/3)

★ **(4) μPD780021AGB-×××-8EU: 64-pin plastic LQFP (10 x 10)**
μPD780022AGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780023AGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780024AGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780021AYGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780022AYGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780023AYGB-×××-8EU: 64-pin plastic LQFP (10 x 10)
μPD780024AYGB-×××-8EU: 64-pin plastic LQFP (10 x 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

★ **(5) μPD780021AF1-×××-CN3: 73-pin plastic FBGA (9 x 9)**
μPD780022AF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780023AF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780024AF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780021AYF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780022AYF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780023AYF1-×××-CN3: 73-pin plastic FBGA (9 x 9)
μPD780024AYF1-×××-CN3: 73-pin plastic FBGA (9 x 9)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR60-203-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-203-3

Note After opening the dry pack, store it at 25°C or less and 65%RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

Table 14-2. Insertion Type Soldering Conditions

μPD780021ACW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780022ACW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780023ACW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780024ACW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780021AYCW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780022AYCW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780023AYCW-xxx: 64-pin plastic SDIP (19.05 mm (750))
μPD780024AYCW-xxx: 64-pin plastic SDIP (19.05 mm (750))

Soldering Method	Soldering Conditions
Wave soldering (only for pins)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780024A, 780024AY Subseries.

Also refer to **(6) Cautions on Using Development Tools.**

(1) Software Package

SP78K0	CD-ROM in which various software tools for 78K/0 development are integrated in one package

(2) Language Processing Software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780024	Device file for μPD780024A, 780024AY Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

★ (3) Flash Memory Writing Tools

Flashpro III (FL-PR3, PG-FP3) Flashpro IV (FL-PR4, PG-FP4)	Flash programmer dedicated to microcontrollers with on-chip flash memory
FA-64CW FA-64GC FA-64GC-8BS-A FA-64GK-9ET FA-64GB-8EU FA-73F1-CN3-A	Adapter for flash memory writing used connected to the Flashpro III/Flashpro IV. • FA-64CW: 64-pin plastic SDIP (CW type) • FA-64GC: 64-pin plastic QFP (GC-AB8 type) • FA-64GC-8BS-A: 64-pin plastic LQFP (GC-8BS type) • FA-64GK-9ET: 64-pin plastic TQFP (GK-9ET type) • FA-64GB-8EU: 64-pin plastic LQFP (GB-8EU type) • FA-73F1-CN3-A: 73-pin plastic FBGA (F1-CN3 type)

(4) Debugging Tools

★ • **When using in-circuit emulator IE-78K0-NS or IE-78K0-NS-A**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-78K0-NS-PA	Performance board to enhance and expand the functions of IE-78K0-NS
IE-78K0-NS-A	Combination of IE-78K-NS and IE-78K0-NS-PA
IE-70000-MC-PS-B	Power supply unit for IE-78K0-N and IE-78K0-NS-A
IE-70000-98-IF-C	Adapter required when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter required when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using PC in which PCI bus is incorporated as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780024A, 780024AY Subseries
NP-64CW NP-H64CW	Emulation probe for 64-pin plastic SDIP (CW type)
NP-64GC NP-64GC-TQ NP-H64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type)
NP-64GK NP-H64GK-TQ	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
NP-H64GB-TQ	Emulation probe for 64-pin plastic LQFP (GB-8EU type)
NP-73F1-CN3**Note**	Emulation probe for 73-pin plastic FBGA (F1-CN3 type)
EV-9200GC-64	Conversion socket to connect the NP64GC and a target system board on which a 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type) can be mounted.
TGC-064SAP	Conversion adapter to connect the NP-64GC-TQ or NP-H64GC-TQ and a target system board on which a 64-pin plastic QFP (GC-AB8 type), 64-pin plastic LQFP (GC-8BS type) can be mounted
TGK-064SBW	Conversion adapter to connect the NP-64GK or NP-H64GK-TQ and a target system on which a 64-pin plastic TQFP (GK-9ET type) can be mounted
TGB-064SDP	Conversion socket to connect the NP-H64GB-TQ and a target system board on which a 64-pin plastic LQFP (GB-8EU type) can be mounted
CSICE73A0909N01, LSPACK73A0909N01, CSSOCKET73A0909N01	Conversion socket to connect the NP-73F1-CN3 and a target system board on which a 73-pin plastic FBGA (F1-CN3 type) can be mounted
ID78K0-NS	Integrated debugger for IE-78K0-NS and IE-78K0-NS-A
SM78K0	System simulator common to 78K/0 Series
DF780024	Device file for μPD780024A, 780024AY Subseries

Note The conversion socket (CSICE73A0909N01, LSPACK73A0909N01, or CSSOCKET73A0909N01) is supplied with the emulation probe (NP-73F1-CN3).

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Adapter required when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter required when using PC in which PCI bus is incorporated as host machine
IE-780034-NS-EM1	Emulation board to emulate μPD780024A, 780024AY Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic SDIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
EV-9200GC-64	Conversion socket to connect the EP-78240GC-R and a target system board on which a 64-pin plastic QFP (GC-AB8 type) can be mounted
TGK-064SBW	Conversion adapter to connect the EP-78012GK-R and a target system board on which a 64-pin plastic TQFP (GK-9ET type) can be mounted
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780024	Device file for μPD780024A, 780024AY Subseries

(5) Real-Time OS

RX78K0	Real-time OS for 78K/0 Series

★ **Caution The 64-pin plastic LQFP (GB-8EU type) and 73-pin plastic FBGA (F1-CN3 type) do not support the IE-78001-R-A.**

★ **(6) Cautions on Using Development Tools**

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780024.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and the DF780024.
- FL-PR3, FL-PR4, FA-64CW, FA-64GC, FA-64GC-8BS-A, FA-64GK-9ET, FA-64GB-8EU, FA-73F1-CN3-A, NP-64CW, NP-H64CW, NP-64GC, NP-64GC-TQ, NP-H64GC-TQ, NP-64GK, NP-H64GK-TQ, NP-H64GB-TQ, and NP-73F1-CN3 are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).
- TGC-064SAP, TGK-064SBW, TGB-064SDP, CSICE73A0909N01, LSPACK73A0909N01, and CSSOCKET73A0909N01 are products made by TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (+81-3-3820-7112)
  Osaka Electronic Division (+81-6-6244-6672)
- For third-party development tools, see the **Single-chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine / [OS] / Software	PC PC-9800 series [Japanese Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√ **Note**	√
CC78K0	√ **Note**	√
ID78K0-NS	√	–
ID78K0	√	–
SM78K0	√	–
RX78K0	√ **Note**	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual	U14046E
μPD780021A, 780022A, 780023A, 780024A, 780021AY, 780022AY, 780023AY, 780024AY Data Sheet	This document
μPD780021A(A), 780022A(A), 780023A(A), 780024A(A), 780021AY(A), 780022AY(A), 780023AY(A), 780024AY(A) Data Sheet	U15131E
μPD78F0034A, 78F0034AY Data Sheet	U14040E
★ μPD78F0034B, 78F0034BY, 78F0034B(A), 78F0034BY(A) Data Sheet	To be prepared
78K/0 Series Instructions User's Manual	U12326E

★ Documents Related to Development Software Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
SM78K Series System Simulator Ver. 2.30 or Later	Operation (Windows Based)	U15373E
	External Part User Open Interface Specifications	U15802E
ID78K Series Integrated Debugger Ver. 2.30 or Later	Operation (Windows Based)	U15185E
RX78K0 Real-time OS	Fundamentals	U11537E
	Installation	U11536E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

Documents Related to Development Hardware Tools (User's Manuals)

Document Name	Document No.
IE-78K0-NS In-Circuit Emulator	U13731E
★ IE-78K0-NS-A In-Circuit Emulator	U14889E
IE-780034-NS-EM1 Emulation Board	U14642E
★ IE-78001-R-A In-Circuit Emulator	U14142E
IE-78K0-R-EX1 In-Circuit Emulator	To be prepared

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

★ **Documents Related to Flash Memory Writing**

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E
PG-FP4 Flash Memory Programmer User's Manual	U15260E

Other Related Documents

Document Name	Document No.
★ SEMICONDUCTOR SELECTION GUIDE - Products & Packages -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 408-588-6130
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Hong Kong
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Fax: 2886-9022/9044

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Seoul, Korea
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