Silicon NPN Power Transistors 2SD850

DESCRIPTION

·With TO-3 package
·High voltage ,high speed

APPLICATIONS

·Line-operated horizontal deflection output applications

PINNING(see fig.2)

PIN DE	SCRIPTION
1	Base
2	Emitter
3	Collector

Fig.1 simplified o utline (TO-3) a nd s ymbol

Absolute maximum ratings(Ta=□)

SYMBOL P	ARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	700	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		3	A
I_{CM} C	ollector current-peak		5	A
P_T	Total power dissipation	T_C=90□ 25		W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-65~150	□

Silicon NPN Power Transistors 2SD850

CHARACTERISTICS

Tj=25□ u nless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	I_C=0.1A; I_B=0 600				V
$V_{(BR)EBO}$	Emitter-base breakdown votage	I_E=10mA; I_C=0	5			V
V_{CEsat} C	ollector-emitter saturation voltage	I_C=2.5 A;I_B=0.8A			4.0	V
V_{BEsat} B	ase-emitter saturation voltage	I_C=2.5 A;I_B=0.8A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=750V;I_E=0			50	μA
		V_{CB}=1500V;I_E=0			1.0 m	A
h_{FE-1}	DC current gain	I_C=0.5A ; V_{CE}=5V 8				
h_{FE-2}	DC current gain	I_C=2.5A ; V_{CE}=10V 4			15	
t_f	Fall time	I_C=2.5A;I_{Bend}=0.8A;L_B=5μH			1.0	μs
t_s	Storage time		13			μs

PACKAGE OUTLINE

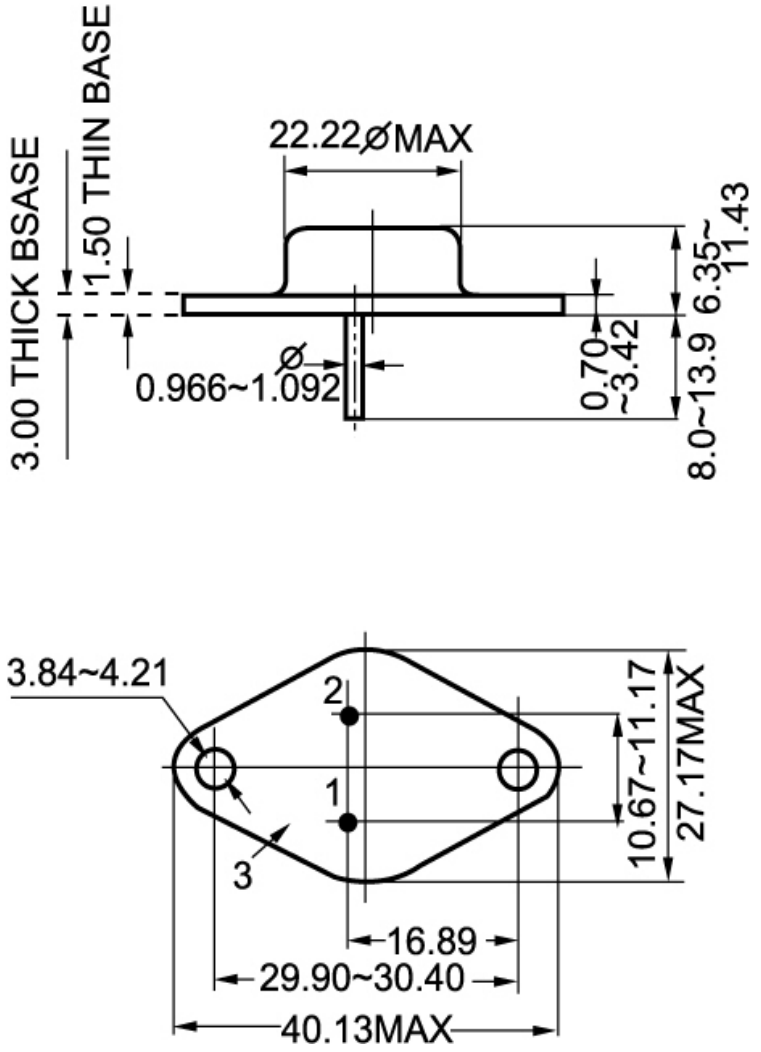

Fig.2 Outline dimensions