ADVANCE INFORMATION

89151
T-LINK COMMUNICATIONS CONTROLLER

- Complete Implementation of the T-Link Rate Adaption Protocol in a Single Device
- Adapts Synchronous or Asynchronous Terminals to 64 Kbit/s Clear or Restricted Channels
- Rate Adaption of Asynchronous Data at Rates of 300 Bit/s to 19.2 Kbit/s
- Rate Adaption of Synchronous Data at Rates of 1200 Bit/s to 64 Kbit/s
- Implements CCITT I.515 Protocol Identification for use in Multiple Rate Adaption Environments
- Provides Interworking Capability to the ISDN
- Supports Exchange of Terminal Status Indicators
- Provides Error Correction for Data Rates of 9600 Bit/s or Less
- Supports Parallel and Serial DTE Data
- Serial Terminal Interface Including EIA or CCITT Handshake Leads
- General Purpose Parallel Microprocessor Interface
- Stand-Alone Mode of Operation
- Synchronous Serial Network Interface
- SLD Compatible
- IDL Compatible
- Low Power, High Density CHMOS
- Available in 40-Pin CERDIP Package
  (See Packaging Spec. Order # 231369)

The Intel 89151 T-Link Communications Controller (TCC) is a highly integrated communications controller which provides a complete implementation of the T-Link rate adaption protocol. The 89151 is used to adapt synchronous or asynchronous terminals to the public switched digital network, or an ISDN, providing transparent, digital end to end communications. The 89151 includes a serial terminal interface which supports synchronous or asynchronous terminals, a synchronous serial network interface, and a general purpose parallel microprocessor interface. The 89151 can operate as a peripheral to a wide variety of microprocessors.

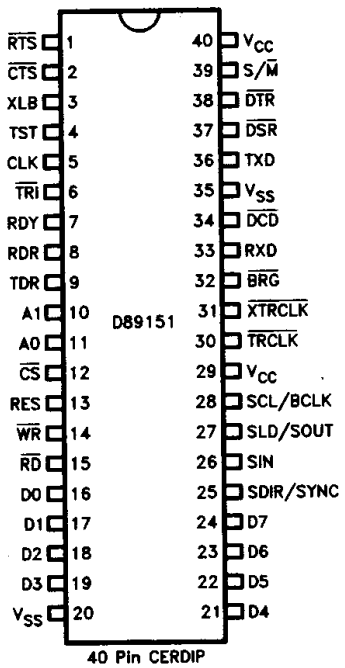


Figure 1. 89151 Pin Configuration

September 1989
Order Number: 290223-001

Table 1. 89151 Pin Description

Symbol	Pin No.	Type	Function
V_{CC}	29, 40		**POWER:** +5V Power supply.
V_{SS}	20, 35		**GROUND:** 0V
CLK	5	I	**SYSTEM CLOCK:** The 12 MHz internal system clock is input on this pin.
RES	13	I	**RESET:** (Active high input.) A high pulse on this pin instructs the 89151 to perform a self test of its internal functions and initializes the registers to the default settings. A high pulse lasting 100 ms after power-up or a 10 μs pulse while powered up will reset the 89151. Operation begins after the high level is removed.
S/$\overline{M}$	39	I	**SLAVE/MASTER SELECT:** A high level on this pin selects the 89151 to operate in the slave mode. In the slave mode a local microprocessor is required to control the state transitions of the 89151. A low level on this pin selects the 89151 to operate in the master or stand-alone mode. In the stand-alone mode the 89151 functions without a local microprocessor and the state transitions are controlled internally.
$\overline{TRI}$	6	I	**THREE-STATE:** (Active low input.) When both this pin and the S/$\overline{M}$ pin are low, all output pins and the SLD/SOUT pin are three-stated, and D0–D7 become input pins. For normal operation of the 89151 the $\overline{TRI}$ pin must be high.
TST	4	I	**TEST PIN:** This test pin should be connected to V_{SS}.
XLB	3	I	**INVERT SLD/IDL DATA:** A high level on this pin complements the transmit and receive data on the serial network interface independent of which interface, SLD or IDL, the 89151 has been configured to support. For normal SLD/IDL data this pin should be low.
SLD/SOUT	27	I/O	**SUBSCRIBER LINE DATALINK/IDL TRANSMIT DATA:** The function of this pin is dependent upon which serial network interface the 89151 has been configured to support. If the SLD interface is supported, this pin is a ping-pong data I/O used to transfer serial data between the 89151 and an SLD master device (e.g., 29C53AA). Receive SLD data is clocked into the SLD pin on the falling edge of SCL; transmit SLD data is clocked out of the SLD pin on the rising edge of SCL. If the IDL interface is supported, this pin is a data output used to transmit serial data to an IDL master device. Transmit IDL data is clocked out of the SOUT pin on the rising edge of BCLK.
SIN	26	I	**IDL RECEIVE DATA:** If the 89151 has been configured to support the IDL interface, serial data is received on this pin from an IDL master device. Receive IDL data is clocked into the SIN pin on the falling edge of BCLK. If the 89151 is configured to support the SLD interface, this pin has no function and should be connected to either V_{SS} or V_{CC}.

Table 1. 89151 Pin Description (Continued)

Symbol	Pin No.	Type	Function
SCL/BCLK	28	I	**SUBSCRIBER CLOCK/IDL CLOCK:** The serial network interface data clock is input on this pin. The frequency of the signal applied to this pin is dependent upon which serial network interface the 89151 is configured to support. If the SLD interface is supported, a 512 KHz signal should be applied to the SCL pin to clock data into and out of the SLD pin. If the IDL interface is supported and the 89151 is using the B1 channel, a 64 KHz to 2.56 MHz signal can be applied to the BCLK pin to clock data into and out of the SIN and SOUT pins. When the 89151 is using the B2 channel of the IDL interface, a 160 KHz to 2.56 MHz signal can be applied to the BCLK pin.
SDIR/SYNC	25	I	**SUBSCRIBER DIRECTION/IDL SYNC:** The function of the 8 KHz signal applied to this pin is dependent upon which serial network interface the 89151 has been configured to support. If the SLD interface is supported, the 8 KHz signal applied to the SDIR pin indicates SLD data direction and provides SLD data framing. A high level indicates that the 89151 is receiving data on the SLD pin; a low level indicates that the 89151 is transmitting data on the SLD pin. If the IDL interface is supported, the 8 KHz signal applied to the SYNC pin provides IDL data framing, with the falling edge of this signal indicating the beginning of a frame.
D0 D1 D2 D3 D4 D5 D6 D7	16 17 18 19 21 22 23 24	I/O I/O I/O I/O I/O I/O I/O I/O	**DATA PINS:** These data pins interface with the system data bus and allow the transfer of data to and from the 89151. D0 is the least significant bit and D7 is the most significant bit of the data bus. When the 89151 is selected to operate in the stand-alone mode, pins D0–D7 become an input port which defines the operational parameters of the 89151. Refer to Table 2.
A0 A1	11 10	I I	**ADDRESS PINS:** These address pins are used to select one of the directly addressable internal registers of the 89151. Refer to Table 3. When the 89151 is selected to operate in the stand-alone mode, the A1 pin selects which serial network interface the 89151 is going to support. A high level on A1 selects the SLD interface; a low level on A1 selects the IDL interface.
$\overline{CS}$	12	I	**CHIP SELECT:** (Active low input.) A low level on this pin selects the 89151 and allows read or write operations.
$\overline{WR}$	14	I	**WRITE:** (Active low input.) When the 89151 is selected and $\overline{WR}$ changes from a low to a high, data on pins D0–D7 is latched into the selected register of the 89151.
$\overline{RD}$	15	I	**READ:** (Active low input.) When the 89151 is selected and $\overline{RD}$ is low, data is transferred from the selected register of the 89151 to the data pins D0–D7.

Table 1. 89151 Pin Description (Continued)

Symbol	Pin No.	Type	Function
RDY	7	O	**READY:** (Active high output.) A high level on this pin indicates to the local microprocessor that the address register (ADR) can be written, or that the bus interface register (BIR) can be written or read. Writing to ADR causes the RDY pin to go low. See Figure 9 for details on accessing the indirect registers of the 89151. When the 89151 is selected to operate in the stand-alone mode, RDY, RDR, and TDR indicate the status of the 89151. Refer to Table 2.
RDR	8	O	**RECEIVE DATA READY:** (Active high output.) A high level on this pin indicates to the local microprocessor or DMA controller that data is available to be read from the DTE data register (DTED). When the 89151 is selected to operate in the stand-alone mode, RDY, RDR, and TDR indicate the status of the 89151. Refer to Table 2.
TDR	9	O	**TRANSMIT DATA READY:** (Active high output.) A high level on this pin indicates to the local microprocessor or DMA controller that data can be written to the DTE data register (DTED). When the 89151 is selected to operate in the stand-alone mode, RDY, RDR, and TDR indicate the status of the 89151. Refer to Table 2.
$\overline{DTR}$	38	I	**DATA TERMINAL READY:** (Active low input.) A low level on this pin indicates to the 89151 that the DTE is ready to operate. Data terminal ready can alternatively be asserted by the local microprocessor through configuration register 1 (CFR1).
$\overline{DSR}$	37	O	**DATA SET READY:** (Active low output.) A low level on this pin indicates to the DTE that the 89151 is ready to exchange further control signals to initiate the transfer of data.
$\overline{RTS}$	1	I	**REQUEST TO SEND:** (Active low input.) A low level on this pin indicates to the 89151 that the DTE is requesting the 89151 to assume the network transmit mode. Request to send can alternatively be asserted by the local microprocessor through configuration register 1 (CFR1).
$\overline{CTS}$	2	O	**CLEAR TO SEND:** (Active low output.) A low level on this pin indicates to the DTE that the 89151 is prepared to accept data for transmission to the network.
$\overline{DCD}$	34	O	**DATA CARRIER DETECT:** (Active low output.) This pin reflects the complement of the RTS T-Link signaling bit sent by the far-end TE. When the $\overline{DCD}$ pin goes low, the 89151 then sends a clear to send indicator back to the far-end TE through the CTS T-Link signaling bit.
TXD	36	I	**TRANSMIT DATA:** Serial data transmitted by the DTE is input on this pin. When the 89151 is configured for synchronous serial DTE data, the serial data input on the TXD pin is sampled on the rising edge of $\overline{TRCLK}$ or $\overline{XTRCLK}$, depending on the source of the serial terminal interface clock.

Table 1. 89151 Pin Description (Continued)

Symbol	Pin No.	Type	Function
RXD	33	O	**RECEIVE DATA:** Serial data received by the DTE is output on this pin. When the 89151 is configured for synchronous serial DTE data, the serial data is shifted out of the RXD pin on the falling edge of $\overline{TRCLK}$ or $\overline{XTRCLK}$, depending on the source of the serial terminal interface clock.
$\overline{TRCLK}$	30	O	**TRANSMIT/RECEIVE CLOCK:** This clock output provides the timing for the synchronous serial data exchange between the DTE and the 89151 when the 89151 is configured to provide the serial terminal interface clock. If the 89151 is configured to use the serial terminal interface clock provided by the DTE on the $\overline{XTRCLK}$ pin, then $\overline{TRCLK} = \overline{XTRCLK}$. The $\overline{TRCLK}$ pin is clamped high during asynchronous operation.
$\overline{XTRCLK}$	31	I	**EXTERNAL TRANSMIT/RECEIVE CLOCK:** The clock input on this pin provides the timing for the synchronous serial data exchange between the DTE and the 89151 when the 89151 is configured to use the serial terminal interface clock provided by the DTE. If the 89151 is configured for asynchronous operation or configured to provide the serial terminal interface clock on the $\overline{TRCLK}$ pin, the $\overline{XTRCLK}$ pin should be connected to V_{CC} through a weak pull up resistor.
$\overline{BRG}$	32	O	**BAUD RATE GENERATOR CLOCK:** This clock output provides the 1X baud rate clock during synchronous operation and the 16X baud rate clock during asynchronous operation.

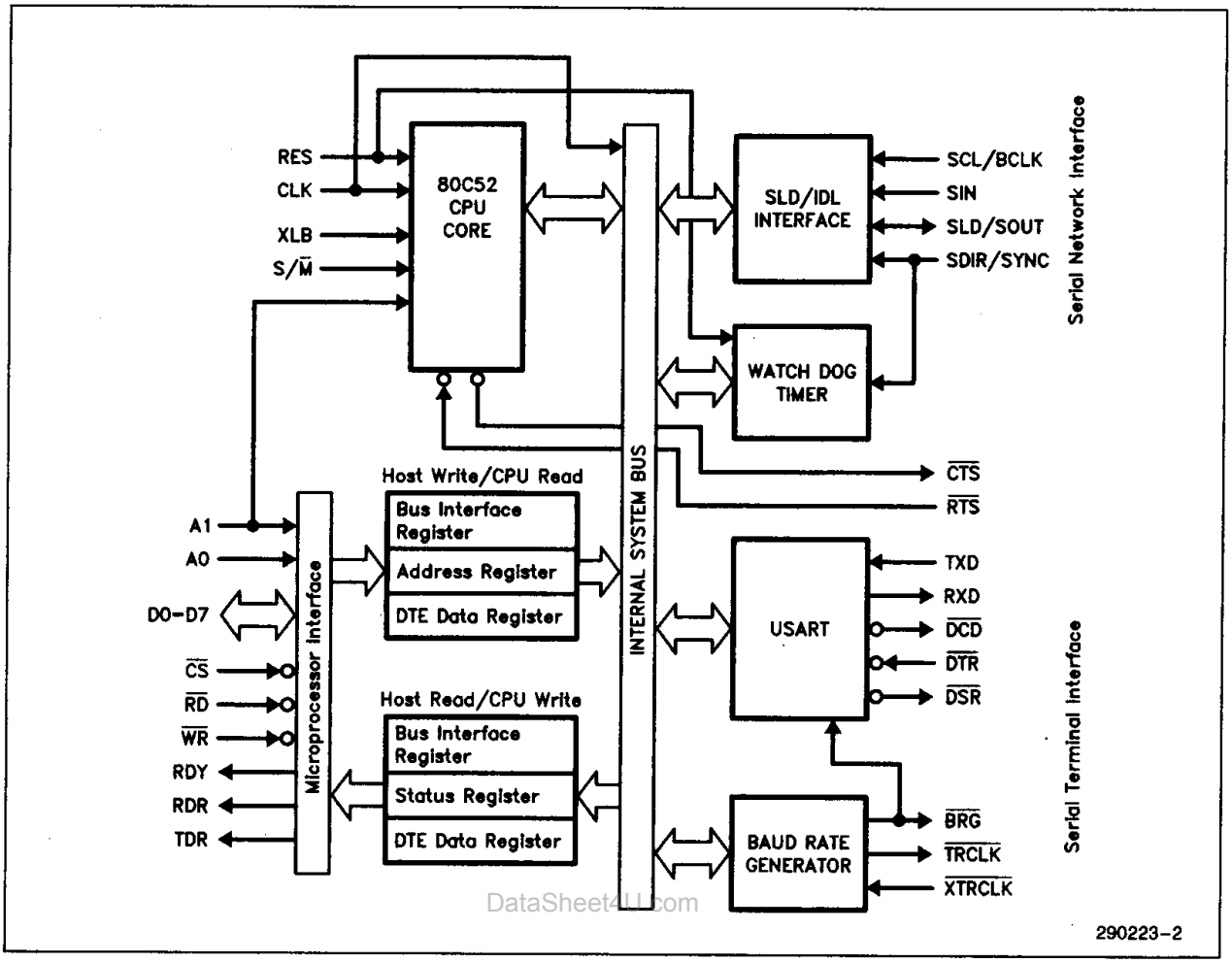


Figure 2. 89151 Block Diagram

INTRODUCTION

The 89151 T-Link Communications Controller provides a T-Link building block for implementing a Terminal Adaption Device (TAD) that may be used for an ISDN Terminal Adaptor (TA) or other TAD application. The complete T-Link rate adaption protocol is built into the 89151. The 89151 rate adapts both synchronous and asynchronous Data Terminal Equipment (DTE) to a full duplex 64 Kbit/s channel.

In ISDN TA applications the rate adaption protocol to be supported is left up to the Customer Premises Equipment (CPE) manufacturers. The protocol identifier (PID) as defined in appendix A of CCITT I.515 is used to coordinate the rate adaption protocol used in a TA. The 89151 implements the CCITT I.515 protocol identification to assist CPE manufacturers who are implementing multiple rate adaption protocols in their TAs.

T-LINK RATE ADAPTION PROTOCOL

T-Link is a full duplex byte oriented rate adaption protocol designed to transfer either synchronous or asynchronous data over a switched digital circuit at data rates from 300 bit/s to 64 Kbit/s. The T-Link protocol can be used over a 64 Kbit/s clear channel, or over a 64 Kbit/s restricted channel that permits the use of the full 64 Kbit/s capacity, but with a 1's density requirement. T-Link can also be used over a 64 Kbit/s channel with capacity restricted to 56 Kbit/s due to the use of inband signaling or a 1's density requirement of today's T1 networks. The T-Link rate adaption protocol provides:

- End to end synchronization.
- Support of terminals with synchronous data rates from 1200 bit/s to 64 Kbit/s.
- Support of terminals with asynchronous data rates from 300 bit/s to 19.2 Kbit/s.
- Exchange of EIA or CCITT terminal status indicators.
- Error correction for data rates of 9600 bit/s or less.
- Optional capability of requesting the restart of the rate adaption procedure.
- Optional capability of adapting to the requested parameters from the originating Terminal Equipment (TE).
- Far-end loopback requests.

Networks providing circuit switched 64 Kbit/s data transmission are ideal for providing high speed, wide area data transfer. T-Link provides a rate adaption protocol which can be used by a TAD to connect present DTEs to such networks. The T-Link protocol can be used over existing networks as well as over the ISDN. See Figure 3.

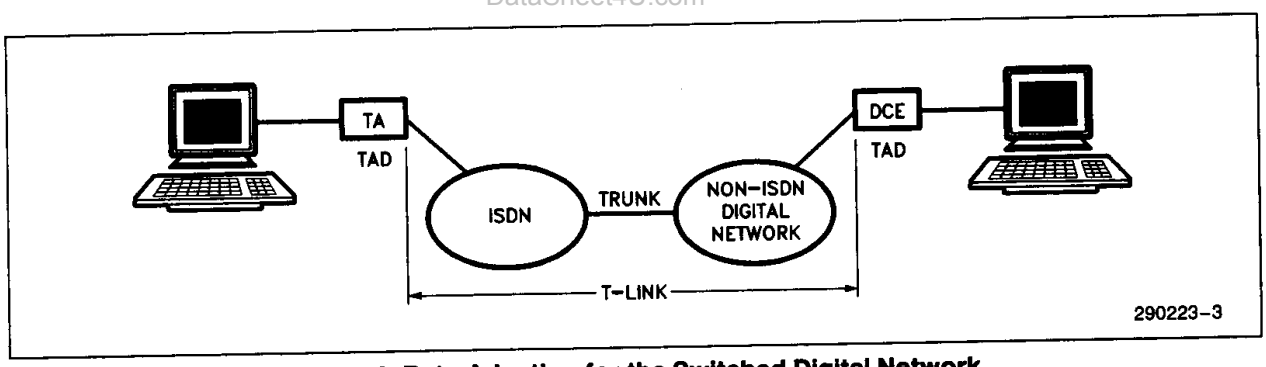


Figure 3. Rate Adaption for the Switched Digital Network

89151 ARCHITECTURAL OVERVIEW

There are three separate interfaces to the 89151 which facilitate its use in Data Communication Equipment (DCE) applications supporting the T-Link rate adaption protocol. The general purpose parallel microprocessor interface which allows the 89151 to operate as a peripheral to a wide variety of microprocessors. The serial terminal interface which supports both synchronous and asynchronous terminals. The serial network interface which supports both the Intel Subscriber Line Datalink (SLD) and the Northern Telecom Interchip Digital Link (IDL) interfaces. See Figure 2.

MICROPROCESSOR INTERFACE

The general purpose parallel microprocessor interface allows the 89151 to operate with a wide variety of microprocessors and microcontrollers. This interface is used to support both the slave and standalone modes of operation as selected by the level on the S/$\overline{M}$ pin.

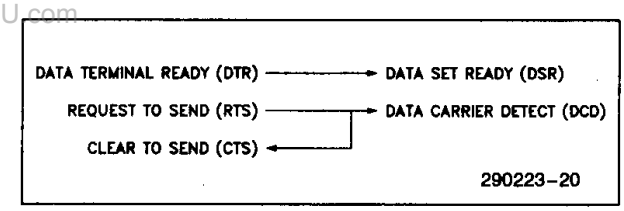
In the slave mode, S/$\overline{M}$ = 1, a local microprocessor is required to control the state transitions of the 89151 in order to establish and maintain a T-Link connection with the far-end TE. The local microprocessor must also configure the operating parameters of the 89151 when in the slave mode. The RDY, RDR, and TDR output pins are available to facilitate the process of transferring commands, status, or data between the 89151 and a local microprocessor or DMA controller. Alternatively, the complement of these output pins are available by reading the status register (SR) of the 89151.

In the stand-alone mode, S/$\overline{M}$ = 0, the 89151 functions without a local microprocessor, and the state transitions required to establish and maintain a T-Link connection are done internally by the 89151. The operating parameters to be used by the 89151 are configured by the levels on the D7–D0 and A1 pins. The status of the 89151 is indicated by the levels on the RDY, RDR, and TDR output pins. Refer to Table 2.

SERIAL TERMINAL INTERFACE

The serial terminal interface supports synchronous terminals with data rates from 1200 bit/s to 64 Kbit/s, and asynchronous terminals with data rates from 300 bit/s to 19.2 Kbit/s. Since the T-Link protocol carries the terminal status indicators across the connection through the T-Link Sd bytes (EIA/CCITT signaling), the standard EIA/CCITT handshake leads are provided. The complement of the output EIA/CCITT handshake leads are available by reading the status register (SR) of the 89151. The input EIA/CCITT handshake signals can be asserted by the local microprocessor through configuration register 1 (CFR1).

The translation of the terminal status indicators as they are carried across the connection through the T-Link Sd bytes (EIA/CCITT signaling) to the far-end TE is as follows:



The function of the EIA/CCITT handshake signals differs slightly depending on the configuration of the 89151 when in the data mode state.

For asynchronous operation:

If DCD or DSR is off, no data is sent to the DTE on the RXD pin.

If RTS is off or if a break has been received from the far-end TE through the break bit in the T-Link Sd bytes, no data is sent to the far-end TE. The EIA/CCITT handshake signal information is still sent to the far-end TE through the T-Link Sd bytes.

For synchronous operation below 48 Kbit/s:

If DCD is off, all 1's are sent to the DTE on the RXD pin.

If RTS if off, all 1's are sent to the serial network interface.

If DSR is off, the data being transmitted or received by the DTE is unaffected.

For 48, 56, and 64 Kbit/s synchronous operation:

If DTR is off, the local RTS and DCD get turned off. All 1's are sent to the DTE on the RXD pin, and all 1's are sent to the serial network interface.

In all cases, CTS is logically "ANDed" with the local RTS to allow CTS to turn off quickly when RTS if off.

The clock which provides the timing for the synchronous serial data exchange between the DTE and the 89151 can either be supplied by the 89151 on the $\overline{\text{TRCLK}}$ pin, or the 89151 can accept an external clock from the DTE on the $\overline{\text{XTRCLK}}$ pin. Only one end of a T-Link connection should be accepting an external clock from the DTE. If both ends are accepting an external clock from the DTE, the T-Link parameter exchange will not be successfully completed. When the 89151 is configured for synchronous serial DTE data, the data input on the TXD pin is sampled on the rising edge of $\overline{\text{TRCLK}}$ or $\overline{\text{XTRCLK}}$, depending on the source of the serial terminal interface clock. The falling edge of $\overline{\text{TRCLK}}$ or $\overline{\text{XTRCLK}}$, depending on the source of the serial terminal interface clock, shifts data out of the 89151 on the RXD pin when the 89151 is configured for synchronous serial DTE data.

The 89151 provides a baud rate generator clock on the $\overline{\text{BRG}}$ pin which can be used for external timing purposes. The 1X baud rate clock is provided on the $\overline{\text{BRG}}$ pin during synchronous operation, and the 16X baud rate clock is provided during asynchronous operation.

SERIAL NETWORK INTERFACE

The serial network interface is designed to transfer serial data between the 89151 and the network side of the TAD. The serial data is coded according to the T-Link protocol and transferred at a rate of 64 Kbit/s. The serial network interface supports both the Intel Subscriber Line Datalink (SLD) and the Northern Telecom Interchip Digital Link (IDL) interfaces.

SLD Interface

When the 89151 is configured to support the SLD interface, serial data is transferred bidirectionally on the SLD pin between the 89151 and a SLD master device (e.g., 29C53AA). A 512 KHz data clock should be input on the SCL pin, and a 8 KHz signal should be input on the SDIR pin to indicate SLD data direction and provide SLD data framing. The SIN pin has no function when the SLD interface is supported, so this input pin should be connected to V_{SS} or V_{CC}. Receive SLD data is clocked into the SLD pin on the falling edge of SCL when SDIR is high. Transmit SLD data is clocked out of the SLD pin on the rising edge of SCL when SDIR is low. See Figure 4.

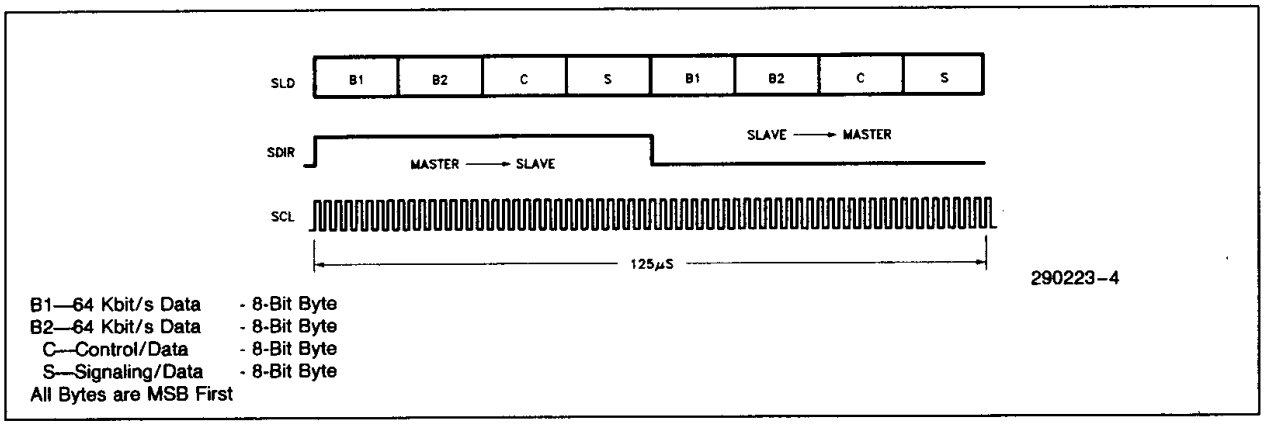


Figure 4. SLD Interface

The 89151 can operate over either the B1 or B2 channel, but only transmits data on the SLD pin during the assigned channel. This allows the 89151 to share the SLD interface with another SLD slave device, such as the 29C48 programmable CODEC/Filter. The 89151 places the SLD pin in a high impedance state during the transmit control and signaling bytes of the SLD interface.

IDL Interface

When the 89151 is configured to support the IDL interface, serial data is transferred in both directions simultaneously on the SIN and SOUT pins between the 89151 and a IDL master device. The 89151 can operate over either the B1 or B2 channel, but only the B1 channel of the IDL interface should be used in Data Unit applications, as shown in Figure 5. If the 89151 is using the B1 channel, a 64 KHz to 2.56 MHz data clock can be input on the BCLK pin. Whereas a 160 KHz to 2.56 MHz data clock can be input on the BCLK pin if the 89151 is using the B2 channel. A 8 KHz synchronization signal should be input on the SYNC pin to provide IDL data framing, with the falling edge of this signal indicating the beginning of a frame. Receive IDL data is clocked into the SIN pin on the falling edge of BCLK. Transmit IDL data is clocked out of the SOUT pin on the rising edge of BCLK. See Figure 5.

The 89151 only transmits data on the SOUT pin during the assigned B1 or B2 channel. The 89151 does not transmit during the D channel, auxiliary, or maintenance time slots of the IDL interface. The 89151 places the SOUT pin in a high impedance state during these time slots.

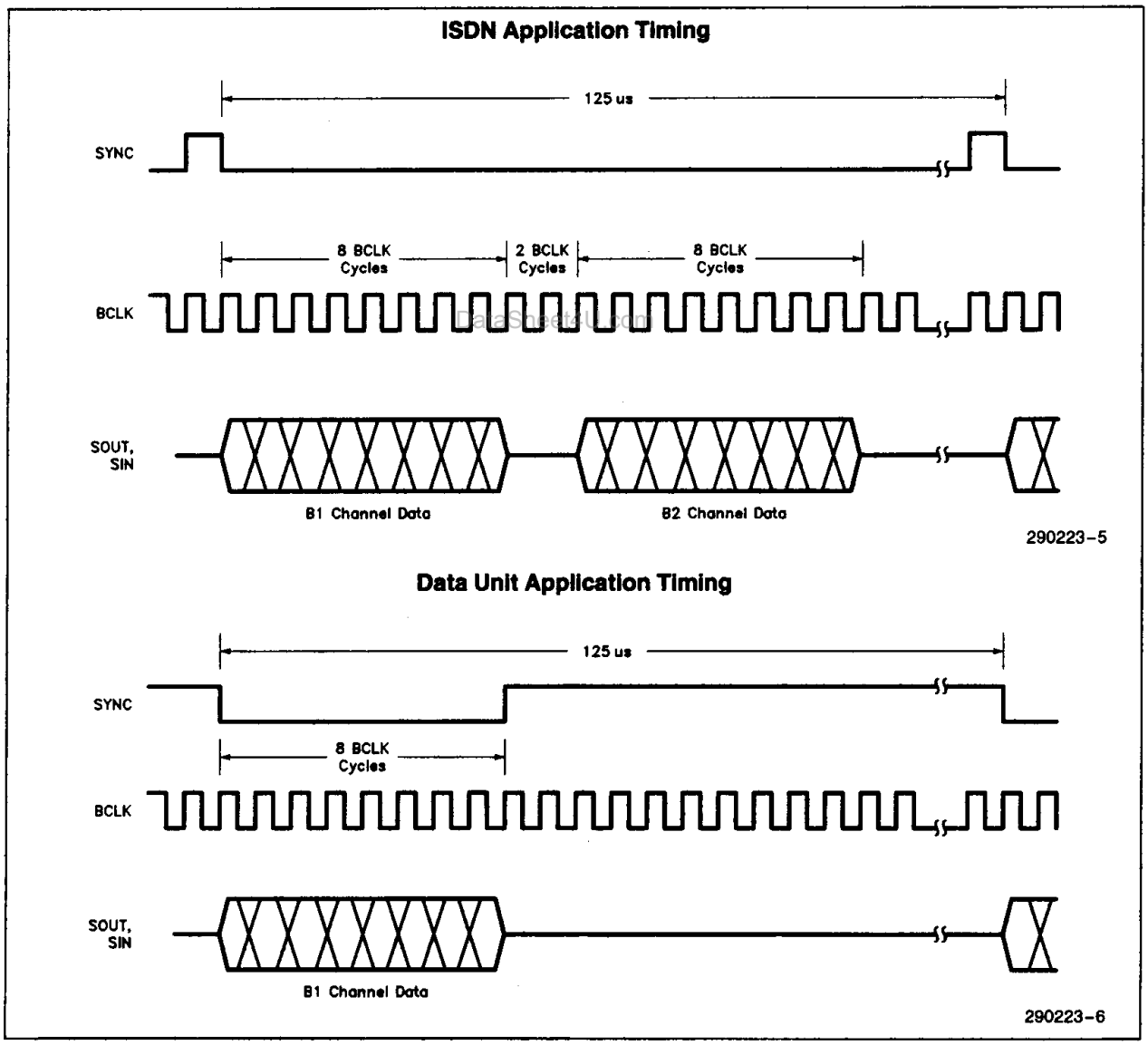


Figure 5. IDL Interface

The 89151 can complement the transmit and receive data on the serial network interface independent of which interface, SLD or IDL, is supported. If the XLB pin is high, the serial network interface data will be complemented. For normal serial network interface data the XLB pin should be low. The 89151 reads the XLB pin during execution of a self test to determine if the serial network interface data should be complemented.

The SLD/SOUT pin is three-stated after the 89151 enters the self test state, and it can be three-stated at any time by setting the NIT bit in configuration register 0 (CFR0) to 1. The 89151 constantly monitors the NIT bit, and as soon as this bit is set to 1 the SLD/SOUT pin is three-stated. If the SLD/SOUT pin has been three-stated by setting the NIT bit to 1, the SLD/SOUT pin can be enabled by setting the NIT bit to 0 and instructing the 89151 to enter the setup state. This is useful for TAs which support multiple rate adaption protocols. The 89151 can be used to perform the PID exchange, and then if necessary the SLD/SOUT pin can be three-stated and another rate adaption device enabled onto the serial network interface.

INTERNAL STATES

The 89151 functions as a state machine with each internal state of the 89151 performing a distinct part of the T-Link protocol. When the 89151 is in the slave mode, a local microprocessor controls the state transitions of the 89151 to establish and maintain a T-Link connection with the far-end TE. In the stand-alone mode the 89151 performs the required state transitions internally. Figure 6 shows the allowed state transitions of the 89151, and the corresponding command codes that need to be written to the general command status register (GCSR) in order for these state transitions to occur when the 89151 is in the slave mode.

Self Test

The 89151 performs internal self test routines during this state. During the self test the internal ROM, internal RAM, USART, baud rate generator, and the serial network interface are tested. The registers of the 89151 are initialized to the default settings during the self test state. The self test state can only be entered from the idle state.

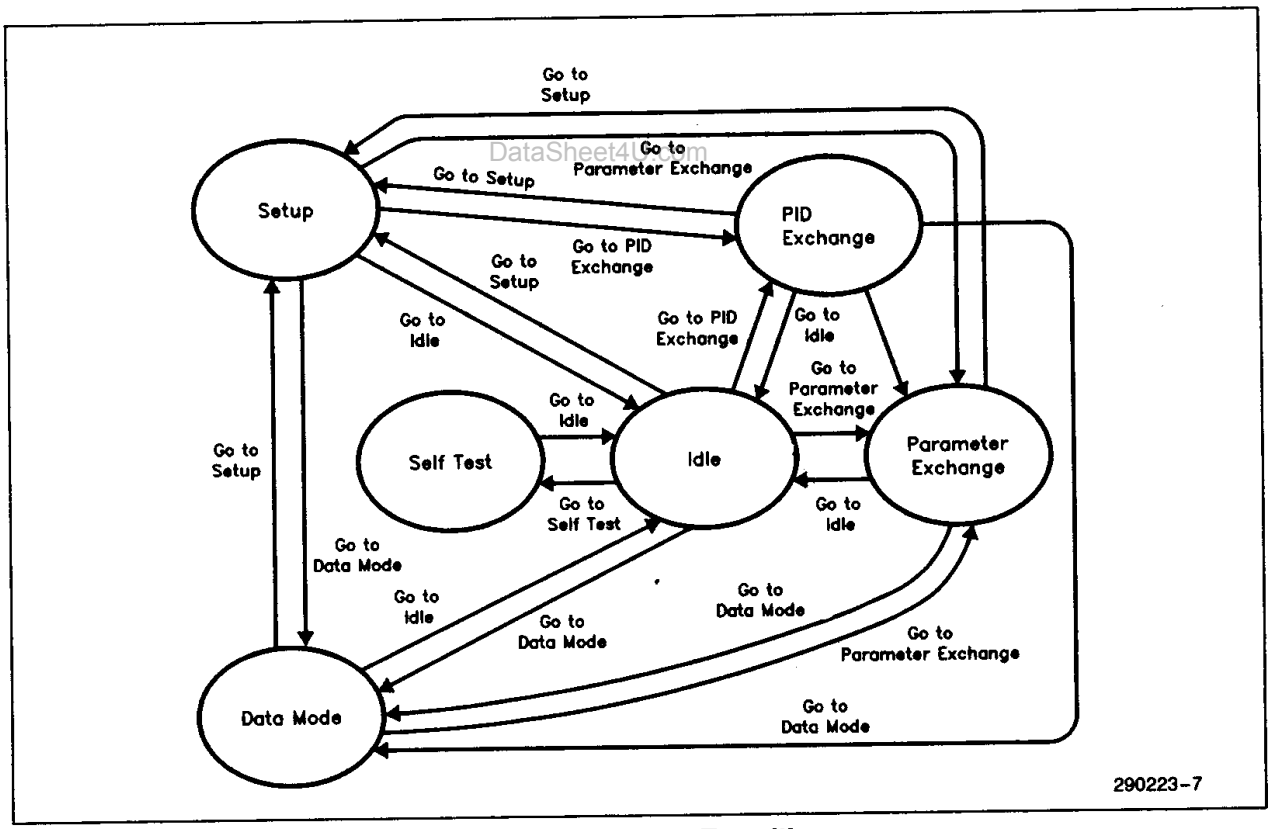


Figure 6. 89151 State Transitions

Idle

During this state the 89151 is inactive and T-Link Sgidle bytes (channel idle) are being transmitted on the serial network interface.

Setup

The operating parameters of the 89151 that have been programmed by the local microprocessor in the configuration registers (CFR0–CFR3) and the loopback control register (LCR) are checked for correctness during this state. If the operating parameters are correct, the 89151 then configures itself for communication using these parameters. During the setup state the 89151 transmits T-Link Sgidle bytes (channel idle) on the serial network interface.

PID Exchange

During this state the 89151 performs the protocol identifier (PID) exchange with the far-end TA. This PID exchange supports the protocol identification as defined in appendix A of CCITT I.515. The PID exchange is used to coordinate which rate adaption protocol is used in a TA that supports multiple rate adaption protocols.

Parameter Exchange

During this state the 89151 performs a T-Link handshake, called a parameter exchange, with the far-end TE. If the parameter exchange state was not entered from the PID exchange state, then both ends of the T-Link connection acquire T-Link synchronization to each other, exchange T-Link protocol version identifiers (T-Link PID), and exchange their desired operating parameters to be used for communication. Upon successful completion of the T-Link parameter exchange, both ends of the T-Link connection agree on the version of the T-Link protocol to be used as well as the operating parameters to be used for communication.

When the parameter exchange state is entered from the PID exchange state, both ends of the T-Link connection are already synchronized to each other and the version of the T-Link protocol to be used is already agreed upon. Both ends of the T-Link connection then exchange their desired operating parameters and agree upon which parameters are going to be used for communication. The only time that the parameter exchange state is entered from the PID exchange state is when the local microprocessor has instructed the 89151 to go to the PID exchange state and upon completion of the PID exchange the protocol agreed upon is T-Link. The 89151 then automatically enters the parameter exchange state.

Data Mode

During this state the 89151 passes data between the serial network interface and either the serial terminal interface or the DTE data register (DTED), while rate adapting this data according to the T-Link protocol.

When the 89151 is operating in the slave mode, the local microprocessor should instruct the 89151 to enter the data mode state after a successful parameter exchange. If the data mode state is entered directly from the setup state, the 89151 automatically uses version 2 of the T-Link protocol. Then the operating parameters that will be used by the 89151 are those that the local microprocessor programmed in the configuration registers (CFR0–CFR3) and the loopback control register (LCR) prior to the 89151 entering the setup state. This method of going directly to the data mode state from the setup set allows the local microprocessor to configure the 89151 for transparent operation.

When transparent operation is required, the local microprocessor should write the desired operating parameters into the configuration registers (CFR0–CFR3) and the loopback control register (LCR) making sure that the 89151 is configured for 64 Kbit/s synchronous operation. The local microprocessor should instruct the 89151 to go to the setup state, and then directly to the data mode state. Once in the data mode state, the 89151 will pass 64 Kbit/s synchronous data transparently between the serial network interface and either the serial terminal interface or the DTE data register (DTED).

The 89151 can be configured for similar transparent operation when the 64 Kbit/s network channel is restricted to 56 Kbit/s due to the use of inband signaling or a 1's density requirement. In this case the local microprocessor should configure the 89151 for 56 Kbit/s synchronous operation before instructing the 89151 to go to the setup state, and then directly to the data mode state. Once in the data mode state, the 89151 will pass 56 Kbit/s synchronous data transparently between the serial network interface and either the serial terminal interface or the DTE data register (DTED). For 56 Kbit/s transparent operation the least significant bit of the B1 or B2 channel on the serial network interface is set to 1 for transmission and ignored on reception.

SLAVE MODE

When the S/$\overline{M}$ pin is high, the 89151 is selected to operate in the slave mode. This mode is intended to be the normal operating mode of the 89151. A local microprocessor, communicating with the 89151 over the parallel microprocessor interface, is responsible for controlling the state transitions of the 89151.

The following illustrates the sequence of actions that a local microprocessor would perform to establish and maintain a T-Link connection:

1. Reset

After being reset the 89151 enters the self test state. During the self test the RDY pin is low, and once the self test is complete the RDY pin goes high. The results of the self test can then be read from the bus interface register (BIR) as shown below. These self test results are no longer available from BIR once the local microprocessor has accessed an indirect register of the 89151.

7	6	5	4	3	2	1	0
X	X	X	USART Test	Clock Test	Network Interface Test	RAM Test	ROM Test

0 = test passed; 1 = test failed

Alternatively, the local microprocessor could read the general command status register (GCSR) for the self test status, once the RDY pin is high, to determine if the self test passed or failed. This is the only way for the local microprocessor to determine the status of the self test when the 89151 has been instructed to enter the self test state by a command written to GCSR. The self test results read from BIR are only available after completion of a self test that was initiated by the 89151 having been reset. If the self test passed, the 89151 should then be instructed to enter the idle state.

NOTE:
In order for the network interface test to pass valid SCL/BCLK and SDIR/SYNC signals must be applied to the 89151.

2. Configuration of Operating Parameters

Once the 89151 is idle, the desired operating parameters should be configured. The operating parameters of the 89151 are configured through the configuration registers (CFR0–CFR3) and the loopback control register (LCR). Although these registers may be written at any time, it is recommended that they be written when the 89151 is in the idle state. Once the local microprocessor has configured the operating parameters, it should then instruct the 89151 to enter the setup state.

NOTE:
If the 89151 is not instructed to go to the setup state, it will continue to use the parameters that were in use during the last T-Link connection, or the default operating parameters. The default operating parameters are defined by the default settings of the 89151 registers which are initialized during the self test state.

Once in the setup state, the 89151 checks the correctness of operating parameters that have been previously received in CFR0–CFR3 and LCR. If there is an error in these operating parameters received from the local microprocessor, the status message of "bad setup" will be returned in the general command status register (GCSR). New and correct operating parameters should then be sent and the 89151 should be instructed to reenter the setup state.

3. Establishment of the Link

This function is not performed by the 89151. Call setup and take down must be handled by the local microprocessor.

4. Establishment of a T-Link Connection

To start a T-Link parameter exchange with the far-end TE the local microprocessor must send the 89151 the command to go to the parameter exchange state. Two forms of this command are available, one for the originating TE and one for the answering TE. It is important that these distinctions be observed and these commands be used correctly. The local microprocessor is responsible for determining when the parameter exchange is complete by periodically reading the general command status register (GCSR) to determine the status of the 89151. If the parameter exchange is not completed after a reasonable period of time, the local microprocessor is responsible for initiating corrective action.

Alternatively, the 89151 could be instructed to perform a PID exchange with the far-end TA. To start the PID exchange the local microprocessor must send the 89151 the command to go to the PID exchange state. Two forms of this command are available, one for the originating TA and one for the answering TA. The same distinctions that need to be observed when using the two parameter exchange commands also need to be observed when using the two PID exchange commands. Once the PID exchange is complete and the protocol agreed upon is

T-Link, the 89151 automatically enters the parameter exchange state. If the PID exchange is complete and the protocol agreed upon is not T-Link, the 89151 will indicate this status in GCSR. The local microprocessor should then read the PID from the protocol identifier register (PIR) and take the necessary actions to activate the appropriate rate adaption method.

5. Transition to and Maintaining Data Mode

Once the T-Link parameter exchange has been successfully completed, the 89151 should be instructed to go to the data mode state. When in the data mode state, the 89151 is passing data between the serial network interface and either the serial terminal interface or the DTE data register (DTED), while rate adapting this data according to the T-Link protocol. The local microprocessor is responsible for periodically reading the status of the 89151 from the general command status register (GCSR) and taking any necessary actions.

6. Completion of a Call

Actual take down of the call is the responsibility of the local microprocessor. When a call has been completed, the 89151 should be sent to the idle state.

Serial DTE Data

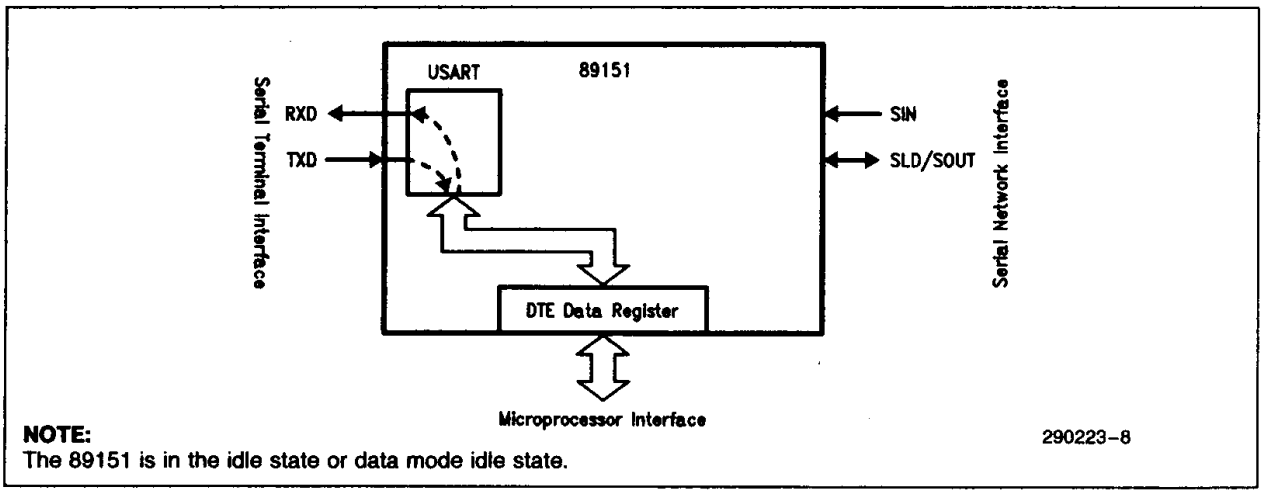
When the 89151 is in the slave mode, DTE data can be sent and received through the serial terminal interface. The 89151 is configured for serial DTE data when the PDTE bit in configuration register 0 (CFR0) is set to 0. The following data rates are supported by the 89151 when configured for serial DTE data.

Asynchronous: 300, 1200, 2400, 4800, 9600, 19200 bit/s

Synchronous: 1200, 2400, 4800, 9600, 19200, 48000, 56000, 64000 bit/s

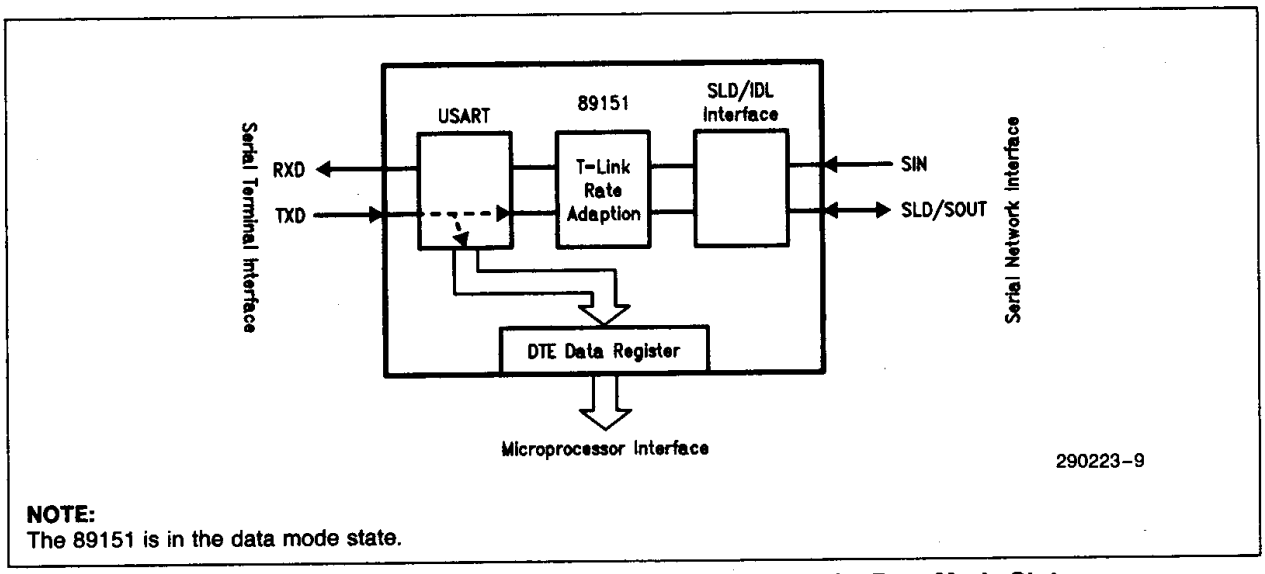
The 89151 provides some special features when configured for asynchronous serial DTE data. Once the 89151 has been configured and is currently in the idle state or data mode idle state, data written to the DTE data register (DTED) is sent out the serial terminal interface on the RXD pin. Likewise, data input on the TXD pin can be read from DTED. When the RDR pin is high or the $\overline{RDR}$ bit in the status register (SR) is 0, data is available to be read from DTED. When the TDR pin is high or the $\overline{TDR}$ bit in SR is 0, data can be written to DTED. This feature allows the local microprocessor to directly communicate with the DTE connected to the serial terminal interface of the 89151. See Figure 7.

If the local microprocessor wants to communicate with the DTE connected to the serial terminal interface while the 89151 is in the idle state, the local microprocessor needs to first configure the appropriate operating parameters of the 89151. The 89151 needs to be configured for asynchronous serial DTE data (SYNC=0 and PDTE=0 in CFR0), and the SLD/SOUT pin should be three-stated (NIT=1 in CFR0). The various asynchronous operating parameters should be configured in CFR2, and the appropriate data rate should be configured in CFR3. The local microprocessor should instruct the 89151 to go to the setup state, and then directly to the data mode state. The 89151 should then be instructed to enter the idle state. Once the 89151 is in the idle state, the local microprocessor can communicate with the DTE connected to the serial terminal interface of the 89151.



NOTE:
The 89151 is in the idle state or data mode idle state.

Figure 7. Microprocessor to DTE Communication in the Idle or Data Mode Idle State



NOTE:
The 89151 is in the data mode state.

Figure 8. Microprocessor to DTE Communication in the Data Mode State

When the 89151 is configured for asynchronous serial DTE data and is currently in the data mode state, data input on the TXD pin can be read from DTED, but data written to DTED will not get sent out the serial terminal interface on the RXD pin. When the RDR pin is high or the $\overline{RDR}$ bit in SR is 0, data is available to be read from DTED. This allows the local microprocessor to monitor the data transmitted by the DTE connected to the serial terminal interface of the 89151. See Figure 8.

If the local microprocessor wants to regain control of sending data to the DTE when the 89151 is configured for asynchronous serial DTE data and is currently in the data mode state, the 89151 should be instructed to enter the data mode idle state. The 89151 will maintain the T-Link connection by sending T-Link Sd bytes (EIA/CCITT signaling) to the far-end TE while scanning for Sgr bytes (T-Link restart request) received from the far-end TE. When the local microprocessor is done communicating with the DTE, the 89151 should be instructed to enter the data mode state.

Parallel DTE Data

When the 89151 is in the slave mode, DTE data can be sent and received through the parallel microprocessor interface instead of the serial terminal interface. The 89151 is configured for parallel DTE data when the PDTE bit in configuration register 0 (CFR0) is set to 1.

The DTE data register (DTED) and the RDR and TDR pins are used to implement this parallel mode of operation. The input EIA/CCITT handshake leads at the serial terminal interface are ignored during the parallel mode of operation, but these handshake signals can be controlled by the local microprocessor through configuration register 1 (CFR1). The output EIA/CCITT handshake leads are maintained at the serial terminal interface during the parallel mode of operation, and the complement of these handshake leads can be read from the status register (SR). When the 89151 is configured for parallel DTE data, the TXD pin is internally connected to the RXD pin once the data mode state has been entered. This ensures that any data received on the serial terminal interface is looped back and does not interfere with the parallel mode of operation. The following data rates are supported by the 89151 when configured for parallel DTE data.

Asynchronous: 300, 1200, 2400, 4800, 9600, 19200 bit/s

Synchronous: 48000, 56000, 64000 bit/s

For asynchronous data up to 8 bits can be sent and received. For synchronous data 6 bits are supported for 48 Kbit/s, 7 bits for 56 Kbit/s, and 8 bits for 64 Kbit/s. Data less than 8 bits is always justified to the least significant bit of the DTE data register (DTED). The 89151 accepts parallel DTE data at the effective rate which was negotiated during the T-Link parameter exchange. For example, if after the T-Link parameter exchange the 89151 is configured for 7-bit asynchronous data, 1 start bit, even parity, 1 stop bit, at 9600 bit/s, the 89151 will expect new data to be written to DTED no faster than once every 1.04 ms.

To maintain a high data transfer rate the RDR and TDR pins can be used for interrupts or DMA requests. The complement of these pins can be read from the status register (SR) if polling is used. When the RDR pin is high or the $\overline{RDR}$ bit in SR is set to 0, this indicates that data should be read from DTED. If

this data is not read from DTED before new decoded data arrives from the serial network interface, the old data will be overwritten. When the TDR pin is high or the $\overline{TDR}$ bit in SR is set to 0, this indicates that data should be written to DTED. If new data is not written to DTED when the 89151 is configured for synchronous operation, all ones will be sent to the serial network interface. The RDR and TDR pins are self clearing after DTED is read or written respectively.

STAND-ALONE MODE

When the S/$\overline{M}$ pin is low, the 89151 is selected to operate in the stand-alone mode. This mode allows the 89151 to function without a local microprocessor. In the stand-alone mode the 89151 actively reads the microprocessor interface to establish the operating parameters. The 89151 then automatically executes the state transitions required to establish a T-Link connection with the far-end TE.

The 89151 reads the S/$\overline{M}$ pin after being reset and periodically thereafter to determine if the A1 pin should be read. When the 89151 is selected to operate in the stand-alone mode, the A1 pin selects which serial network interface the 89151 is going to support. A high level on A1 selects the SLD interface; a low level on A1 selects the IDL interface. The operating parameters are configured by the levels on the D7–D0 pins. Refer to Table 2. The 89151 continuously polls these pins checking for changes in the operating parameters. When the 89151 is polling the D7–D0 pins it is actually reading this data from the address register (ADR). Therefore, the other pins of the microprocessor interface should be set for an ADR write as follows: A0 = 1, $\overline{CS}$ = 0, $\overline{WR}$ = 0, and $\overline{RD}$ = 1. This allows the operating parameters of the 89151 to be configured by a set of dip switches. When in the stand-alone mode, the status of the 89151 is indicated by the levels on the RDY, RDR, and TDR pins. Refer to Table 2.

When the 89151 is in the stand-alone mode, an alternate method of configuring the operating parameters of the 89151 requires a local microprocessor to write the configuration information, as shown in Table 2, to the address register (ADR). This is a simplified method of the slave mode since the local microprocessor only needs to perform one write to configure the operating parameters of the 89151. The local microprocessor can read the bus interface register (BIR) to obtain the current status of the 89151. The status messages read from BIR are the same as those read from the general command status register (GCSR) when the 89151 is in the slave mode. Refer to Table 6. The EIA/CCITT signaling bits and the break bit received in the T-Link Sd bytes (EIA/CCITT signaling), as well as the ready flags, can be read by the local microprocessor from the status register (SR).

In the stand-alone mode the 89151 is configurable for a subset of its full capabilities. The 89151 is non-adaptive or fixed when in the stand-alone mode. Therefore, the 89151 will not adapt to any of the operating parameters received from the far-end TE during the T-Link parameter exchange. This is because there is no way to determine the adapted configuration of the 89151 even if it was able to adapt to the received operating parameters. In the stand-alone mode the 89151 always uses the B1 channel of the serial network interface.

The 89151 supports both version 1 and 2 of the T-Link protocol when in the stand-alone mode. The 89151 does not have the capability to perform the originate function of the CCITT I.515 PID exchange in the stand-alone mode, since there is no way to pass the results of a PID exchange to a local microprocessor. When in the stand-alone mode, the 89151 can be the originating or answering end of a T-Link connection. The 89151 performs the T-Link protocol version exchange, which in the answering mode does follow the answering function of the CCITT I.515 PID exchange.

The following illustrates the sequence of actions that is repeated by the 89151 while operating in the stand-alone mode:

1. Self Test (RDY = 0, RDR = 0, TDR = 0)

The self test is automatically executed after the 89151 has been reset. If the 89151 passes the self test, it proceeds to step 2. RDY = 0, RDR = 1, and TDR = 1 indicate that the self test failed. If the self test failed, the 89151 will continue to indicate the self test failed status until it is reset.

2. Setup (RDY = 1, RDR = 0, TDR = 0)

The 89151 will read the address register (ADR) and decode the D7–D0 pins according to Table 2, and enter the setup state. The 89151 then configures itself for communication using the parameters read from ADR and proceeds to step 3.

3. Parameter Exchange (RDY = 1, RDR = 0, TDR = 1)

The 89151 will enter the parameter exchange state. The 89151 will remain in this state until the T-Link parameter exchange is successfully completed. Once a successful T-Link parameter exchange has been completed the 89151 proceeds to step 4.

4. Data Mode (RDY = 1, RDR = 1, TDR = 0)

The 89151 will enter the data mode state and begin passing data between the serial terminal interface and the serial network interface, while rate adapting this data according to the T-Link protocol. The 89151 responds to restart received and inband sync lost conditions by repeating steps 2 through 4.

The operating parameters of the 89151 may be changed at any time by altering the logic levels on the D7–D0 pins. When the 89151 detects that the D7–D0 pins have changed, it will go to the idle state and proceed with steps 2 through 4 of the above sequence.

Table 2. Stand-Alone Mode Interface

89151 Pins												Parameter/Status	
RDY	RDR	TDR	A1	D7	D6	D5	D4	D3	D2	D1	D0	**Async. (bit/s)**	**Sync. (bit/s)**
									0	0	0	1200	1200
									0	0	1	2400	2400
									0	1	0	4800	4800
									0	1	1	9600	9600
									1	0	0	19200	19200
									1	0	1	300	48000
									1	1	0	300	56000
									1	1	1	300	64000
								0				Asynchronous Data	
								1				Synchronous Data	
							0					Originate Parameter Exchange	
							1					Answer Parameter Exchange	
												Async.	**Sync.**
						0						No Parity	External Clock
						1						Odd Parity	Internal Clock
					0							7-Bit Characters	Restarts Disabled
					1							8-Bit Characters	Restarts Enabled
				0								1 Stop Bit	Not Used
				1								2 Stop Bits	Not Used
			0									IDL Interface	
			1									SLD Interface	
		0										Busy/Idle	
		1										In Parameter Exchange	
	0											Not in Data Mode	
	1											In Data Mode	
0												Under Test	
1												Self Test Passed	

89151 REGISTER DEFINITIONS

The following register definitions are applicable when the 89151, operating in the slave mode, is communicating with a local microprocessor over the parallel microprocessor interface.

89151 Directly Addressable Registers

The following registers are directly connected to the microprocessor interface. These registers are accessible and are available by a single microprocessor cycle access.

Table 3. 89151 Directly Addressable Registers

A1	A0	Access	Symbol	Function
0	0	RD, WR	BIR	Bus Interface Register
0	1	RD	SR	Status Register
0	1	WR	ADR	Address Register
1	0	RD, WR	DTED	DTE Data Register
1	1	RD, WR		Reserved

Address Register (ADR)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

This register is used to intermediately store the address of registers during indirect addressing. Writing to ADR causes the RDY pin to go low and the $\overline{RDY}$ bit in the status register (SR) to be set to 1.

Bus Interface Register (BIR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

This register is used to intermediately store data that is written or read from the indirectly addressable registers (GCSR, LCR, PIR, CFR0, CFR1, CFR2, and CFR3).

DTE Data Register (DTED)

7	6	5	4	3	2	1	0
DTE Data							

When the 89151 is configured for parallel DTE data (PDTE = 1 in CFR0), this register is used for passing parallel DTE data to and from the 89151. This register is written with data to be sent to the serial network interface, and when read contains data received from the serial network interface. When the TDR pin is high or the $\overline{TDR}$ bit in the status register (SR) is set to 0, this indicates that DTED should be written. When the RDR pin is high or the $\overline{RDR}$ bit in SR is set to 0, this indicates that DTED should be read. Data less than 8 bits is justified to the least significant bit, bit 0, of DTED.

Status Register (SR)

7	6	5	4	3	2	1	0
X	BRK	DCD	DSR	CTS	$\overline{RDR}$	$\overline{TDR}$	$\overline{RDY}$

This register indicates the current status of the EIA/CCITT signaling bits and the break bit received in the T-Link Sd bytes (EIA/CCITT signaling) from the far-end TE, as well as the current status of the ready flags. This register may be read at any time. There is no ready handshake pin associated with reading SR.

BRK — Break received. When this bit is set to 1, the 89151 has received a break from the far-end TE through the break bit in the T-Link Sd bytes. When the 89151 is configured for asynchronous serial DTE data (SYNC = 0 and PDTE = 0 in CFR0) and a break has been received from the far-end TE, the 89151 will send a break on the serial terminal interface to the DTE.

DCD — Data carrier detect. This bit reflects the complement of the serial terminal interface $\overline{DCD}$ handshake lead.

DSR — Data set ready. This bit reflects the complement of the serial terminal interface $\overline{DSR}$ handshake lead.

CTS — Clear to send. This bit reflects the complement of the serial terminal interface $\overline{CTS}$ handshake lead.

$\overline{RDR}$ — Receive data ready. When this bit is set to 0, data is available to be read from the DTE data register (DTED). This bit reflects the complement of the RDR output pin.

$\overline{TDR}$ — Transmit data ready. When this bit is set to 0, data can be written to the DTE data register (DTED). This bit reflects the complement of the TDR output pin.

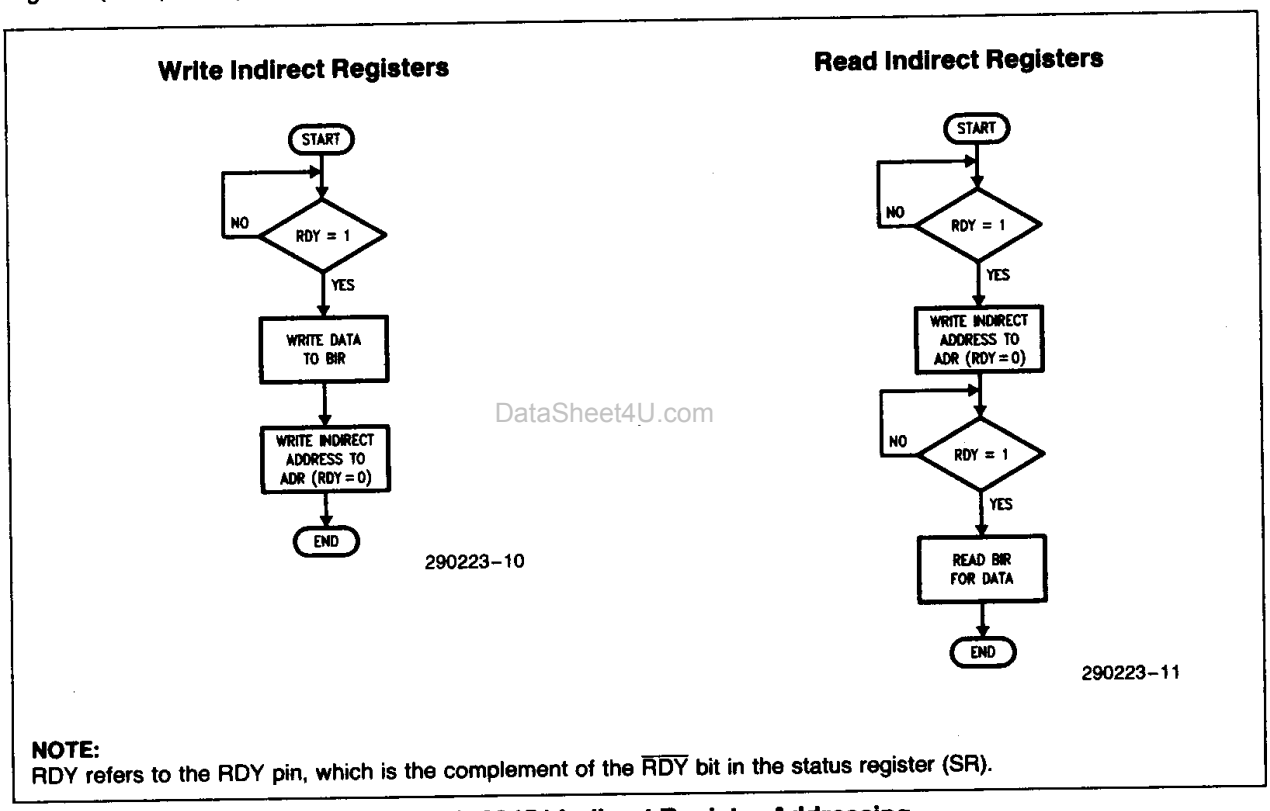
$\overline{RDY}$ — Ready. This bit along with the address register (ADR) and the bus interface register (BIR) are used to access the indirectly addressable registers of the 89151. Writing to ADR causes this bit to be set to 1 and the RDY pin to go low. This bit reflects the complement of the RDY output pin.

89151 Indirectly Addressable Registers

The following registers are not directly connected to the microprocessor interface and may be accessed through indirect addressing as detailed in Figure 9. Indirect addressing uses the contents of the address register (ADR) as a pointer to the indirect registers.

Example: The following sequence illustrates how a local microprocessor would instruct the 89151 to go to the setup state by writing to the indirectly addressable general command status register (GCSR).

1. Once the RDY pin is high or the $\overline{RDY}$ bit in the status register (SR) is 0, the local microprocessor writes the GSUP command code of 01H to the bus interface register (BIR). Refer to Table 5.
2. The local microprocessor writes 00H to the address register (ADR), which is the address of GCSR for a write operation. Refer to Table 4. The 89151 then transfers the contents of BIR to GCSR.



NOTE:
RDY refers to the RDY pin, which is the complement of the $\overline{RDY}$ bit in the status register (SR).

Figure 9. 89151 Indirect Register Addressing

Table 4. 89151 Indirectly Addressable Registers

ADR (A7–A0)		Symbol	Register Name
Read Address	Write Address		
X000XXX1	X000XXX0	GCSR	General Command Status Register
X001XXX1	X001XXX0	LCR	Loopback Control Register
X010XXX1	X010XXX0	PIR	Protocol Identifier Register
X100XXX1	X100XXX0	CFR0	Configuration Register 0
X101XXX1	X101XXX0	CFR1	Configuration Register 1
X110XXX1	X110XXX0	CFR2	Configuration Register 2
X111XXX1	X111XXX0	CFR3	Configuration Register 3

Example: The following sequence illustrates how a local microprocessor would obtain the current status of the 89151 by reading the indirectly addressable general command status register (GCSR).

1. Once the RDY pin is high or the $\overline{RDY}$ bit in the status register (SR) is 0, the local microprocessor writes 01H to the address register (ADR), which is the address of GCSR for a read operation. Refer to Table 4. The RDY pin goes low and the $\overline{RDY}$ bit in SR is set to 1.
2. Once the RDY pin is high or the $\overline{RDY}$ bit in SR is 0, the local microprocessor can read the contents of GCSR from the bus interface register (BIR). If the local microprocessor read 19H from BIR, this status message means that the 89151 received a good setup. Refer to Table 6.

Configuration Register 0 (CFR0)

7	6	5	4	3	2	1	0
NIS	NIT	ADPT	PDTE	B1B2	ICLK	SYNC	RSE

(default = 00001100)

This configuration register controls some of the various operating parameters of the 89151.

NIS — Network interface select. This bit selects which serial network interface the 89151 will support. When NIS = 1, the 89151 is configured for SLD operation. When NIS = 0, the 89151 is configured for IDL operation.

NIT — Network interface three-state. When NIT = 1, the SLD/SOUT pin is three-stated. When NIT = 0, the SLD/SOUT pin is enabled for normal operation. The 89151 constantly monitors the NIT bit, and as soon as this bit is set to 1 the SLD/SOUT pin is three-stated. If the SLD/SOUT pin has been three-stated by setting the NIT bit to 1, the SLD/SOUT pin can be enabled by setting the NIT bit to 0 and instructing the 89151 to enter the setup state.

NOTE:

The SLD/SOUT pin is three-stated after the 89151 enters the self test state. If CFR0 is read by the local microprocessor after completion of the self test, the NIT bit will be set to 1. If the local microprocessor does not write to the configuration registers (CFR0–CFR3) or the loopback control register (LCR) before instructing the 89151 to enter the setup state, the 89151 will use the default operating parameters which were initialized during the self test state. In this case, the NIT bit will be set to 0 and the SLD/SOUT pin enabled once the setup state has been entered.

ADPT — Adaptive. When ADPT = 1, the 89151 is adaptive. This means that the 89151 will use the operating parameters received from the far-end TE during the T-Link parameter exchange instead of those received from the local microprocessor. The operating parameters that the 89151 has adapted to can be determined by reading the appropriate configuration registers. These registers will reflect the operating parameters currently in use by the 89151 rather than those that were originally sent by the local microprocessor. When ADPT = 0, the 89151 is fixed. This means that the 89151 will not adapt to the operating parameters received from the far-end TE during the T-Link parameter exchange, and only the operating parameters received from the local microprocessor will be used.

PDTE — Parallel DTE data. When PDTE = 1, the 89151 is configured for parallel DTE data. In the parallel mode of operation the flow of data is between the serial network interface and the DTE data register (DTED). When PDTE = 0, the 89151 is configured for serial DTE data. In the serial mode of operation the flow of data is between the serial network interface and serial terminal interface.

NOTE:

When the 89151 is configured for parallel DTE data, the TXD pin is internally connected to the RXD pin, as shown by loopback A in Figure 10, once the data mode state has been entered. This ensures that any data received on the serial terminal interface is looped back and does not interfere with the parallel mode of operation.

B1B2 — B1/B2 channel select. This bit selects which B channel of the serial network interface will be used by the 89151. When B1B2 = 1, the 89151 will use the B1 channel. When B1B2 = 0, the 89151 will use the B2 channel.

ICLK — Internal clock. This bit determines the source of the clock that provides the timing for the synchronous serial data exchange between the DTE and the 89151. When ICLK = 1, internal clock, the 89151 provides the clock on the $\overline{TRCLK}$ pin. When ICLK = 0, external clock, the 89151 uses the clock that is input on the $\overline{XTRCLK}$ pin.

NOTE:
When the 89151 is configured for asynchronous DTE data (SYNC = 0), the internal clock is used for a baud rate reference, and the $\overline{TRCLK}$ pin is clamped high. For asynchronous DTE data the ICLK bit returns a 0 when CFR0 is read.

NOTE:
When the 89151 is configured for synchronous parallel DTE data (SYNC = 1 and PDTE = 1), the internal clock is always used.

NOTE:
Only one end of a T-Link connection can use an external clock source. If both ends are configured for an external clock source, the T-Link parameter exchange will not be successfully completed.

NOTE:
If the 89151 is going to use the serial terminal interface clock that is input on the $\overline{XTRCLK}$ pin for 48, 56, or 64 Kbit/s synchronous serial DTE data (SYNC = 1 and PDTE = 0), this clock must be phase locked to the network clock to avoid clock slippage. Therefore, it is recommended to have the 89151 provide the serial terminal interface clock on the $\overline{TRCLK}$ pin for 48, 56, or 64 Kbit/s synchronous serial DTE data.

SYNC — Synchronous data. This bit configures the 89151 for either synchronous or asynchronous DTE data. When SYNC = 1, synchronous operation is selected. When SYNC = 0, asynchronous operation is selected.

RSE — Restarts enabled. Only when the 89151 is configured for 48, 56, or 64 Kbit/s synchronous DTE data (SYNC = 1) does the RSE bit have an effect on the operation of the 89151. For these data rates the entire bandwidth of the network channel is used for carrying data and none is left over for signaling purposes. When RSE = 1, restarts enabled, the 89151 scans the data received from the serial network interface for a series of T-Link Sgr bytes (T-Link restart request), and informs the local microprocessor of a T-Link restart request through the "restart received" status message in the general command status register (GCSR). When RSE = 0, restarts disabled, the 89151 does not scan the data received from the serial network interface for T-Link Sgr bytes. Restarts are always enabled during asynchronous operation (SYNC = 0) and for synchronous operation (SYNC = 1) below 48 Kbit/s. This is because there is always excess network channel bandwidth that can be used for signaling purposes, such as sending T-Link Sgr bytes. During asynchronous operation or synchronous operation below 48 Kbit/s the RSE bit reflects whatever the local microprocessor programmed.

Configuration Register 1 (CFR1)

7	6	5	4	3	2	1	0
X	X	X	X	X	SBRK	DTR	RTS

(default = 00000000)

This configuration register is constantly monitored while the 89151 is in the data mode state. The local microprocessor can write new data to this configuration register at any time. The 89151 reads this register while in the data mode state, and sends the appropriate bits through the T-Link Sd bytes (EIA/CCITT signaling) to the far-end TE. This allows the local microprocessor to control the input EIA/CCITT handshake signals. When the 89151 is configured for parallel DTE data (PDTE = 1 in CFR0), the input EIA/CCITT handshake signals are controlled exclusively through this register since the input EIA/CCITT handshake leads of the serial terminal interface are ignored.

SBRK — Send Break. This bit allows the local microprocessor to send a break to the far-end TE only when the 89151 is configured for asynchronous parallel DTE data (SYNC = 0 and PDTE = 1 in CFR0). When SBRK = 1, a break is sent to the far-end TE through the break bit in the T-Link Sd bytes. When SBRK = 0, no break is sent to the far-end TE. When the 89151 is configured for asynchronous serial DTE data (SYNC = 0 and PDTE = 0 in CFR0), a break is sent to the far-end TE through the break bit in the T-Link Sd bytes only if a break is received on the serial terminal interface from the DTE. Setting the SBRK bit to 1 has no effect on the break bit sent in the T-Link Sd bytes when the 89151 is configured for asynchronous serial DTE data.

DTR — Data terminal ready. When the 89151 is configured for serial DTE data (PDTE = 0 in CFR0), setting the DTR bit to 1 sends the data terminal ready indicator to the far-end TE independent of the level on the $\overline{DTR}$ EIA/CCITT handshake lead. If the DTR bit is set to 0, control of the DTR T-Link signaling bit sent to the far-end TE is done exclusively by the $\overline{DTR}$ EIA/CCITT handshake lead. When the 89151 is configured for parallel DTE data (PDTE = 1 in CFR0), setting the DTR bit to 1 sends the data terminal ready

indicator to the far-end TE. When the DTR bit is set to 0, no data terminal ready indicator is sent to the far-end TE.

RTS — Request to send. When the 89151 is configured for serial DTE data (PDTE=0 in CFR0), setting the RTS bit to 1 sends the request to send indicator to the far-end TE independent of the level on the $\overline{RTS}$ EIA/CCITT handshake lead. If the RTS bit is set to 0, control of the RTS T-Link signaling bit sent to the far-end TE is done exclusively by the $\overline{RTS}$ EIA/CCITT handshake lead. When the 89151 is configured for parallel DTE data (PDTE=1 in CFR0), setting the RTS bit to 1 sends the request to send indicator to the far-end TE. When the RTS bit is set to 0, no request to send indicator is sent to the far-end TE.

Configuration Register 2 (CFR2)

7	6	5	4	3	2	1	0
X	Parity			Stop Bit(s)		Char. Length	

(default = 00000010)

This configuration register controls the various asynchronous operating parameters of the 89151. If the 89151 is configured for synchronous operation (SYNC=1 in CFR0), this register should be set to 00H.

Parity. Bits 6, 5, and 4 define the parity used by the 89151. Parity is not transported through the network. The 89151 removes the parity bit from the asynchronous data transmitted by the DTE on the serial terminal interface prior to sending this data to the serial network interface. The 89151 also generates a parity bit based on the received data from the serial network interface. This parity bit is then added to the asynchronous data prior to sending this data to the serial terminal interface. This allows the type of parity used at one TE to differ from that of the far-end TE.

Bits			Parity
6	5	4	
0	0	0	No Parity
0	0	1	Odd Parity
0	1	0	Even Parity

Stop bit(s). Bits 3 and 2 define the number of stop bit(s) per character. Stop bit(s) are not transported through the network. The 89151 removes the stop bit(s) from the asynchronous data transmitted by the DTE on the serial terminal interface prior to sending this data to the serial network interface. The 89151 also adds the stop bit(s) to the received data from the serial network interface prior to sending this asynchronous data to the serial terminal interface. This allows the number of stop bit(s) used at one TE to differ from that of the far-end TE, assuming that the number of bits per character is the same for both ends. For example, one end could be configured for 7-bit asynchronous data, no parity, and 2 stop bits. Whereas the far-end could be configured for 7-bit asynchronous data, even parity, and one stop bit.

Bits		Stop Bit(s)
3	2	
0	0	1 Stop Bit
0	1	1.5 Stop Bits
1	0	2 Stop Bits

Character Length. Bits 1 and 0 define the number of data bits per character.

Bits		Character Length
1	0	
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Configuration Register 3 (CFR3)

7	6	5	4	3	2	1	0
X	X	X	Data Rate				

(default = 00001111)

This configuration register controls the data rate of the asynchronous or synchronous DTE data that the 89151 will rate adapt to the 64 Kbit/s network channel.

Data rate. The 89151 supports the following DTE data rates.

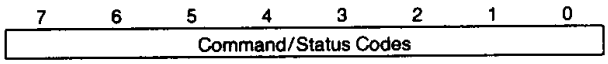
Asynchronous serial or parallel DTE data: 300, 1200, 2400, 4800, 9600, 19200 bit/s.

Synchronous serial DTE data: 1200, 2400, 4800, 9600, 19200, 48000, 56000, 64000 bit/s.

Synchronous parallel DTE data: 48000, 56000, and 64000 bit/s.

Bits					Data Rate
4	3	2	1	0	
0	0	1	1	0	300 Bit/s
0	1	0	0	0	1200 Bit/s
0	1	0	1	1	2400 Bit/s
0	1	1	0	1	4800 Bit/s
0	1	1	1	1	9600 Bit/s
1	0	0	0	1	19200 Bit/s
1	0	1	0	0	48000 Bit/s
1	0	1	1	0	56000 Bit/s
1	0	1	1	1	64000 Bit/s

General Command Status Register (GCSR)



Writing one of the following command codes, as shown in Table 5, to GCSR instructs the 89151 to enter a particular state. This allows the local microprocessor to control the state transitions of the 89151 required to establish and maintain a T-Link connection with the far-end TE. Figure 6 shows the allowed state transitions of the 89151, and the corresponding command codes that need to be written to GCSR in order for these state transitions to occur.

GIDL — Go to idle. This command instructs the 89151 to go to the idle state.

GSUP — Go to setup. This command instructs the 89151 to go to the setup state. The 89151 has to be instructed to go to the setup state whenever new data written to the configuration registers (CFR0–CFR3) or loopback control register (LCR) is to be used to configure the 89151 for new operating parameters.

GPIXO— Go to PID exchange (originate). This command instructs the 89151 to go to the protocol identifier (PID) exchange state in the originate mode.

GPIXA — Go to PID exchange (answer). This command instructs the 89151 to go to the PID exchange state in the answer mode.

NOTE:

The GPIXO and GPIXA commands must be used correctly. If both ends are in the originate mode (GPIXO), PID sync will not be found. If both ends are in the answer mode (GPIXA), unexpected results may occur during the parameter exchange state if the T-Link protocol has been agreed upon during the PID exchange state and both ends are adaptive.

GPXO — Go to parameter exchange (originate). This command instructs the 89151 to go to the parameter exchange state in the originate mode.

GPXA — Go to the parameter exchange (answer). This command instructs the 89151 to go to the parameter exchange state in the answer mode.

NOTE:

The GPXO and GPXA commands must be used correctly. If both ends are in the originate mode (GPXO), inband synchronization will not be found. If both ends are in the answer mode (GPXA), unexpected results may occur during the T-Link parameter exchange if both ends are adaptive.

GDM — Go to data mode. This command instructs the 89151 to go to the data mode state. This command should be issued by the local microprocessor after a successful T-Link parameter exchange.

Table 5. 89151 Command Codes

Code (Bits 7–0)	Command	Event
00000000	GIDL	Go to Idle
00000001	GSUP	Go to Setup
00000010	GPIXO	Go to PID Exchange (Originate)
00001010	GPIXA	Go to PID Exchange (Answer)
00000100	GPXO	Go to Parameter Exchange (Originate)
00001100	GPXA	Go to Parameter Exchange (Answer)
00000101	GDM	Go to Data Mode
00001101	GDMI	Go to Data Mode Idle
00000110	GST	Go to Self Test
Otherwise	No Effect	No Action Taken

NOTE:
If the local microprocessor wants to configure the 89151 for transparent operation, the GDM command may be issued from the setup state after a "good setup" status message has been read from GCSR, which configured the 89151 for 56 or 64 Kbit/s synchronous operation. Once in the data mode state, the 89151 will pass 56 or 64 Kbit/s synchronous data, according to version 2 of the T-Link protocol, between the serial network interface and either the serial terminal interface or the DTE data register (DTED).

GDMI — Go to data mode idle. This command instructs the 89151 to go to the data mode idle state. The 89151 will only enter the data mode idle state if configured for asynchronous serial DTE data (SYNC = 0 and PDTE = 0 in CFR0).

NOTE:
If the 89151 is in the data mode state configured for asynchronous serial DTE data and the local microprocessor wants to communicate directly with the DTE connected to the serial terminal interface, the 89151 should be instructed to enter the data mode idle state. The local microprocessor can then send and receive data to and from the serial terminal interface through the DTE data register (DTED).

The 89151 maintains the T-Link connection by sending T-Link Sd bytes (EIA/CCITT signaling) to the far-end TE while scanning for T-Link Sgr bytes (T-Link restart request) received from the far-end TE. Once the local microprocessor is finished communicating with the DTE, the 89151 should be instructed to enter the data mode state.

GST — Go to self test. This command instructs the 89151 to go to the self test state. This command can only be issued when the 89151 is in the idle state.

Reading GCSR allows the local microprocessor to obtain the current status of the 89151, as shown in Table 6. GCSR should be polled by the local microprocessor to monitor the status of the 89151 during the establishment and maintenance of a T-Link connection.

Table 6. 89151 Status Messages

Status Bits					State Code			Status Message	State
7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	0	Busy	Idle
0	0	0	0	1	0	0	0	Idle	
0	0	0	0	0	0	0	1	Checking Configuration	Setup
0	0	0	0	1	0	0	1	Bad Setup	
0	0	0	1	1	0	0	1	Good Setup	
0	0	0	0	0	0	1	0	PID Exchange in Progress	PID Exchange
0	X	X	X	1	0	1	0	PID Sync Received	
0	X	X	1	X	0	1	0	PID Received	
0	X	1	X	X	0	1	0	PID Transmit Complete	
0	1	X	X	X	0	1	0	PID Complete, Not T-Link	
0	0	0	0	0	1	0	0	Parameter Exchange in Progress	Parameter Exchange
0	0	0	0	1	1	0	0	Sgvi Received	
0	0	0	1	0	1	0	0	Inband Sync Found	
0	0	0	1	1	1	0	0	Parameter Exchange Complete	
0	1	0	0	0	1	0	0	Originate Parameter Exchange, Restart Received	
X	X	X	X	0	1	0	1	Data Mode	Data Mode
X	X	X	X	1	1	0	1	Data Mode Idle	
X	X	X	0	X	1	0	1	Far-End Loopback Off	
X	X	X	1	X	1	0	1	Far-End Loopback On	
X	X	0	X	X	1	0	1	Local Loopback Off	
X	X	1	X	X	1	0	1	Local Loopback On	
X	0	X	X	X	1	0	1	No Restart Received	
X	1	X	X	X	1	0	1	Restart Received	
0	X	X	X	X	1	0	1	In Sync	
1	X	X	X	X	1	0	1	Inband Sync Lost	
0	0	0	0	0	1	1	0	Self Test Failed	Self Test
0	0	0	0	1	1	1	0	Self Test Passed	

Idle Status Messages

Busy — This status message indicates that the 89151 can't go immediately to the idle state. The local microprocessor should continue to poll GCSR to monitor the status of the 89151.

Idle — This status message indicates that the 89151 is in the idle state.

Setup Status Messages

Checking configuration — This status message indicates that the 89151 is checking the correctness of the operating parameters previously received in the configuration registers (CFR0–CFR3) and the loopback control register (LCR). The local microprocessor should continue to poll GCSR to monitor the status of the 89151.

Bad setup — This status message indicates that there is an error in the operating parameters previously received from the local microprocessor.

Good setup — This status message indicates that the operating parameters previously received from the local microprocessor are correct. The 89151 is now configured for communication using these operating parameters.

Protocol Identifier (PID) Exchange Status Messages

PID exchange in progress — This status message indicates that the 89151 has not yet recognized a connection to the far-end TA. If the PID exchange originate command (GPIXO) was written to GCSR, the 89151 is sending PID ready bytes and waiting to receive PID sync bytes. If the PID exchange answer command (GPIXA) was written to GCSR, the 89151 is sending PID sync bytes and waiting to receive PID sync bytes.

NOTE:
The following PID exchange status bits get set to 1 as they occur. The local microprocessor may not be capable of requesting status updates from the 89151 fast enough to capture each PID exchange status message as it occurs. If at the end of the PID exchange the PID in use is not T-Link, the "PID complete, not T-Link" status message will remain as the current status until the local microprocessor writes another command code to GCSR.

PID sync received — This status message indicates that PID sync bytes have been received by the 89151. If the PID exchange originate command (GPIXO) was written to GCSR, the 89151 is sending PID sync bytes while waiting to receive the PID from the far-end TA. If the PID exchange answer command (GPIXA) was written to GCSR, the 89151 proceeds to send the PID to the far-end TA. The PID that is sent to the far-end TA is that which has been written to the protocol identifier register (PIR) by the local microprocessor.

PID received — This status message indicates that the 89151 has received the PID from the far-end TA. If the PID exchange originate command (GPIXO) was written to GCSR, the local microprocessor should read the received PID from the protocol identifier register (PIR) and decide which rate adaption protocol to use. The local microprocessor should then write the desired operating PID to the protocol identifier register (PIR) with only the bit corresponding to the desired rate adaption protocol being set to 1. If the local microprocessor wants to use the T-Link protocol, the protocol identifier register (PIR) can be written with both bits corresponding to version 1 and version 2 of the T-Link protocol being set to 1. This is because if the terminal equipment at both ends indicate that they are compatible with both version 1 and version 2 of the T-Link protocol, as is the case with the 89151, then version 2 of the T-Link protocol will be used. Once the operating PID has been written to PIR, the 89151 logically "ANDs" this PID with the PID that was received from the far-end TA and proceeds to send the resulting PID back to the far-end TA. If the PID exchange answer command (GPIXA) was written to GCSR, this status message indicates that the PID has been received from the far-end TA.

NOTE:
When the PID exchange originate command (GPIXO) has been written to GCSR, the local microprocessor should read and write the protocol identifier register (PIR) within 1 second after the "PID received" status message has been read from GCSR. This ensures proper T-Link interworking with other vendors' T-Link implementations.

PID transmit complete — This status message indicates that the 89151 has sent the PID to the far-end TA.

PID complete, not T-Link — This status message indicates that the PID exchange is complete and the PID in use is not T-Link. The local microprocessor should read the PID from the protocol identifier register (PIR) and activate the appropriate rate adaption protocol. At this point the 89151 could be sent to the 64 Kbit/s transparent mode configured for serial DTE data and providing the serial terminal interface clock (PDTE = 0 and ICLK = 1 in CFR0), or configured for parallel DTE data (PDTE = 1 in CFR0). Alternatively, the local microprocessor could three-state the SLD/SOUT pin of the 89151 (NIT = 1 in CFR0) and enable another rate adaption device onto the serial network interface.

NOTE:
If at the end of the PID exchange the PID in use is T-Link, the 89151 will automatically enter the parameter exchange state and proceed with the normal T-Link parameter exchange. This is indicated by the status message read from GCSR changing to "Sgvi received".

Parameter Exchange Status Messages

NOTE:
The following parameter exchange status messages get updated as they occur. The local microprocessor may not be capable of requesting status updates from the 89151 fast enough to capture each parameter exchange status message as it occurs. If the T-Link parameter exchange is successfully completed, the "parameter exchange complete" status message will remain as the current status until the local microprocessor writes another command code to GCSR.

Parameter exchange in progress — This status message indicates that the 89151 has not yet recognized a connection to the far-end TE which supports the T-Link rate adaption protocol. If the parameter exchange originate command (GPXO) was written to GCSR, the 89151 is sending T-Link Sgr bytes (T-Link restart request) and waiting to receive T-Link Sgvi bytes (protocol version follows). If the parameter exchange answer command (GPXA) was written to GCSR, the 89151 is sending T-Link Sgvi bytes and waiting to receive T-Link Sgvi bytes.

Sgvi received — This status message indicates that the 89151 has received T-Link Sgvi bytes (protocol version follows). If the parameter exchange originate command (GPXO) was written to GCSR, the 89151 is sending T-Link Sgvi bytes while waiting to receive a valid T-Link protocol version identifier (T-Link PID) from the far-end TE. If the parameter exchange answer command (GPXA) was written to GCSR, the 89151 proceeds to send the T-Link protocol version identifier (T-Link PID) to the far-end TE.

Inband sync found — This status message indicates that the 89151 has received a valid T-Link protocol version identifier (T-Link PID), and operating parameters have been exchanged at least once with the far-end TE.

NOTE:
If the "parameter exchange in progress", "Sgvi received", and "inband sync found" status messages are being repeated, this is an indication that the two ends of the T-Link connection can't agree on the operating parameters to be used. This would be the case if both ends are operating in the fixed or non-adaptive mode with incompatible operating parameters. One way to overcome this situation is for the answering device to become adaptive and restart the T-Link parameter exchange in the answer mode. If the 89151 is the answering device, then once the "parameter exchange complete" status message is read from GCSR the local microprocessor should read the appropriate configuration registers to determine the operating parameters that where agreed upon during the T-Link parameter exchange.

Parameter exchange complete — This status message indicates that the T-Link parameter exchange has been successfully completed. If the 89151 is adaptive (ADPT = 1 in CFR0) and the parameter exchange answer command (GPXA) was written to GCSR, the local microprocessor should read the appropriate configuration registers to determine the current operating parameters of the 89151.

Originate parameter exchange, restart received — This status message indicates that the 89151 was sent to the parameter exchange state in the originate mode and is currently receiving T-Link Sgr bytes (T-Link restart request) from the far-end TE. If the 89151 was the originating device at the beginning of the call, it is up to the far-end TE to back down to the answer mode. However, if the 89151 was the answering device at the beginning of the call and this status message is read from GCSR, the 89151 should be sent to the idle state, and then to the parameter exchange state in the answer mode. This is the method used to avoid restart contention when both ends of the T-Link connection are trying to be the originator by sending T-Link Sgr bytes.

Data Mode Status Messages

Data mode — This status message indicates that the 89151 is in the data mode state. The 89151 is now passing data between the serial network interface and either the serial terminal interface or the DTE data register (DTED), while rate adapting this data according to the T-Link protocol. GCSR should continue to be polled periodically by the local microprocessor to monitor the status of the 89151.

Data mode idle — This status message indicates that the 89151 is in the data mode idle state. The local microprocessor can now communicate directly with the DTE connected to the serial terminal interface through the DTE data register (DTED). The 89151 maintains the T-Link connection by sending T-Link Sd bytes (EIA/CCITT signaling) to the far-end TE while scanning for T-Link Sgr bytes (T-Link restart request) received from the far-end TE.

Far-end loopback off — This status message indicates that the far-end TE has not enabled any

loopbacks due to a loopback request sent by the 89151 during the T-Link parameter exchange.

Far-end loopback on — This status message indicates that the far-end TE received a loopback request from the 89151 during the T-Link parameter exchange. The far-end TE should now be looped back to the 89151. Therefore, data and T-Link Sd bytes (EIA/CCITT signaling) that the far-end TE receives on the serial network interface are to be returned back to the 89151.

Local loopback off — This status message indicates that the serial terminal interface loopbacks of the 89151 have not been enabled by a loopback request sent by the far-end TE during the T-Link parameter exchange.

NOTE:
The serial terminal interface loopbacks can be enabled by the local microprocessor setting the STILB bit in the loopback control register (LCR) to 1, but the "local loopback off" status message will still be read from GCSR. This is because the serial terminal interface loopbacks, as shown by loopbacks A and B in Figure 10, have been enabled by the local microprocessor instead of by a loopback request from the far-end TE.

Local loopback on — This status message indicates that the serial terminal interface loopbacks of the 89151, as shown by loopbacks A and B in Figure 10, have been enabled by a loopback request received from the far-end TE during the T-Link parameter exchange.

NOTE:
When the 89151 is configured for parallel DTE data (PDTE = 1 in CFR0) and the "local loopback on" status message is read from GCSR, then parallel DTE data that is written to the DTE data register (DTED) is not sent to the serial network interface, but instead is echoed back in DTED. Likewise data received on the serial network interface is not available to be read from DTED, since this data will be looped back at the serial terminal interface, as shown by loopback B in Figure 10.

No restart received — This status message indicates that no T-Link Sgr bytes (T-Link restart request) have been received on the serial network interface from the far-end TE.

Restart received — This status message indicates that the 89151 has received a series of contiguous T-Link Sgr bytes (T-Link restart request) on the serial network interface from the far-end TE. This status message takes priority over an "inband sync lost" status message. If the TE supports T-Link restarts, the local microprocessor should instruct the 89151 to go to the parameter exchange state in the answer mode, otherwise the local microprocessor should terminate the T-Link connection.

In sync — This status message indicates that the T-Link connection between the 89151 and the far-end TE is synchronized.

Inband sync lost — This status message indicates that the 89151 has lost T-Link synchronization with the far-end TE. The local microprocessor may now attempt to restart the T-Link connection by instructing the 89151 to go to the parameter exchange state in the originate mode, otherwise the local microprocessor should terminate the T-Link connection.

Self Test Status Messages

Self test failed — This status message indicates that the 89151 failed its self test routines.

Self test passed — This status message indicates that the 89151 passed its self test routines. The configuration registers (CFR0–CFR3), loopback control register (LCR), and protocol identifier register (PIR) are now initialized to the default settings.

Loopback Control Register (LCR)

7	6	5	4	3	2	1	0
X	X	X	LBR*	FELB	IDLLB	STILB	X

(default = 00000000)
(* = read only)

This register controls the various internal loopbacks of the 89151. LCR is also used to send a loopback request to the far-end TE during the T-Link parameter exchange. The local microprocessor must instruct the 89151 to go to the setup state after LCR has been written. The 89151 will then enable or disable the appropriate loopbacks. Figure 10 shows the various internal loopbacks of the 89151.

LBR — Loopback request. The LBR bit is set to 1 when the 89151 has received and accepted a loopback request from the far-end TE during the T-Link parameter exchange. The 89151 will then enable the serial terminal interface loopbacks, as shown by loopbacks A and B in Figure 10, once the data mode state has been entered.

NOTE:
The 89151 will always accept a loopback request received from the far-end TE. The exception to this is when both ends of a T-Link connection send a loopback request simultaneously during the T-Link parameter exchange. If the 89151 is the originating end of the T-Link connection, it will ignore the loopback request from the far-end TE and the LBR bit will be set to 0. However, the far-end TE will become looped back, since it is the answering end of the T-Link connection.

FELB — Far-end loopback. When FELB = 1, the 89151 sends a loopback request to the far-end TE during the T-Link parameter exchange. When FELB = 0, no loopback request is sent to the far-end TE during the T-Link parameter exchange.

IDLLB — IDL loopback. When IDLLB = 1, the 89151 enables the serial network interface loopbacks, as shown by loopbacks C and D in Figure 10, once the setup state has been entered. When IDLLB = 0, the 89151 disables the serial network interface loopbacks once the setup state has been entered.

NOTE:
The serial network interface loopbacks can only be enabled when the 89151 is configured for IDL operation (NIS = 0 in CFR0). If the 89151 is configured for SLD operation (NIS = 1 in CFR0) and the IDLLB bit is set to 1, then when the 89151 is instructed to go to the setup state the "bad setup" status message will be returned in the general command status register (GCSR).

STILB — Serial terminal interface loopback. If the STILB bit is set to 1 by the local microprocessor, the serial terminal interface loopbacks, as shown by loopbacks A and B in Figure 10, are enabled once the setup state has been entered. If the local microprocessor sets the STILB bit to 0, the serial terminal interface loopbacks are disabled once the setup state has been entered.

NOTE:
When the loopback control register (LCR) is read by the local microprocessor, the STILB bit always reflects if the serial terminal interface loopbacks are enabled or disabled. Therefore, the STILB bit is automatically set to 1 upon entry into the data mode state when the LBR bit has been set to 1. Likewise, the STILB bit is automatically set to 1 upon entry into the data mode state when the 89151 is configured for parallel DTE data (PDTE = 1 in CFR0), although only loopback A, as shown in Figure 10, is enabled. If the STILB bit was automatically set to 1, then the 89151 will automatically set this bit to 0, thereby disabling the serial terminal interface loopbacks, once the setup state has been entered.

NOTE:
If the serial terminal interface loopbacks, as shown by loopbacks A and B in Figure 10, are enabled by a loopback request received from the far-end TE during the T-Link parameter exchange, the output EIA/CCITT handshake leads are clamped high in order to support CCITT V.54 remote loopbacks. If the serial terminal interface loopbacks are enabled by the local microprocessor setting the STILB bit to 1, the output EIA/CCITT handshake leads are maintained at the serial terminal interface by the EIA/CCITT signaling bits received in the T-Link Sd bytes (EIA/CCITT signaling) from the far-end TE.

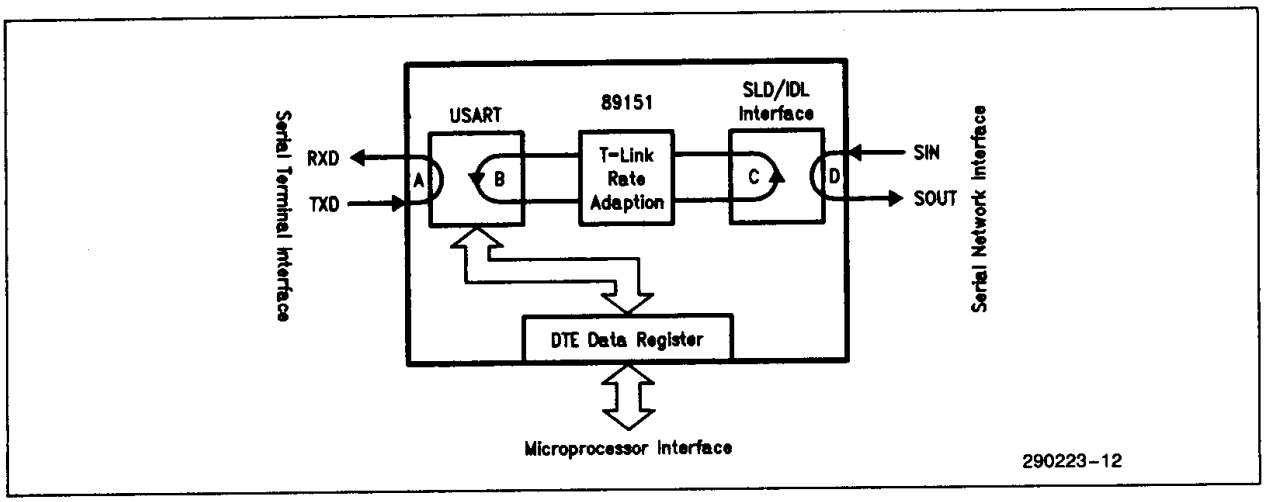


Figure 10. 89151 Internal Loopbacks

Protocol Identifier Register (PIR)

7	6	5	4	3	2	1	0
P4	P5	P6	P7	P0	P1	P2	P3

(default = 00000011)

This register allows the local microprocessor to write and read the protocol identifier (PID) that is sent and received to and from the far-end TA during the PID exchange state. The definition of the PID bits contained in Appendix A of CCITT I.515 are mapped into the protocol identifier register (PIR) as follows:

P3 = T-Link version 1
P2 = T-Link version 2
P1 = reserved
P0 = reserved for the future extension bit
P7 = V.110 protocol
P6 = V.120 protocol
P5 = X.30 protocol
P4 = X.31 protocol

NOTE:
The reserved PID bits, P1 and P0, should be set to 0.

If the TA only supports T-Link, the protocol identifier register (PIR) should be programmed for T-Link version 1 and 2. If the 89151 is going to be instructed to go to the PID exchange state in the answer mode, then additional bits in the protocol identifier register (PIR) should be set to 1 for those rate adaption protocols which the TA supports.

Example: T-Link only, PIR = 03H. This is the default setting of PIR since the 89151 supports both version 1 and 2 of the T-Link protocol.

Example: T-Link and V.110, PIR = 13H.

NOTE:
If the local microprocessor is going to instruct the 89151 to go to the parameter exchange state in either the originate or answer mode, the protocol identifier register (PIR) does not have to be programmed. The 89151 will automatically send the T-Link protocol version identifier (T-Link PID) for T-Link version 1 and 2 to the far-end TE during the protocol version exchange phase of the T-Link parameter exchange. Once the "parameter exchange complete" status message is read from the general command status register (GCSR), the local microprocessor may read the protocol identifier register (PIR) to determine which version of the T-Link protocol is being used for the T-Link connection with the far-end TE.

If the 89151 is going to be instructed to go to the PID exchange state, it is the responsibility of the local microprocessor to program the PID in the protocol identifier register (PIR). This is the case for both the originate and answer modes of operation. However, there are shortcuts which can be taken. The 89151 initializes the protocol identifier register (PIR) for T-Link version 1 and 2 during the self test state. If the 89151 is going to be instructed to go to the PID exchange state in the answer mode and T-Link is the only protocol that is going to be supported by the TA, the local microprocessor does not have to program the PID in the protocol identifier register (PIR). This is assuming that PIR has already been initialized for T-Link version 1 and 2 during the self test state. The local microprocessor simply instructs the 89151 to go to the PID exchange state in the answer mode, and then polls the general command status register (GCSR) for status messages.

If the 89151 is going to be instructed to go to the PID exchange state in the originate mode, the local microprocessor must program the PID in the protocol identifier register (PIR). Again, there are shortcuts which can be taken. The local microprocessor can write the desired operating PID to the protocol identifier register (PIR) before instructing the 89151 to enter the PID exchange state in the originate mode. This way the local microprocessor does not have to read and write the protocol identifier register (PIR) within 1 second after the "PID received" status message is read from GCSR since the desired operating PID is already programmed in PIR. This method does not guarantee PID compatibility because the 89151 logically "ANDs" the received PID from the far-end TA with the PID that was programmed by the local microprocessor in PIR, and if a mismatch occurs the null PID will be sent to the far-end TA.

NOTE:
If the 89151 has been instructed to go to the PID exchange state in the originate mode, the 89151 will not send the PID to the far-end TA until the local microprocessor has written the desired operating PID to protocol identifier register (PIR).

When the local microprocessor reads the protocol identifier register (PIR), the PID read from this register can take on different values during the PID exchange. If a data call has not been established since PIR was initialized by the 89151 during the self test state, the PID read from the protocol identifier register (PIR) will equal T-Link version 1 and 2. If the 89151 was instructed to go to the PID exchange state in the originate mode and the "PID received" status message has been read from the general command status register (GCSR), the PID read from the protocol identifier register (PIR) is the PID received from the far-end TA. Now, if the "PID transmit complete" status message has been read from GCSR, the PID read from PIR is that which has been sent to the far-end TA. This PID is the "ANDed" version of the PID received from the far-end TA with the PID that was programmed in PIR by the local microprocessor. If the 89151 was instructed to go to the PID exchange state in the answer mode and the "PID received" status message has been read from GCSR, the PID read from the protocol identifier register (PIR) is the "ANDed" version of the PID received from the far-end TA with the PID that was programmed in PIR by the local microprocessor.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to V_{SS} ..... −0.5V to V_{CC} + 0.5V
Maximum Voltage on V_{CC} with Respect to V_{SS} ..... +7V
Power Dissipation 1.0W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS V_{CC} = +5V ± 10%; V_{SS} = 0V; T_A = 0°C to +70°C

Typical Values are at T_A = 25°C and Nominal Power Supply Values

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except CLK, RES, D0–D7, SDIR/SYNC, SIN, SCL/BCLK, SLD)			0.8	V	
V_{IL1}	Input Low Voltage (CLK, RES, D0–D7)			0.2 V_{CC} − 0.1	V	
V_{IL2}	Input Low Voltage (SDIR/SYNC, SIN, SCL/BCLK, SLD)			1.2	V	
V_{IH}	Input High Voltage (Except CLK, RES, D0–D7, SDIR/SYNC, SIN, SCL/BCLK, SLD)	2.0			V	
V_{IH1}	Input High Voltage (CLK, RES)	0.7 V_{CC}			V	
V_{IH2}	Input High Voltage (D0–D7)	0.2 V_{CC} + 0.9			V	
V_{IH3}	Input High Voltage (SDIR/SYNC, SIN, SCL/BCLK, SLD)	3.5			V	
V_{OL}	Output Low Voltage (Except SLD/SOUT)			0.45	V	I_{OL} = 3.2 mA
V_{OL1}	Output Low Voltage (SLD/SOUT)			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage (Except SLD/SOUT)	2.4			V	I_{OH} = −80 µA I_{OH} = −800 µA (D0–D7)
V_{OH1}	Output High Voltage (SLD/SOUT)	4.0			V	I_{OH} = −2.4 mA
I_{OFL}	Output Float Leakage Current			±10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$
I_{IL}	Input Leakage Current			±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{CC}	V_{CC} Supply Current		35		mA	
C	Pin Capacitance			10	pF	

A.C. CHARACTERISTICS V_{CC} = +5V ±10%; V_{SS} = 0V; T_A = 0°C to +70°C

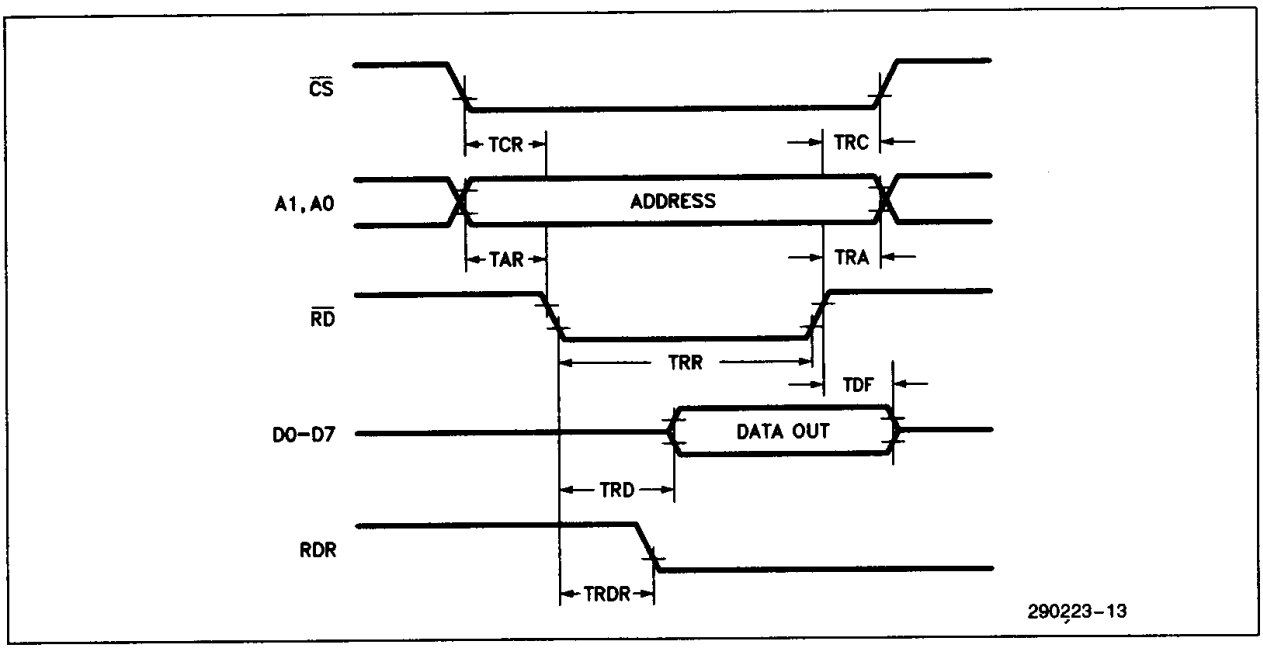


Figure 11. Microprocessor Bus Read Cycle Timing

MICROPROCESSOR BUS READ CYCLE TIMING

Symbol	Parameter	Min	Max	Units
TCR	$\overline{CS}$ Setup before $\overline{RD}$ Falling Edge	30		ns
TAR	Address Setup before $\overline{RD}$ Falling Edge	30		ns
TRR	$\overline{RD}$ Width	125	2000	ns
TRD	$\overline{RD}$ Low to Valid Data Out		100	ns
TRDR	$\overline{RD}$ Low to RDR Low		90	ns
TDF	Data Float after $\overline{RD}$ Rising Edge		60	ns
TRA	Address Hold after $\overline{RD}$ Rising Edge	20		ns
TRC	$\overline{CS}$ Hold after $\overline{RD}$ Rising Edge	20		ns

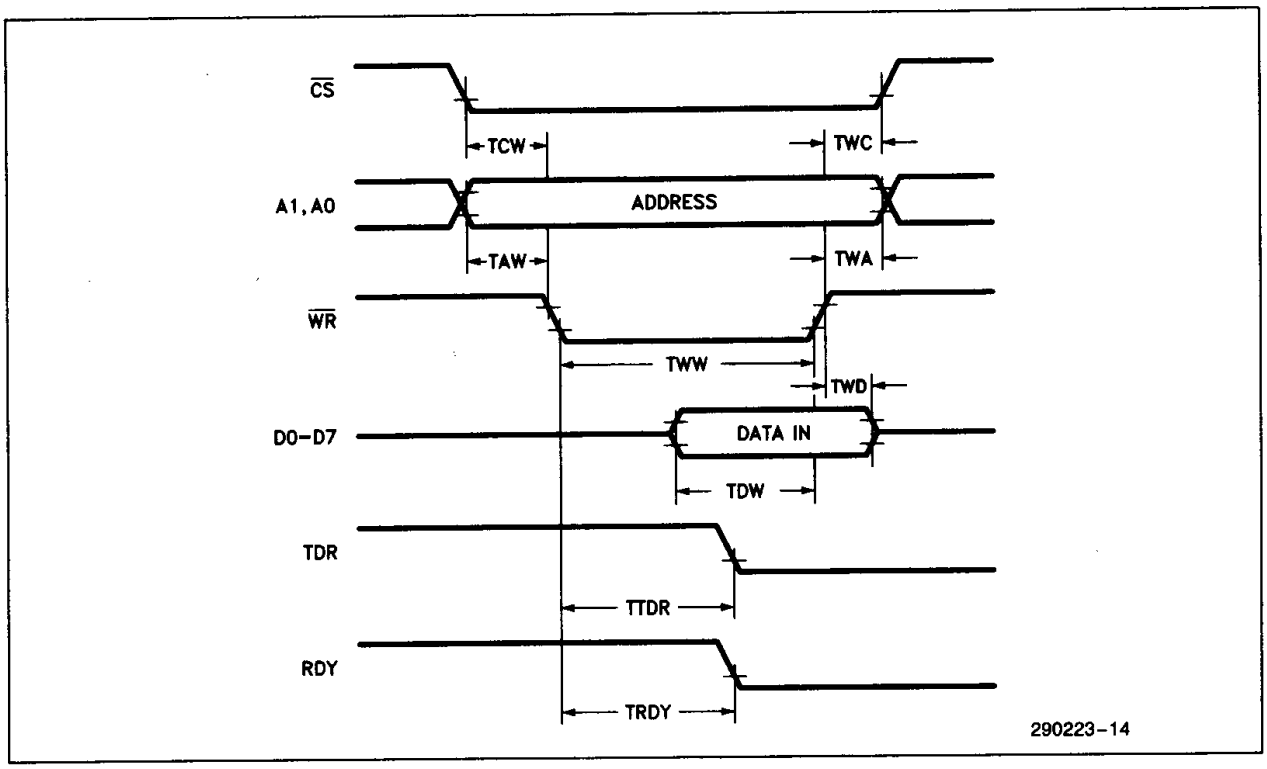


Figure 12. Microprocessor Bus Write Cycle Timing

MICROPROCESSOR BUS WRITE CYCLE TIMING

Symbol	Parameter	Min	Max	Units
TCW	$\overline{CS}$ Setup before $\overline{WR}$ Falling Edge	30		ns
TAW	Address Setup before $\overline{WR}$ Falling Edge	30		ns
TWW	$\overline{WR}$ Width	125	2000	ns
TTDR	$\overline{WR}$ Low to TDR Low		90	ns
TRDY	$\overline{WR}$ Low to RDY Low		90	ns
TDW	Data Setup before $\overline{WR}$ Rising Edge	65		ns
TWD	Data Hold after $\overline{WR}$ Rising Edge	15		ns
TWA	Address Hold after $\overline{WR}$ Rising Edge	20		ns
TWC	$\overline{CS}$ Hold after $\overline{WR}$ Rising Edge	20		ns

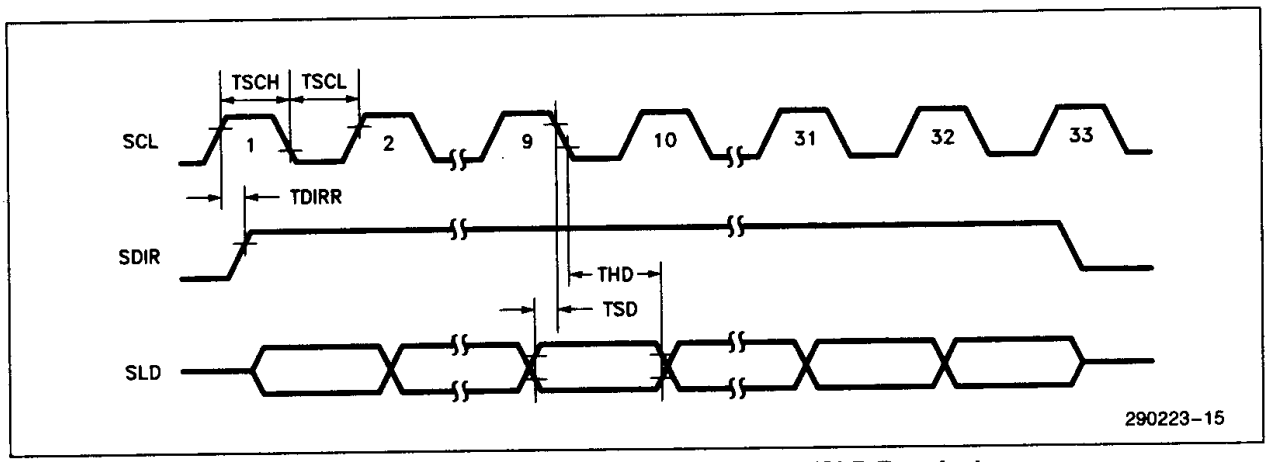


Figure 13. Serial Network Interface Timing (SLD Receive)

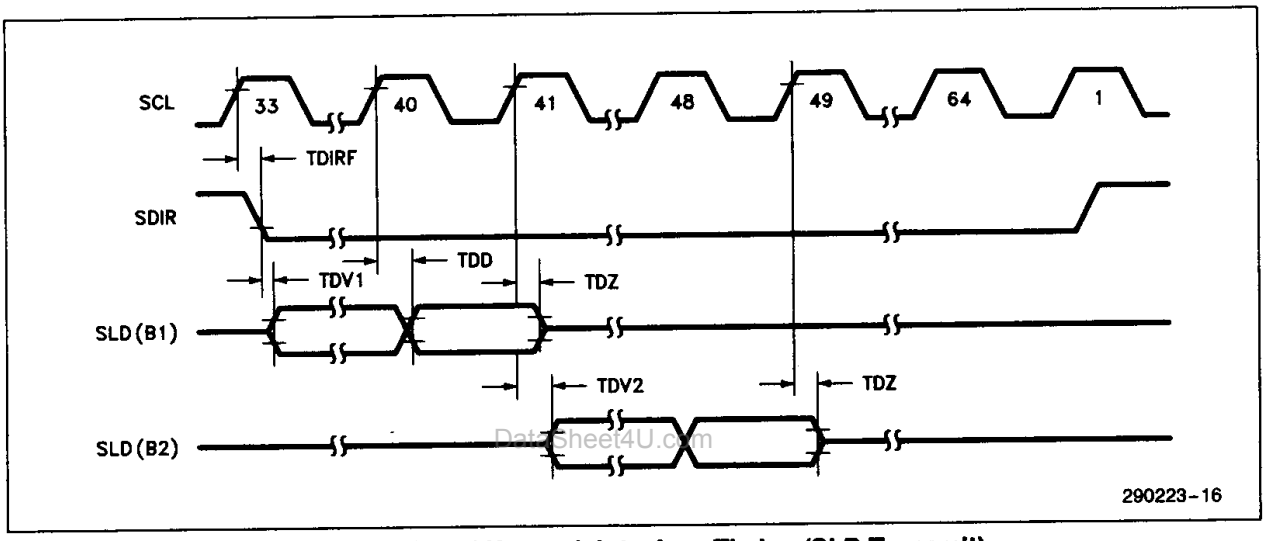


Figure 14. Serial Network Interface Timing (SLD Transmit)

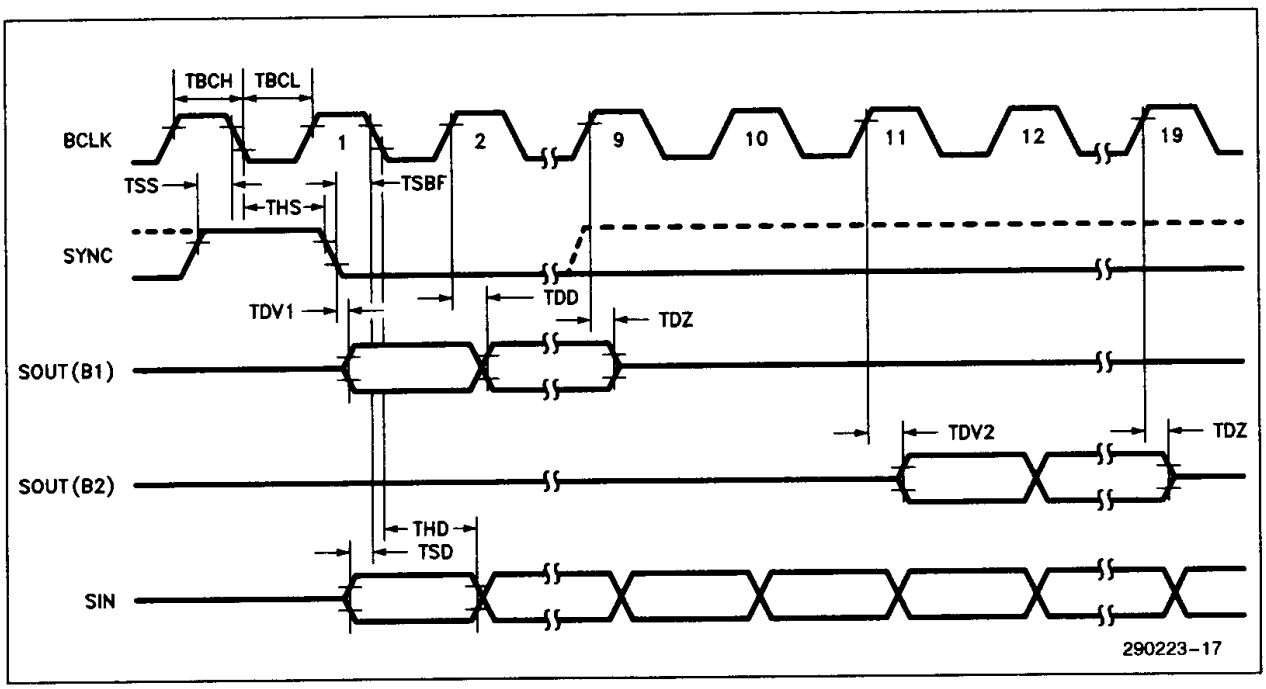


Figure 15. Serial Network Interface Timing (IDL)

SERIAL NETWORK INTERFACE TIMING

Symbol	Parameter	Min	Max	Units
TSCH	SCL High Time	586	1367	ns
TSCL	SCL Low Time	586	1367	ns
	SCL Duty Cycle	30	70	%
TDIRR	SCL to SDIR Rising Edge	−400	+400	ns
TSD	SLD/SIN Setup before SCL/BCLK Falling Edge	30		ns
THD	SLD/SIN Hold after SCL/BCLK Falling Edge	30		ns
TDIRF	SCL to SDIR Falling Edge	−400	+400	ns
TDV1	SDIR/SYNC to SLD/SOUT Active	0	100	ns
TDD	SCL/BCLK to SLD/SOUT Delay	0	100	ns
TDZ	SLD/SOUT Float after SCL/BCLK Rising Edge	0	50	ns
TDV2	SCL/BCLK to SLD/SOUT Active	0	100	ns
	BCLK Frequency	64	2560	KHz
TBCH	BCLK High Time	160(1)	9375(2)	ns
TBCL	BCLK Low Time	160(1)	9375(2)	ns
	BCLK Duty Cycle	40	60	%
TSS	SYNC Setup before BCLK Falling Edge	50		ns
THS	SYNC Hold after BCLK Falling Edge	50		ns
TSBF	SYNC to BCLK Falling Edge	120		ns

NOTES:
1. Minimum TBCH and TBCL are for a BCLK frequency of 2560 KHz.
2. Maximum TBCH and TBCL are for a BCLK frequency of 64 KHz.

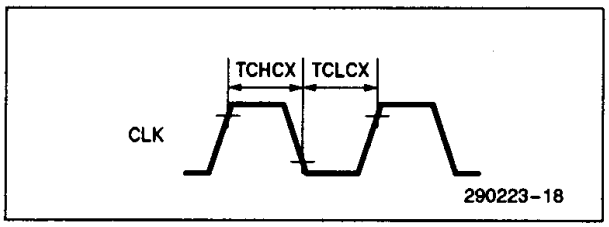
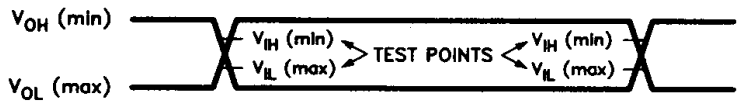


Figure 16. System Clock Waveform

SYSTEM CLOCK

Symbol	Parameter	Min	Max	Units
TCHCX	CLK High Time	37	46	ns
TCLCX	CLK Low Time	37	46	ns
	CLK Frequency		12.000	MHz

NOTE:
1. The frequency of the system clock input on the CLK pin must be 12.000 MHz ±100 ppm.



A.C. Testing: Inputs are driven at V_{OH} min. for a logic "1" and V_{OL} max. for a logic "0". Timing measurements are made at V_{IH} min. for a logic "1" and V_{IL} max. for a logic "0".

Figure 17. A.C. Testing Input, Output Waveform