

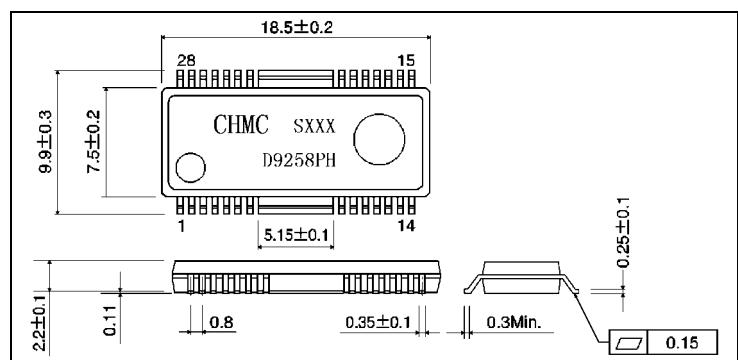


4-CH MOTOR DRIVER D9258PH

DESCRIPTION

The D9258PH is a monolithic integrated circuit, and suitable for 4-CH motor driver which drives tracking actuator, focus actuator, sled motor and loading motor of CD/CD-ROM/DVD system, and can also drive spindle motor of CD system.

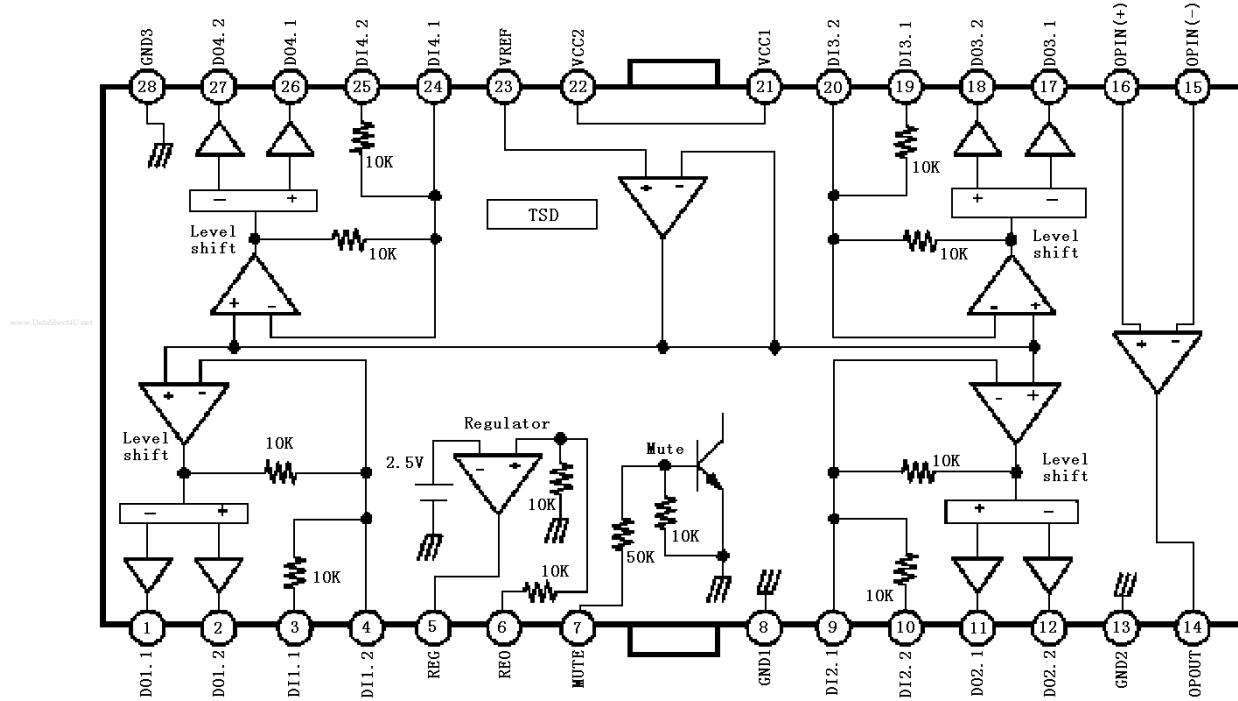
Outline Drawing



FEATURE

- 1-phase, full-wave, linear DC motor driver
- Output gain adjustable
- Built in OP-amp
- Built in mute function
- Built in level shift circuit
- Built in thermal shutdown function
- Operating range 6~13.2V

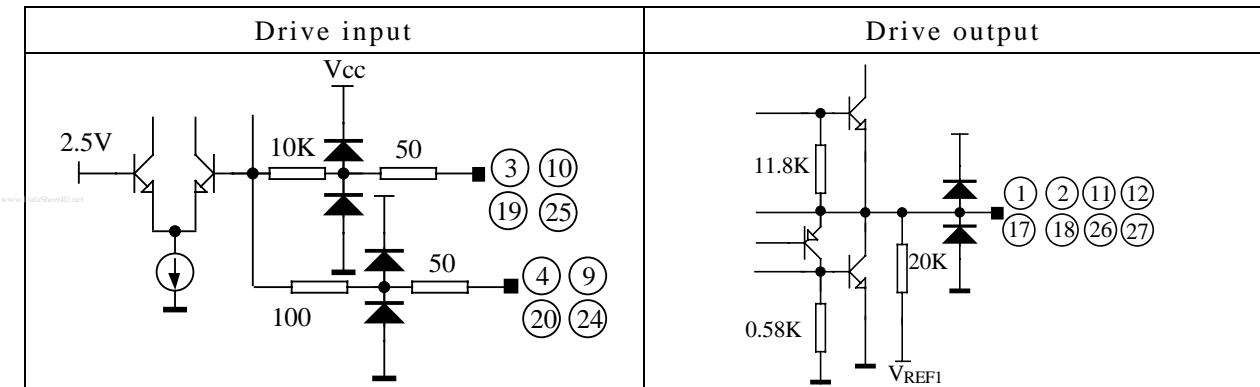
BLOCK DIAGRAM AND PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	DO1.1	O	Drive output	15	OPIN(-)	I	Op-amp input(-)
2	DO1.2	O	Drive output	16	OPIN(+)	I	Op-amp input(+)
3	DI1.1	I	Drive input	17	DO3.1	O	Drive output
4	DI1.2	I	Drive input	18	DO3.2	O	Drive output
5	REG	-	Regulator	19	DI3.1	I	Drive input
6	REO	O	Regulator output	20	DI3.2	I	Drive input
7	MUTE	I	Mute	21	Vcc1		Supply voltage
8	GND1	-	Ground 1	22	Vcc2		Supply voltage
9	DI2.1	I	Drive input	23	V _{REF}	I	2.5V bias voltage
10	DI2.2	I	Drive input	24	DI4.1	I	Drive input
11	DO2.1	O	Drive output	25	DI4.2	I	Drive input
12	DO2.2	O	Drive output	26	DO4.1	O	Drive output
13	GND2	-	Ground 2	27	DO4.2	O	Drive output
14	OPOUT	O	Op-amp output	28	GND3		Ground 3

EQUIVALENT CIRCUITS



EQUIVALENT CIRCUITS

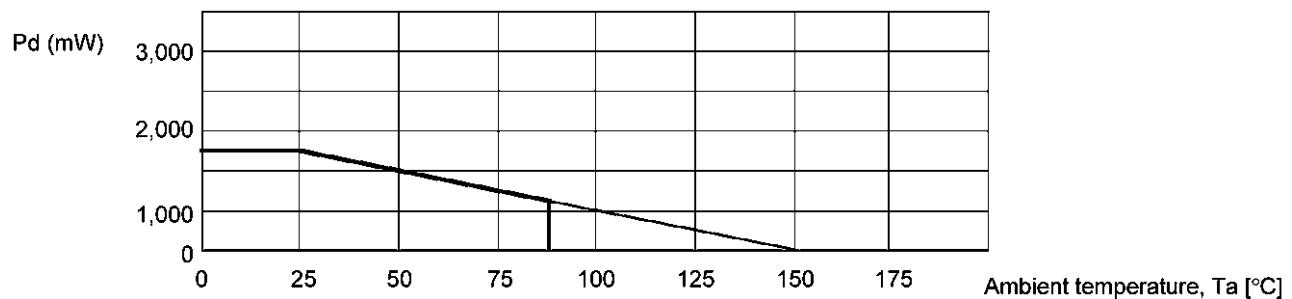
Regulator	Regulator output
Mute input	Bias input
Op-amp input	Op-amp output

ABSOLUTE MAXIMUM RATING (Ta=25°C)

Characteristics	Symbol	Value	Unit
Supply voltage	V _{CC}	15	V
Power dissipation	P _D	1.7(note)	W
Operating temperature	T _{OPR}	-40~+85	°C
Storage temperature	T _{STG}	-55~150	°C
Maximum output current	I _{OMAX}	1	A

Note:

1. When mounted on 76.2mm × 114mm × 1.57mm PCB (Phenolic resin material).
2. Power dissipation reduces 13.6mW / °C for using above Ta=25°C
3. Do not exceed Pd and SOA.

**RECOMMENDED OPERATING CONDITION (Ta=25°C)**

Characteristics	Symbol	Value	Unit
Operating supply voltage	V _{OVR}	6~13.2	V

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ELECTRICAL CHARACTERISTICS(unless otherwise specified: Ta=25°C, V_{CC}=8V)

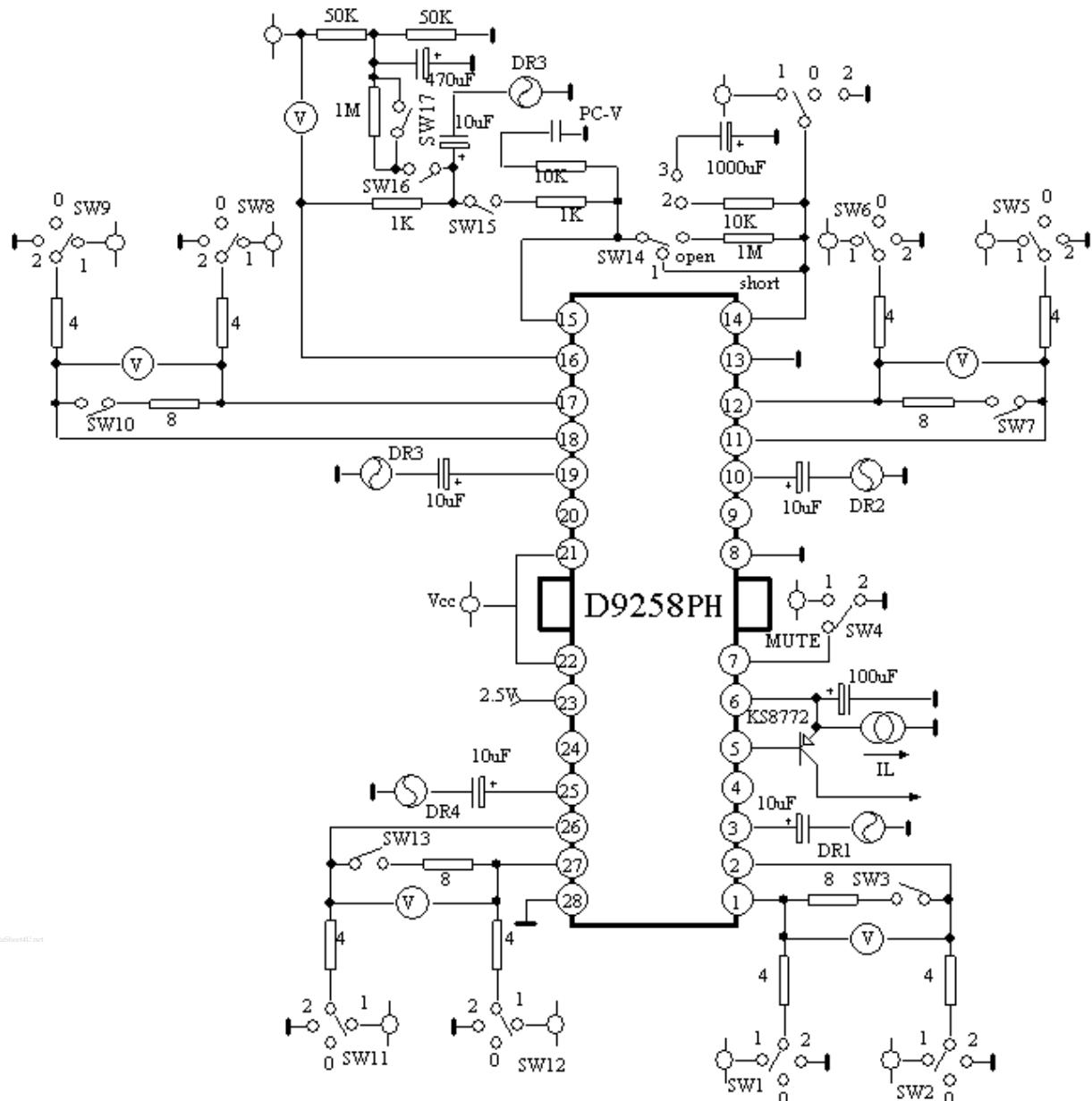
Characteristics	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Regulator part						
Regulator output voltage	I _L =100mA	V _{REG}	3.15	3.3	3.45	V
Load regulation	I _L =0~200mA	ΔV _{RL}	-40.0	0	10.0	mV
Line regulation	I _L =200mA, V _{CC} =6~9V	ΔV _{CC}	-10	0	20.0	mV

ELECTRICAL CHARACTERISTICS

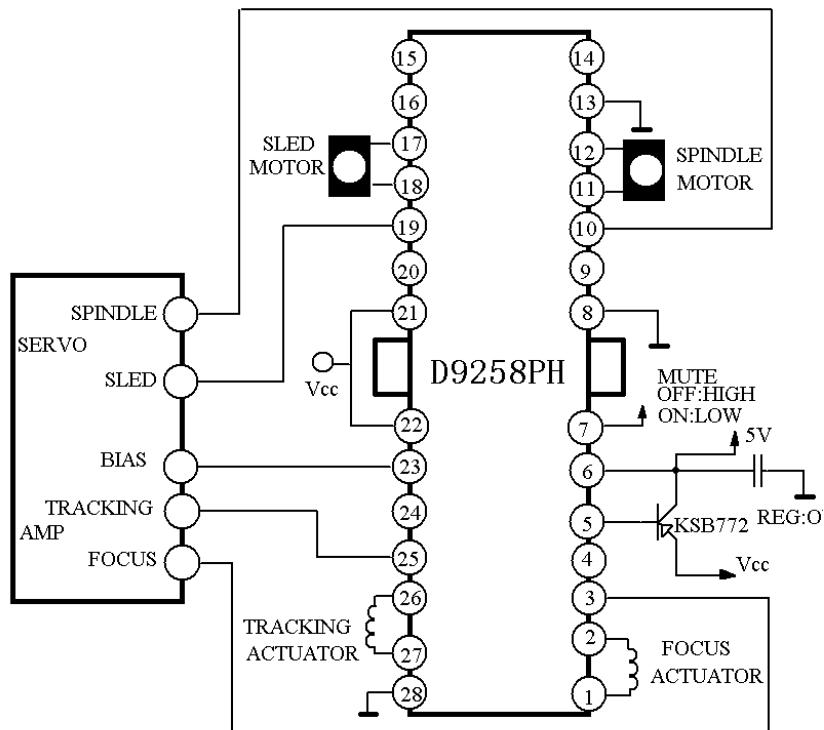
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Characteristics	Test conditions	Symbol	Min.	Typ.	Max.	Unit
Drive part						
Quiescent circuit current	Vi=0	I _{CCQ}	5.5	9.5	13.5	mA
Input bias current	Vi=0	I _{BOP}			300	nA
Input offset voltage		V _{OFO}	-5.0	0	5.0	mV
Output offset voltage		V _{OO}	-30	0	30	
Maximum sink current	R _L =4Ω, V _{cc}	I _{SINK}	0.5	0.8		A
Maximum source current	R _L =4Ω, GND	I _{SOURCE}	0.5	0.8		
Maximum output voltage	Vi=2VRMS, 1kHz	V _{OM}	2.5	3.0		V
Closed loop voltage gain	Vi=0.1VRMS, 1kHz	A _{VF}	4.5	6.5	7.5	dB
Ripple rejection ratio	Vi=-20dB, 120Hz	RR	60	80		
Slew rate	100Hz, Square wave	SR	1.0	2.0		V/μs
OP-amp part						
Input offset voltage		V _{OF1}	-5		5	mV
Input bias current		I _{B1}			300	nA
High level output voltage		V _{OH1}	6			V
Low level output voltage		V _{OL1}			1.8	V
Output sink current	R _L =50Ω, V _{cc}	I _{SINK1}	10	40		mA
Output source current	R _L =50Ω, GND	I _{SOURCE1}	10	50		mA
Open loop voltage gain	V _{in} =-75dB, f=1kHz	G _{vo1}	65	78		dB
Ripple rejection ratio	V _{in} =-20dB, f=120kHz	RR1	50	70		dB
Slew Rate	Square, V _{out} =2Vpp, f=120kHz	SR1	0.5	1		V/μs
Common mode rejection ratio	V _{in} =-20dB, f=1kHz	CMRR1	70	84		dB

TEST CIRCUIT



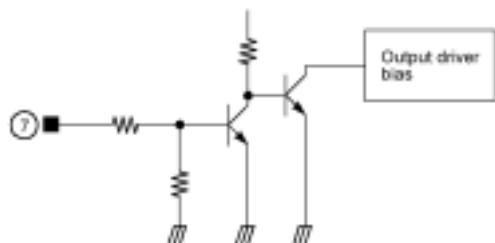
APPLICATION CIRCUIT



APPLICATION INFORMATION

1. MUTE

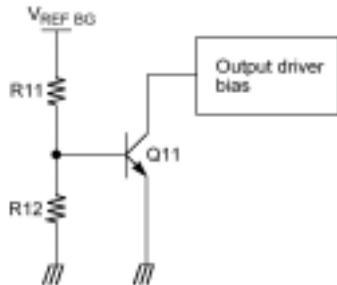
Pin#7	Mute circuit
High	Turn-off
Low	Turn-on
Open	Turn-on



- When the mute pin #7 is open or the voltage of the mute pin #7 is below 0.5V, the mute circuit is activated so that the output circuit will be muted.
- When the voltage of the mute pin is above 2V, the mute circuit is stopped and the output circuit is operated normally.
- If the chip temperature rises above 175°C, then the TSD (Thermal Shutdown)

circuit is activated and the output circuit is muted.

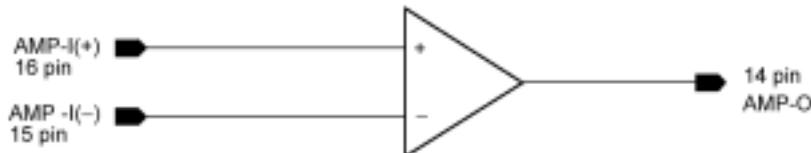
2. TSD (THERMAL SHUTDOWN)



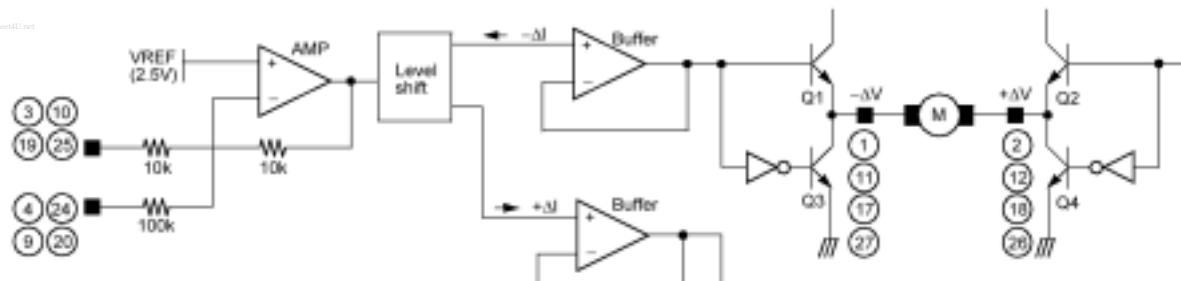
- The V_{REF BG} is the output voltage of the band-gap-referenced biasing circuit and acts as the input voltage of the TSD circuit.
- The base-emitter voltage of the TR, Q11 is designed to turn-on at below voltage.
 $V_{BE} = V_{REF\ BG} \times R12 / (R11 + R12) = 460\text{mV}$
- When the chip temperature rises up to 175°C, then the turn-on voltage of the Q11 would drop down to 460mV. (Hysteresis: 25°C)
 Hence, the Q11 would turn on so the output circuit will be muted.

3. OP-AMP

OP-amp is integrated in the IC for user convenience.



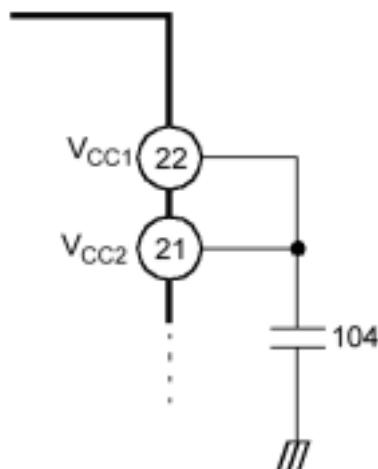
4. DRIVER



- The voltage, V_{REF}, is the reference voltage given by the bias voltage of the pin #23.
- The input signal through the pin #3 is amplified by 10k/10k times and then fed to

the level shift.

- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as $+\Delta I$ and $-\Delta I$ is fed into the driver buffer.
 - Driver Buffer operates the power TR of the output stage according to the state of the input signal.
 - The output stage is the BTL driver and the motor is rotating in forward direction by operating TR Q1 and TR Q4. On the other hand, if TR Q2 and TR Q3 is operating, the motor is rotating in reverse direction
 - When the input voltage through the pin #3 is below the V_{REF}, then the direction of the motor in forward direction.
 - When the input voltage through the pin #3 is above the V_{REF}, then the direction of the motor in reverse direction.
 - If it is desired to change the gain, then the pin #4 or #24 can be used.
5. Connect a by-pass capacitor, $0.1\mu F$ between the supply voltage source.

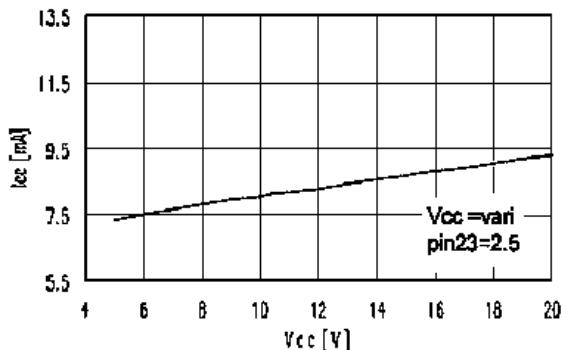


6. Radiation fin is connecting to the internal GND of the package.

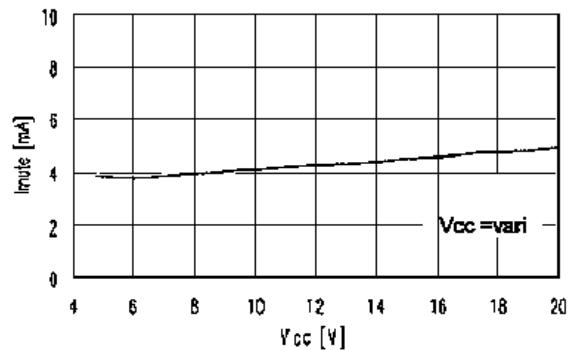
Connect the fin to the external GND.

CHARACTERISTICS CURVES

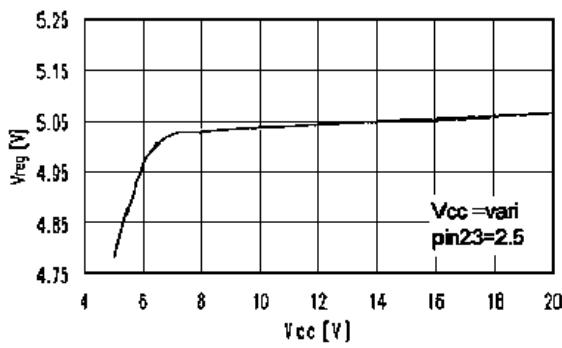
V_{CC} vs. I_{CC}



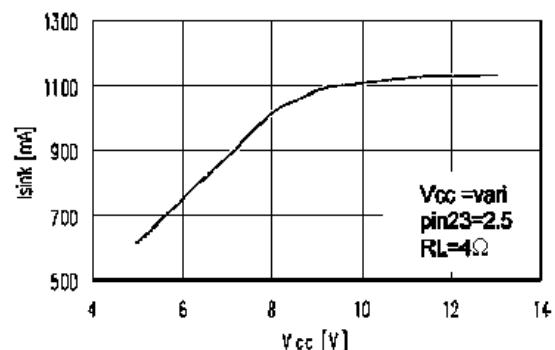
V_{CC} vs. I_{olute}



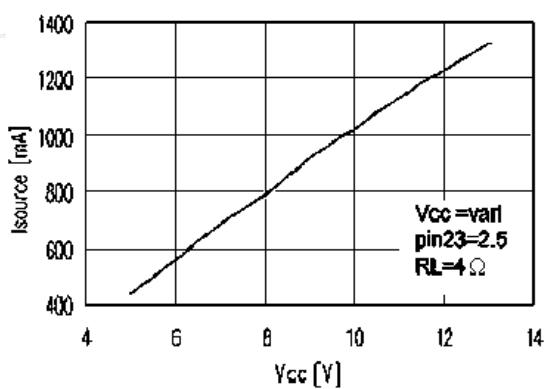
V_{CC} vs. V_{reg}



V_{CC} vs. I_{sink}



V_{CC} vs. I_{source}



V_{CC} vs. Avf

