System PMIC with high efficiency USB power manager

General description

The DA9021/22 family is a highly integrated PMIC subsystem with supply domains to support a wide range of application processors, associated peripherals, and user interface functions. Combining a switched-mode USB compatible charger, full power-path management, three bucks, five linear regulators and support for multiple sleep modes, the DA9021 offers an energy-optimised solution suitable for portable handheld, wireless and, infotainment applications.

DA9021/22 comes in a 4 x 4 mm, 64-bump, WLCSP package making it ideal for space constrained applications.

The high-efficiency Li-Ion/Polymer switching charger supports precise current/voltage charging as well as pre-charge and USB modes without processor interaction. During charging, the die temperature is thermally regulated enabling high-capacity batteries to be rapidly charged at currents up to 1.26 A with minimum thermal impact to space-constrained PCBs.

DA9021 offers a merged buck configuration for a combined 1.6 A or DA9022 offers a higher voltage capability on one DC-DC buck converter which is ideal for peripherals and memory running up to 3.6 V. USB suspend mode operation is supported and, for robustness, the power input is protected against over-voltage conditions.

The internally generated system power rail supports power scenarios such as instant-on with a fully discharged battery.

The power efficiency and flexibility of the switching DC-DC bucks is maintained to generate the various supply domains.

Controlled by a programmable digital power manager, the eight user-programmable switched/linear regulators may be configured to meet the start-up sequence, voltage, and timing requirements for most applications. The power manager includes supply-rail qualification and system reset management. For optimal processor energy-per-task performance, Dynamic Voltage Scaling (DVS) is available on up to four supply domains. Dialog's patented SmartMirror™ dynamic biasing is implemented on all linear regulators.

Key features

- Switched USB charger with power path management
- Three buck converters with DVC, 0.5 V to 3.6 V, up to 800 mA
- Five programmable LDOs, high PSRR, 1 % accuracy
- 32 kHz RTC oscillator
- An integrated 7-channel general purpose ADC
- 9-bit GPIO bus for enhanced wakeup and peripheral control
- HS2-wire and 4-wire control interfaces
- Unique USB supply detection and charge current selection
- 64 WLCSP 4x4 mm, 0.5 mm pitch package

Applications

- Personal media players
- Smartphone handsets
- Personal navigation devices
- Consumer infotainment devices
- IoT

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1 Terms and definitions

ADC	Analog to Digital Converter
BCD	Binary Coded Decimal
CC	Constant Current
CV	Constant Voltage
DCCC	Dynamic Charger Current Control
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GND	Ground
GSM	Global System for Mobile Communication
IoT	Internet of Things
IRQ	Interrupt Request
LDO	Low Dropout Voltage Regulator
LED	Light Emitting Diode
NTC	Negative Temperature Coefficient
OTP	One Time Programmable
OV	Overvoltage
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMIC	Power Management Integrated Circuit
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RTC	Real Time Clock
TDMA	Time Division Multiple Access
TRC	Trimming Release Code
USB	Universal Serial Bus
WLCSP	Wafer Level Chip Scale Package

2 Block diagram

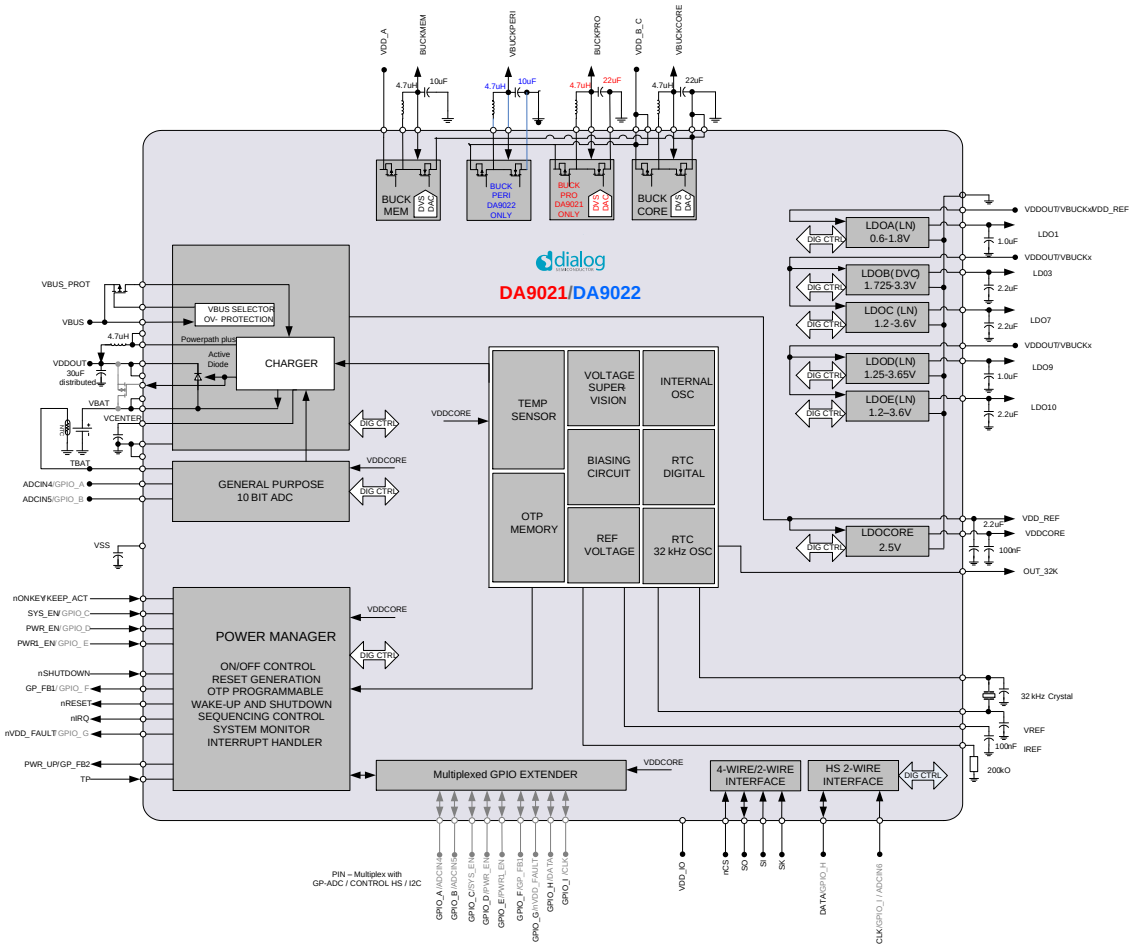


Figure 1: Block diagram

3 Generated supply domains

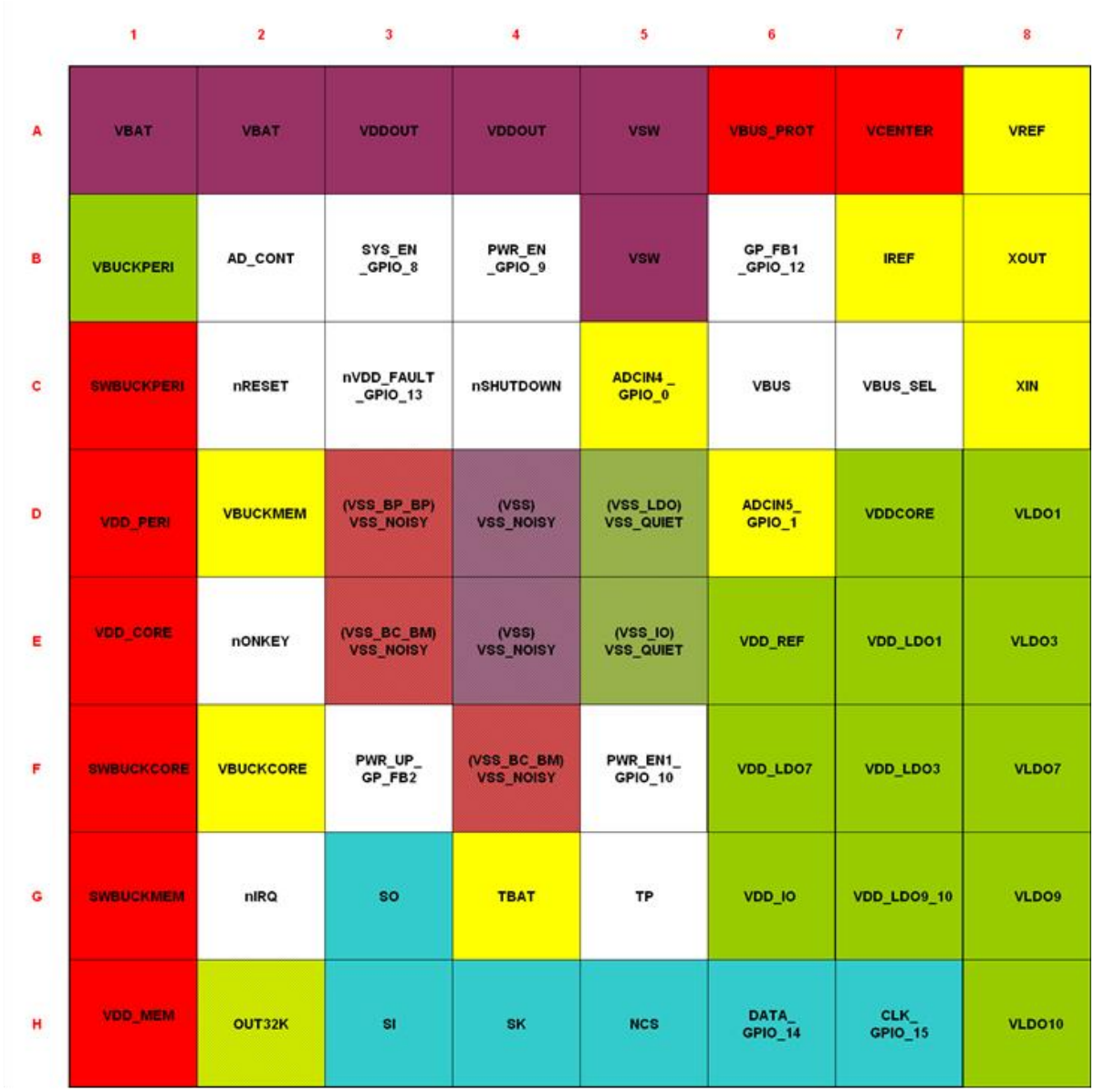
The default voltages in Table 1 indicate the voltages obtained from an un-programmed device.

Table 1: Regulator overview

Regulator	Supplied voltage	Supplied max. current (mA)	External component	Notes
BUCKCORE	0.5 V to 2.075 V ±3 % accuracy default 1.8 V	700	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off
		800		Between DVC transitions
BUCKPRO **DA9021** only	0.5 V to 2.075 V ±3 % accuracy default 1.2 V	700	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
		800		Between DVC transitions
BUCKPERI **DA9022** only	1.8 V to 3.6 V ±3 % accuracy default 3.3 V	650	2.2 µH to 4.7 µH	2 MHz, 50 or 100 mV steps At low input voltages the buck switches to a follower mode (100 % duty cycle), second output with sequencer controllable switch
		750		< 2.1 V
BUCKMEM	0.95 V to 2.525 V ±3 % accuracy default 2.0 V	650	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
		750		< 2.075 V and between DVC transitions
LDO1	0.6 V to 1.8 V ±3 % accuracy default 1.2 V	40	1.0 µF	High PSSR, low noise LDO, 50 mV steps, pull-down resistor switch off
LDO3	1.725 V to 3.3 V ±3 % accuracy default 2.85 V	200	2.2 µF	DVC, digital LDO, 25 mV steps, DVC with controlled slew rate
LDO7	1.2 V to 3.6 V ±3% accuracy default 3.1 V	200	2.2 µF	High PSRR, low noise, 50 mV steps
LDO9	1.25 V to 3.6 V ±1 % accuracy default 2.5 V	100	1.0 µF	High PSRR, low noise, 50 mV steps, OTP trimmed, optional hardware control, common supply with LDOE
LDO10	1.2 V to 3.6 V ±3 % accuracy default 1.8 V	250	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDOD
LDOCORE	2.5 V ±2 % accuracy	4	100 nF	Not for external use

4 Pad description

Figure 2: PCB board DA9021 pad arrangement (view from the top)



	1	2	3	4	5	6	7	8
A	VBAT	VBAT	VDDOUT	VDDOUT	VSW	VBUS_PROT	VCENTER	VREF
B	VBUCKPERI	AD_CONT	SYS_EN _GPIO_8	PWR_EN _GPIO_9	VSW	GP_FB1 _GPIO_12	IREF	XOUT
C	SWBUCKPERI	nRESET	nVDD_FAULT _GPIO_13	nSHUTDOWN	ADCIN4 _ GPIO_0	VBUS	VBUS_SEL	XIN
D	VDD_PERI	VBUCKMEM	(VSS_BP_BP) VSS_NOISY	(VSS) VSS_NOISY	(VSS_LDO) VSS_QUIET	ADCIN5_ GPIO_1	VDDCORE	VLDO1
E	VDD_CORE	nONKEY	(VSS_BC_BM) VSS_NOISY	(VSS) VSS_NOISY	(VSS_IO) VSS_QUIET	VDD_REF	VDD_LDO1	VLDO3
F	SWBUCKCORE	VBUCKCORE	PWR_UP_ GP_FB2	(VSS_BC_BM) VSS_NOISY	PWR_EN1_ GPIO_10	VDD_LDO7	VDD_LDO3	VLDO7
G	SWBUCKMEM	nIRQ	SO	TBAT	TP	VDD_IO	VDD_LDO9_10	VLDO9
H	VDD_MEM	OUT32K	SI	SK	NCS	DATA_ GPIO_14	CLK_ GPIO_15	VLDO10

Figure 3: PCB board DA9022 pad arrangement (view from the top)

Figure 4: Pad arrangement colour key

Table 2: Pin description for DA9021

Pin no.	Pin name	Type (Table 4)	Description
Power manager			
E2	nONKEY	DI	On/off key with optional long press shutdown
B3	SYS_EN	DI/DIO	Hardware enable of power domain SYSTEM/GPIO_8
B4	PWR_EN	DI/DIO	Hardware enable of power domain POWER/GPIO_9
F5	PWR1_EN	DI/DIO	Hardware enable of power domain POWER1/GPIO_10 with high power output and blinking feature, input for power sequencer WAIT ID
C4	nSHUTDOWN	DI	Active low input from switch or error indication line from host to initiate shutdown
C2	nRESET	DO	Active low RESET towards host
B6	GP_FB1	DO/DIO	Status indication towards host for a valid wakeup event (EXT_WAKEUP) or indicator for ongoing power mode transition (READY) /GPIO_12, enables hardware control of LDO9
G2	nIRQ	DO	Active low IRQ line towards host
C3	nVDD_FAULT	DO/DIO	Active low indication for low supply voltage/GPIO_13
F3	PWR_UP	DO/DO	Sequencer status indicator: All POWER IDs powered up (PWR_UP) or programmable level controlled from the power sequencer (GP_FB2)
G6	VDD_IO	PS	Supply I/O voltage rail

Pin no.	Pin name	Type (Table 4)	Description
G5	TP	DIO	Test pin, enables POWER COMMANDER boot mode
4-/2-wire interfaces			
G3	SO	DIO	4-wire data output or 2-wire data
H3	SI	DI	4-wire data input
H4	SK	DI	4-wire/2-wire clock
H4	nCS	DI	4-wire chip select
H6	DATA	DIO	HS-2-wire Data/GPIO_14 (enables reset if long press in parallel with GPI15) with high-power output and PWM LED control
H7	CLK	DI	HS-2-wire Clock/GPIO_15 (enables reset if long press in parallel with GPI14) with high-power output and PWM LED control
Voltage regulators			
D8	VLDO1	AO	Output voltage from LDO1
E7	VDD_LDO1	PS	Supply voltage for LDO1
E8	VLDO3	AO	Output voltage from LDO3
F7	VDD_LDO3	PS	Supply voltage for LDO3
F8	VLDO7	AO	Output voltage from LDO7
F6	VDD_LDO7	PS	Supply voltage for LDO7
G8	VLDO9	AO	Output voltage from LDO9
H8	VLDO10	AO	Output voltage from LDO10
G7	VDD_LDO9_10	PS	Supply voltage for LDO9 and LDO10
D7	VDDCORE	AO	Supply for internal circuitry
E6	VDD_REF	AO	Switched supply from VBAT or VBUS
DC-DC buck converters			
F2	VBUCKCORE	AI	Sense node for DVC DC-DC BUCKCORE
F1	SWBUCKCORE	AO	Switching node for BUCKCORE to be connected to SWBUCKPRO for buck merge
B1	VBUCKPRO	AI	Sense node for DVC DC-DC BUCKPRO
C1	SWBUCKPRO	AO	Switching node for BUCKPRO to be connected to SWBUCKCORE for buck merge
D2	VBUCKMEM	AI	Sense node for DVC DC-DC BUCKMEM
G1	SWBUCKMEM	AO	Switching node for BUCKMEM
D1	VDD_COR_PRO	PS	Supply voltage for BUCKCORE and BUCKPRO to be connected to VDDOUT
E1	VDD_COR_PRO	PS	Supply voltage for BUCKCORE and BUCKPRO to be connected to VDDOUT
H1	VDD_MEM	PS	Supply voltage for BUCKMEM to be connected to VDDOUT

Pin no.	Pin name	Type (Table 4)	Description
Reference voltage generation			
A8	VREF	AIO	Reference voltage output Decouple with 100 nF
B7	IREF	AO	Connection for bias setting Configure with high precision 200 kΩ resistor
Internal oscillator			
C8	XIN	AIO	32 kHz crystal connection Adjust with 10 pF
B8	XOUT	AIO	32 kHz crystal connection Adjust with 10 pF
H2	OUT_32K	DO	32 kHz oscillator buffer output
Charger			
C7	VBUS_SEL	AO	Control for external over voltage protection and input selection of VBUS To be connected to gate of PFET
A6	VBUS_PROT	PS	Overvoltage protected VBUS charger input
C6	VBUS	PS	USB or wall charger input
A7	VCENTER	PS	Protected input for switching charger (decouple with 10 µF)
A5	VSW	PS	Switching node for charger buck
B5	VSW	PS	Switching node for charger buck
A3	VDDOUT	PS	System power supply output
A4	VDDOUT	PS	System power supply output
B2	AD_CONT	AO	Active diode controller output To be connected to gate of PFET (leave unconnected, if not used)
A1	VBAT	PS	Connection to main battery
A2	VBAT	PS	Connection to main battery
General purpose ADC			
G4	TBAT	AIO	Connection to battery NTC resistor
C5	ADCIN4	AI/DIO	Connection to GP ADC auto channel 4 with threshold IRQ and resistor measurement option/GPIO_0
D6	ADCIN5	AI/DIO	Connection to GP ADC channel 5 with 1.2 V hardware comparator IRQ/GPIO_1, enables hardware control of LDO4
VSS			
D5	GND	VSS_QUIET	VSS_LDO
E5	GND	VSS_QUIET	VSS_IO
D3	GND	VSS_NOISY	VSS_BP_BP
D4	GND	VSS_NOISY	VSS
E3	GND	VSS_NOISY	VSS_BC_BM
E4	GND	VSS_NOISY	VSS
F4	GND	VSS	VSS_BC_BM

Table 3: Pin description for DA9022

Pin no.	Pin name	Type (Table 4)	Description
Power manager			
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C4	nSHUTDOWN	DI	Active low input from switch or error indication line from host to initiate shutdown
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B6	GP_FB1	DO/DIO	Status indication towards host for a valid wakeup event (EXT_WAKEUP) or indicator for ongoing power mode transition (READY) /GPIO_12, enables hardware control of LDO9
G2	nIRQ	DO	Active low IRQ line towards host
C3	nVDD_FAULT	DO/DIO	Active low indication for low supply voltage/GPIO_13
F3	PWR_UP	DO/DO	Sequencer status indicator: All POWER IDs powered up (PWR_UP) or programmable level controlled from the power sequencer (GP_FB2)
G6	VDD_IO	PS	Supply I/O voltage rail
G5	TP	DIO	Test pin, enables POWER COMMANDER boot mode
4-/2-wire interfaces			
G3	SO	DIO	4-wire data output or 2-wire data
H3	SI	DI	4-wire data input
H4	SK	DI	4-wire/2-wire clock
H4	nCS	DI	4-wire chip select
H6	DATA	DIO	HS-2-wire Data/GPIO_14 (enables reset if long press in parallel with GPI15) with high-power output and PWM LED control
H7	CLK	DI	HS-2-wire Clock/GPIO_15 (enables reset if long press in parallel with GPI14) with high-power output and PWM LED control
Voltage regulators			
D8	VLDO1	AO	Output voltage from LDO1
E7	VDD_LDO1	PS	Supply voltage for LDO1
E8	VLDO3	AO	Output voltage from LDO3
F7	VDD_LDO3	PS	Supply voltage for LDO3
F8	VLDO7	AO	Output voltage from LDO7
F6	VDD_LDO7	PS	Supply voltage for LDO7
G8	VLDO9	AO	Output voltage from LDO9
H8	VLDO10	AO	Output voltage from LDO10
G7	VDD_LDO9_10	PS	Supply voltage for LDO9 and LDO10
D7	VDDCORE	AO	Supply for internal circuitry
E6	VDD_REF	AO	Switched supply from VBAT or VBUS

Pin no.	Pin name	Type (Table 4)	Description
DC-DC buck converters			
F2	VBUCKCORE	AI	Sense node for DVC DC-DC BUCKCORE
F1	SWBUCKCORE	AO	Switching node for BUCKCORE to be connected to SWBUCKPERI for buck merge
B1	VBUCKPERI	AI	Sense node for DVC DC-DC VBUCKPERI
C1	SWVBUCKPERI	AO	Switching node for BUCKPERI to be connected to SWBUCKCORE for buck merge
D2	VBUCKMEM	AI	Sense node for DVC DC-DC BUCKMEM
G1	SWBUCKMEM	AO	Switching node for BUCKMEM
D1	VDD_PERI	PS	Supply voltage for BUCKPERI To be connected to VDDOUT
E1	VDD_COR	PS	Supply voltage for BUCKCORE To be connected to VDDOUT
H1	VDD_MEM	PS	Supply voltage for BUCKMEM To be connected to VDDOUT
Reference voltage generation			
A8	VREF	AIO	Reference voltage output
Decouple with 100 nF			
B7	IREF	AO	Connection for bias setting Configure with high precision 200 kΩ resistor
Internal oscillator			
C8	XIN	AIO	32 kHz crystal connection adjust with 10 pF
B8	XOUT	AIO	32 kHz crystal connection adjust with 10 pF
H2	OUT_32K	DO	32 kHz oscillator buffer output
Charger			
C7	VBUS_SEL	AO	Control for external overvoltage protection and input selection of VBUS To be connected to gate of PFET
A6	VBUS_PROT	PS	Overvoltage protected VBUS charger input
C6	VBUS	PS	USB or wall charger input
A7	VCENTER	PS	Protected input for switching charger (decouple with 10 µF)
A5	VSW	PS	Switching node for charger buck
B5	VSW	PS	Switching node for charger buck
A3	VDDOUT	PS	System power supply output
A4	VDDOUT	PS	System power supply output
B2	AD_CONT	AO	Active diode controller output To be connected to gate of PFET (leave unconnected, if not used)
A1	VBAT	PS	Connection to main battery
A2	VBAT	PS	Connection to main battery
General purpose ADC			
G4	TBAT	AIO	Connection to battery NTC resistor

Pin no.	Pin name	Type (Table 4)	Description
C5	ADCIN4	AI/DIO	Connection to GP ADC auto channel 4 with threshold IRQ and resistor measurement option/GPIO_0
D6	ADCIN5	AI/DIO	Connection to GP ADC channel 5 with 1.2 V hardware comparator IRQ/GPIO_1, enables hardware control of LDO4
VSS			
D5	GND		VSS_LDO
E5	GND		VSS_IO
D3	GND		VSS_BP_BP
D4	GND		VSS
E3	GND		VSS_BC_BM
E4	GND		VSS
F4	GND		VSS_BC_BM

Table 4: Pin type definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output Open Drain	BP	Backdrive Protection
PU	Fixed Pull-Up Resistor	SPU	Switchable Pull-Up Resistor
PD	Fixed Pull-Down Resistor	SPD	Switchable Pull-Down Resistor

5 Absolute maximum ratings

The maximum continuous charger voltage must be less than 5.5 V. The overvoltage protection (OVP) circuit will help protect against transients above this level minimising effects on operation lifetime.

VDDOUT must not be driven from an external supply if the charger buck is used.

Table 5: Absolute maximum ratings

Parameter	Symbol	Conditions (Note 1)	Min	Max	Unit
Storage temperature			-40	+95	°C
Operating temperature	Ta(max)		-25	+85	°C
Power supply Input	VBAT, VBUS_PROT, VDDOUT, VDD_REF		-0.3	5.5	V
Supply voltage charger	VBUS		-0.3	12	V
Supply voltage buck input pins			VDDOUT -0.3 V	VDDOUT + 0.3 V 5 V max.	V
Supply voltage all pins except listed above			-0.3	VDDOUT + 0.3 V 5 V max.	V
Maximum power dissipation				1.86	W
Package thermal resistance			Note 2	21.5	K/W
ESD susceptibility		Human body model		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 JEDEC 6 layer board, still air, influenced by PCB technology and layout. The numbers of supplies that can be used at the same time at maximum dissipation power is limited by the thermal resistance of the package and the PCB layout.

6 Recommended operating conditions

All voltages are referenced to VSS unless otherwise stated. Currents flowing into DA9021/22 are deemed positive, currents flowing out are deemed negative. All parameters are valid over the recommended temperature range and power supply range unless otherwise noted. Please note that the power dissipation must be limited to avoid overheating of DA9021/22. The maximum power dissipation should not be reached with maximum ambient temperature.

Table 6: Recommended operating conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-25		+70	°C
Supply voltage	VBAT		0		4.4	V
Supply voltage charger	VBUS		0		5.5	V
Supply voltage IO	VDD_IO		1.2		3.6 Note 1	V

Note 1 VDD_IO must not exceed VDDOUT.

7 Current consumption

Table 7: Current consumption

Operating mode	Conditions (Ta = 25 °C)	Min	Typ	Max	Unit
NO-POWER	Detection circuits running, oscillator off			15	µA
RESET	VDD_REF > 2.2 V, bucks and LDOs off (except LDOCORE), RTC unit on			45	µA
POWERDOWN (standby)	VDD_REF > 2.8 V, supplies off (except LDOCORE), all blocks in POWERDOWN mode, RTC unit on			45	µA
POWERDOWN (hibernate)	BUCKCORE, LDOCORE, enabled, RTC and GPIO on			155 Note 1	µA
ACTIVE	All supplies, GPIO, RTC and GPADC on			375	µA

Note 1 Enabled bucks are set to FORCED SLEEP mode setting ”00”

8 Electrical characteristics

8.1 Digital I/O characteristics

Table 8: Digital I/O (VDD_REF > 2.8 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GPI0 – GPI15, nONKEY, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN, CLK, DATA, Input High Voltage	VIH	VDDCORE mode VDD_IO mode	1.0 0.7*VDD_IO		VDDOUT	V
GPI0 – GPI15, nONKEY, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN CLK, DATA, Input Low Voltage	VIL	VDDCORE mode VDD_IO mode			0.4 0.3*VDD_IO	V
SK, nCS, SI Input High Voltage	VIL	VDDCORE mode VDD_IO mode	0.7*VDDCORE 0.7*VDD_IO		VDDOUT	V
SK, nCS, SI Input Low Voltage	VIH	VDDCORE mode VDD_IO mode	-0.3		0.3*VDD_IO	V
GPO0 – GPO15, nVDD_FAULT, SO nRESET, nIRQ, PWR_UP, GP_FB2, OUT_32K, Output High Voltage	VIH	VDD_IO mode	0.8*VDD_IO			
GPO0 – GPO15,DATA, SO, nRESET, nIRQ, (open drain mode) Output High Voltage	VIL	VDD_IO mode				V
GPO0 – GPO15,DATA, SO, nVDD_FAULT, nRESET nIRQ, PWR_UP, GP_FB2, OUT_32K Output Low Voltage	VOH @1 mA		0	Open drain	VDDOUT	V

8.2 GPIO characteristics

Table 9: GPIOs

Parameter	Conditions	Min	Typ	Max	Unit
Sink current capability GPO 14, 15	VGPIO = 0.1 V		30		mA
Sink current capability GPO 10,	VGPIO = 0.5 V		15		mA
Source current capability GPO 10, 14,15	VGPIO = 0.8 * VDD_IO		-4 Note 1		mA
Sink current capability GPO 0 to 9, 12 to 13	VGPIO = 0.3 V		1		mA
Source current capability GPO 0 to 9, 12 to 13	VGPIO = 0.8 * VDD_IO		-1 Note 2		mA
GPO pull-up resistor	= 1.5 V VDD_IO = 1.8 V = 3.3 V	100 60 25	180 120 40	340 175 60	kΩ

Note 1 For V_{SUPPLY} < 1.5 V the source current for min 0.8 * VDD is limited to 0.8 mA

Note 2 For V_{SUPPLY} < 1.5 V the source current for min 0.8 * VDD is limited to 0.5 mA

8.3 Power on reset characteristics

Table 10: Power on reset

Parameter	Symbol	Min	Typ	Max	Unit
Deep discharge lockout lower threshold	VPOR_LOWER		2.0		V
Deep discharge lockout upper threshold	VPOR_UPPER		2.3		V
Under voltage lower threshold	VDD_FAULT_LOWER	2.4	2.9	3.15	V
Under voltage lower threshold accuracy	VDD_FAULT_LOWER_ACCURACY		±2		%
Under voltage upper threshold	VDD_FAULT_UPPER		VDD_FAULT_LOWER + 0.15		V
Charger buck under voltage	VDDOUT_MIN	3.35	3.40	3.45	V

8.4 4-wire control bus

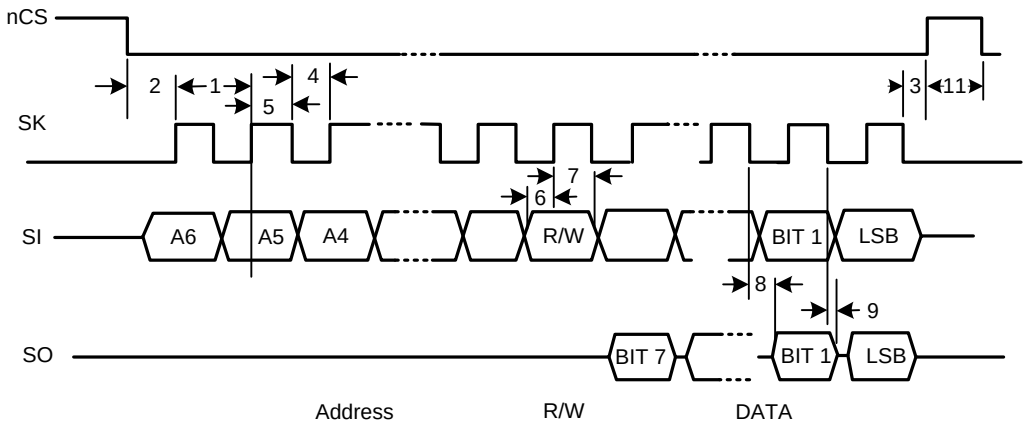

Figure 5: 4-wire control bus timing diagram

NOTE
The above timing is valid for active low and high CS

Table 11: 4-wire timing

Parameter	Symbol	Label in Figure 5	Min	Typ	Max	Unit
Cycle time	t_C	1	70			ns
Enable lead time	t_{CSS}	2, from CS active to first SK edge	20			ns
Enable lag time	t_{SCS}	3, from last SK edge to CS idle	20			ns
Clock low time	t_{CL}	4	0.4 * t_C			ns
Clock high time	t_{CH}	5	0.4 * t_C			ns
Data in setup time	t_{SIS}	6	5			ns
Data in hold time	t_{SIH}	7	5			ns
Data out valid time	t_{SOV}	8			22	ns
Data out hold time	t_{SOH}	9	6			ns
Data access time	t_H	10			22	ns

8.5 Oscillator characteristics

Table 12: Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal oscillator frequency		before trimming	1.4	2.0	2.6	MHz
		after trimming	1.9		2.1	

8.6 Reference voltage generation and temperature supervision

Table 13: Reference voltage generation and temperature supervision

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage	VREF Pin		-1.25 %	1.2	+1 %	V
VREF decoupling capacitor				100		nF
Reference current resistor	IREF Pin		-1 %	200	+1%	kΩ
Thermal shutdown	T_{OVER}		125	140	155	ºC
Charge current reduction	$T_{CHARGELOW}$		75	90	115	ºC
Charge suspend	$T_{CHARGESUSPEND}$		105	120	135	ºC
Hysteresis				10		ºC

8.7 LDO voltage regulators

8.7.1 LDO1

Table 14: LDO1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD	(power stage, if supplied from buck)	2.0 (1.5)		V_{DD_OUT} + 0.3 V 5 V max.	V
Output voltage	VLD01	$I_{OUT} = I_{MAX}$	0.6	Note 1	1.8	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3	Note 2	+3	%
Stabilisation capacitor	C_{OUT}	including voltage and temperature coefficient @ configured VLD01	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	40	Note 3		mA
Short circuit current	I_{SHORT}			80		mA
Dropout voltage	$V_{DROPOUT}$	VDD > 2.15 V I_{OUT}= I_{MAX} (VDD = 2.0 V I_{OUT} = 0.4 * I_{MAX} or VDD = 1.5 V I_{OUT} = 0.25 * I_{MAX})		200 100	350 150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	50	60		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 4		8 + 1.25 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LD01_PD_DIS		100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Sourced from LDOCORE band gap.

Note 3 Max. current is 10 mA if supplied from VDD_REF.

Note 4 Internal regulator current flowing to ground.

8.7.2 LDO3

Table 15: LDO3

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD	(if supplied from buck)	2.8 (1.9)		VDD_OUT + 0.3 V 5 V max	V
Output voltage	VLD03	I_{OUT} = I_{MAX}	1.725	Note 1	3.3	V
Output accuracy		I_{OUT} = I_{MAX}	-3		+3	%
Stabilisation capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLD03)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1MHz			0.1	Ω
Maximum output current	I_{MAX}				200	mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = I_{MAX} (for VDD = 1.9 V I_{OUT} = I_{MAX} *2/3)	100		150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 V to 5.0 V I_{OUT} = I_{MAX}		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = I_{MAX} t_r = t_f = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} t_r = t_f = 1 µs		20	50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 +0.3 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} – V D_{ROPOUT}.

Note 2 Internal regulator current flowing to ground

8.7.3 LDO7

Table 16: LDO7

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD	(if supplied from buck)	2.8 (1.5)		V_{DD_OUT} + 0.3 V 5 V max	V
Output voltage	VLD07	$I_{OUT} = I_{MAX}$	1.2	Note 1		V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilisation capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured output voltage)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		20	50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V I_{OUT} = I_{MAX}/2	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 +0.4 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			600	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD – $V_{DROPOUT}$.

Note 2 Internal regulator current flowing to ground

8.7.4 LDO9

Table 17: LDO9

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD	(if supplied from buck)	2.8 (1.5)		V_{DD_OUT} + 0.3 V 5 V max	V
Output voltage	VLD09	I_{OUT} = I_{MAX}	1.25	Note 1	3.6	V
Output accuracy		I_{OUT} = I_{MAX}	-1		+1	%
Stabilisation capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLD09)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = I_{MAX} (for VDD = 1.5 V I_{OUT} = I_{MAX}/3)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 V to 5.0 V I_{OUT} = I_{MAX}		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = I_{MAX} t_r = t_f = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} t_r = t_f = 1 µs		15	50	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V I_{OUT} = I_{MAX}/2	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 +0.7 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			200	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - $V_{DROPOUT}$.

Note 2 Internal regulator current flowing to ground.

8.7.5 LDO10

Table 18: LDO10

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD	(if supplied from buck)	2.8 (1.5)		V_{DD_OUT} + 0.3 V 5 V max	V
Output voltage	VLD010	I_{OUT} = I_{MAX}	1.2	Note 1	3.6	V
Output accuracy		I_{OUT} = I_{MAX}	-3		+3	%
Stabilisation capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO10)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	250			mA
Short circuit current	I_{SHORT}			500		mA
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = I_{MAX} (for VDD < 1.8 V I_{OUT} = I_{MAX}/3)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 V to 5.0 V I_{OUT} = I_{MAX}		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = I_{MAX} t_r = t_f = 10 µs		5	20	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		30	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 +0.3 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}	Note 2			1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV steps, maximum output voltage is determined by VDD - $V_{DROPOUT}$.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing.

8.7.6 LDOCORE

Table 19: LDOCORE (T_a = -25 ºC to +85 ºC)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage	VDDCORE	I_{OUT} = 0 mA to I_{MAX} (when supplied from VBAT)	2.45 2.15	2.5 2.2	2.55 2.25	V
Decoupling capacitor	C_{IN}	On VDD_REF	-35 %	220	+35 %	nF
Stabilisation capacitor	C_{OUT}	(including voltage and temperature coefficient @ 2.5 V)	-55 %	100	+35 %	nF
ESR resistance		f > 1 MHz			0.1	Ω
Dropout voltage	$V_{DROPOUT}$	I_{OUT} < 10 µA , FOLLOWER mode		0.05	0.1	V
Max output current	I_{MAX}		4			mA
Maximum quiescent current	IQ	POWERDOWN mode: I_{OUT} < 20 µA		13	17	µA

8.8 DC/DC buck converters

8.8.1 BUCKCORE

Table 20: BUCKCORE

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD		VDDOUT -0.3 V 2.8 V min		VDDOUT + 0.3 V 5 V max	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2 to 4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBCORE	I_{OUT} = I_{MAX}	0.725	Note 1	2.075	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 2	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		5		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA / 500 mA, dI/dt = 50 mA/µs		15	35	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 500 mA t_r=t_f=10 µs		3	8	mV
Output current	I_{MAX}	During DVC transitions Between DVC transitions	700 800 Note 3			mA
Current limit (programmable)	I_{LIM} Note 4	BUCKCORE_ILIM=00	-20 %	700	20 %	mA
		BUCKCORE_ILIM=01	-20 %	800	20 %	mA
		BUCKCORE_ILIM=10	-20 %	1000	20 %	mA
		BUCKCORE_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	f			2		MHz
Switching duty cycle			10		95	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via CORE_PD_DIS			200	Ω
Efficiency	η	I_{OUT} = 30 mA to I_{MAX} VDD < 4.2 V		85		%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On resistance pMOS	R_{pMOS}	incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Output voltage	VBCORE	I_{OUT} < 70 mA	0.5	Note 5	2.075	V
Typical mode switching current				40		mA
Output current	I_{OUT}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0 mA		25	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 70 mA		80		%
Mode transition time				16	18	µs

Note 1 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing

Note 2 Minimum tolerance is +/-30 mV

Note 3 VDD > 3.0 V, using Coilcraft LPS3015-222ML

Note 4 The current limits will be automatically doubled when BUCKCORE is merged with BUCKPRO

Note 5 Max. V_{DD} – 1.0 V

8.8.2 BUCKPRO

Table 21: BUCKPRO (DA9021 only)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD		VDDOUT - 0.3 V 2.8 V min		VDDOUT + 0.3 V 5 V max	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2 to 4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBPRO	I_{OUT} = I_{MAX}	0.725	Note 1	2.075	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 1	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		5		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA to 500 mA step, dI/dt = 50 mA/µs		15	30	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 500 mA t_r=t_f=10 µs		3	8	mV
Output current	I_{MAX}	During DVC transitions Between DVC transitions	700 800 Note 2			mA
Current limit (programmable)	I_{LIM}	BUCKPRO_ILIM=00	-20 %	700	20 %	mA
		BUCKPRO_ILIM=01	-20 %	800	20 %	mA
		BUCKPRO_ILIM=10	-20 %	1000	20 %	mA
		BUCKPRO_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	f			2		MHz
Switching duty cycle			10		90	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via PRO_PD_DIS			200	Ω
Efficiency	η	I_{OUT}=30 mA to I_{MAX} VDD < 4.2 V		85		%
On resistance pMOS	R_{pMOS}	incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Output voltage	VBPRO	I_{OUT} < 70 mA	0.5	Note 3	2.075	V
Typical mode switching current				40 Note 4		mA
Output current	I_{MAX}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		20	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 70 mA		80		%
Mode transition time				16	18	µs

Note 1 Minimum tolerance is +/- 30 mV

Note 2 VDD > 3.0 V using Coilcraft LPS3015-222ML

Note 3 Max. VDD – 1.0 V

Note 4 Minimum tolerance is +/- 35 mV

8.8.3 BUCKPERI

Table 22: BUCKPERI (DA9022 only)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD		VDDOUT -0.3 V 2.8 V min		V_{DD_OUT} + 0.3 V 5 V max	V
Output capacitor	C_{OUT}		-30 %	10	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2 or 4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBPERI	$I_{OUT} = I_{MAX}$	1.8	Note 1	3.6	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 2	+3	%
Output voltage ripple		$I_{OUT} = I_{MAX}$		10		mV
Load regulation transient	VTR_{LOAD}	VDD = 3.6 V, VBPERI < 3.0 V I_{OUT} = 0 mA to 500 mA step, dI/dt = 50 mA/µs		20	40	mV
	VTR_{LOAD}	VDD = 3.6 V, VBPERI= 3.3 V I_{OUT} = 0 mA to 500 mA step, dI/dt = 50 mA/µs		40	80	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 300 mA $t_r = t_f = 10$ µs		10	20	mV
Output current	I_{MAX} I_{LIM}	During DVC transitions Between DVC transitions VBMEM < 2.1 V	650 750 Note 3			mA
Current limit (programmable)		BUCKPERI_ILIM=00	-20 %	700	20 %	mA
		BUCKPERI_ILIM=01	-20 %	800	20 %	mA
		BUCKPERI_ILIM=10	-20 %	1000	20 %	mA
		BUCKPERI_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			3		mA
Switching frequency	f			2		MHz
Switching duty cycle			20		100	%
Turn on time	T_{ON}				2.2	ms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output pull down resistor		@ V_{OUT} = 0.5 V			200	Ω
Efficiency	η	I_{OUT} < I_{MAX} VDD < 4.2 V		80	85	%
Efficiency (half pass device) Note 4	η_2	I_{OUT}=50 mA to 300 mA VDD < 4.2 V		90	95	%
On resistance pMOS	R_{pMOS}	incl. pin and routing			0.25	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
Bypass resistance	R_{BYPASS}	at VDDPERI=3.6 V			1.0	Ω
PFM mode						
Typical mode switching current				40		mA
Output current	I_{max}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		25	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 70 mA		80		%
Mode transition time				16	18	µs

Note 1 Programmable in 50 mV increments up to 3 V then in 100 mV increments, maximum output voltage is less than VDD

Note 2 Minimum tolerance is +/- 35 mV

Note 3 VDD > 3.0 V using Coilcraft LPS3015-222ML

Note 4 See control BPERI_HS

8.8.4 BUCKMEM

Table 23: BUCKMEM

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	VDD		VDDOUT - 0.3 V 2.8 V min		VDDOUT + 0.3 V, 5 V max	V
Output capacitor	C_{OUT}		-30 %	10	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2 to 4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBMEM	I_{OUT} = I_{MAX}	0.95	Note 1	2.525	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 2	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		10		mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA and 300 mA step, dI/dt = 30 mA/µs		20	40	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 300 mA $t_r = t_f$ = 10 µs		5	10	mV
Output current	I_{MAX}	During DVC transitions Between DVC transitions < 2.075 V	650 750 Note 3			mA
Current limit (programmable)	I_{LIM}	BUCKMEM_ILIM=00	-20 %	700	20 %	mA
		BUCKMEM_ILIM=01	-20 %	800	20 %	mA
		BUCKMEM_ILIM=10	-20 %	1000	20 %	mA
		BUCKMEM_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	f			2		MHz
Switching duty cycle			10		90	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via MEM_PD_DIS			250	Ω
Efficiency	η	I_{OUT}=30 mA to I_{MAX} VDD < 4.2 V		85		%
On resistance pMOS	R_{pMOS}	incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Typical mode switching current				40		mA
Output current	I_{max}		70			mA
Current limit	I_{LIM}		-20 %	150	+ 30%	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		20	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 70 mA	80			%
Mode transition time				16	18	µs

Note 1 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing

Note 2 Minimum tolerance is +/- 35 mV

Note 3 VDD > 3.0 V, using Coilcraft LPS3015-222ML

8.9 Battery charger

Table 24: Battery charger

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
VBUS	VUSB		4.4		5.5	V
USB2.0 host/hub mode (default)	ISET_USB		70	Note 1	1300	mA

Note 1 Programmable in 10 mA increments from 70 mA to 120 mA and 100 mA increments from 400 mA to 1300 mA

8.9.1 Charger buck

Table 25: Charger buck

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VCENTER		4.4		5.6	V
Output capacitor	C_{OUT}		30			µF
ESR of output capacitor		f > 100 kHz			20	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}	f = 1 MHz		100	150	mΩ
Output voltage	VDDOUT	I_{OUT}= 1000 mA	3.6	VBAT + 200 mV		V
Ripple voltage		I_{OUT} = 1000 mA		10		mV
Line regulation transient	VTR_{LINE}	VBUS_PROT = 4.4 V - 5.5 V, I_{OUT} = 1000 mA $t_r = t_f$ = 10 µs		10		mV
Output current	I_{MAX}		1300			mA
Current limitation	I_{LIM}	2-wire programmable (different step sizes for different ranges)	70		1300	mA
Quiescent current in OFF mode					1	µA
Quiescent current in synchronous rectification mode				5		mA
F_BUCK Frequency of operation				2		MHz
Switching duty cycle			10		100	%
T_{on} Turn on time					2.2	m
Efficiency		I_{OUT} = 1000 mA VBUS_PROT = 5 V	85	90		%
R_PMOS PMOS on resistance		incl. pin and routing	0.08	0.15	0.2	Ω
R_NMOS NMOS on resistance		incl. pin and routing	0.15	0.25	0.3	Ω

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
R_VBUS_PROT internal switch on resistance		incl pin and routing, VBUS_PROT= 4.8 V	0.05	0.1	0.2	Ω
Sleep mode – PFM mode						
Sleep mode output current	$I_{OUTSLEEP}$		100			mA
Current limitation			300		550	mA
IQ_ SLEEP – No load supply current in SLEEP mode		I_{OUT} = 0 mA (due to high precision current limit)		80	100	µA
F_BUCK Frequency of operation			0		3	MHz
Efficiency		I_{OUT} = 10 mA to 100 mA	85			%
Efficiency		I_{OUT} = 1 mA to 50 mA VDD =4.8 V	75			%
Mode transition time				16	18	µs

8.9.2 Voltage levels on VBAT

Table 26: Voltage levels on VBAT

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
VBAT_FAULT	V_{BAT_FAULT}			2.9		V
ICHG_BAT (ICHG_PRE over-ride)	ICHG_BAT	VBAT < V_{BAT_FAULT}	20	40	60	mA

8.9.3 Charging modes

Table 27: Charging modes

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
CC mode output current		6 bits ICHG_BAT (20 mA steps)	0	200	1260	mA
CC absolute accuracy		ICHG_BAT < 100 mA	-10		+10	mA
CC absolute accuracy		ICHG_BAT > 100 mA	-10		+10	%
CV mode output voltage		VCHG_BAT (25 mV steps)	3.65	4.2	4.425	V
CV output voltage accuracy		VCHG_BAT	-25		+25	mV

8.9.4 Charger detection circuit

Table 28: Charger detection circuit

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Charger detect threshold	VCH_DET		4.25	4.35	4.4	V
Charger current limit reduction threshold		VCHG_THR (configurable)	3.7	3.8	4.35	V
Charger insertion debounce time	VCHG_INS_DEB			10		ms
VBUS, excess voltage threshold	VCHG_EXCESS		5.5	5.6	5.8	V

8.9.5 VBUS charge control

Table 29: VBUS charge control

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
VBUS load in low power SUSPEND mode	$I_{VBUS\_SUSPEND}$	0 V ≤ VBUS ≤ 5.25 V T_{AVG} = <1 s, no spikes higher than 100 mA			500	µA

8.9.6 Charge timer

Table 30: Charge timer

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Total charging timer setting	TCTR	Total charge time is defined as the total charge time from when the charger was enabled (both for LINEAR and PRE-CHARGE mode charging). If the timer expires, the CHG_TO flag is set in the EVENT register, an IRQ issued and the charging is disabled. The default TCTR setting is 0x0A. Setting the TCTR to 0x00 disables the timer.	0	30	450	min
Read back of current timer value	CHG_TIME	This register can be used to read back the current value of the charge time counter, counting down from the value loaded by the TCTR	0	2	510	min

8.9.7 DCCC and active-diode

Table 31: DCCC and active-diode

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Active diode on resistance	R_{ON}	VBAT=3.6 V I=500 mA incl pin and routing		0.14		Ω
Circuit activation voltage		VBAT - VDDOUT	10	20	40	mV
Maximum diode current	ID_{MAX}			2.2		A

8.10 Oscillator

Table 32: Oscillator (T_A = -25 ºC to +85 ºC)

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Internal oscillator frequency		before trimming after trimming	1.4 1.9	2.0	2.6 2.1	MHz

8.11 Reference voltage generation and temperature supervision

Table 33: Reference voltage generation and temperature supervision (T_A = -25 ºC to +85 ºC)

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Reference voltage	VDD_REF_Pin		-1 %	1.2	+1 %	V
VDD_REF decoupling capacitor				100		nF
Reference current resistor	IREF Pin		-1 %	200	+1 %	kΩ
Thermal shutdown	T_{OVER}		125	140	155	ºC
Charge current reduction	$T_{CHARGELOW}$		75	90	115	ºC
Charge suspend	$T_{CHARGE\_SUSPEND}$		105	120	135	ºC
Hysteresis				10		ºC

9 Real time clock and 32 kHz oscillator

The real time clock (RTC) block keeps track of the RTC clock counter and alarm function. The RTC block will operate from the LDO_CORE power supply.

9.1 32 kHz oscillator

The clock oscillator cell is used to drive the RTC counter. It works with an external piezoelectric oscillator crystal at 32.768 kHz.

In order to achieve the desired crystal frequency connect an external capacitor (10 pF to 20 pF, depending on the parasitic capacitance of the board) to ground from each of the crystal pins. The start-up time of the oscillator is typically 0.5 s over the voltage range. When the crystal is not mounted, ground the unpopulated crystal pins. The 32 kHz clock signal is made available at the OUT_32K pin and the buffer can be disabled from the sequencer during POWERDOWN mode.

The timekeeping error from the frequency variance of crystal oscillators (typ. +/- 20 ppm) can be trimmed individually by +/- 242 ppm with a resolution of 1.9 ppm (1/(32768 * 16)). More advanced solutions will be able to dynamically correct the temperature related oscillator frequency drift (> 100 ppm) by using a periodic temperature measurement located close to the crystal. The timekeeping correction will be applied only towards the on-chip RTC block. To avoid potential clock jitter issues, the 32 kHz clock signal at the OUT_32K pin provides the original frequency of the crystal.

9.2 RTC counter and alarm

The RTC counter can count the number of 32 kHz clock periods, providing a seconds, minutes, hours, day, month and year output, up to 63 years. Year 0 corresponds to 2000. The value of the RTC calendar shall be read-/write-able via the power manager communication. The calendar is reset to zero when VDDCORE is lost.

There is an alarm register containing minutes, hours, day, month and year. When the RTC counter register value corresponds to the value set in the alarm an interrupt request (IRQ) event and a wakeup (if DA9021/22 is in POWERDOWN mode) will be triggered. The trigger will also set a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_TYPE, is either asserted every second or minute. In the case the host has enabled both alarms it can determine from the status of ALARM_TYPE whether the IRQ/wakeup was caused by the timer or the tick.

NOTE
The oscillator inputs can withstand a leakage current, corresponding to at least a 10 MΩ connected between the pin and any signal level between VDDOUT and GND.

The power manager registers ALARM_ON and TICK_ON enable/disable the alarm/tick. The power manager register bit MONITOR is set to ‘0’ each time the RTC is powered up. The software sets this bit to ‘1’ when setting the time and date, which allows the software to detect a subsequent loss of the clock.

NOTE
Values written into the RTC calendar and alarm registers must be within the allowed range (see register description, for example maximum 60 for seconds or minutes).

The RTC seconds registers define a 32-bit seconds counter (approximately 136 years), that can only be reset via the nPOR and starts counting seconds after nPOR is released. Using the RTC input clock the output port GPO10 can be toggled with a configurable periodic pulse. In this mode GPO10 offers blinking LED drivers that are able to run in POWERDOWN mode.

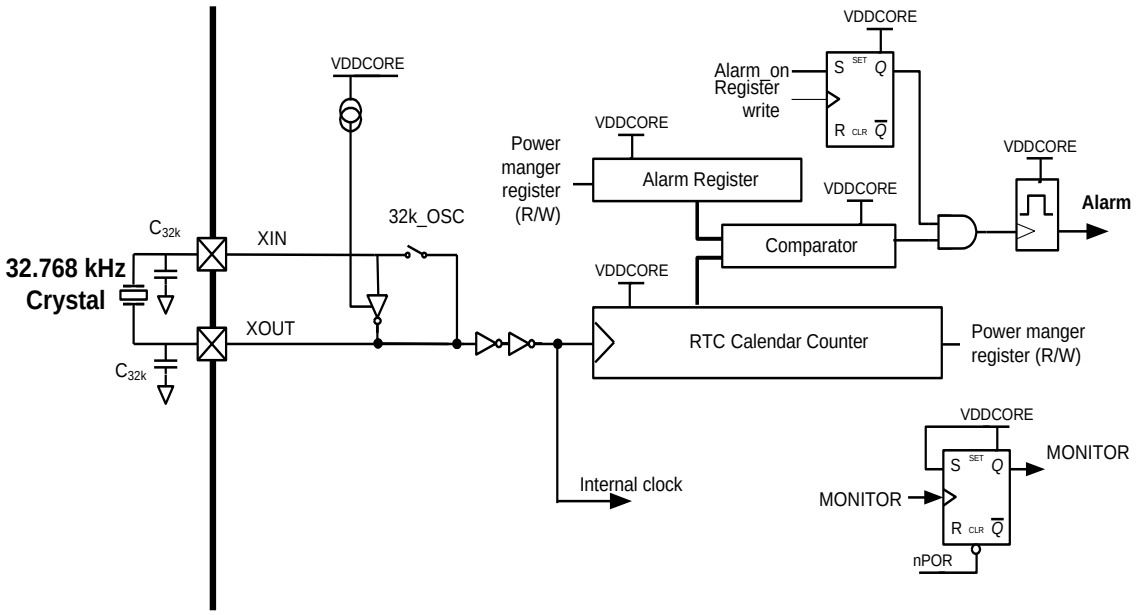

Figure 6: Schematics of the RTC oscillator and counter functionality

10 Typical characteristics

10.1 Buck regulator performance

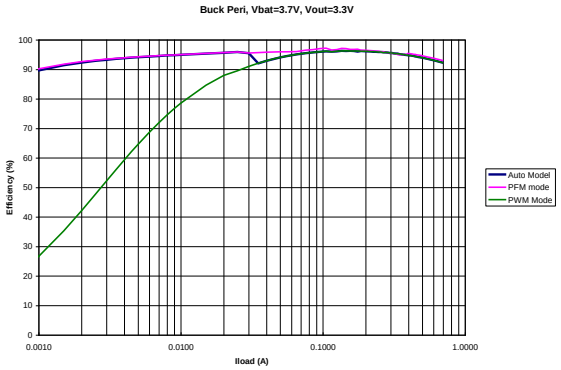

Figure 7: BUCKPERI efficiency curves

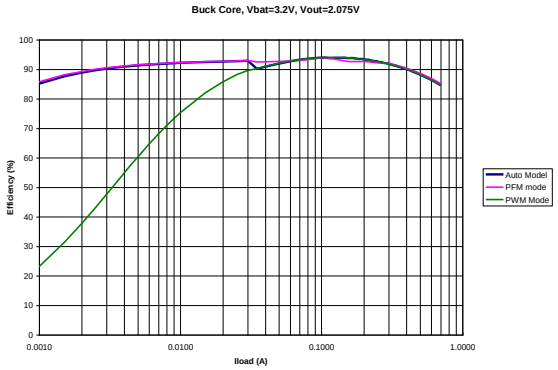

Figure 8: BUCKCORE efficiency curves

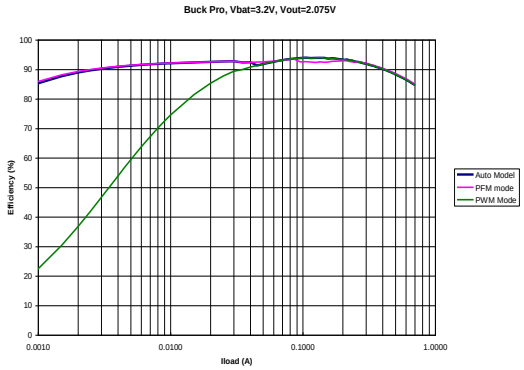

Figure 9: BUCKPRO efficiency curves

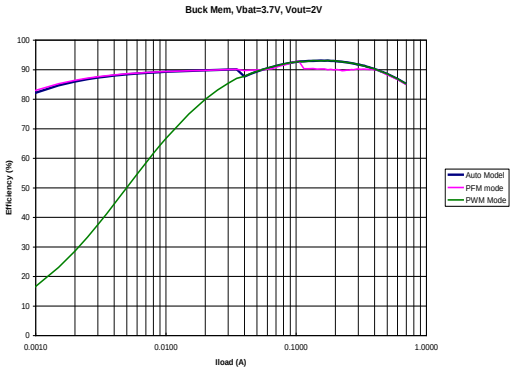

Figure 10: BUCKMEM efficiency curves

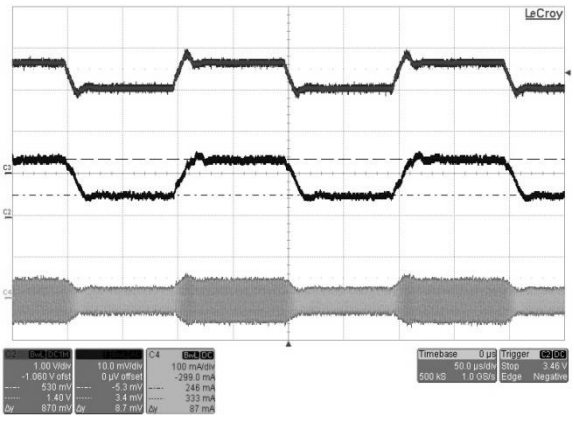

Figure 11: Typical buck line transient

Note 1 Ch2: VBAT, Ch3: V_{OUT}, Ch4: I_{COIL}
V_{OUT} = 2.5 V, no load,
VBAT = 3.0 V to 3.6 V step,
t_rise = t_fall = ~10 µs

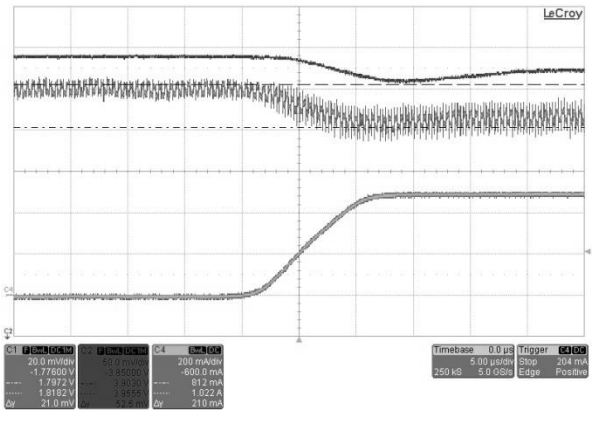

Figure 12: Typical buck load transient

Note 1 Ch1: I_{COIL}, Ch2: V_{OUT}, Ch4: I_{LOAD}
V_{OUT} = 1.8 V, VBAT = 4 V,
I_{LOAD} = 0 V to 500 mA, dI/dt~50 mA/µs, rising

10.2 Linear regulator performance

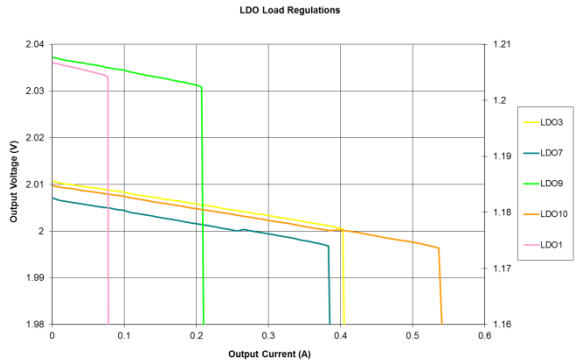

Figure 13: Typical LDO load regulation

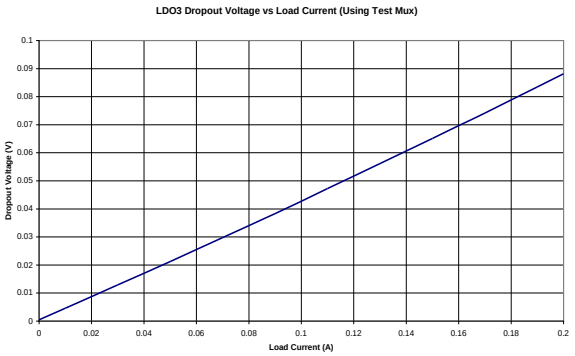

Figure 14: Typical LDO drop-out voltage

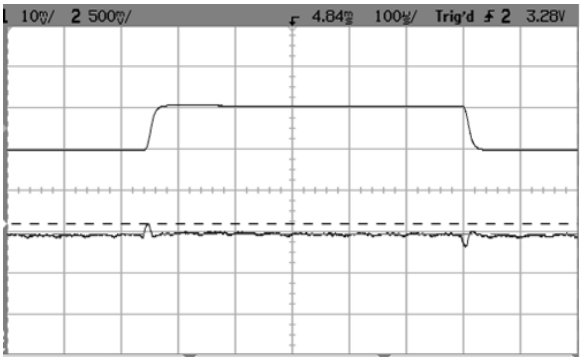

Figure 15: Typical LDO line transient

(Transient of 3.6 V to 4.2 V at VBAT).
Top trace = VBAT, bottom trace = VLD01

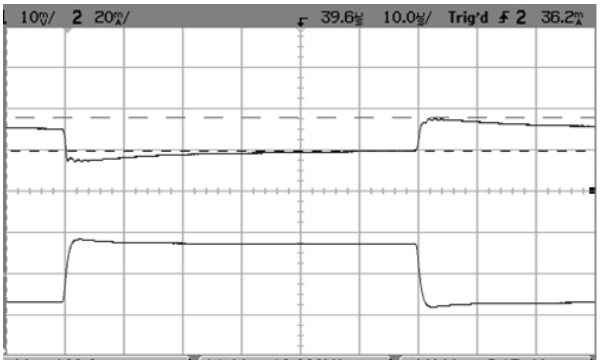

Figure 16: LDO load transient

(1 mA to I_{MAX} of 40 mA) VLDO = 1.2 V
Top trace = VLD01, bottom trace = Load

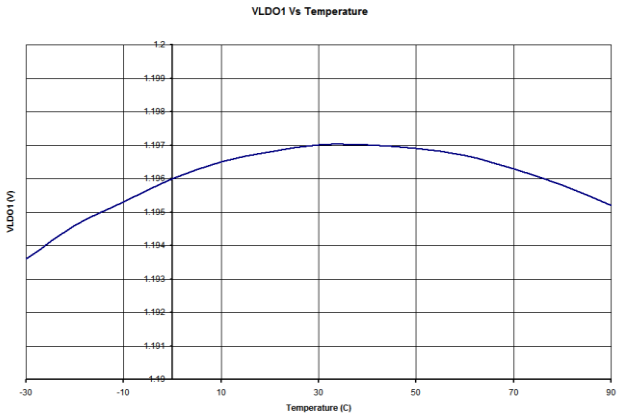

Figure 17: Typical LDO voltage vs temperature

10.3 ADC performance

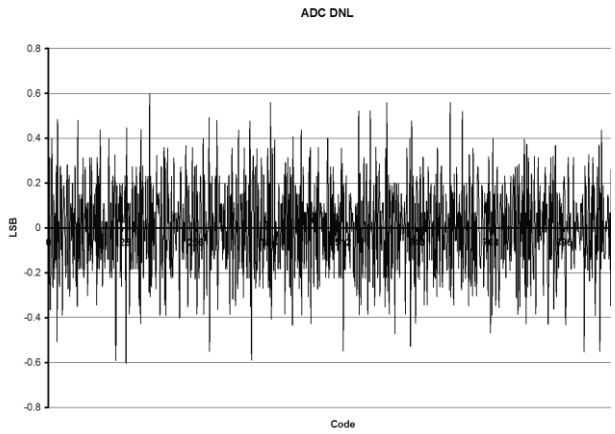

Figure 18: ADC DNL performance

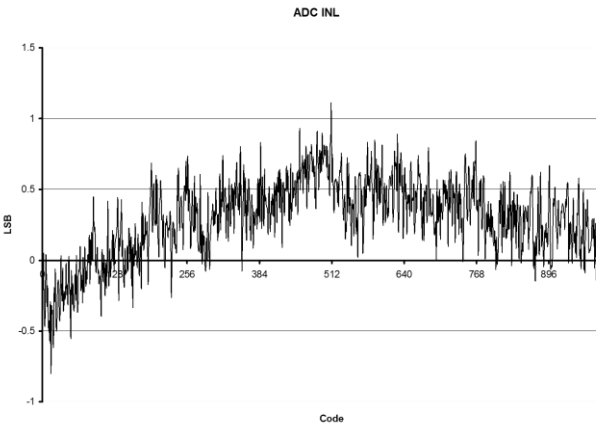

Figure 19: ADC INL performance

10.4 Power path performance

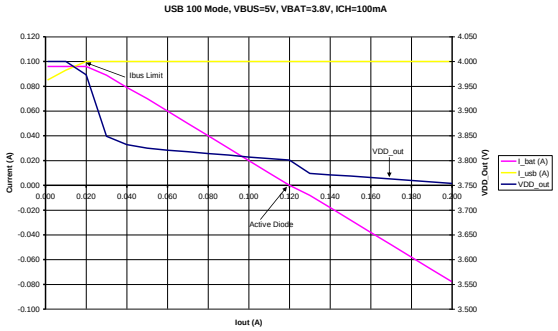

Figure 20 Power path behaviour USB100 mode

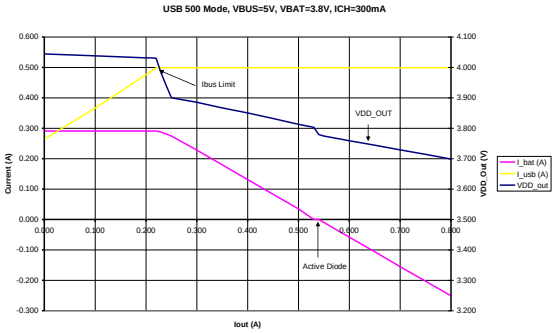

Figure 21 Power path behaviour USB500 mode

Figures 20 and 21 show increasing load current supplied from VBUS, power path loop reduces ICH until active diode turns on which then allows current from battery to supply system load current via VDDOUT.

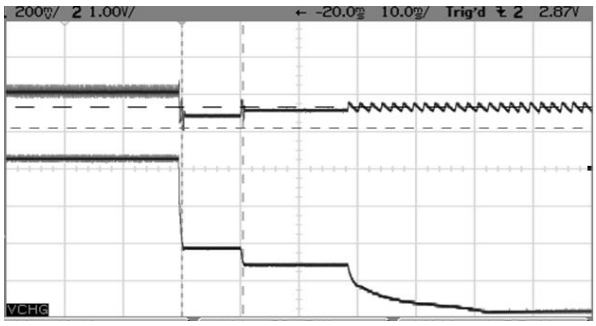

Figure 22: Transitioning supply from USB 5 V (via VBUS) to VBAT

Top trace = VDDOUT, bottom trace = VBUS

11 Functional description

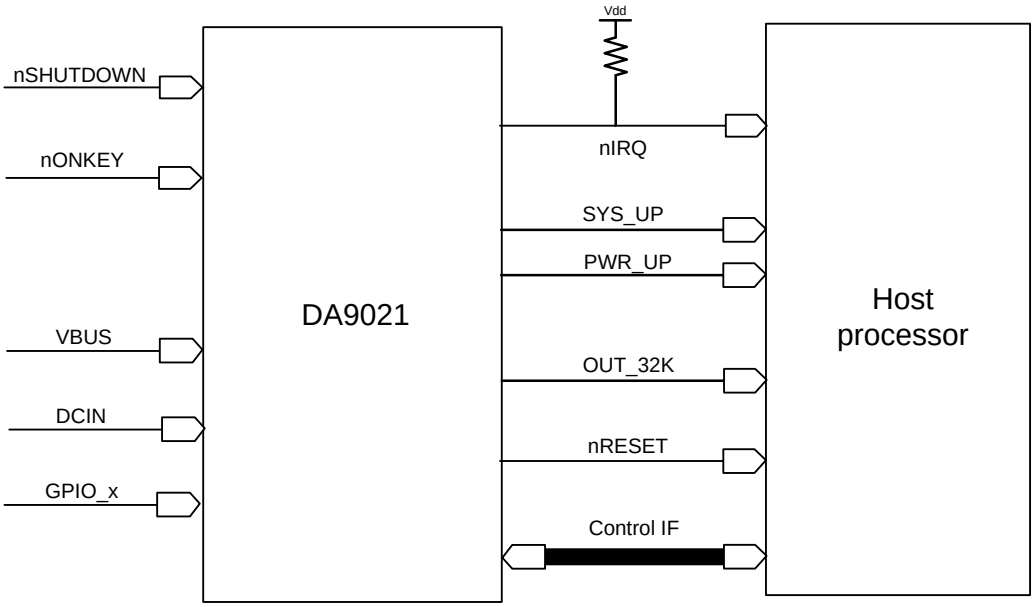

Figure 23: Control ports and interface

11.1 Power manager IO ports

The power manager input ports are supplied either from the internal rail VDDCORE or VDD_IO, selected via PM_I_V. The output ports are supplied from VDD_IO. During the initial start-up sequence the power manager IO ports are in tri-state mode until being configured from OTP when leaving RESET mode, except nRESET, nIRQ, PWR_UP/GP_FB2. Output ports are push-pull type except for nRESET and nIRQ, which can also be configured to open drain.

11.2 On/off (nONKEY)

The nONKEY signal is a level active low wakeup interrupt/event intended to switch-on the DA9021/22 supplied application. nONKEY is always enabled during POWERDOWN mode, so that the application can be also switched-on with a disabled GPIO extender. The wakeup event can be disabled via the interrupt mask M_nONKEY.

11.3 Hardware reset (nSHUTDOWN, nONKEY, GPIO14 & GPIO15)

A user-initiated hard reset at the DA9021/22 nSHUTDOWN is an active low input initiated typically by a push button switch or an asserted error detection line from a host processor. The sequencer then powers down all domains in reverse order down to step 0 and all supplies of DA9021/22 except LDOCORE are switched off.

DA9021/22 includes a second hardware reset that follows the nONKEY after being asserted for a period of 5 s ± 30 %. The same can be achieved by a parallel connection of GPI14 and GPI15 to ground for 5 s ± 30 %.

This feature provides the ability to emergency turn-off the application in the event of a software lock-up without the need for a dedicated RESET hardware switch or removing the battery.

After a minimum time-out of 500 ms DA9021/22 will start to power up again. It will wait for a valid wakeup event (for example key press) or will start the power sequencer automatically. By asserting EXT_WAKEUP it can request the host processor to control the subsequent start-up. Alternatively the power up sequence can be performed autonomously by the PMIC following OTP pre-configurations.

A detection of a hard reset forces the assertion of nRESET to low when the sequencer returns from POWERDOWN mode to RESET mode.

This type of reset is typically used only for severe or unrecoverable hardware or software problems, because it completely resets the processor and can result in data loss.

11.4 Reset output (nRESET)

The nRESET signal is an active-low output signal from DA9021/22 to the host processor, which tells the host to enter the hardware-reset state. nRESET is always asserted at the beginning of a DA9021/22 cold start from NO-POWER mode and when the DA9021/22 returns to RESET mode. nRESET can also be asserted as a soft reset after the sequencer finishes powering down without progressing to RESET-mode.

The reset timer trigger signal can be configured to be EXT_WAKEUP, SYS_UP or PWR_UP. After being asserted nRESET remains low until the reset timer is started from the selected trigger signal and expires. The expiry time can be configured from 1 ms to 1024 ms.

11.5 System enable (SYS_EN)

SYS_EN is an input signal from the host processor to DA9021/22 (or can be default enabled via OTP settings), which initiates enabling the system power supplies. The control SYS_EN will be initialised from OTP if the related port is configured as GPI or GPO. The register bit SYS_EN can be read and changed via the control interfaces. DA9021/22 will not accept any power mode transition commands until the sequencer has stopped processing IDs. De-asserting SYS_EN informs the DA9021/22 that the host processor is going into a standby/hibernate mode. When the port is changing from active to passive state there is no IRQ or wakeup event trigger. With the exception of supplies that are configured in ACTIVE mode with a voltage preset before powering down, all regulators and buck converters in power domain POWER1, POWER and SYSTEM will be sequentially disabled in reverse order.

11.6 Power enable (PWR_EN)

PWR_EN is an input signal from the host processor to DA9021/22 (or is configured via OTP or host commands). Initialisation, IRQ assertion and register bit PWR_EN control is similar to SYS_EN. To ensure the correct sequencing SYS_EN has to be active before asserting PWR_EN. When de-asserting SYS_EN the sequencer will sequentially power down POWER1, POWER and SYSTEM domains respectively.

11.7 Power1 enable (PWR1_EN)

PWR1_EN is an input signal from a host to DA9021/22 and is configured via OTP or host commands. Initialisation, IRQ assertion and register bit PWR1_EN control is similar to SYS_EN. The domain POWER1 is a sub power domain for general purpose.

11.8 General purpose feedback signal 1 (GP_FB1: EXT_WAKEUP/READY)

The feedback GP_FB1 supports two different modes. If configured as EXT_WAKEUP it is an active high output signal to the host processor that indicates a valid wakeup event during POWERDOWN mode. External signals that are causing wakeup events are debounced before DA9021/22 asserts the EXT_WAKEUP signal. EXT_WAKEUP is released when entering the ACTIVE mode. If configured as READY signal it indicates ongoing DVC or power sequencer activities. The signal is active low and is asserted from DA9021/22 as long as the power sequencer processes IDs or DVC voltage transitions are ongoing.

11.9 Power domain status (PWR_UP/GP_FB2)

The power domain status indicators are active high and assigned after the sequencer has processed all IDs of a power domain (all assigned supplies are up). When domains are disabled during power mode transitions the status indicator is released before the DA9021/22 sequencer processes the last step of a domain.

PWR_UP is one mode of the general purpose indicator GP_FB2 that can also be used as a configurable feedback signal that is level/time controlled from the power sequencer.

11.10 Supply rail fault (nVDD_FAULT)

nVDD_FAULT is an active low output signal to the host processor to indicate a VDDOUT low status. The assertion of nVDD_FAULT indicates that the main battery and the supply input voltage is low and therefore informs the host processor that the power will shut down very soon. After that the processor may operate for a limited time from the backup battery, which can provide power to the processor for a few cycles. In the event of nVDD_FAULT assertion the processor may be programmed to enter an emergency mode, for example external memory data refresh is no longer performed.

11.11 Interrupt request (nIRQ)

The nIRQ is an active low output signal which indicates that an interrupt causing event has occurred and that the event and status information is available in the related registers. Such information can be temperature and voltage of the PMIC, fault conditions, charging status, status changes at GPI ports, and others. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ will not be released until the event registers have been cleared.

11.12 Real time clock output (OUT_32K)

The OUT_32K is an output signal that generates a buffered signal of the DA9021/22 32 kHz oscillator. The 32 kHz oscillator will always run on the DA9021/22 following the initial start-up from NO-POWER mode until the device has reached NO-POWER mode again. The signal output buffer can be disabled during POWERDOWN mode with bit OUT_32K_PD.

11.13 IO_supply voltage (VDD_IO)

VDD_IO is an independent IO supply rail input of DA9021/22 that can be assigned to the power manager interface, power manager IOs and GPIOs. The rail assignment determines the IO voltage levels and logic. The selection of the supply rail for GPIOs is also partially used for their alternate functions. GPOs configured in open drain mode have to use the VDD_IO rail if an internal pull-up resistor is required.

12 Control interfaces

The DA9021/22 is completely software controlled from the host by registers. DA9021/22 offers two independent serial control interfaces to access these registers. The communication via the main power manager interface is selectable to be either a 2-wire or a 4-wire connection (I^2C or SPI compliant). The alternate interface is fixed towards a 2-wire bus. Data is shifted in to or out from DA9021/22 under the control of the host processor that also provides the serial clock.

12.1 Power manager interface (4-wire and 2-wire control bus)

This is the dedicated power control interface from the primary host processor. In 4-wire mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

12.2 4-wire communication

In 4-wire mode the DA9021/22 register map is split into two pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after reset includes registers R1 to R127. Writing to the page control register changes the active page for all subsequent read/write operations. After modifying the active page it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

The 4-wire interface features a half-duplex operation (data can be transmitted and received within a single 16-bit frame) at enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.

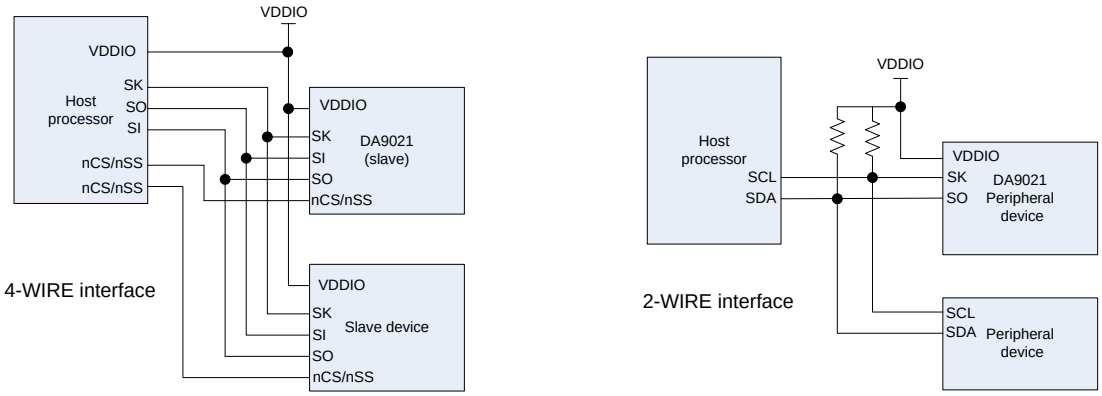

Figure 24: Schematic of 4-wire and 2-wire power manager bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0 to 127, decimal) which will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which specifies the direction of the following data exchange.

During register writing the host continues sending out data during the following 8 SK clocks. For reading the host stops transmitting and the 8-bit register is clocked out of DA9021/22 during the consecutive eight SK clocks of the frame. Address and data are transmitted with MSB first. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9021/22 is normally in high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal is causing unintended current consumption inside other circuits.

Table 34: 4-wire clock configurations

CPOL clock polarity	CPHA clock phase	Output data is updated at SK edge	Input data is registered at SK edge
0 (idle low)	0	falling	rising
0 (idle low)	1	rising	falling
1 (idle high)	0	rising	falling
1 (idle high)	1	falling	rising

The DA9021/22 4-wire interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0 setting DA9021/22 latches data on the SK rising edge.

If the CPHA is set to '1' the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9021/22 must be set to the same CPOL and CPHA states to communicate with each other.

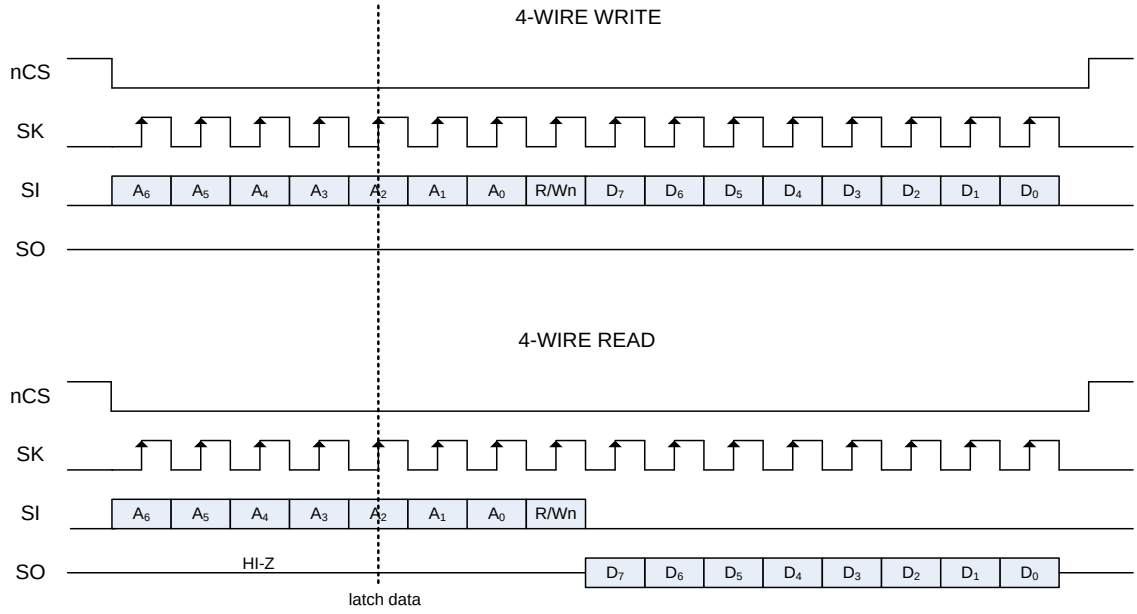

Figure 25: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '0')

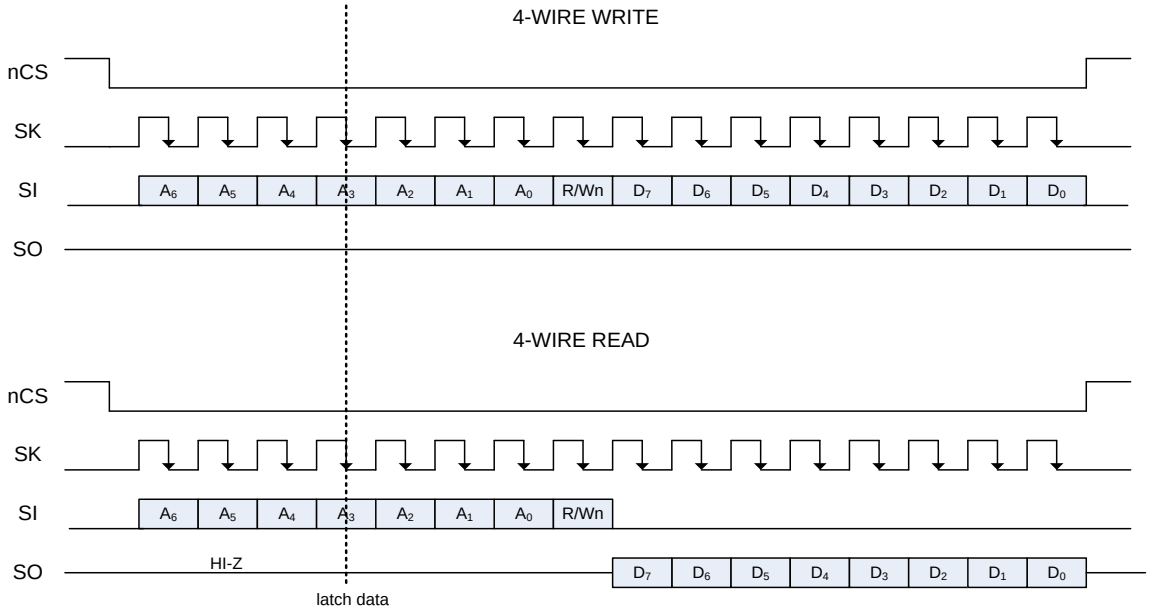

Figure 26: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '1')

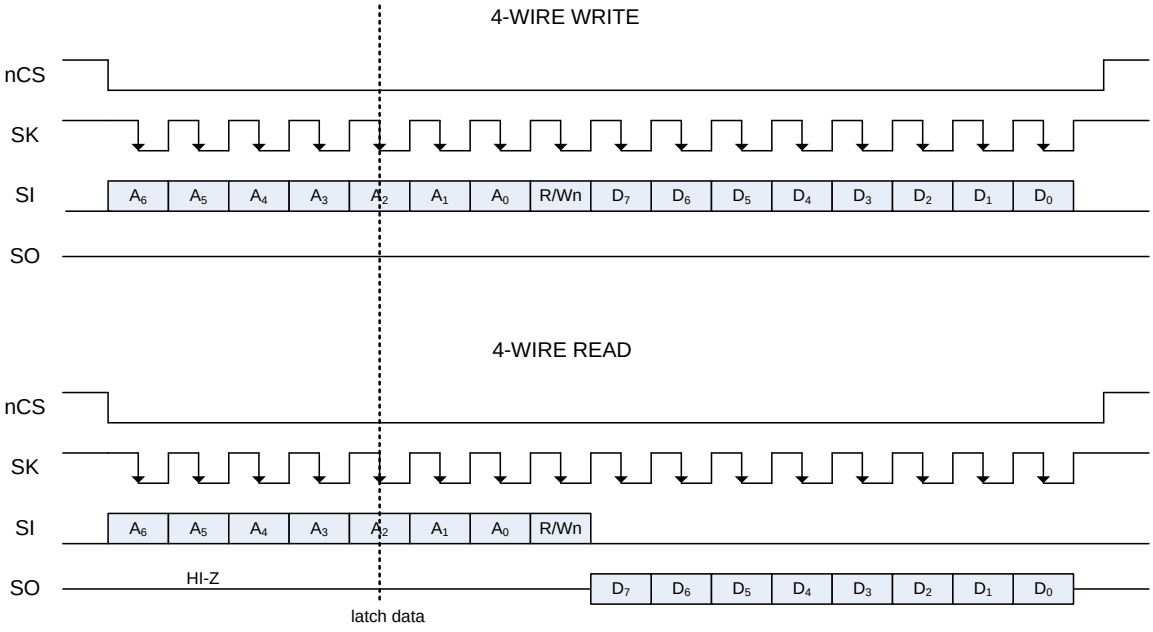

Figure 27: 4-wire host write and read timing (nCS_POL = '0', CPOL = '1', CPHA = '0')

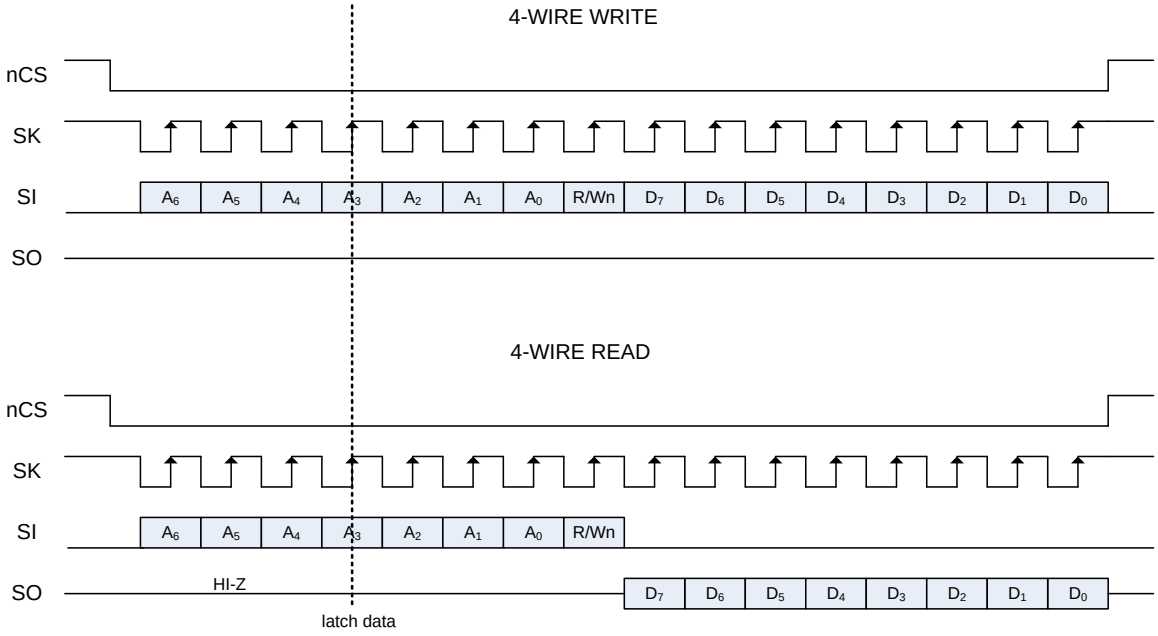

Figure 28: 4-wire host write and read timing (nCS_POL = '0', CPOL = '1', CPHA = '1')

Table 35: 4-wire interface summary

PARAMETER		
Signal lines	nCS	Chip select
	SI Serial input data	Master out Slave in
	SO Serial output data	Master in Slave out
	SK	Transmission clock
Interface	Push-pull with tristate	
Supply voltage	VDD_IO	1.6 V to 3.3 V
Data rate	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16-bit cycles	7-bit address, 1-bit read/write, 8-bit data
Configuration	CPOL	Clock polarity
	CPHA	Clock phase
		NCS is active low/high

NOTE
Reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example by writing/reading another register address in between).

12.3 2-wire communication

The power manager interface can be configured for a 2-wire serial data exchange. It has a configurable SLAVE write address (default: 0x90) and a configurable SLAVE read address (default: 0x91).

SK provides the 2-wire clock and SO carries all the power manager bidirectional 2-wire data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict, if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9021/22 internal clock signals. DA9021/22 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down.

In high speed mode the maximum frequency of the bus can be increased up to 1.7 MHz. This mode is supported if the SK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SO pin to decrease the rise time of the data. In this mode the SO line on DA9021/22 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave. The DA9021/22 will only operate as a slave. As opposed to the 4-wire mode the 2-wire interface has direct (linear) access to the whole DA9021/22 register space (except R0/R128). This is achieved by using the MSB of the 2-wire, 8-bit register address as a selector of the register page (this does not modify the page control register R0/R128 that is accessible only in 4-wire mode).

12.3.1 2-wire control bus protocol

All data is transmitted across the 2-wire bus in groups of 8 bits. To send a bit the SO line is driven towards the independent state while the SK is LOW (a low on SO indicates a zero bit). Once the SO has settled the SK line is brought HIGH and then LOW. This pulse on SK clocks the SO bit into the receivers shift register.

A two byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer is MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SO line while the SK is in the HIGH state (a STOP condition is indicated by a low to high transition on the SO line while the SK is in the HIGH state).

The 2-wire bus will be monitored by DA9021/22 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. These acknowledge is done by pulling the SO line low during the following clock cycle (white blocks marked with “A” in Figure 29 to Figure 33).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded by DA9021/22 with Acknowledge):

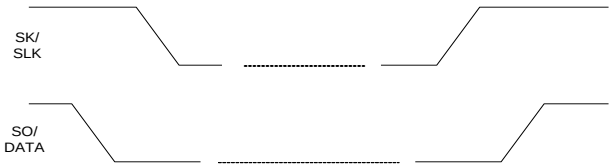

Figure 29: Timing of 2-wire START and STOP condition

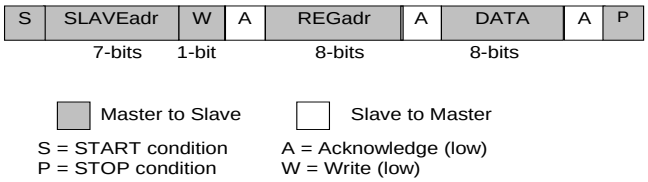

Figure 30: 2-wire byte write (SO/DATA line)

When the host reads data from a register it first has to write access DA9021/22 with the target register address and then read access DA9021/22 with a Repeated START or alternatively a second START condition. After receiving the data the host sends Not Acknowledge and terminates the transmission with a STOP condition:

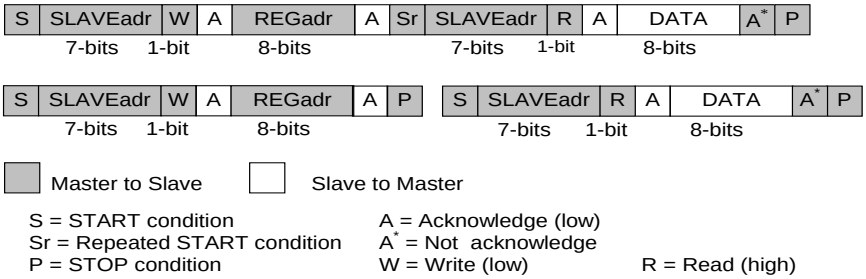

Figure 31: Examples of 2-wire byte read (SO/DATA line)

NOTE
The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

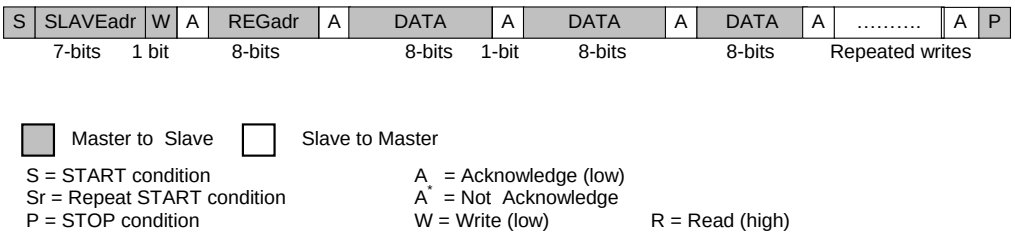

Figure 32: 2-wire page write (SO/DATA line)

An alternate write mode receiving alternated register address and data can be configured to support host repeated write operations that access several but non-consecutive registers.

Data will be stored at the previously received register address:

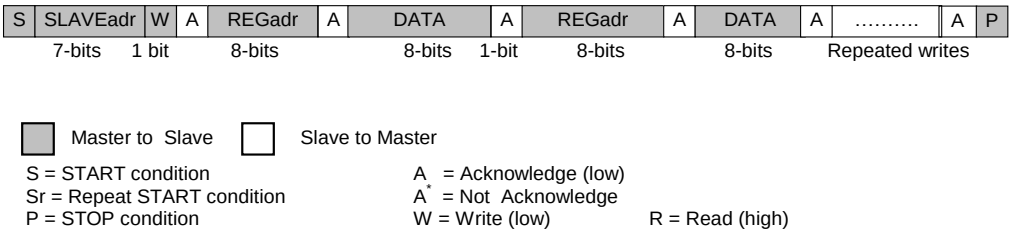

Figure 33: 2-wire repeated write (SO/DATA line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE mode.

12.3.2 Alternative high speed 2-wire interface

The high speed 2-wire (HS-2-wire) interface is the alternative serial control bus, which consists of a DATA (data line) and a CLK (clock line) that can be used as an independent control interface for data transactions between DA9021/22 and a second host processor. The DA9021/22 HS-2-wire interface has a configurable 8-bit SLAVE write address (default: 0x92) and a configurable SLAVE read address (default: 0x93).

The interface is enabled if DATA was selected via configuration GPIO14_PIN. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). GPIO15_TYPE defines the supply rail of the interface (used for input logic levels and the internal pull-up resistors). The controls GPIO15_PIN and GPIO15_ MODE are disabled when the interface was enabled via GPIO14_PIN. Whenever the interface receives a READ or WRITE command that includes a matching slave address it is able to trigger the assertion of an nIRQ including an optional wakeup event (enabled via GPIO14_ MODE).

NOTE
If the nIRQ assertion from interface access is enabled it may by masked as long as the HS-2-wire is in use (this nIRQ cannot be cleared via the HS-2_wire interface because every interface access will trigger a re-assertion).

With the exception of the interface base address and the optional wakeup, the characteristics of the HS-2-wire interface are identical to the power manager 2-wire interface (see above).

NOTE
By connecting TP to VDDCORE the DA9021/22 (POWER COMMANDER mode) will load the register default values via the HS 2-wire interface instead of from OTP cells. In this mode the interface will be supplied from VDDCORE (independent to the settings at GPIO15_TYPE).

13 DA9021 operating modes

13.1 ACTIVE mode

A running application is typically in ACTIVE mode. In addition to PMIC core functions (for example LDOCORE, Binary Coded Decimal (BCD) counter and internal oscillator) in ACTIVE mode a set of supplies and peripheral features like the battery charger and GP-ADC are usually enabled. If required in ACTIVE mode the host processor can take over the control of the automatic battery charging block and is able to respond to any faults that have been detected. Status information can be read from the host processor via the power manager bus and DA9021/22 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ). Temperature and voltages inside and outside the DA9021/22 can be monitored and any fault conditions are flagged to the host processor.

13.2 POWERDOWN mode

DA9021/22 is in POWERDOWN mode whenever the power domain SYSTEM is disabled (even partially). This can be achieved when progressing from RESET mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low power mode instructions from the host or occurs as an interim state during an application shutdown to RESET mode.

During POWERDOWN mode the LDOCORE, the bandgap, the nONKEY and the BCD counter are active. Dedicated power supplies can be enabled during POWERDOWN mode if power down voltages have been pre-configured during ACTIVE mode. In addition GPIO-ports, the GP-ADC, battery charger and the control interfaces remain enabled if not disabled via register PD_DIS.

Disabling blocks during POWERDOWN mode will save quiescent current especially if all blocks are disabled that require an oscillator clock. If the host will no longer communicate during POWERDOWN mode the control interfaces may be temporarily disabled (see controls PM-IF_PD/HS-2-wire_PD.). Dedicated power supplies can be enabled in POWER-DOWN mode if power down voltages has been pre-configured during ACTIVE mode.

The internal oscillator (2 MHz) will only run on demand (for example for a running GP-ADC or enabled bucks that are not forced to PFM mode). The digital control logic of disabled features (regulators, bucks, chargers, GP-ADC, and others) will be disconnected from the clock tree by clock gating, so that the device offers an optimised dissipation power in POWERDOWN mode.

Following the next wakeup event all supplies are re-configured with their default voltage values from OTP and the sequencer timers are set to their default OTP values. If the POWERDOWN mode was caused by releasing SYS_EN the sequencer pointer is located at position 0 allowing default enabling / disabling of supplies (beside LDOCORE).

13.3 RESET mode

DA9021/22 is in RESET mode whenever a complete application reset is required. The RESET mode happens after cold start when progressing from NO-POWER mode or can be forced by the user via a pressed reset switch that is connected to port nSHUTDOWN, a long press of nONKEY (if the RESET feature was enabled) or a long parallel assertion of GPIO14 and GPIO15 (if this RESET feature was enabled), from the host processor by asserting port nSHUTDOWN or via an error detection from DA9021/22.

DA9021/22 error conditions that force a RESET mode:

- An under-voltage detected at VDDOUT (VDDOUT < VDD_FAULT_LOWER)
- An internal die over-temperature detected
- An over voltage or over current at the boost

In order to allow the host to determine the reason for the RESET a FAULTLOG register records the cause.

When returning from POWERDOWN mode the RESET mode will be achieved after powering down domain SYSTEM completely and continue towards a state with absolute minimum current consumption, with the only active circuits being LDOCORE, the BCD counter, the band gap and the

VDD_REF, VBUS, ACC_ID_DET and VDDOUT comparators. Except LDO1, if correctly configured, other supplies and blocks on DA9021/22 are automatically disabled to avoid draining the battery. During DA9021/22 RESET mode the host processor can be held in a RESET state via port nRESET which is always asserted to low when DA9021/22 progresses from RESET mode (for example after cold start from NO-POWER mode) and can be asserted (depending on configuration of sequencer step 0) when the sequencer has finished powering down domain SYSTEM (even partially).

Except E_B_FAULT and E_ALARM, all asserted events will automatically be cleared and the DA9021/22 register configuration will be re-loaded from OTP when leaving RESET mode (with the exception of AUTO_BOOT in case of emergency charging).

NOTE
FAULT_LOG and other non OTP loaded registers, for example the RTC calendar and alarm, will not be changed when leaving RESET mode.

Some RESET conditions such as the SHUTDOWN via register bit, will automatically expire over-temperature. Other conditions like asserting the port nSHUTDOWN need to be released to enable a progress from RESET to POWERDOWN mode. If the RESET was initiated by a hardware reset from user keys or port nSHUTDOWN a 500 ms time out will be inserted before trying to power up again. When the RESET condition has disappeared DA9021/22 requires either a connected good main battery (VDDOUT > VDD_FAULT_UPPER) or a detected supply (VBUS > VCH_THR) that is able to provide enough power to VDDOUT (VDDOUT > VDDOUT_MIN) to start-up to POWERDOWN mode.

13.4 NO-POWER mode

DA9021/22 will enter the NO-POWER mode when VDDCORE drops below VPOR_LOWER (for example during continued discharge of main battery). As long as VDDCORE is now lower than VPOR_UPPER the core supply LDOCORE, the 32 kHz oscillator and the BCD counter are switched off, an internal power-on-reset (nPOR) is asserted and only the VDDCORE comparator is active and checks for a condition that allows DA9021/22 to turn on again. When DA9021/22 detects either a good main battery or a connected supply charger which rises VDDCORE > VPOR_UPPER it will reset the BCD counter and FAULT_LOG register and progress to RESET mode.

13.5 POWER COMMANDER mode

This is a special mode for evaluation and configuration. In POWER COMMANDER mode DA9021/22 is configured to load the control register default values from the HS 2-wire interface instead of from the OTP cells so that un-programmed DA9021 samples will power up and allow a PC running the Power Commander software to load all the configuration registers. POWER COMMANDER mode is enabled by connecting TP to VDDCORE.

In RESET-mode DA9021/22 will do an initial OTP read to setup the trim values. However, if the OTP values loaded into these registers are not as required they can be updated during the subsequent POWER COMMANDER mode programming sequences.

NOTE
In POWER COMMANDER mode GPI14/15 will be configured for HS-2-wire interface operation (with VDDCORE as the supply) and GPO13 will be configured as an output for nVDD_FAULT. Any register writes or OTP loads which can change this configuration are ignored until DA9021/22 has exited from POWER COMMANDER mode.

After the initial OTP read has completed, DA9021/22 informs the system that it is waiting for a programming sequence by driving nVDD_FAULT low. The software running on the PC monitors nVDD_FAULT and responds by downloading the values into the configuration registers within DA9021/22. nVDD_FAULT is automatically released after the release register is loaded.

There are two programming sequences performed in POWER COMMANDER mode. The first takes place between RESET and POWERDOWN mode and the second takes place between POWERDOWN and SYSTEM mode. Two release registers are used support these two programming sequences:

- a write to register R106 will end the first programming sequence
- a write to register R61 will end the second programming sequence

During these programming sequences any registers can be written to in any order The sequence will terminate after the appropriate release register has been written to.

NOTE
To correctly configure DA9021/22 registers, R10 to R105 should be programmed during the first sequence and FAULT LOG register (R9) bit VDD_FAULT has to be cleared by writing a '1'. Registers R14 and R43 to R61 should be programmed during the second sequence.

The host can determine whether DA9021/22 is in the first or second programming sequence by reading the FAULT LOG register. If a read of the FAULT LOG register bit VDD_FAULT returns a zero, then the DA9021/22 is in the second programming sequence otherwise it is in the first.

After the first programming sequence has been completed DA9021/22 will be in POWERDOWN mode. Progression from this mode is determined by the values programmed for SYS_EN and AUTO_BOOT.

If DA9021/22 has been directed to progress from POWERDOWN mode then it will drive pin nVDD_FAULT low for a second time to request that the software performs the second programming sequence.

Once the second programming sequence has completed, the progress of the power-up sequence will be controlled by the values loaded during the programming sequence.

The programmed configuration can be identified by reading the fuse register CONFIG_ID.

NOTE
During POWER COMMANDER mode the fault detection status bit VDD_FAULT and the level at the related pin nVDD-FAULT do not match and do not indicate a low voltage level at VDDOUT. An enabled shutdown from the 5 s assertion of GPIO14/15 will be ignored during POWER COMMANDER mode.

13.6 Start up from NO POWER mode

13.6.1 Power-On-Reset (nPOR)

To guarantee the correct start-up of DA9021/22 an internal power-on-reset nPOR (active low) is generated for the initial connection of either a supply or a good battery following a phase of not being supplied with sufficient power. To allow DA9021/22 to start up even if the main battery is completely discharged an internal VDDREF rail is used to supply the charger blocks, comparators and the control logic. If no charger is present VDD_REF is switched to the main battery

While VDDCORE < VPOR_UPPER the internal nPOR is asserted and DA9021/22 will not switch on (NO-POWER mode). When VDDCORE rises above VPOR_UPPER the nPOR is negated, LDOCORE will be switched on, the BCD counter and FAULT_LOG register is reset and DA9021/22 progresses to RESET mode.

When an external charger is detected (rising edge on VBUS_DET) having no or only a deep discharged main battery connected to DA9021/22 the internal charger, oscillator and bandgap are enabled and the whole OTP trim block is read and stored to the register bank. If the supply voltage is below the charger detection threshold (VCH_THR) after a debouncing period of tdelay (10 ms to allow for de-bouncing of the input signal and the bandgap reference to settle) the device returns to RESET mode.

If the external charger is still present and the CHG_ATT comparator flags a minimum of 100 mV head room from charger input VCENTER to VDDOUT, DA9021/22 starts up the charger buck to supply VDDOUT at the default current limit (loaded from OTP) and starts supplying power to VDDOUT, which enables an application start-up also with a flat battery. When VDDOUT rises above VDDOUT_MIN DA9021/22 enters the POWERDOWN mode. If this does not happen within 128 ms it will return to RESET mode.

From POWERDOWN mode DA9021/22 will continue with powering up supplies if the power domain SYSTEM was asserted via input port (or set via OTP settings) and AUTO_BOOT was enabled (or a valid wakeup event has happened). The simplified flow diagram (Figure 34) shows the start-up events and an example of a typical initial sequence.

If DA9021/22 causes a RESET from an under voltage detected within 10 s after releasing nRESET (the start-up initiating supply is not strong enough to supply the application) DA9021/22 will assert VDD_START inside the FAULTLOG register and temporarily disable AUTO_BOOT for the consecutive start-up (enabling only the battery charger and start waiting for a valid wakeup event).

Only events generated from user inputs (GPIs or nONKEY) trigger a wakeup during this emergency charging but a flashing LED connected to GPIO 10 or 11 can be automatically enabled via control BLINK_FRQ. AUTO_BOOT is set back to its default value when the battery voltage VBAT > VCHG_BAT - VCHG_DROP.

A similar start-up to POWERDOWN mode will be performed when a pre-charged battery is inserted (VDDOUT>VDD_FAULT_UPPER) following a state where DA9021/22 has not been provided with any supply voltage as shown in Figure 37

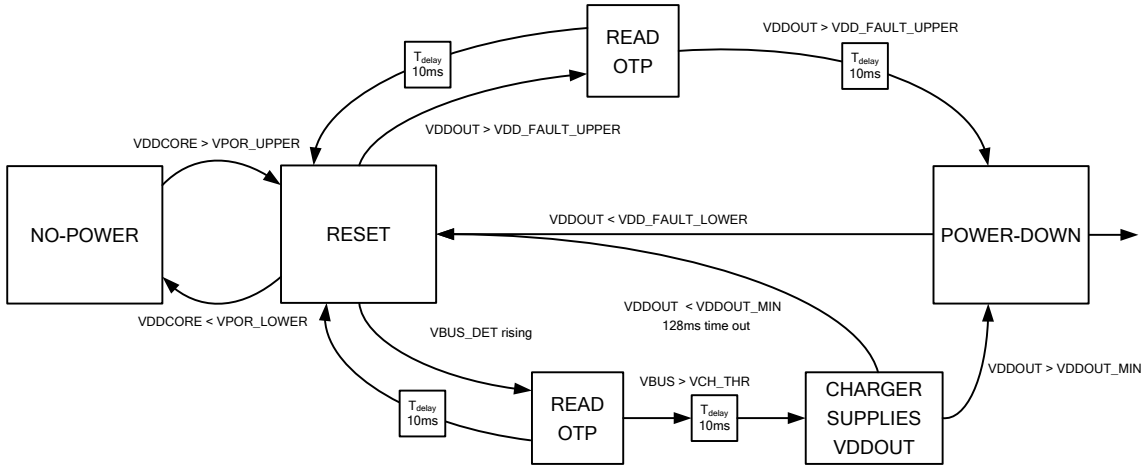

Figure 34: Start-up from NO-POWER to POWERDOWN mode

13.6.2 Application wakeup

A valid wakeup event (for example nONKEY, SYS_EN, RTC-alarm or a trigger from GPIOs) initiates an application power up from POWERDOWN mode. The wakeup from GPIOs (or selected alternative features that use a shared GPI event) has to be enabled via GPIx_MODE and can be masked in addition with the related nIRQ mask. After a wakeup condition is detected the OTP values for registers R14 and R43 to R61are read. These values re-configure the supplies and the sequencer timer.

If the POWERDOWN mode was reached by progressing from RESET mode the power sequencer can also be started without waiting for a wakeup event if AUTO_BOOT was asserted. DA9021/22 will assert the EXT_WAKEUP signal toward the host processor and if the power domains are not pre-enabled by OTP the host processor has to control the further application start-up (for example via the power domain enable lines). Alternatively DA9021/22 continues stand-alone powering up the OTP enabled domains via the power domain sequencer. A start-up from RESET mode powers up the application automatically only if SYS_EN is asserted from the host processor or was default set from OTP.

Table 36: Wakeup events

Signal / Condition	Wakeup	User event	System event	IRQ
Charger attach: E_VBUS_DET	X		X	X
Charger removal: E_VBUS_REM	X		X	X
VDDOUT low prewarning: E_VDD_LOW	X		X	X
RTC alarm: E_ALARM	X		X	X
Sequencing finished: E_SEQ_RDY			X	X
Voltage comparator: E_COMP_1V2	X		X	X
Pressed On key: E_nONKEY	X	X		X
End of battery charging: E_CHG_END	X		X	X
Battery temperature: E_TBAT			X	X
Manual ADC result ready: E_ADC_EOM			X	X
GPIOs: E_GPIx	X	X		X
ADC 4, 5, threshold: via GPI01	X		X	X
SYS_EN, PWR_EN, PWR1_EN (passive to active transition): via GPIO8, 9, 10	X		X	X
HS-2-wire interface: via GPIO14	X		X	X

13.6.3 Power supply sequencer

The start-up of DA9021/22 supplies is performed with a sequencer that contains a programmable step timer, a variable ID array of time slot pointers and four predefined pointers (SYSTEM_END, POWER_END, MAX_COUNT and PART_DOWN). The sequencer is able to control up to 14 IDs (3 buck converters, 5 LDOs, 4 feedback pin level controls, a Wait ID (GPI10) and a POWERDOWN register), which can be grouped in three power domains. The power domains have configurable size and their borders are described by the location pointers SYSTEM_END, POWER_END and MAX_COUNT.

The lowest level power domain SYSTEM starts at step one and ends at the step that is described by the location pointer SYSTEM_END. The second level domain POWER starts at the successive step and ends at POWER_END. The third level domain POWER1 starts at the consecutive step and ends at MAX_COUNT. The values of pointers SYSTEM_END, POWER_END and MAX_COUNT are predefined in OTP registers and should be configured to be SYSTEM_END < POWER_END < MAX_COUNT.

The domain SYSTEM by can be understood as a basic set of supplies that are mandatory to maintain the application in (at least) a standby/hibernate mode. If enabled via control OTPREAD_EN all supplies of DA9021/22 and the sequencer timer (registers R14 and R43 to R61) are configured with the default value from OTP before powering up the domain SYSTEM. This will cause a reconfiguration of all supplies that have been powered down with a preset voltage level.

The second level domain POWER includes additional supplies required to power the main application and to set DA9021/22 in to ACTIVE mode.

POWER1 can be understood as a subdomain of POWER that can be used for additional hardware/software initiated control of supply blocks during ACTIVE mode (for example for a sub-application like WLAN or GSM baseband). Supplies in domain POWER and POWER1 can be voltage pre-configured and by that sequentially changed during powering down, but will not be reset to their default values from OTP unless there is a power-up from domain SYSTEM.

NOTE
Running applications should be configured to ACTIVE mode (domain POWER is up) and pointer POWER_END has to be at least one time slot higher than SYSTEM_END.

All buck converters and five LDOs of DA9021/22 have received a unique sequencer ID. The power-up sequence is then defined by an OTP register bank that contains a series of supplies (and other features) which are pointing towards a sequencer time slot. Several supplies can point in to the same time slot and by that will be enabled by the sequencer in parallel. Time slots that have no IDs pointing towards it are dummy steps that insert a configurable time delay (marked as 'D' in Figure 36). Supplies that are not pointing towards a sequencer time slot (with a step number greater than zero and less than MAX_COUNT) will not be enabled by the power sequencer and have to be controlled individually by the host (via the power manager bus).

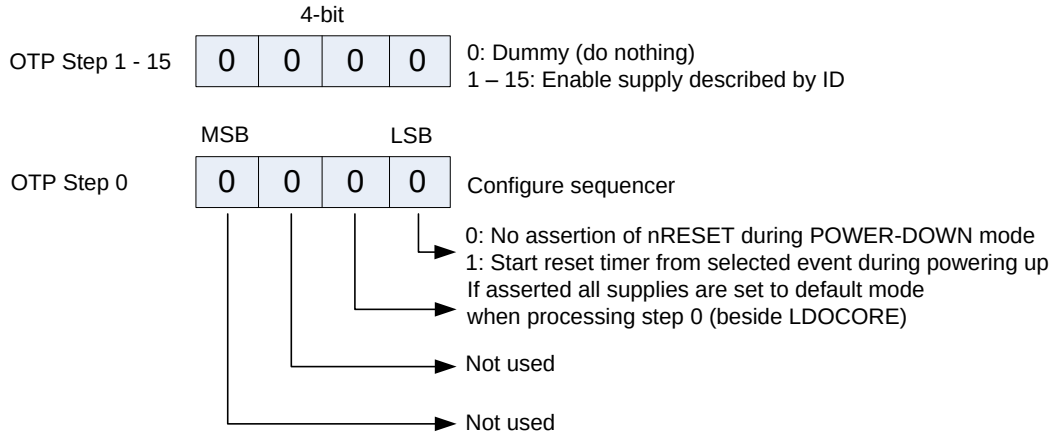

Figure 35: Content of OTP power sequencer register cell

During power-up the sequencer will start at step 0 where the sequencer behaviour is configured. If DEF_SUPPLY is asserted this includes an optional enabling of supplies (depending on the OTP default settings of the supplies). If SYS_EN was asserted via port (or OTP) the sequencer will assert the READY signal (if selected for the feedback pin) and continue with step 1 which enables all supplies (features) from the OTP register bank that are pointing towards step 1. The sequencer will progress until it has reached the position of pointer SYSTEM_END. Now all supplies of the first power domain SYSTEM are enabled and DA9021/22 will release the READY signal and assert the E_SEQ_RDY interrupt.

NOTE
It is recommended that supplies having an asserted ENABLE bit in the OTP are not controlled via IDs of the power sequencer if DEF_SUPPLY is asserted (IDs of these supplies should point into time slot 0).

Table 37: Power sequencer controlled actions

Action	Sequencer time slot	Comment
Step 0: Configure power sequencer	ID_0	
LDO1_EN	LDO1_STEP	
LDO3_EN	LDO3_STEP	
LDO7_EN	LDO7_STEP	
LDO9_EN	LDO9_STEP	
LDO10_EN	LDO10_STEP	
PD_DIS	PD_DIS_STEP	
BCORE_EN	BUCKCORE_STEP	
BPRO_EN	BUCKPRO_STEP	DA9021 only
BMEM_EN	BUCKMEM_STEP	
BPERI_EN	BUCKPERI_STEP	DA9021 only

Action	Sequencer time slot	Comment
Assert/Release GP_FB2	GP_RISE1_STEP	
Assert/Release GP_FB2	GP_RISE2_STEP	
Release/Assert GP_FB2	GP_FALL1_STEP	
Release/Assert GP_FB2	GP_FALL2_STEP	
Wait for active state at GPI 10	WAIT_STEP	

NOTE
IDs (for example supplies) not controlled by the sequencer should point into step 0.

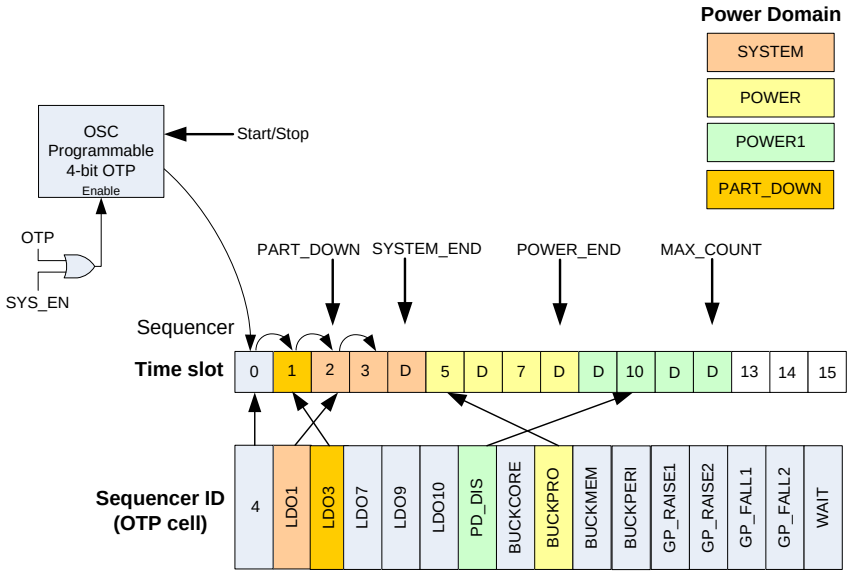

Figure 36: Allocation of supplies (IDs) into to the sequencer time slots

To continue the sequencer checks for PWR_EN to be asserted (via PWR_EN port, register write or OTP). When this is available the feedback signal READY will be asserted and supplies of domain POWER will be enabled sequentially. The sequencer stops at step POWER_END, releases the READY signal, asserts PWR_UP, asserts the E_SEQ_RDY interrupt, starts the ACTIVE mode of DA9021/22 and releases an asserted EXT_WAKEUP signal.

A third power domain POWER1 can be enabled from PWR1_EN (asserted via PWR1_EN port, register write or OTP). It enables all consecutive supplies until step MAX_COUNT has been reached, asserts PWR1_UP and asserts the E_SEQ_RDY interrupt. The READY signal will be asserted as long as IDs are processed (if enabled). The domain POWER1 offers no dedicated status indicator, but the end of its power-up sequence can be selected to start the RESET timer.

The delay between the steps of a sequence is controlled via a 4-bit OTP programmable timer unit SEQ_TIME with a default delay of 1285 µs per step (minimum 32 µs and max. 816 ms). The delay time between individual supplies can be extended by leaving consecutive steps having no IDs pointing to it (dummy supply), which provides an independent delay configured via control SEQ_DUMMY. The delay timers are configured with their default values from OTP (R43) every time before powering up inside domain SYSTEM.

NOTE
During entering and leaving a power domain a 32 µs delay will always be inserted.

When DA9021/22 is powering down, the sequencer will disable the supplies in reverse order and timing. Supplies that are configured with a preset value (LDOx_CONF or BUCKxxx_CONF bit is set) will not be disabled but configured with their preset voltage when the related time slot/ID is

processed. If a domain contains at least one supply with an assigned preset, the power domain status indicator (PWR1_UP, PWR_UP) will not be released. Otherwise the indicator will be released before the first supply of a power domain is disabled.

If powering down was initiated from releasing PWR_EN1 the sequencer will stop to modify the supplies where the domain pointer POWER_END reached. If PWR_EN was disabled the domain POWER1 will be powered down followed by POWER until the sequencer reaches pointer SYSTEM_END. If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0.

If the low power mode was initiated by asserting the control register DEEP_SLEEP the sequencer will first power down POWER1 and POWER, then continue with SYSTEM and stop when pointer PART_DOWN has been reached (PART_DOWN has to point into domain SYSTEM). If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0 (ignoring the PART_DOWN pointer).

The sequencer asserts the E_SEQ_RDY interrupt on reaching the target pointer position. During processing step 0 all supplies (except LDOCORE) can be set to their OTP default state (if bit DEF_SUPPLY of step 0 is asserted), but the voltage levels are unchanged. Due to the risk of in-rush currents on the battery the default enable of more than a single supply at step 0 is not recommended.

Asserting control register bit SHUTDOWN will first power down to step 0 and then force DA9021/22 to RESET mode. DA9021/22 features (for example the OUT_32K output buffer or an auto ADC measurement) can be disabled temporarily in POWERDOWN mode via register PD_DIS. The timing for processing PD_DIS can be defined by the placement of PD_DIS inside the sequence. Features asserted in PD_DIS are re-enabled when PD_DIS is processed during the next power-up sequence. If the READY signal is enabled, it will be asserted during processing the IDs for powering down.

NOTE
Any reconfiguration of supplies from the host in ACTIVE mode will not affect the domain status indicators (SYS_UP, and PWR_UP). During sequencing (indicated from DA9021/22 via signal READY or the E_SEQ_RDY interrupt) the host is not allowed to send additional power mode transition requests (via power manger interface or power domain enable lines).

A CONDITIONAL mode transition can be achieved using ID WAIT_STEP. If pointing into the sequence the progress of an initiated mode transition can be synchronised, for example with the state of a host that is indicated via a signal connected to GPI10. Via GPIO10_ MODE a security time-out of 500 ms can be selected, that will trigger a power down to RESET mode (including the assertion of WAIT_SHUT inside register FAULT_LOG) if E_GPI10 was not asserted until then.

NOTE
In the case of a shutdown sequence towards RESET mode (or POWERDOWN from fault condition) any waiting from ID WAIT_STEP will be skipped.

When powering up from NO_POWER mode ID WAIT_STEP can alternatively be used as a configurable delay to allow the 32 kHz oscillator to stabilise before the TTL signal is provided at the OUT_32K output pin (see register WAIT_CONT).

The configuration at sequencer step 0 (nRES_MODE) enables the assertion of nRESET at the end of a power down sequence and starts the reset timer during the consecutive powering up.

This is also true for partial POWERDOWN mode, when the sequencer powers down to pointer position PART_DOWN.

The reset timer will start to run from the selected event RESET_EVENT and release the nRESET port after the reset timer has expired (see also description for powering up from NO-POWER/RESET mode.

NOTE
By connecting TP to VDDCORE DA9021/22 can be configured to load control register default values from the HS 2-wire interface instead from OTP cells. During start-up the power sequencer will then assert pin nVDD_FAULT (set to zero) and wait until an external device has loaded default values into the control registers R10 to R106 after RESET MODE (if VDD_FAULT is asserted), R14 and R43 to R61 when leaving POWERDOWN mode (if VDD_FAULT is not asserted) via HS 2-wire interface. The host has to clear the FAULT_LOG register after loading R10 to R106. When the last register has been loaded nVDD_FAULT will be released and the start-up sequence is continued. During this mode the settings of GPI14 and 15 will be ignored (pins are assigned as 2-wire interface supplied from VDDCORE).

14 Register page control

Table 38: Register page control

Register address	Bit	Type	Label	Default	Description
R0 to R128 PAGE_CON_P0	6:0	R		0000000	
	7	RW	REG_PAGE	0	0: selects register R1 to R127 1: selects register R129 to R255

14.1 Register page 0

14.1.1 Power manager control and monitoring

The STATUS register reports the current value of the various signals at the time that it is read out.

NOTE
All the status bits have the same polarity as their corresponding signals.

Table 39: STATUS_A

Register address	Bit	Type	Label	Default	Description
R1 STATUS_A	0	R	nONKEY	1	Current nONKEY state
	4	R	VBUS_DET	0	0: VBUS voltage not detected (@ VBUS pin) 1: VBUS voltage detected
	6	R	VBUS_SEL	0	0: No valid charger at VBUS (over voltage) 1: VBUS charger selected
	7	R	VDAT_DET	0	0: USB host/hub detected (100 mA) 1: Dedicated or host/hub charger detected

Table 40: STATUS_B

Register address	Bit	Type	Label	Default	Description
R2 STATUS_B	0	R	CHG_ATT	0	0: No charger attached (drop from VCENTER to VDDOUT < 100 mV) 1: Charger attached (drop from VCENTER to VDDOUT > 100 mV)
	1	R	CHG_PRE	0	Asserted if charger is in pre-charge mode
	2	R	CHG_LIM	0	0: Charging as configured 1: Charge current in constant current mode reduced to less than ICHG_THD
	3	R	CHG_END	0	0: Battery charging 1: Battery charging completed cleared automatically when starting charging/re-charging
	4	R	CHG_TO	0	0: Battery charging timer OK or disabled 1: Battery charging timeout caused charging finished cleared automatically when starting charging/re-charging and when loading TCTR
	5	R	GP_FB2	0	Status of GP_FP2 pin: configured from power sequencer

Register address	Bit	Type	Label	Default	Description
	6	R	SEQUENCING	0	0: Sequencer is idle 1: Sequencer is processing IDs
	7	R	COMP_DET	0	0: Comparator at ADCIN5 (1.2 V) not asserted 1: Comparator asserted

Table 41: STATUS_C

Register address	BIT	TYPE	LABEL	DEFAULT	DESCRIPTION
R3 STATUS_C	0	R	GPI0	0	GPI0 level or ADCIN4 threshold indicator ('1' when overriding high limit)
	1	R	GPI1	0	GPI1 level or ADCIN5 threshold indicator ('1' when overriding high limit)

Table 42: STATUS_D

Register address	Bit	Type	Label	Default	Description
R4 STATUS_D	0	R	GPI8	0	GPI8/SYS_EN level
	1	R	GPI9	0	GPI9/PWR_EN level
	2	R	GPI10	0	GPI10/PWR1_EN level
	4	R	GPI12	0	GPI12/EXT_WAKEUP/READY level
	5	R	GPI13	0	GPI13 level
	6	R	GPI14	0	GPI14 level
	7	R	GPI15	0	GPI15 level

The EVENT registers hold information about events that have occurred in DA9021/22. Events are triggered by a change in the status registers that contains the status of monitored signals. When an EVENT bit is set in the event register the nIRQ signal is asserted (unless the nIRQ is masked by a bit in the IRQ mask register). The nIRQ is also masked during the power-up sequence and will not be released until the event registers have been cleared.

The IRQ triggering event register is cleared from the host by writing a byte containing a '1' at the bit to be reset (bits written containing a '0' will leave the related event register bits unchanged thus avoiding accidentally clearing events that occur after the initial event register read). New events that occur during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Table 43: EVENT_A

Register address	Bit	Type	Label	Default	Description
R5 EVENT_A	1	R	E_VBUS_DET	0	VBUS 4.4 V detection caused event
	3	R	E_VBUS_REM	0	VBUS removal caused event
	4	R	E_VDD_LOW	0	VDDOUT less than VDDOUT_MON threshold caused event
	5	R	E_ALARM	0	RTC alarm caused event
	6	R	E_SEQ_RDY	0	Sequencer reached stop position caused event
	7	R	E_COMP_1V2	0	1.2 V comparator caused event

Table 44: EVENT_B

Register address	Bit	Type	Label	Default	Description
R6 EVENT_B	0	R	E_nONKEY	0	nONKEY caused event
	3	R	E_CHG_END	0	Battery charging complete caused event
	4	R	E_TBAT	0	Battery over/ under temp caused event
	5	R	E_ADC_EOM	0	ADC manual conversion result ready caused event

Table 45: EVENT_C

Register address	Bit	Type	Label	Default	Description
R7 EVENT_C	0	R	E_GPI0	0	GPI event according to active state setting/ ADCIN4 high / low threshold exceeded caused event
	1	R	E_GPI1	0	GPI event according to active state setting/ ADCIN5 high / low threshold exceeded caused event

Table 46: EVENT_D

Register address	BIT	TYPE	LABEL	DEFAULT	DESCRIPTION
R8 EVENT_D	0	R	E_GPI8	0	GPI event according to active state setting/SYS_EN assertion caused event
	1	R	E_GPI9	0	GPI event according to active state setting/PWR_EN assertion caused event
	2	R	E_GPI10	0	GPI event according to active state setting/PWR1_EN assertion caused event
	4	R	E_GPI12	0	GPI event according to active state setting
	5	R	E_GPI13	0	GPI event according to active state setting
	6	R	E_GPI14	0	GPI event according to active state setting/Event caused from host addressing HS-2-wire interface
	7	R	E_GPI15	0	GPI event according to active state setting

The nIRQ line will be released only when all events have been cleared from the host processor by writing a '1' to each asserted event bit (to prohibit missing events it is recommended to clear event bits individually).

Table 47: FAULT_LOG

Register address	Bit	Type	Label	Default	Description
R9 FAULT_LOG	0	R			
	1	R	VDD_FAULT	1	Power down by VDDOUT under voltage detect
	2	R	VDD_START	0	Power down by VDDOUT under voltage detect within 10 s from releasing nRESET
	3	R	TEMP_OVER	0	Junction over temperature detected
	4	R			
	5	R	KEY_SHUT	0	Power down by a long press of the nONKEY or GPI14 and GPI15 in parallel
	6	R	nSD_SHUT	0	Power down by assertion of port nSHUTDOWN
	7	R	WAIT_SHUT	0	Power down by time out of ID WAIT_STEP

Table 48: IRQ_MASK_A

Register address	Bit	Type	Label	Default	Description
R10 IRQ_MASK_A	0	R/W		1	RESERVED
	1	R/W	M_VBUS_VLD	0	Mask VBUS 4.4 V detection caused nIRQ
	2	R/W		1	RESERVED
	3	R/W	M_VBUS_REM	0	Mask VBUS removal caused nIRQ
	4	R/W	M_VDD_LOW	0	Mask VDDOUT low caused nIRQ
	5	R/W	M_ALARM	0	Mask RTC alarm caused nIRQ
	6	R/W	M_SEQ_RDY	0	Mask Sequencer reached stop position caused nIRQ
	7	R/W	M_COMP_1V2	0	Mask 1.2 V comparator caused nIRQ

Table 49: IRQ_MASK_B

Register address	Bit	Type	Label	Default	Description
R11 IRQ_MASK_B	0	R/W	M_nONKEY	0	Mask nONKEY caused nIRQ
	1	R/W		1	RESERVED
	2	R/W		1	RESERVED
	3	R/W	M_CHG_END	0	Mask battery charging complete caused nIRQ
	4	R/W	M_TBAT	0	Mask battery over / under temp caused nIRQ
	5	R/W	M_ADC_EOM	0	Mask ADC manual conversion result

Register address	Bit	Type	Label	Default	Description
					ready caused nIRQ
	6	R/W		1	RESERVED
	7	R/W		1	RESERVED

Table 50: IRQ_MASK_C

Register address	Bit	Type	Label	Default	Description
R12 IRQ_MASK_C	0	R/W	M_GPI0	0	Mask GPI caused/ ADCIN4 high / low threshold exceeded caused nIRQ
	1	R/W	M_GPI1	0	Mask GPI caused/ ADCIN5 high / low threshold exceeded caused nIRQ, assert for LDO hardware control
	2	R/W		1	RESERVED
	3	R/W		1	RESERVED
	4	R/W		1	RESERVED
	5	R/W		1	RESERVED
	6	R/W		1	RESERVED
	7	R/W		1	RESERVED

Table 51: IRQ_MASK_D

Register address	Bit	Type	Label	Default	Description
R13 IRQ_MASK_D	0	R/W	M_GPI8	0	Mask GPI/SYS_EN caused nIRQ
	1	R/W	M_GPI9	0	Mask GPI/PWR_EN caused nIRQ
	2	R/W	M_GPI10	0	Mask GPI/PWR1_EN caused nIRQ
	3	R/W		1	RESERVED
	4	R/W	M_GPI12	0	Mask GPI caused nIRQ, assert for LDO hardware control
	5	R/W	M_GPI13	0	Mask GPI caused nIRQ
	6	R/W	M_GPI14	0	Mask GPI/HS-2-wire caused nIRQ
	7	R/W	M_GPI15	0	Mask GPI caused nIRQ

Table 52: CONTROL_A

Register address	Bit	Type	Label	Default	Description
R14 CONTROL_A	0	R/W	SYS_EN Note 1	1	Target status of power domain SYSTEM: state of GPI8 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_8_PIN)
	1	R/W	PWR_EN Note 2	1	Target status of power domain POWER: state of GPI9 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_9_PIN)

Register address	Bit	Type	Label	Default	Description
	2	R/W	PWR1_EN Note 3	0	Target status of power domain POWER1: state of GPI10 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_10_PIN)
	4	R/W	PM_I_V	0	nONKEY, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN are supplied from: 0: VDDCORE 1: VDD_IO
	6	R/W	PM_O_TYPE	0	nRESET, nIRQ output are: 0: Push-pull 1: Open drain
	7	R/W	GPI_V	0	GPIs (not configured as PM control inputs) are supplied from: 0: VDDCORE 1: VDD_IO

Note 1 SYS_EN hardware control can be configured as high or low active via GPIO_8_TYPE

Note 2 PWR_EN hardware control can be configured as high or low active via GPIO_9_TYPE

Note 3 PWR1_EN hardware control can be configured as high or low active via GPIO_10_TYPE

Table 53: CONTROL_B

Register address	Bit	Type	Label	Default	Description
R15 CONTROL_B	0	R/W	BUCK_MERGE	0	Has to be set if the outputs of BUCKCORE and BUCKPRO are merged towards a single coil; the control from BUCKPRO registers is disabled
	1	R/W	ACT_DIODE	0	Battery provides power 0: through internal active diode path (mandatory, if no external FET connected!) 1: through internal active diode and external power FET
	2	R/W	AUTO_BOOT	1	0: Start-up of power sequencer after progressing from RESET mode requires a valid wakeup event 1: PMIC automatically starts power sequencer after progressing from RESET mode
	3	R/W	OTPREAD_EN	1	0: OTP read after POWERDOWN mode disabled 1: Power supplies are configured with OTP values when leaving POWERDOWN mode
	5	R/W	WRITE_MODE	1	2-wire multiple write mode (setting used for both 2-wire interfaces) 0: Page Write mode 1: Repeated Write mode
	6	R/W	DEEP_SLEEP	0	If set to ‘1’ DA9021/22 goes to deep sleep mode (sequencer stops at pointer

Register address	Bit	Type	Label	Default	Description
					PART_DOWN). The bit is cleared back to '0' automatically before powering up from POWERDOWN mode
	7	R/W	SHUTDOWN	0	If set to '1' the sequencer powers down to RESET mode The bit is cleared back to '0' automatically before leaving the RESET mode

Table 54: CONTROL_C

Register address	Bit	Type	Label	Default	Description
R16 CONTROL_C	0	R/W	PM_FB1_PIN	0	0: Feedback pin indicates EXT_WAKEUP events (active high) 1: Feedback pin is used as READY indicator, signalling ongoing power mode transitions (power sequencer and DVC) (active low)
	1	R/W	PM_FB2_PIN	0	0: Feedback pin indicates the status of domain POWER (active high PWR_UP) 1: Feedback pin is used as a configurable GP_FB indicator, that is asserted from the power sequencer
	4:2	R/W	DEBOUNCING	001	GPI, nONKEY and nSHUTDOWN debounce time 000: no debounce time 001: 10.24 ms 010: 20.48 ms 011: 40.96 ms 100: 102.4 ms 101: 1024 ms 110: 2048 ms 111: 5120 ms
	6:5	R/W	BLINK_FRQ	11	GPO10/GPO11 flashing frequency 00: no blinking 01: every second 10: every two seconds 11: every two seconds enabled during PRE-CHARGE mode and emergency charging
	7	R/W	BLINK_DUR	0	GPO10/GPO11 flashing on-time 0:10 ms 1:40 ms

Table 55: CONTROL_D

Register address	Bit	Type	Label	Default	Description
R17 CONTROL_D	2:0				
	4	R/W	nONKEY_SD	0	0: Disables shutdown via nONKEY 1: Enables shutdown via nONKEY
	5	R/W	GPI14_15_SD	0	0: Disables shutdown via parallel assertion of GPI14 and GPI15 1: Enables shutdown via GPI14 & GPI15
	6	Reserved		0	

Table 56: PD_DIS

Register address	Bit	Type	Label	Default	Description
R18 PD_DIS	0	R/W	GPIO_PD	0	0: GPIO extender enabled during POWERDOWN 1: Auto-Disable of features configured as GPIO pins during POWERDOWN mode and force the detection of a pending Active state on GPIs by re-enabling the pin through a passive state of the related GPI status register
	1	R/W	GP-ADC_PD	1	0: ADC/TSI measurements continue during POWERDOWN as configured 1: Auto-Disable auto measurements on A4, A5, A6, A7(TSI) and manual measurement on all channels during POWERDOWN mode; if no auto measurements for charging and on A0 are required switch off the ADC completely
	2	R/W	PM-IF_PD	1	0: Power manager interface not disabled during POWERDOWN 1: Auto-Disable of Power manager interface during POWERDOWN mode
	3	R/W	HS-2-wire_PD	1	0: HS-2-wire not disabled during POWERDOWN 1: Auto-Disable of HS-2-wire interface during POWERDOWN mode
	4	R/W	CHG_PD	0	0: Enables battery charging during POWERDOWN 1: Auto-Disable battery charging during POWERDOWN mode
	5	R/W		1	RESERVED
	6	R/W	OUT_32K_PD	1	0: Enables OUT_32K during POWERDOWN 1: Auto-Disable OUT_32K output buffer during POWERDOWN mode and auto-enable during power-up from NO-POWER mode when executing this ID
	7	R/W	PM-CONT_PD	0	0: SYS_EN, PWR_EN, PWR1_EN enabled during POWERDOWN 1: Auto-Disable of SYS_EN, PWR_EN

Register address	Bit	Type	Label	Default	Description
					and PWR1_EN during POWERDOWN mode and force the detection of a pending Active state by re-enabling the pin through a passive state of the related GPI status register

Table 57: INTERFACE

Register address	Bit	Type	Label	Default	Description
R19 INTERFACE	0	R37	IF_TYPE	0	0: Power manager interface is 4-wire 1: Power manager interface is 2-wire
	1	R	CPOL	0	4-wire interface clock polarity 0: SK is low during idle 1: SK is high during idle
	2	R	CPHA	0	4-wire interface clock phase (see Table 34: 4-wire clock configurations)
	3	R	R/W_POL	1	4-wire: Read/Write bit polarity 0: Host indicates reading access via R/W bit = ‘0’ 1: Host indicates reading access via R/W bit = ‘1’
	4	R	nCS_POL	1	4-wire chip select polarity 0: nCS is low active 1: nCS is high active
	7:5	R	IF_BASE_ADDR	100	3 MSB of 2-wire control interfaces base address XXX10000 10010000 = 0x90 write address of PM 2-wire interface 10010001 = 0x91 read address of PM 2-wire interface 10010010 = 0x92 write address of HS-2-wire interface 10010011 = 0x93 read address of HS-2-wire interface

Table 58: RESET

Register address	Bit	Type	Label	Default	Description
R20 RESET	5:0	R/W	RESET_TIMER	000101	000000: RESET disabled 000001: 1.024 ms 000010: 2.048 ms 000011: 3.072 ms 000100: 4.096 ms 000101: 5.120 ms …. 011110: 30.720 ms 011111: 31.744 ms 100000: 32.768 ms 100001: 65.536 ms 100010: 98.304 ms ….. 111101: 983.040 ms 111110: 1015.808 ms 111111: 1048.576 ms
	7:6	R/W	RESET_EVENT	01	RESET timer started by 00: EXT_WAKEUP 01: SYS_UP 10: PWR_UP 11: PWR1_UP (internal signal)

15 GPIO Extender

The DA9021/22 includes a GPIO extender that offers VDDOUT-tolerant (5.5 V max) general purpose input/output pins; each controlled by registers from the host.

NOTE
The input voltage has to be lower than the VDD_IO level

The GPIO ports are pin-shared with ports from GP-ADC, HS-2-wire interface and signals from the power manager and can be individually assigned. Configuration settings and events from several GPIx ports are shared with alternative features. If, for example, ADCIN5 was selected overriding the configured thresholds this will trigger a GPI1 event that generates a maskable GPI1 interrupt. The GPI active HIGHLOW setting from GPIOx_TYPE register and the selection of supply rail (and pull-up resistor) is also valid for the alternative port features selected via GPIOx_PIN (for example SYS_EN, PWR_EN and PWR1_EN). The same applies to GPIOx_MODE to enable triggering a wakeup event (ADCIN4, ADCIN5, SYS_EN, PWR_EN, PWR1_EN, HS-2-wire interface) for the alternative features.

In ACTIVE and POWERDOWN modes the GPIO extender can continuously monitor the level of ports that are selected as general purpose inputs. GPIs are supplied from the internal rail VDDCORE or VDD_IO and can be configured to trigger events in active high or active low mode. The input signals can be debounced or directly change the state of the assigned status register GPIx to high or low. Whenever the status has changed to its configured active state (edge sensitive) the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked inside the nIRQMASK register).

GPI0 13 will generate a system wakeup if debouncing is enabled. In debouncing off mode GPI 12 enables/disables LDO9, the minimum enable time is 100 µs. Events on GPI10 can be used to control the progress of the power sequencer. Processing ID WAIT_STEP will cause the sequencer to wait until GPI 10 changes into active state.

If defined as an output the GPO can be configured as open-drain or push-pull. The supply rail is VDD_IO. When selecting VDD_IO in open-drain mode, there is an internal pull-up resistor against this rail, otherwise an external pull-up resistor towards the target voltage level is required. The output state will be assigned as configured by the GPIO register bit GPIOx_MODE.

GPO 10 is a high power GPO port, where the maximum sink current is rated to be 15 mA and the maximum source current is 4 mA. This enables driving LEDs with optional RTC timer controlled flashing.

GPO 14 and 15 are high power GPO ports able to sink up to 30 mA and include an optional PWM control. The PWM control can also be made to dim the brightness between its current value and a new value at a rate of 32 ms per step.

15.1 GPIO control

Table 59: GPIO0 to 1

Register address	Bit	Type	Label	Default	Description
R21 GPIO_0-1	1:0	R/W	GPIO0_PIN	00	PIN assigned to 00: ADCIN4 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO0_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode
	3	R/W	GPIO0_ MODE	1	0: GPI/ADCIN4: debouncing off GPO: Sets output to low level 1: GPI/ADCIN4: debouncing on and generate wakeup GPO: Sets output to high level
	5:4	R/W	GPIO1_PIN	00	PIN assigned to 00: ADCIN5/1.2 V comparator 01: GPI (LDO4 hardware control) 10: GPO (open drain) 11: GPO (push-pull)
	6	R/W	GPIO1_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode
	7	R/W	GPIO1_ MODE	1	0: GPI/ADCIN5: debouncing off, Set LDO4_EN when GPI transfers to active state (reset when GPI gets to passive state) GPO: Sets output to low level 1: GPI: debouncing on, no LDO4_EN control ADCIN5: debouncing on and generate wakeup GPO: Sets output to high level

Table 60: RESERVED

Register address	Bit	Type	Label	Default	Description
R22, R23, R24	7:0	R/W		11101110	RESERVED

Table 61: GPIO8 to 9

Register address	Bit	Type	Label	Default	Description
R25 GPIO_8-9	1:0	R/W	GPIO8_PIN	01	PIN and status register bit assigned to 00: SYS_EN (requires GPIO8_ MODE = '1') 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO8_TYPE	0	0: GPI/SYS_EN: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI/SYS_EN: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode
	3	R/W	GPIO8_ MODE	1	0: GPI: debouncing off GPO: Sets output to low level 1: GPI/SYS_EN: debouncing on and generate wakeup GPO: Sets output to high level
	5:4	R/W	GPIO9_PIN	01	PIN and status register bit assigned to 00: PWR_EN (requires GPIO9_ MODE = '1') 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO9_TYPE	0	**0: GPI/PWR_EN: active low** GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI/PWR_EN: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode
	7	R/W	GPIO9_ MODE	1	0: GPI: debouncing off GPO: Sets output to low level 1: GPI/PWR_EN debouncing on and generate wakeup GPO: Sets output to high level

Table 62: GPIO10 to 11

Register	Bit	Type	Label	Default	Description
R26 GPIO_10-11	1:0	R/W	GPIO10_PIN	01	PIN and status register bit assigned to 00 : PWR1_EN (requires GPIO10_ MODE = '1') 01 : GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO10_TYPE	0	0: GPI/PWR1_EN: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI/PWR1_EN: active high GPO: blinking from RTC counter, supplied from VDD_IO/ external pull-up in open-drain mode
	3	R/W	GPIO10_ MODE	1	0: GPI: debouncing off GPO: Sets output to low level (active low for blinking) Note 1 1: GPI/PWR1_EN: debouncing on and generate wakeup, time out from processing ID WAIT_STEP after 500 ms GPO: Sets output to high level (active high for blinking) Note 1
	7:4	R/W		1110	RESERVED

Note 1 Active low/high selection available from BC silicon

Table 63: GPIO12 to 13

Register address	Bit	Type	Label	Default	Description
R27 GPIO_12-13	1:0	R/W	GPIO12_PIN	11	PIN and status register bit assigned to 00: GP_FB1 (EXT_WAKEUP/READY) 01: GPI (LDO9 hardware control) 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO12_TYPE	0	0: GPI: active low GPO/GP_FB1: supplied from VDD_IO/internal pull-up for open-drain 1: GPI: active high GPO/GP_FB1: supplied from VDD_IO/external pull-up in open-drain mode
	3	R/W	GPIO12_ MODE	0	**0:** GPI: debouncing off, Set LDO9_EN when GPI transfers to active state (reset when GPI gets to passive state) **GPO: Sets output to low level** 1: GPI: debouncing on, no LDO9_EN control GPO: Sets output to high level
	5:4	R/W	GPIO13_PIN	00	PIN assigned to 00: nVDD_FAULT 01: GPI

Register address	Bit	Type	Label	Default	Description
					10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO13_TYPE	0	0: GPI: active low GPO/nVDD_FAULT: supplied from VDD_IO/internal pull-up for open-drain 1: GPI: active high GPO/nVDD_FAULT: supplied from VDD_IO/external pull-up in open-drain mode
	7	R/W	GPIO13_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Table 64: GPIO14 to 15

Register address	Bit	Type	Label	Default	Description
R28 GPIO_14-15	1:0	R/W	GPIO14_PIN	11	PIN assigned to 00: DATA (assigns GPIO15_PIN to CLK) 01: GPI 10: GPO (Open drain, PWM control) 11: GPO (Push-pull)
	2	R/W	GPIO14_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode
	3	R/W	GPIO14_ MODE	0	0: GPI: debouncing off, no wakeup HS-2-wire: no wakeup GPO: Sets output to low level (active low for blinking) 1: GPI:debouncing on and generate wakeup HS-2-wire: generate wakeup when interface was accessed GPO: Sets output to high level (active high for blinking)
	5:4	R/W	GPIO15_PIN	11	PIN assigned to 00: CLK (see GPIO14_PIN) 01: GPI 10: GPO (Open drain, PWM control) 11: GPO (Push-pull)

Register address	Bit	Type	Label	Default	Description
	6	R/W	GPIO15_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO/internal pull-up in open-drain mode DATA/CLK supplied from VDD_IO (Note 1): GPI: active high GPO: supplied from VDD_IO/external pull-up in open-drain mode DATA/CLK supplied from VDD_IO
	7	R/W	GPIO15_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level (active low for blinking) Note 2 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level (active high for blinking) Note 2

Note 1 In POWER COMMANDER mode the HS-2-wire interface is always supplied from VDDCORE

Note 2 Active low/high selection available from BC silicon

16 Power supply sequencer

The start-up of DA9021/22 supplies is performed with a sequencer. The sequencer is able to control up to 14 IDs (3 buck converter, 5 LDOs, 4 feedback pin level controls, a Wait ID and a POWERDOWN register), which can be grouped in three power domains. The power sequences for each domain have configurable size.

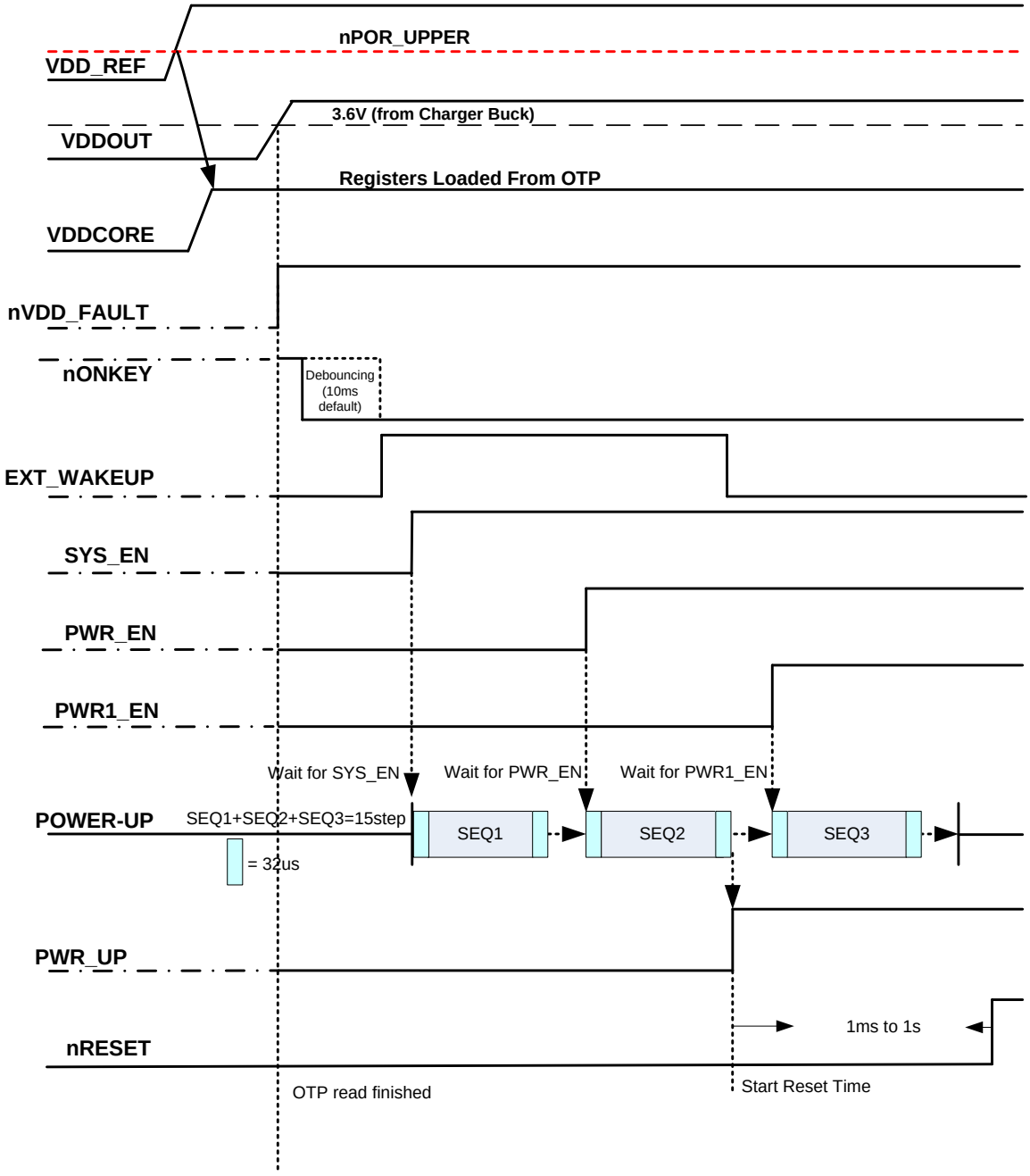

Figure 37: Typical power-up timing

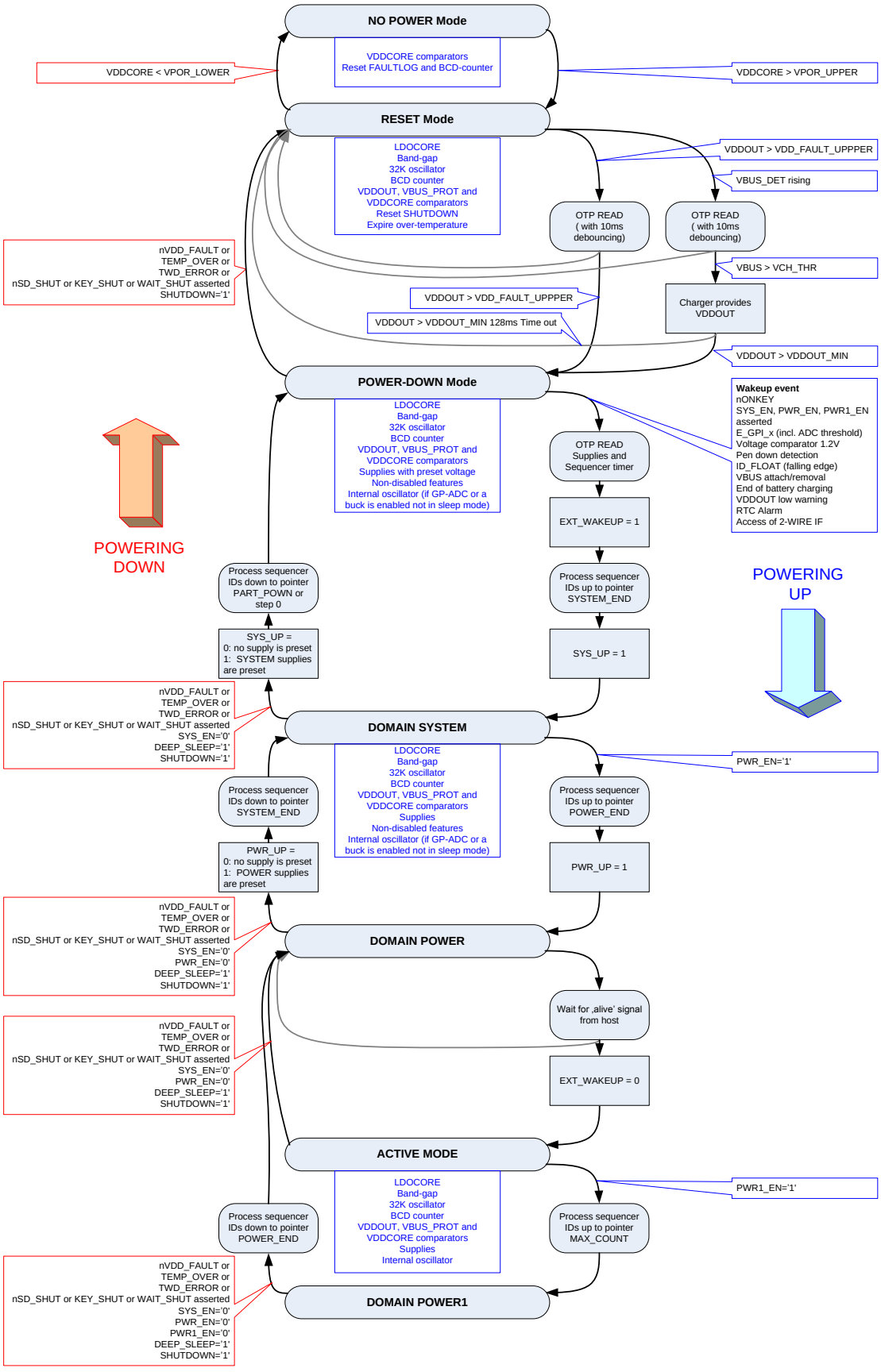

Figure 38: Power mode transitions

16.1 Power sequencer

Table 65: ID 0 to 1

Register address	Bit	Type	Label	Default	Description
R29 ID_0_1	0	R/W	NRES_MODE	1	0: No assertion of nRESET during POWERDOWN mode 1: Assert nRESETwhen entering POWERDOWN mode (release after leaving POWERDOWN mode)
	1	R/W	DEF_SUPPLY	0	When asserted all supplies (beside LDOCORE) are enabled/disabled from OTP default mode
	2	R/W		0	RESERVED
	7:4	R/W	LDO1_STEP	1001	Power sequencer time slot 9

Table 66: ID 2 to 3

Register address	Bit	Type	Label	Default	Description
R30 ID_2_3	3:0	R/W		0000	RESERVED
	7:4	R/W	LDO3_STEP	1000	Power sequencer time slot 8

Table 67: RESERVED

Register address	Bit	Type	Label	Default	Description
R31	3:0	R/W		0000	RESERVED
	7:4	R/W		0000	RESERVED

Table 68: ID 6 to 7

Register address	Bit	Type	Label	Default	Description
R32 ID_6_7	3:0	R/W		0000	RESERVED
	7:4	R/W	LDO7_STEP	0000	**Not controlled by power sequencer**

Table 69: ID 8 to 9

Register address	Bit	Type	Label	Default	Description
R33 ID_8_9	3:0	R/W		0000	RESERVED
	7:4	R/W	LDO9_STEP	0000	**Not controlled by power sequencer**

Table 70: ID 10 to 11

Register address	Bit	Type	Label	Default	Description
R34 ID_10_11	3:0	R/W	LDO10_STEP	0000	**Not controlled by power sequencer**
	7:4	R/W	PD_DIS_STEP	0101	Power sequencer time slot 5

Table 71: ID 12 to 13

Register address	Bit	Type	Label	Default	Description
R35	3:0	R/W		0000	RESERVED
	7:4	R/W		0000	RESERVED

Table 72: ID 14 to 15

Register address	Bit	Type	Label	Default	Description
R36 ID_14_15	3:0	R/W	BUCKCORE_STEP	0001	Power sequencer time slot 1
	7:4	R/W	BUCKPRO_STEP	0111	Power sequencer time slot 7

Table 73: ID 16 to 17

Register address	Bit	Type	Label	Default	Description
R37 ID_16_17	3:0	R/W	BUCKMEM_STEP	0000	**Not controlled by power sequencer**
	7:4	R/W		0000	RESERVED

Table 74: ID 18 to 19

Register address	Bit	Type	Label	Default	Description
R38 ID_18_19	3:0	R/W	GP_RISE1_STEP	0000	**Not controlled by power sequencer**
	7:4	R/W	GP_RISE2_STEP	0000	**Not controlled by power sequencer**

Table 75: ID 20 to 21

Register address	Bit	Type	Label	Default	Description
R39 ID_20_21	3:0	R/W	GP_FALL1_STEP	0000	**Not controlled by power sequencer**
	7:4	R/W	GP_FALL2_STEP	0000	**Not controlled by power sequencer**

Table 76: SEQ status

Register address	Bit	Type	Label	Default	Description
R40 SEQ_STATUS	3:0	R/W	WAIT_STEP	0000	**Not controlled by power sequencer**
	7:4	R/W	SEQ_POINTER	0000	Actual pointer position (time slot) of power sequencer

Table 77: SEQ_A

Register address	Bit	Type	Label	Default	Description
R41 SEQ_A	3:0	R/W	SYSTEM_END	0110	OTP pointer to last supply of domain SYSTEM
	7:4	R/W	POWER_END	1001	OTP pointer to last supply of domain POWER

Table 78: SEQ_B

Register address	Bit	Type	Label	Default	Description
R42 SEQ_B	3:0	R/W	MAX_COUNT	1001	OTP pointer to last supply of domain POWER1
	7:4	R/W	PART_DOWN	0100	OTP pointer for partial POWERDOWN mode

Table 79: SEQ timer

Register address	Bit	Type	Label	Default	Description
R43 SEQ_TIMER	3:0	R/W	SEQ_TIME	0011	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms
	7:4	R/W	SEQ_DUMMY	0011	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms

17 Voltage regulators

Three types of low dropout regulators are integrated on the DA9021/22, each optimised for performance depending on the most critical parameter of the circuitry supplied. For high performance analogue supplies (for example audio) the regulators have been designed to offer high PSRR and low noise, for the digital supplies PSRR is relaxed saving quiescent current and for the PMIC core/RTC supplies quiescent current has been optimised as the most important performance parameters. The regulators employ Dialog Semiconductor's Smart Mirror™ dynamic biasing, removing the need for a low power operating mode and associated software or hardware overhead.

Smart Mirror™ technology guarantees a high phase margin within the regulator control loop and has been designed to offer stable performance with small output capacitances over a wide range of output currents. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is also maintained across the full operating current range however quiescent current consumption is scaled to demand giving improved efficiency when current demand is low.

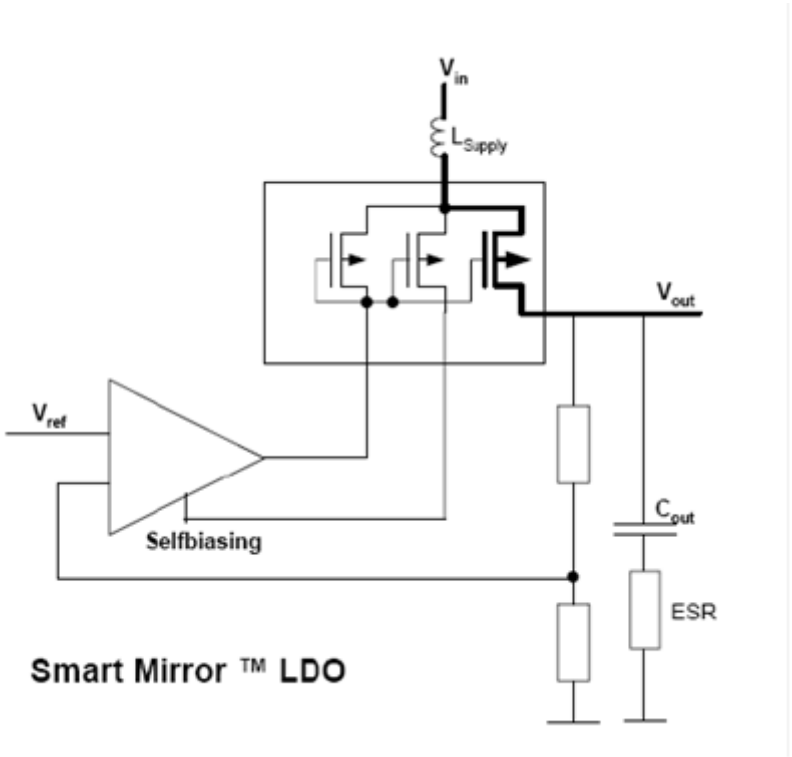

Figure 39: Smart Mirror™ voltage regulator

The regulator output voltages are fully programmable via the control interface allowing optimisation of the complete system for maximum performance and power efficiency. For security reasons the re-programming of output voltages from the control interfaces can be disabled. The default output voltage is loaded from after start-up from OTP.

A power saving mode is not required for the LDOs due to the use of dynamic biasing in the LDO internal circuitry, so when operating at low current, the quiescent current taken by the regulator is automatically minimised. LDO1 to LDO10 can optionally be supplied from a buck output (VDD < 2.8 V), in this mode some specification parameters will change.

LDO1 to LDO10 can be controlled inside the power manager sequence. If enabled at sequencer step 0 (bit DEF_SUPPLY) supplies can be default enabled via OTP whenever the sequencer passes step 0 (OTP settings are used). To limit the battery rush current it is recommended that no more than one supply (including bucks) is enabled at step 0

When powering down (for example to POWERDOWN mode) sequencer controlled supplies can be pre-configured with a new target voltage (LDOx_CONF bit is set). If LDOx_CONF was asserted in

parallel with LDOx_EN, the supply enable is deferred until the sequencer is processing the related ID. The previous output voltage and enable state will be kept unchanged until the sequencer processes the related time slot/ID during powering down (ignoring any assertions of VLDOx_GO while LDOx_CONF is high).

Before wakeup from POWERDOWN mode (processing time slots from domain SYSTEM) the sequencer will reset the LDOx_CONF bits and, if enabled via setting OTPREAD_EN, configure all regulators with their default voltage values from OTP. The regulators can also be enabled/disabled/configured via the power manager and HS-2-wire interface when the DA9021/22 is in the ACTIVE state. Voltage transitions on LDOs including DVC will always be ramped.

NOTE
Powering down to RESET mode will automatically disable all regulators except for LDO1.

LDO 3 includes dynamic DVC control to enable power savings on peripheral domains:

- The output voltage is programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.

The DVC control is handled by the following registers:

- Output voltage setting register VLDO3 to configure the new target voltage.
- Activate bit VLDO3_GO will implement the changes on the LDO output (also used from the sequencer for deferred voltage changes). After being started DA9021/22 will block (not accept any re-programming of) the related voltage setting registers until slewing has been finished.

If selected the READY signal will be asserted during ramping.

LDO9 includes an optional hardware enable/disable via GPIO12 by selecting the GPI feature with debouncing off. After detecting an E_GPI1, E_GPI2 or E_GPI12 event DA9021/22 will configure LDO4_EN, LDO5_EN or LDO9_EN by the status of GPI1, GPI2 or GPI9 and the event bit E_GPI1, E_GPI2 or E_GPI12 is automatically cleared. A parallel write access to LDO4_EN, LDO5_EN or LD09_EN from the control interfaces or the power sequencer is delayed and will later override the hardware configuration.

NOTE
It is recommended to assert the IRQ mask bit of GPIOs, which are configured for LDO hardware control, to prevent the host being disturbed by IRQ strobes from the automatically cleared events.

Disabling regulators LDO1, 2 and 5 can switch off their pull down resistor, which is required for usage in parallel to an alternate supply.

17.1 DA9021/22 core regulator LDOCORE

The LDOCORE will be used for running the DA9021/22 internal RTC module, internal state machine, GPIO pins with comparators, bias, reference, GPADC, OTP and power manager registers. It is supplied by the battery switch either from an external supply or VBAT.

18 DC/DC buck converters

DA9021/22 includes three DC-DC buck converters with Dynamic Voltage Control (DVC). DA9022 also includes three DC-DC buck converters, two with DVC and one with fixed output voltage (programmable from OTP). The output voltages are fully programmable via the control interface allowing optimisation of the complete system for maximum performance and power efficiency. For security reasons the reprogramming of output voltages from the control interfaces can be disabled via control V_LOCK.

NOTE
Powering down to RESET mode will automatically disable all buck converters.

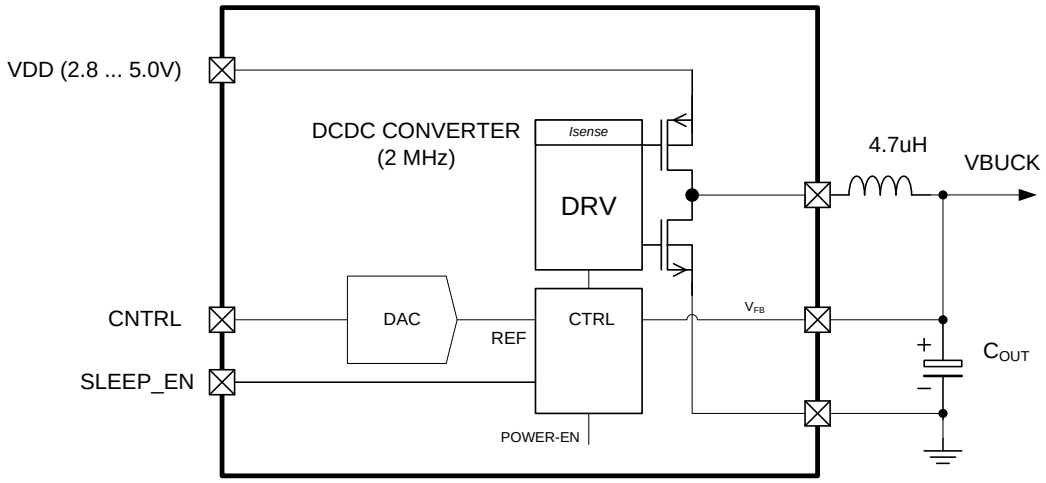

Figure 40: DC-DC buck converter

18.1 Converters BUCKCORE, BUCKPRO (DA9021 only) and BUCKMEM with DVC

These converters are high efficiency, synchronous, step down regulators operating at a high frequency (2 MHz) and supplying individual output voltages with ± 3% accuracy. Default output voltage is loaded from OTP and can be set in 25 mV steps.

DVC allows the following features:

- The buck converter output voltage to be programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.
- Output voltages below 0.725 V will only be supported in Pulse Frequency Modulation (PFM) mode. During a voltage reduction below 0.725 V the slew rate control ends at 0.725 V and the buck mode is automatically changed to sleep mode (with reduced maximum current capability). The timing of voltage transitions between 0.5 V and 0.725 V depends on the load.

The DVC is handled by the following registers:

- Output voltage setting register VBCORE, VBPRO and VBMEM to configure the new target voltage.
- Activate bit VB_CORE_GO, VB_PRO_GO and VB_MEM_GO will implement the changes at the buck output (also used from the sequencer for deferred voltage changes). After being started DA9021/22 will block (not accept any re-programming of) the related voltage setting registers until slewing has been finished. If selected the READY signal will be asserted during ramping.

The supply current during PWM (synchronous rectification) operation is in the order of 2.2 mA (quiescent current and charge/discharge current) and drops to <1µA in shutdown. Switching frequency is chosen to be high enough to allow the use of a small 4.7 µH inductor.

The operating mode of the buck converter is selected via the buck control register bits. The buck converter can be forced to operate in either SYNCHRONOUS mode or SLEEP mode. Additionally the buck converter has an AUTOMATIC mode where it will switch between SYNCHRONOUS and SLEEP mode depending on the load current.

In SLEEP mode the buck converter works in PFM mode. An internal zero crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode.

All buck converters can be controlled via an ID from the power manager sequencer. If enabled at sequencer step 0 (bit DEF_SUPPLY) buck converters can be default enabled via OTP whenever the sequencer passes step 0 (OTP default settings are used). To limit the battery rush current it is recommended that not more than a single supply (including LDOs) is enabled at step 0 During powering down supplies can be pre-configured with a new target value (Bxxx_CONF bit is set).

If Bxxx_CONF is asserted in parallel with BUCKx_EN, the supply enable is deferred until the sequencer is processing the related ID. The output voltage and enable state will be kept unchanged until the sequencer processes the related time slot/ID during powering down (ignoring any assertions of VB_xxx_GO while Bxxx_CONF is high). When powering up from POWERDOWN mode (processing time slots in domain SYSTEM) the sequencer will configure bucks with their default voltage values from OTP and by that reset the BUCKxxx_CONF bits. The bucks can also be enabled/disabled/configured via the power manager and HS-2-wire interface when the DA9021/22 is in the ACTIVE state.

Voltage transitions on bucks including DVC will always be ramped. Disabled bucks BUCKCORE, BUCKPRO and BUCKMEM can switch off their pull down resistor (required for usage in parallel to an alternative supply).

NOTE
Powering down to RESET mode will automatically disable all buck converters.

The converter BUCKCORE can additionally be merged with BUCKPRO towards a single DC-DC converter with a maximum output current of 1.4 A. The routing of the switcher output pins towards the common inductor has to be symmetrical and the feedback signal VBUCKPRO should be connected to GND (if PRO_PD_DIS is asserted BUCKCOREORE can alternatively be connected to VBUCKCORE). The inductor and the output capacitor have to be selected according to the intended increased output current.

NOTE
The configuration controls of BUCKPRO are automatically disabled by asserting the bit BUCK_MERGE and the selected current limits of BUCKCORE will be automatically doubled

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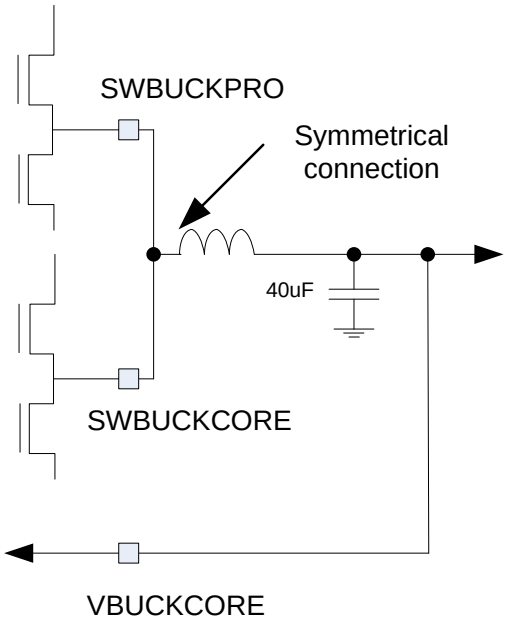

Figure 41: BUCKCORE merged with BUCKPRO

18.2 Converter BUCKPERI with OTP programmable output voltage and bypass mode (DA9022 only)

The BUCKPERI converter is a high efficiency synchronous step down regulator operating at a high frequency (2 MHz). The default output voltage is loaded from OTP and can be set from 1.8 V to 3.6 V in 50 mV steps from 1.8 to 3.0 V and 100 mV steps from 3.0 V to 3.6 V.

NOTE
Changes to the output voltage have to be executed in disabled mode as this regulator does not offer DVC

The supply current during PWM mode operation is in the order of 3 mA (quiescent current and charge/discharge current) and drops to < 1 µA in shutdown. Switching frequency is chosen to be high enough to allow the use of a small 2.2 µH to 4.7 µH inductor.

The operating mode of the buck converter is selected via the buck control register bits. The buck converter can be forced to operate in either SYNCHRONOUS mode or SLEEP mode. Additionally the buck converter has an AUTOMATIC mode where it will switch between SYNCHRONOUS and SLEEP mode depending on the load current.

In SLEEP mode, the buck converter works in PFM mode.

An internal zero crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode.

If reduced output power is required for improved efficiency it can run with a smaller pass device. BUCKPERI is able to operate up to a duty cycle of 100%, where a bypass switch across the coil will be enabled to prevent LC oscillations introduced by load-current spikes.

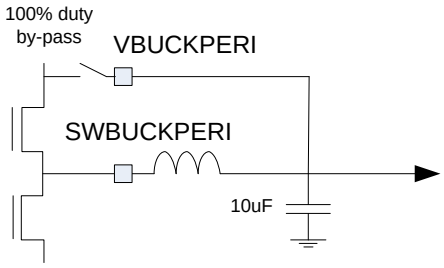

Figure 42: BUCKPERI BYPASS mode

Table 80: Selection of buck current limit from coil parameters

Min. ISAT (mA)	Frequency (MHz)	Buck current limit (mA)
1450	2	1200
1200	2	1000
960	2	800
840	2	700

18.3 Power supplies

Table 81: Buck A

Register address	Bit	Type	Label	Default	Description
R44 BUCK_A	1:0	R/W	BCORE_MODE	01	00: BUCKCORE always operates in Sleep mode 01: BUCKCORE operates in Automatic mode 10: BUCKCORE always operates in Synchronous mode 11: BUCKCORE in Automatic forcing to Synchronous mode
	3:2	R/W	BCORE_ILIM	10	00: BUCKCORE current limit 700 mA (1400 mA in merged mode) 01: BUCKCORE current limit 800 mA (1600 mA in merged mode) 10: BUCKCORE current limit 1000 mA (2000 mA in merged mode) 11: BUCKCORE current limit 1200 mA (2400 mA in merged mode)
	5:4	R/W	BPRO_MODE	01	00: BUCKPRO always operates in Sleep mode 01: BUCKPRO operates in Automatic mode 10: BUCKPRO always operates in Synchronous mode 11: BUCKPRO in Automatic forcing to Synchronous mode
	7:6	R/W	BPRO_ILIM	10	00 : BUCKPRO current limit 700 mA 01 : BUCKPRO current limit 800 mA 10 : BUCKPRO current limit 1000 mA 11 : BUCKPRO current limit 1200 mA

Table 82: Buck B

Register address	Bit	Type	Label	Default	Description
R45 BUCK_B	1:0	R/W	BMEM_MODE	01	00: BUCKMEM always operates in Sleep mode 01: BUCKMEM operates in Automatic mode 10: BUCKMEM always operates in Synchronous mode 11: BUCKMEM in Automatic forcing to Synchronous mode
	3:2	R/W	BMEM_ILIM	10	00 : BUCKMEM current limit 700 mA 01 : BUCKMEM current limit 800 mA 10 : BUCKMEM current limit 1000 mA 11: BUCKMEM current limit 1200 mA
	5:4	R/W		00	RESERVED
	7:6	R/W		00	RESERVED

Table 83: BUCKCORE

Register address	Bit	Type	Label	Default	Description
R46 BUCKCORE	5:0	R/W	VBCORE	110100	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V … 011011: 1.175 V 011100: 1.200 V 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V 100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V 101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V

Register address	Bit	Type	Label	Default	Description
					110010: 1.750 V 110011: 1.775 V 110100: 1.800 V 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V 111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BCORE_EN	0	0: BUCKCORE disabled 1: BUCKCORE enabled
	7	R/W	BCORE_CONF	0	0: Voltage ramped after assertion of VB_CORE_GO 1: Supply voltage preset

Table 84: BUCKPRO

Register address	Bit	Type	Label	Default	Description
R47 BUCKPRO	5:0	R/W	VBPRO	011100	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V … 011011: 1.175 V 011100: 1.200 V 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V 100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V

Register address	Bit	Type	Label	Default	Description
					101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V 110010: 1.750 V 110011: 1.775 V 110100: 1.800 V 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V 111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BPRO_EN	0	0: BUCKPRO disabled 1: BUCK PRO enabled
	7	R/W	BPRO_CONF	0	0: Voltage ramped after assertion of VB_PRO_GO 1: Supply voltage preset

Table 85: BUCKMEM

Register address	Bit	Type	Label	Default	Description
R48 BUCKMEM	5:0	R/W	VBMEM	101011	000000: 0.950 V 000001: 0.975 V 000010: 1.000 V 000011: 1.025 V 000100: 1.050 V … 010110: 1.500 V 010111: 1.525 V 011000: 1.550 V 011001: 1.575 V 011010: 1.600 V 011011: 1.625 V 011100: 1.650 V 011101: 1.675 V 011110: 1.700 V 011111: 1.725 V 100000: 1.750 V 100001: 1.775 V 100010: 1.800 V 100011: 1.825 V

Register address	Bit	Type	Label	Default	Description
					100100: 1.850 V 100101: 1.875 V 100110: 1.900 V 100111: 1.925 V 101000: 1.950 V 101001: 1.975 V 101010: 2.000 V 101011: 2.025 V 101100: 2.050 V 101101: 2.075 V 101110: 2.100 V 101111: 2.125 V 110000: 2.150 V 110001: 2.175 V 110010: 2.200 V 110011: 2.225 V 110100: 2.250 V 110101: 2.275 V 110110: 2.300 V 110111: 2.325 V 111000: 2.350 V 111001: 2.375 V 111010: 2.400 V 111011: 2.425 V 111100: 2.450 V 111101: 2.475 V 111110: 2.500 V 111111: 2.525 V
	6	R/W	BMEM_EN	0	0: BUCKMEM disabled 1: BUCKMEM enabled
	7	R/W	BMEM_CONF	0	0: Voltage ramped after assertion of VB_MEM_GO 1: Supply voltage preset

Table 86: BUCKPERI

Register address	Bit	Type	Label	Default	Description
R49 BUCKPERI	4:0	R/W	VBPERI	11011	00000: 1.8 V 00001: 1.85 V 00010: 1.9 V 00011: 1.95 V 00100: 2.0 V 00101: 2.05 V 00110: 2.1 V 00111: 2.15 V 01000: 2.2 V 01001: 2.25 V 01010: 2.3 V

Register address	Bit	Type	Label	Default	Description
					01011: 2.35 V 01100: 2.4 V 01101: 2.45 V 01110: 2.5 V 01111: 2.55 V 10000: 2.6 V 10001: 2.65 V 10010: 2.7 V 10011: 2.75 V 10100: 2.8 V 10101: 2.85 V 10110: 2.9 V 10111: 2.95 V 11000: 3.0 V 11001: 3.1 V 11010: 3.2 V 11011: 3.3 V 11100: 3.4 V 11101: 3.5 V 11110: 3.6 V >11110: 3.6 V
	5	R/W	BPERI_HS	0	0: BUCK_PERI PMOS pass device is full size 1: BUCK_PERI PMOS pass device is half size
	6	R/W	BPERI_EN	0	0: BUCKPERI disabled 1: BUCKPERI enabled
	7	R/W	BPERI_CONF	0	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 87: LDO1

Register address	Bit	Type	Label	Default	Description
R50 LDO1	4:0	R/W	VLDO1	01100	00000: 0.600 V 00001: 0.650 V 00010: 0.700 V 00011: 0.750 V 00100: 0.800 V 00101: 0.850 V 00110: 0.900 V 00111: 0.950 V 01000: 1.000 V 01001: 1.050 V 01010: 1.100 V 01011: 1.150 V 01100: 1.200 V 01101: 1.250 V 01110: 1.300 V

Register address	Bit	Type	Label	Default	Description
					01111: 1.350 V 10000: 1.400 V 10001: 1.450 V 10010: 1.500 V 10011: 1.550 V 10100: 1.600 V 10101: 1.650 V 10110: 1.700 V 10111: 1.750 V 11000: 1.800 V >11000: 1.800 V
	6	R/W	LDO1_EN	0	0: LDO1 disabled 1: LDO1 enabled
	7	R/W	LDO1_CONF	0	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 88: RESERVED

Register address	Bit	Type	Label	Default	Description
R51	7:0	R/W		00000000	RESERVED

Table 89: LDO3

Register address	Bit	Type	Label	Default	Description
R52 LDO3	5:0	R/W	VLDO3	101101	000000: 1.725 V 000001: 1.750 V 000010: 1.775 V 000011: 1.800 V 000100: 1.825 V … 010110: 2.275 V 010111: 2.300 V 011000: 2.325 V 011001: 2.350 V 011010: 2.375 V 011011: 2.400 V 011100: 2.425 V 011101: 2.450 V 011110: 2.475 V 011111: 2.500 V 100000: 2.525 V 100001: 2.550 V 100010: 2.575 V 100011: 2.600 V 100100: 2.625 V 100101: 2.650 V

Register address	Bit	Type	Label	Default	Description
					100110: 2.675 V 100111: 2.700 V 101000: 2.725 V 101001: 2.750 V 101010: 2.775 V 101011: 2.800 V 101100: 2.825 V 101101: 2.850 V 101110: 2.875 V 101111: 2.900 V 110000: 2.925 V 110001: 2.950 V 110010: 2.975 V 110011: 3.000 V 110100: 3.025 V 110101: 3.050 V 110110: 3.075 V 110111: 3.100 V 111000: 3.125 V 111001: 3.150 V 111010: 3.175 V 111011: 3.200 V 111100: 3.225 V 111101: 3.250 V 111110: 3.275 V 111111: 3.300 V
	6	R/W	LDO3_EN	0	0: LDO3 disabled 1: LDO3 enabled
	7	R/W	LDO3_CONF	0	0: Voltage ramped after assertion of VLDO3_GO 1: Supply voltage preset

Table 90: RESERVED

Register address	Bit	Type	Label	Default	Description
R53, R54, R55	7:0	R/W		00000000	RESERVED

Table 91: LDO7

Register address	Bit	Type	Label	Default	Description
R56 LDO7	5:0	R/W	VLDO7	001100	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V

Register address	Bit	Type	Label	Default	Description
					000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO7_EN	0	0: LDO7 disabled 1: LDO7 enabled
	7	R/W	LDO7_CONF	0	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 92: RESERVED

Register address	Bit	Type	Label	Default	Description
R57	7:0	R/W		00000000	RESERVED

Table 93: LDO9

Register address	Bit	Type	Label	Default	Description
R58 LDO9	5:0	R/W	VLDO9	011001	7
	6	R/W	LDO9_EN	0	0: LDO9 disabled 1: LDO9 enabled
	7	R/W	LDO9_CONF	0	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 94: LDO10

Register	Bit	Type	Label	Default	Description
R59 LDO10	5:0	R/W	VLDO10	100001	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V

Register	Bit	Type	Label	Default	Description
					100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO10_EN	0	0: LDO10 disabled 1: LDO10 enabled
	7	R/W	LDO10_CONF	0	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 95: SUPPLY

Register address	Bit	Type	Label	Default	Description
R60 SUPPLY	0	R/W	VB_CORE_GO	0	0: Hold VBUCKCORE at current setting. 1: Ramp BUCKCORE to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKCORE_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	1	R/W	VB_PRO_GO	0	0: Hold VBUCKPRO at current setting. 1: Ramp BUCKPRO to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKPRO_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	2	R/W	VB_MEM_GO	0	0: Hold VBUCKMEM at current setting 1: Ramp BUCKMEM to configured voltage. While the voltage is ramping, write access is blocked to BUCKMEM register. VBUCKMEM_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM.
	3	R/W		0	RESERVED
	4	R/W	VLDO3_GO	0	0: Hold VLDO3 at current setting. 1: Ramp VLDO3 to configured voltage. While

Register address	Bit	Type	Label	Default	Description
					the voltage is ramping, write access is blocked to LDO3 register. VLDO3_GO is cleared when the target voltage is reached (ignored if LDO3_CONF was asserted)
	5	R/W		0	RESERVED
	6	R/W		0	RESERVED
	7	R/W	V_LOCK	0	0: Allows writing new values into buck and LDO voltage registers 1: Disables voltage re-programming from the host (enable/disable, DVC ramping, power sequencing including deferred update still possible)

Table 96: PULLDOWN

Register address	Bit	Type	Label	Default	Description
R61 PULLDOWN	0	R/W	CORE_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	1	R/W	PRO_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	2	R/W	MEM_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	3	R/W	LDO1_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	7:4	R/W		0000	RESERVED

19 Programmable battery charger

The system power and charger control block contains the following functions:

- 2-way power path switch with automatic selection of the system power source (VDDOUT) from either VBUS or VBAT. Battery disconnection switch to allow Instant-On system start-up with discharged main battery
- Embedded active diode and external active diode controller provide a low loss power path seamless switching in whenever input power is limited or unavailable
- VBAT tracking switching regulator supplying system power out of USB port with an efficiency > 85 % @ 1000 mA load current
- Full featured autonomous Li-Ion/Polymer battery charger with pre-configurable current limits and programmable EOC voltages (4.1 V to 4.4 V), current monitoring (always active when charger is on) and OTP programmable EOC currents. Integrated control over battery pre-charge (including battery pack wakeup), Constant-Current and Constant-Voltage charging phases
- Automatic charge current reduction via Dynamic Charger Current Control (DCCC), maintaining VDDOUT system power at minimum 3.5 V without exceeding the supply current limits. Individual programmable current limits for the USB supply input
- Automatic USB Battery Charging, Specification Rev.1.0 compliant charger type detection, USB SUSPEND mode support
- Battery temperature qualified charging (using GP-ADC) with default threshold settings loaded from OTP
- Battery charging termination by current (using GP-ADC) with default threshold setting loaded from OTP
- Extended battery life by protection against continuous top charging (configurable re-charge hysteresis)
- Thermal limiting of charge current by IC temperature (using GP-ADC)
- Programmable charge termination by timer for safety

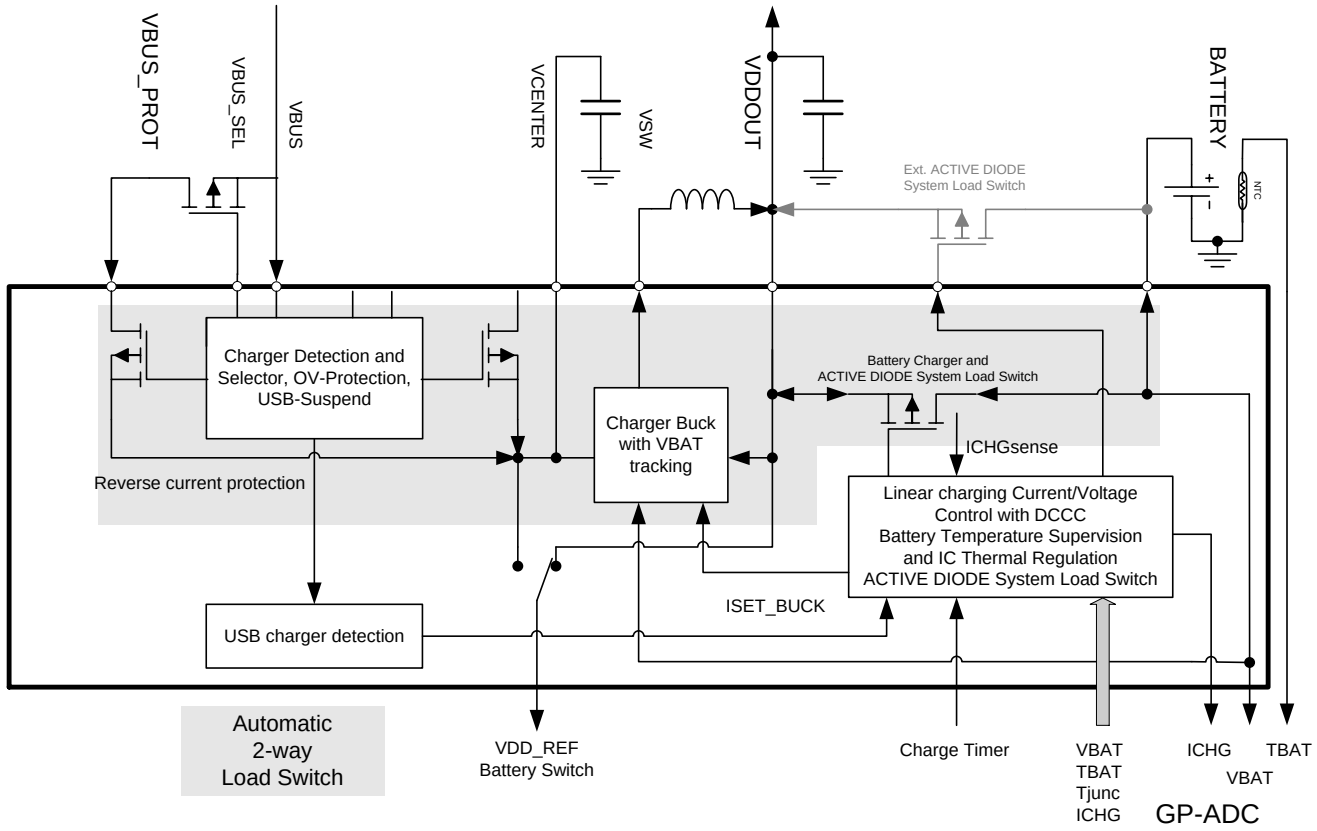

Figure 43: Charger block diagram

19.1 High efficiency charger DC-DC buck converter

In order to minimise the total system power loss at high input currents, DA9021/22's main system power VDDOUT is supplied out of a high efficient DC-DC converter, which is able to track VBAT+200 mV (with minimum VDDOUT = 3.6 V).

When powering up VDDOUT the DC-DC converter provides a soft-start circuitry and the current limit is implemented to meet the USB 2.0 specification for currents spikes where charge peaks are always less than an equivalent bypass capacitive load of 10 µF. An integrated over voltage protection and supply selection controls the behaviour of these power paths.

The buck converter operates at a high frequency (2 MHz). This switching frequency is chosen to be high enough to allow the use of a small 4.7 µH inductor. To guarantee high efficiency at high load currents the series resistance of the coil is limited to 100 mΩ (at 1000 mA). Under light load conditions the buck converter can be forced by the host to a low current PFM mode.

19.2 Charger supply detection/VBUS monitoring

DA9021/22 provides a charger input VBUS, which can be supplied either from a USB host/hub, a USB type host/hub charger or a dedicated wall charger. To protect DA9021/22 against destruction from invalid supplies an overvoltage protection circuitry will disconnect every charger that supplies more than 5.6 V.

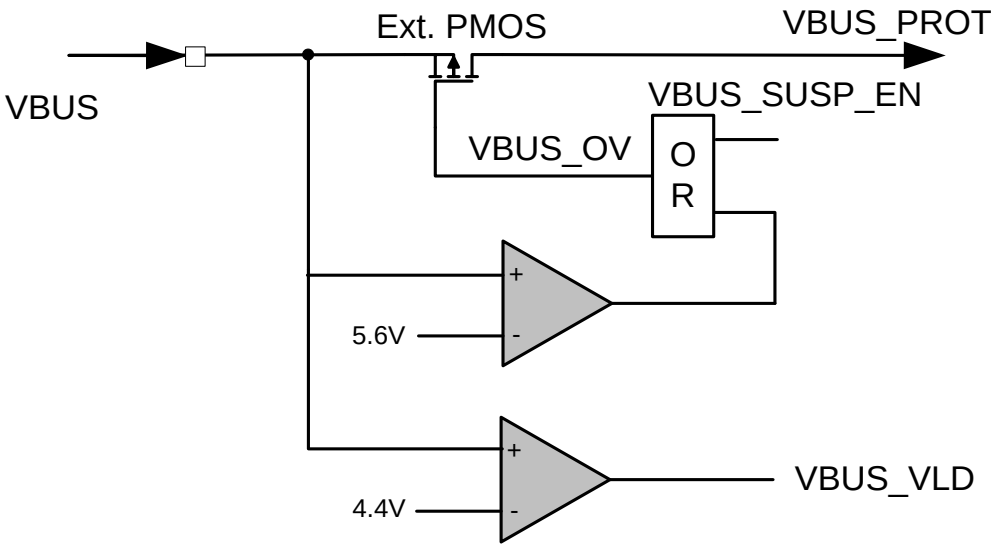

Figure 44: Charger detection

The charger initial insertion is detected when the voltage comparators indicate that VBUS_PROT is still present after a debounce time of 10 ms. At this time the charger buck converter will be enabled via a soft start up to the appropriate current limitation (see above) if the chargers attach comparator flags with enough voltage headroom from VDDOUT to VCENTER to allow the buck converter to operate. The battery is disconnected from VDDOUT as the charger supply takes over. This is done by enabling an active diode function as part of the battery P-FET, giving a clean transfer of power.

The differential charger attach comparator (CHG_ATT) detects a typical drop of 100 mV across VCENTER to VDDOUT and acts together with the charge detection comparators as an under voltage lock out, which is performed in two phases. In the first phase a falling voltage at the charger input towards VCH_THR will force the charger buck state machine to reduce the charger buck current limitation step by step down to its minimum value. If the input voltage will not recover and the CHG_ATT comparator flags a voltage drop from VCENTER to VDDOUT is below 85 mV, the charger buck is disabled as soon the current limit reaches its minimum value. If the input voltage recovers, the state machine starts increasing the current limit again until it reaches its programmed value using a slow attach time.

If during normal operation the CHG_DET signals a valid input voltage, but the CHG_ATT comparator flags a low drop across VCENTER to VDDOUT, the buck current limit is ramped down in the same way as mentioned before. The charger buck will be disabled if the voltage drop across VCENTER to VDDOUT does not rise towards a minimum of 100 mV.

NOTE
CHG_DET is VBUS_DET dependant.

19.3 VBUS overvoltage protection and USB suspend

DA9021/22 includes an overvoltage protection circuit that disconnects VBUS from the VBUS_PROT input via the external PFETs whenever the VBUS voltage is above the VCHG_EXCESS threshold. This circuit supports a USB low power SUSPEND mode, enabled via the control bit VBUS_SUSP, where the VBUS_PROT path is switched off and the VDDOUT main supply is switched to the battery disabling charging (similar to removing the VBUS supply).VBUS_SUSP is cleared when the USB charger is removed.

The charger buck supports a BUS powered low current mode which is enabled via control bit CHG_BUCK_LP. In this mode the charger buck is forced to a PFM mode to ensure the system is backed up with minimum power dissipation when being supplied from an external supply. Charging will be suspended, but with appropriate configurations of the regulators, power to for example, an idle USB PHY can be supplied.

NOTE
USB high power suspend mode allows max. 2.5 mA

Monitoring of the VBUS voltage is always provided, allowing the host processor to detect a removal of the VBUS, including in suspend mode (see VBUS status bit). The removal of supplies will issue E_VBUS_REM interrupt requests and trigger a wakeup in POWER-DOWN mode if is still present after a debounce time of 10 ms. Removing VBUS will clear VBUS_SUSP and when removing the active supply CHG_BUCK_LP is cleared.

19.4 Battery pre-charge mode

Battery PRE-CHARGE mode is started and controlled automatically by DA9021/22. This is needed to ensure that a completely empty battery can be charged without the intervention of the host processor. In the event of a heavily discharged battery the battery is disconnected from the VDDOUT supply so that the system may be started. The charger then powers the VDDOUT rail from one of the supply paths as described above, allowing the LDOs and buck converter to be switched on.

PRE-CHARGE mode is started when a charger has been detected and the VDDOUT voltage is greater than VBAT + 200 mV (or > 3.6 V). The PRE-CHARGE mode also handles the re-enable of a battery pack which has an internal safety switch been opened (from deep discharge). The safety switch will be reset by applying a current through the diode in the safety switch, charging the battery cell up to about 2.8 V where the switch will be closed again. DA9021/22 can optionally drive a flashing LED at GPIO 10 that will indicate the invisible battery charging until the application is able to power up.

Charging is suspended by writing 0 mA to ICHG_PRE in PRE-CHARGE mode.

19.5 Fast linear-charge mode

Battery LINEAR-CHARGE mode is initiated automatically once the battery voltage has exceeded the V_{BAT_FAULT} threshold for a minimum of 40 ms (to allow a battery safety switch to close).

The linear charge mode has two phases of operation:

- Constant Current (CC) mode
- Constant Voltage (CV) mode

If the battery voltage (VBAT) is less than the target voltage, the charging starts in CC mode.

Temperature supervision of the battery by the GP-ADC channel 2 is started and charging is only allowed if the battery temperature is in the correct range. If a TBAT fault condition is detected while charging the battery, charging will be suspended until the battery temperature is back in the correct range, except in the case that the charging end point has been reached.

The CC mode has 64 possible current settings ranging from 20 mA to 1260 mA, controllable by the host processor via the power manager bus. When the battery voltage approaches the target regulation voltage level the charger control loop changes over to CV mode. Note that the CC and CV mode operate in parallel, with the CC loop limiting the charging current and the CV loop limiting the charging voltage.

The charging current will be measured automatically by the GP-ADC, generating an average current reading over 10 s period that will be used to determine the charging end point detection. This allows for flexibility in determining when to automatically stop charging for different sizes and types of battery.

19.6 Thermal charge current control

During charging the temperature of DA9021/22 (T_{JUNC}) is continuously supervised by the GP-ADC against overheating. A thermal supervision circuit reduces the charge current via a current/temperature control whenever the die temperature attempts to rise above a preset value of TCHARGELOW (90°C). It completely suspends charging when TCHARGESUSPEND (120°C) has been reached. This protects DA9021/22 from excessive temperature but allows the application to push the limits of the power handling capability of a given circuit board without risk of damage. Another benefit of the thermal limit is that the charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Whenever the junction temperature (T_{JUNC}), see section 20 Monitoring ADC and touch screen interface, overrides a threshold from below table the thermal control will raise the (internal) temperature class and reduce the battery charge current limit towards the related value. It will increase the charge current limit only if the temperature drops below the threshold of the actual Class 1. This prohibits a continuous change of the charging current around a temperature threshold.

The thermal charge current control can be disabled but this will increase the risk for a complete thermal shutdown from the internal temperature supervision inside high power applications.

Table 97: Thermal charge current control

T_{JUNC} (°C)	Class	Charge current limit (mA)	ICHG_BAT (Register value)
<90	0	1260	111111
>90	1	1100	110111
>95	2	900	101101
>100	3	700	100011
>105	4	500	011001
>110	5	300	001111
>115	6	Charging suspended	000000

19.7 Dynamic charging current control (DCCC) and active-diode

If the combination of the system load plus the battery charging current (pre-charge or fast linear charging) exceeds the charger buck output current (which is limited by the current limitation of the buck) into the VDDOUT node, then the output voltage on VDDOUT will start to drop down to VBAT (which automatically reduces the charging current).

When the VDDOUT voltage drops to 3.6 V, and the charger buck is still in current limit, the charging current to the battery will be reduced until it reaches zero or the buck runs below its current limit. Once the VDDOUT is > 3.6 V or the buck runs below its current limit, the charging will be increased until it reaches the programmed setting.

The battery charging control includes an active-diode circuit that will automatically provide current to the system if the VDDOUT voltage falls below the VBAT voltage. If large currents or very low resistance in series with the battery output is required the path can be extended by an external power FET using the external active-diode controller.

Example of DCCC & active diode operation in USB high power mode

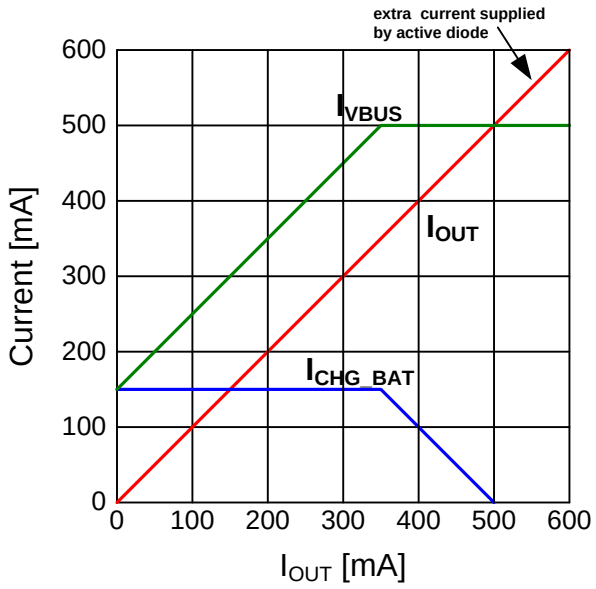

Figure 45: DCCC & active diode operation

19.8 Programmable charge termination by time

The battery charger block will provide a safety timer controlling the maximum time allowed for battery charging. The charge timer is programmable through the power manager bus. The total charge time is defined as the time from when the battery charging was enabled (both for FAST and PRE-CHARGE mode charging).

During FAST charge mode the time is dynamically extended whenever the current into the battery is automatically reduced from DCCC or thermal regulation towards less than (for example) 50 % of the configured maximum charge current. This change in charge time is inversely proportional to the change in charge current. The dynamic safety timer is limited to eight times the programmed clock period and can alternatively be configured towards a fixed timer. If the timer expires (reaches zero) an interrupt request is issued and charging is disabled.

19.8.1 Battery charger

Table 98: CHG_BUCK

Register address	Bit	Type	Label	Default	Description
R62 CHG_BUCK	3:0	R/W	ISET_BUCK	0010 Note 1	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 130 mA 0110: 400 mA 0111: 450 mA 1000: 500 mA 1001: 550 mA 1010: 600 mA 1011: 650 mA 1100: 700 mA 1101: 900 mA 1110: 1100 mA 1111: 1300 mA
	4	R/W	CHG_BUCK_EN	1	This bit is controlled by the charger state machine. If reset by the host only a charger removal and re-attach starts automatic charger control again. If set to 1 the automatic charger control is started immediately.
	5	R/W	CHG_BUCK_LP	0	When set to 1 the charger buck is forced to the PFM (SLEEP) mode and charging will be suspended. Automatically cleared when starting charging/re-charging
	6	R/W		0	RESERVED
	7	R/W	CHG_TEMP	1	0: Thermal charging control disabled 1: Thermal charging control enabled

Note 1 The OTP value is used during manufacturing to trim the max. 100 mA current limit (USB default charge current)

Table 99: WAIT_CONT

Register address	Bit	Type	Label	Default	Description
R63 WAIT_CONT	3:0	R/W	DELAY_TIME	1011	0000: 0 µsec 0001: 540 µs 0010: 1.0 ms 0011: 2.0 ms 0100: 4.1 ms 0101: 8.2 ms 0110: 16.4 ms 0111: 32.8 ms 1000: 65.5 ms 1001: 131 ms 1010: 262 ms

Register address	Bit	Type	Label	Default	Description
					1011: 524 ms 1100: 1.0 s 1101: 2.1 s 1110: 4.2 s 1111: for future use (8.4 s)
	4	R/W	EN_32KOUT	0	0: OUT_32K output buffer disabled. 1: OUT_32K output buffer enabled
	5	R/W	WAIT_MODE	1	0: Wait for GPIO10 to be active 1: Delay timer mode (start timer and wait for expire)
	6	R/W	RTC_CLOCK	1	0: No gating of RTC calendar clock 1: Clock to RTC counter is gated until WAIT is asserted
	7	R/W	WAIT_DIR	0	0: Wait during power-up sequence 1: Wait during power-up and power-down sequence

Table 100: ISET

Register address	Bit	Type	Label	Default	Description
R64 ISET	3:0	R/W	ISET_USB	1000 Note 1	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 130 mA 0110: 400 mA 0111: 450 mA 1000: 500 mA 1001: 550 mA 1010: 600 mA 1011: 650 mA 1100: 700 mA 1101: 900 mA 1110: 1100 mA 1111: 1300 mA
	7:4			0000	

Note 1 Typical OTP value for an activated USB charger detection, see setting at CHG_USB_ILIM

Table 101: BAT_CHG

Register address	Bit	Type	Label	Default	Description
R65 BAT_CHG	5:0	R/W	ICHG_BAT Note 1	001010	Battery charger current limit (CC) 000000: 0 mA (charging suspended) 000001: 20 mA 000010: 40 mA 000011: 60 mA 000100: 80 mA 000101: 100 mA 000110: 120 mA 000111: 140 mA 001000: 160 mA 001001: 180 mA 001010: 200 mA 001011: 220 mA ... 110111: 1100 mA 111000: 1120 mA 111001: 1140 mA 111010: 1160 mA 111011: 1180 mA 111100: 1200 mA 111101: 1220 mA 111110: 1240 mA 111111: 1260 mA
	7:6	R/W	ICHG_PRE	10	Battery pre-charge current limit 00: 0 mA (charging suspended) 01: 20 mA 10: 40 mA 11: 60 mA

Note 1 3-bit trimming are used to tweak the absolute value via OTP

Table 102: CHG_CONT

Register Address	Bit	Type	Label	Default	Description
R66 CHG_CONT	2:0	R/W	VCH_THR	001	Charger buck reduces the actual current limit if external supply voltage drops below: 000: 3.7 V 001: 3.8 V 010: 3.9 V 011: 4.0 V 100: 4.1 V 101: 4.2 V 110: 4.3 V 111: 4.35 V (detection threshold)
	7:3	R/W	VCHG_BAT	10110	Battery charger voltage limit (CV) 00000: 3.650 V 00001: 3.675 V

Register Address	Bit	Type	Label	Default	Description
					00010: 3.700 V 00011: 3.725 V 00100: 3.750 V 00101: 3.775 V 00110: 3.800 V 00111: 3.825 V 01000: 3.850 V 01001: 3.875 V 01010: 3.900 V 01011: 3.925 V 01100: 3.950 V 01101: 3.975 V 01110: 4.000 V 01111: 4.025 V 10000: 4.050 V 10001: 4.075 V 10010: 4.100 V (Li-Polymer) 10011: 4.125 V 10100: 4.150 V 10101: 4.175 V 10110: 4.200 V (Li-Ion) 10111: 4.225 V 11000: 4.250 V 11001: 4.275 V 11010: 4.300 V 11011: 4.3250 V 11100: 4.350 V 11101: 4.375 V 11110: 4.400 V 11111: 4.425 V

Table 103: INPUT_CONT

Register Address	Bit	Type	Label	Default	Description
R67 INPUT_CONT	3:0	R/W	TCTR Note 1	1010	0000: Charge time out disabled 0001: 30 mins remaining 0010: 60 mins remaining 0011: 90 mins remaining … 1010: 300 mins remaining … 1111: 450 mins remaining
	4	R/W	VBUS_SUSP	0	When set to 1, the USB charger path is set into suspend mode, where the power path from VBUS_PROT to VCENTER is switched off. Automatically cleared when USB supply is removed

Register Address	Bit	Type	Label	Default	Description
	6	R/W	VCHG_DROP	0	Charger re-enabled if VBAT drops below VCHG_BAT minus 0: 100 mV 1: 200 mV
	7	R/W	TCTR_MODE	0	0: Total charge time is extended during periods with reduced charge current 1: Total charge time is fixed

Note 1 Changing the value of TCTR sets the timer to the new value. The timer is paused whenever the ICHG_BAT=0 mA. The current timer value can be read from the CHG_TIME register. The timer counts down from the loaded value.

Table 104: CHG_TIME

Register address	Bit	Type	Label	Default	Description
R68 CHG_TIME	7:0	R	CHG_TIME	00000000	Remaining minutes until charging time out 00000000: Charging ended 00000001: 2 mins remaining 00000010: 4 mins remaining … 11111111: 510 mins remaining

20 Monitoring ADC and touch screen interface

20.1 ADC overview

The DA9021/22 provides an Analogue to Digital Converter (ADC) with 10-bit resolution and track and hold circuitry combined with an analogue input multiplexer. The analogue input multiplexer allows conversion of up to 10 different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs:

- Channel 0: VDDOUT – measurement of the system voltage
- Channel 1: ICH – internal battery charger current measurement
- Channel 2: TBAT – output from the battery NTC
- Channel 3: VBAT – measurement of the battery voltage
- Channel 4: ADC_IN4 – high impedance input (0 – 2.5 V)
- Channel 5: ADC_IN5 – high impedance input (0 – 2.5 V)
- Channel 8: Internal T_{JUNC}.-sense (internal temp. sensor)

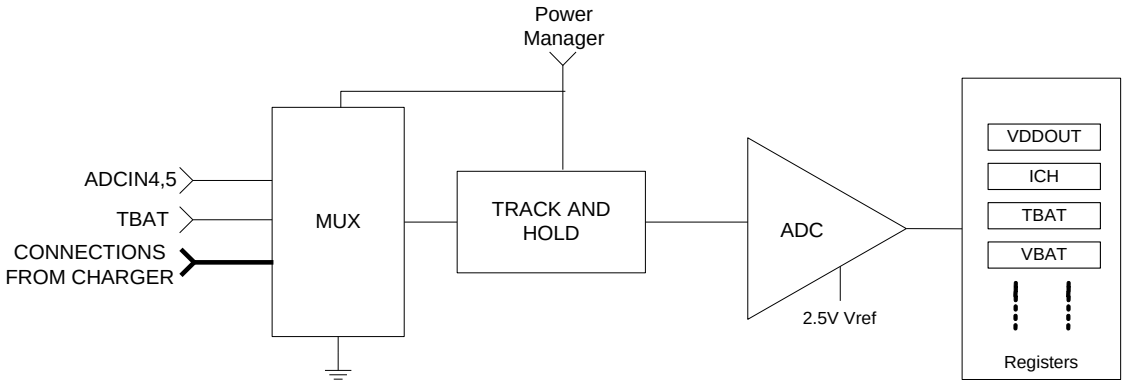

Figure 46: ADC block diagram

20.1.1 Input MUX

The MUX selects from and isolates the inputs and presents the channel to be measured to the ADC input. When selected, an input amplifier on the VDDOUT (and VBAT) channel subtracts the VDDCORE reference voltage and scales the signal to the correct value for the ADC.

20.1.2 ADC

The ADC uses a sample and hold successive approximation switched capacitor architecture. It is supplied from internal core supply rail VDDCORE (2.5 V). It can be used either a HIGH SPEED mode with measurements sequences repeated every 1 ms or in ECONOMY mode with sequences performed every 10 ms.

20.2 MANUAL CONVERSION mode

For manual measurements the ADC powers up, one conversion is done on the specified channel and the 10-bit result is stored. After the conversion is completed, the ADC powers down again and an IRQ event flag is set (end of manual conversion). The generation of this IRQ can be masked by the IRQ mask.

20.3 Automatic measurements scheduler

The automatic measurement scheduler allows monitoring of the system voltage VDDOUT, the charging current ICH, the battery temperature TBAT and the touch screen interface XY. Additionally, the auxiliary channels ADCIN4 to ADCIN6 are able to be automatically monitored with upper and lower thresholds set by power manager registers to give an nIRQ event if a measurement is outside these levels. All measurements are handled by the scheduler system detailed below.

The scheduler performs a sequence of 10 slots continually repeated according to the configured mode. If the TSI is enabled the first half slot performs either an automatic or a manual conversion. The second half slot performs TSI actions and measurements. If the TSI measurement is disabled there is no split of the slot and only the first conversion is performed. A slot requires 100 µs. The pattern of measurements over the 10 slots depends upon the charging mode. Automatic measurements of VDDOUT, ICH and TBAT are made during charging. These cease when not charging. When automatic measurements are disabled, the manual measurements are made immediately and unused automatic measurements will handle manual conversion requests.

Example sequence of AUTO-ADC measurements

Slot No	0	1	2	3	4	5	6	7	8	9	
	A0	M	M	A4	M	M	A5	M	M		No charging
	A0	A1	M	A4	A2	M	A5		M	A8	With charging

Each Slot allows 1 automatic or manual measurement and 1 TSI measurement to be made
A0 - Automatic measurement of VDDOUT (mux channel 0)
A1 - Automatic measurement of ICH (mux channel 1)
A2 - Automatic measurement of TBAT (mux channel 2)
A4 - Automatic measurement of ADCIN4 (mux channel 4)
A5 - Automatic measurement of ADCIN5 (mux channel 5)
A8 - Automatic measurement of Tjunc with gain 3 (mux channel 8)

M indicates time slots when a Manual measurement can be made

Figure 47: ADC sequence

20.3.1 A0: VDDOUT low voltage nIRQ measurement mode

VDDOUT is measured and compared with a threshold. If the reading is below this level for three consecutive readings an error event is generated. After an nIRQ assertion, the automatic measurement of channel VDDOUT is paused for reading. The host must clear the associated event flag (the event causing value is kept inside the result register) to re-enable the supervision of VDDOUT. If no action is taken to restore the VDDOUT voltage (discharging the battery is continued) the host may consider to switch off. Optional Always On blocks (backup battery charger or supplies, that are not disabled when powering down to RESET mode) to save energy later on. The multiple reading provides a debouncing of the VDDOUT voltage before issuing a nIRQ. The assertion of nIRQ can be masked by IRQ mask.

20.3.2 A1: ICH (and ICH_BAT average) measurement mode

When the battery is being charged in FAST CHARGE mode the ICH current is measured automatically every 1 or 10 ms and an average value is determined by adding the result to an 18-bit accumulator and latching the top 8 bits every 1024 samples (during high speed mode nine measurements are ignored before performing an update). This provides an average charging current value every 10.24 s, as long as the system load current is less than the maximum current provided from the external supply. When the ICH_BAT falls below the value set (and the other requirements for charging end detection is met), an IRQ will be flagged. The IRQ can be masked.

20.3.3 A2: TBAT and battery temperature warning nIRQ measurement mode

When the battery is being charged, the TBAT voltage is measured automatically. During this measurement, a 50 µA current is sourced to the battery temperature sense resistor from the TBAT pin. The TBAT high and low thresholds are programmed into the OTP. The measurement result is used to protect the battery pack from damage during charging at too high temperatures. Temperature is flagged by three threshold levels held in the threshold registers (loaded from OTP at start-up). If three consecutive readings of TBAT are outside the configured range, then charging is disabled, an event flag is set and an interrupt is generated. The processor can then either service the IRQ and turn off charging or do nothing. If nothing is done, the FAST CHARGE block will start charging again as soon as the temperature readings are inside the programmed range. The generation of this IRQ can be masked.

20.3.4 A4, A5: automatic measurement and high/low threshold warning nIRQ mode

The automatic measurement result of channel ADC_IN4 is stored. If a reading of ADC_IN4 is outside the programmed range then an event flag is set. If nIRQ was asserted the automatic measurement of channel ADC_IN4 is paused until the host has cleared the associated event flag (the event causing value is kept inside the result register). If debouncing is selected the event will only be asserted if two consecutive measurements override the same threshold. The assertion of nIRQ can be masked by IRQ mask.

The same functionality is available at ADC_IN5 .In addition it is possible to use ADCIN4 with a 15 µA current source that allows automatic measurement of a resistor value. During automatic measurements the enabled current source is dynamically switched off at the end of the conversion and switched on one slot prior to the next ADC_IN4 measurement (to enable minimum current consumption, and allow external capacitance to settle), otherwise its status is static.

20.3.5 A8: automatic measurement of internal temperature

Selection of channel 8 (T_{JUNC}) will be used to measure the output of the internal temperature sensor generated out of a PTAT current from the BGR. The channel 8 measures the output of the temperature sensor with a gain of 3. An offset register can be used for a one point calibration of the temperature sensor.

20.3.6 A3, A9: manual measurement VBAT and VBBAT

Channel 3 will be used to manually measure the main battery voltage and channel 9 can be used to measure the voltage of the backup battery.

20.4 Fixed threshold comparator

A comparator with a threshold of VREF (1.2 V) is connected to the input of channel 5. The comparator is asserted whenever the input voltage is in excess of or drops below 1.2 V for at least 10 ms (debouncing) when being enabled via COMP1V2_EN. A status flag COMP_DET indicates the actual state and a maskable interrupt request E_COMP_v12 is generated at falling and rising edge state transitions. The comparator has to be disabled via COMP1V2_EN when auto measurements with high resolution are executed on ADCIN5.

Table 105: R69 to R78

Register Address	Bit	Type	Label	Default	Description
R69, R70, R71, R72, R73, R74, R75, R76, R77, R78	7:0			00000000	RESERVED

20.4.1 LED driver

Table 106: LED4_CONT

Register Address	Bit	Type	Label	Default	Description
R79 LED4_CONT	6:0	R/W	LED4_PWM	0000000	GPIO14 LED on-time (low level at GPIO 14, period 21 kHz = 95 cycles of 0.5 µs) 0000000: off 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 % 0001011: 11 % 0001100: 12 % 0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % …. 1011111: 100 % >1011111: 100 %
	7	R/W	LED4_DIM	0	0: LED4 PWM ratio changes instantly 1: LED4 ramps between changes in PWM ratio with 40 ms per step

Table 107: LED5_CONT

Register Address	Bit	Type	Label	Default	Description
R80 LED5_CONT	6:0	R/W	LED5_PWM	0000000	GPIO15 LED on-time (low level at GPIO 15, requires GPIO15_ MODE = 1, period 21 kHz = 95 cycles) 0000000: off 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 % 0001011: 11 % 0001100: 12 %

Register Address	Bit	Type	Label	Default	Description
					0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % …. 1011111: 100 % >1011111: 100 %
	7	R/W	LED5_DIM	0	0: LED5 PWM ratio changes instantly 1: LED5 ramps between changes in PWM ratio with 40 ms per step

20.4.2 GP-ADC

Table 108: ADC_MAN

Register Address	Bit	Type	Label	Default	Description
R81 ADC_MAN	3:0	R/W	MUX_SEL	1000	0000: VDDOUT pin (channel 0) selected 0001: ICH (channel 1) selected 0010: TBAT pin (channel 2) selected 0011: VBAT pin (channel 3) selected 0100: ADCIN4 selected 0101: ADCIN5 selected 1000: internal T-Sense using gain 1 (channel 8) selected
	4	R/W	MAN_CONV	0	Perform manual conversion. Bit is reset to 0 when conversion is complete.
	7:5	R		000	

Table 109: ADC_CONT

Register Address	Bit	Type	Label	Default	Description
R82 ADC_CONT	0	R/W	AUTO_VDD_EN	0	0: VDDOUT auto measurements disabled 1: VDDOUT auto measurements enabled
	1	R/W	AUTO_AD4_EN	0	0: ADCIN4 auto measurements disabled 1: ADCIN4 auto measurements enabled
	2	R/W	AUTO_AD5_EN	0	0: ADCIN5 auto measurements disabled 1: ADCIN5 auto measurements enabled
	3	R/W		0	RESERVED
	4	R/W	AD4_ISRC_EN	0	0: Disable ADCIN4 15 µA current source 1: Enable ADCIN4 15 µA current source
	5	R/W	TBAT_ISRC_EN	0	0: TBAT 50 µA current source enabled one slot before measurement (disabled after measurement) 1: Enable TBAT 50 µA current source permanently
	6	R/W	ADC_MODE	0	0: Measurement sequence interval 10 ms

Register Address	Bit	Type	Label	Default	Description
					(economy mode) 1: Measurement sequence interval 1 ms (recommended for TSI mode)
	7	R/W	COMP1V2_EN	0	0: Disable 1.2 V comparator at ADCIN5 1: Enable 1.2 V comparator

Table 110: ADC_RES_L

Register Address	Bit	Type	Label	Default	Description
R83 ADC_RES_L	1:0	R	ADC_RES_LSB	00	10-bit manual conversion result (2 LSBs)

Table 111: ADC_RES_H

Register Address	Bit	Type	Label	Default	Description
R84 ADC_RES_H	7:0	R	ADC_RES_MSB	000000	10-bit manual conversion result (8 MSBs)

Table 112: VDD_RES

Register Address	Bit	Type	Label	Default	Description
R85 VDD_RES	7:0	R	VDDOUT_RES	00000000	0x00 – 0xFF: Auto VDDOUT conversion result (ADCIN0) 00000000 corresponds to 2.5 V 11111111 corresponds to 4.5 V

Table 113: VDD_MON

Register Address	Bit	Type	Label	Default	Description
R86 VDD_MON	7:0	R/W	VDDOUT_MON	00000000	VDDOUT_MON threshold setting (8-bit). 00000000 corresponds to 2.5 V 11111111 corresponds to 4.5 V

Table 114: ICHG_AV

Register Address	Bit	Type	Label	Default	Description
R87 ICHG_AV	7:0	R	ICHG_AV	00000000	Charger current average conversion result, 8 MSBs from an internal 18-bit accumulator, updated every 10.24 sec: 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Table 115: ICHG_THD

Register Address	Bit	Type	Label	Default	Description
R88	7:0	R/W	ICHG_THD	01000000	Reduced battery charging current

Register Address	Bit	Type	Label	Default	Description
ICHG_THD					detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Table 116: ICHG_END

Register Address	Bit	Type	Label	Default	Description
R89 ICHG_END	7:0	R/W	ICHG_END	00000110	Battery charging end point current detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Table 117: TBAT_RES

Register Address	Bit	Type	Label	Default	Description
R90 TBAT_RES	7:0	R	TBAT_RES	00000000	00000000 – 11111111: Auto ADC TBAT conversion result (ADCIN1)

Table 118: TBAT_HIGHP

Register Address	Bit	Type	Label	Default	Description
R91 TBAT_HIGHP	7:0	R/W	TBAT_HIGHP	00000000	00000000 – 11111111: TBAT high temperature threshold

Table 119: TBAT_HIGHN

Register Address	Bit	Type	Label	Default	Description
R92 TBAT_HIGHN	7:0	R/W	TBAT_HIGHN	00000000	00000000 – 11111111: TBAT high temperature resume charging threshold (typically 45 °C)

Table 120: TBAT_LOW

Register Address	Bit	Type	Label	Default	Description
R93 TBAT_LOW	7:0	R/W	TBAT_LOW	11111111	00000000 – 11111111: TBAT low temperature threshold (typically 0 °C)

Table 121: T_OFFSET

Register Address	Bit	Type	Label	Default	Description
R94 T_OFFSET	7:0	R/W	T_OFFSET	00000000	10000000 – 01111111: signed two's complement calibration offset for junction temperature measurement

Table 122: ADCIN4_RES

Register Address	Bit	Type	Label	Default	Description
R95 ADCIN4_RES	7:0	R	ADCIN4_RES	00000000	00000000 – 11111111: Auto ADC ADCIN4 conversion result

Table 123: AUTO4_HIGH

Register Address	Bit	Type	Label	Default	Description
R96 AUTO4_HIGH	7:0	R/W	AUTO4_HIGH	11111111	00000000 – 11111111: ADCIN4 high level threshold

Table 124: AUTO4_LOW

Register Address	Bit	Type	Label	Default	Description
R97 AUTO4_LOW	7:0	R/W	AUTO4_LOW	00000000	00000000 – 11111111: ADCIN4 low level threshold

Table 125: ADCIN5_RES

Register Address	Bit	Type	Label	Default	Description
R98 ADCIN5_RES	7:0	R	ADCIN5_RES	00000000	00000000 – 11111111: Auto ADC ADCIN5 conversion result

Table 126: AUTO5_HIGH

Register Address	Bit	Type	Label	Default	Description
R99 AUTO5_HIGH	7:0	R/W	AUTO5_HIGH	11111111	00000000 – 11111111: ADCIN5 high level threshold

Table 127: AUTO5_LOW

Register Address	Bit	Type	Label	Default	Description
R100 AUTO5_LOW	7:0	R/W	AUTO5_LOW	00000000	00000000 – 11111111: ADCIN5 low level threshold

Table 128: R102, R103

Register Address	Bit	Type	Label	Default	Description
R102	7:0			11111111	RESERVED
R103	7:0			00000000	RESERVED

Table 129: TJUNC_RES

Register Address	Bit	Type	Label	Default	Description
R104 TJUNC_RES	7:0	R	TJUNC_RES	00000000	00000000 – 11111111: Auto TJUNC conversion result (ADCIN8)

Table 130: R105, R106

Register Address	Bit	Type	Label	Default	Description
R105	7:0			00000001	RESERVED
R106	7:0			00000000	RESERVED

20.4.3 RTC calendar and alarm

Table 131: COUNT_S

Register Address	Bit	Type	Label	Default	Description
R111 COUNT_S	5:0	R/W	COUNT_SEC	000000	0x00 – 0x3B: RTC seconds read-out. A read of this register latches the current RTC calendar count into the registers R111 to R116 (coherent for approx. 0.5 s).
	6	R/W	MONITOR	0	Read-out '0' indicates that the power was lost. Read-out of '1' indicates that the clock is OK Set to '1' when setting time to arm RTC monitor function.

Table 132: COUNT_MI

Register Address	Bit	Type	Label	Default	Description
R112 COUNT_MI	5:0	R/W	COUNT_MIN	000000	0x00 – 0x3B: RTC minutes read-out

Table 133: COUNT_H

Register Address	Bit	Type	Label	Default	Description
R113 COUNT_H	4:0	R/W	COUNT_HOUR	00000	0x00 – 0x17: RTC hours read-out

Table 134: COUNT_D

Register Address	Bit	Type	Label	Default	Description
R114 COUNT_D	4:0	R/W	COUNT_DAY	00001	0x01 – 0x1F: RTC days read-out
	7:5	R		000	

Table 135: COUNT_MO

Register Address	Bit	Type	Label	Default	Description
R115 COUNT_MO	3:0	R/W	COUNT_MONTH	0001	0x01 – 0x0C: RTC months read-out

Table 136: COUNT_Y

Register Address	Bit	Type	Label	Default	Description
R116 COUNT_Y	5:0	R/W	COUNT_YEAR	000000	0x00 – 0x3F: RTC years read-out (0 corresponds to year 2000). A write to this register latches the registers R111 to R116 into the current RTC calendar count

Table 137: ALARM_MI

Register Address	Bit	Type	Label	Default	Description
R117 ALARM_MI	5:0	R/W	ALARM_MIN	000000	0x00 – 0x3B: Alarm minutes setting
	6	R	ALARM_TYPE	0	Alarm event caused by: 0: TICK 1: Timer alarm
	7	R/W	TICK_TYPE	1	Tick alarm interval is: 0: 1 second 1: 1 minute

Table 138: ALARM_H

Register Address	Bit	Type	Label	Default	Description
R118 ALARM_H	4:0	R/W	ALARM_HOUR	00000	0x00 – 0x17: Alarm hours setting

Table 139: ALARM_D

Register Address	Bit	Type	Label	Default	Description
R119 ALARM_D	4:0	R/W	ALARM_DAY	00001	0x01 – 0x1F: Alarm days setting

Table 140: ALARM_MO

Register Address	Bit	Type	Label	Default	Description
R120 ALARM_MO	3:0	R/W	ALARM_MONTH	0001	0x01 – 0x0C: Alarm months setting

Table 141: ALARM_Y

Register Address	Bit	Type	Label	Default	Description
R121 ALARM_Y	5:0	R/W	ALARM_YEAR	0000	0x00 – 0x3F: Alarm years setting (0 corresponds to year 2000). A write to this register latches the registers R117 to R121
	6	R/W	ALARM_ON	0	0: Alarm function is disabled 1: Alarm enabled
	7	R/W	TICK_ON	0	0: Tick function is disabled 1: Periodic tick alarm enabled

Table 142: SECOND_A

Register Address	Bit	Type	Label	Default	Description
R122 SECOND_A	7:0	R	SECONDS_A	00000000	RTC seconds counter A (LSBs). A read of this register latches the current 32-bit counter into the registers R122 to R125 (coherent for approx. 0.5 s).

Table 143: SECOND_B

Register Address	Bit	Type	Label	Default	Description
R123 SECOND_B	7:0	R	SECONDS_B	00000000	RTC seconds counter B

Table 144: SECOND_C

Register Address	Bit	Type	Label	Default	Description
R124 SECOND_C	7:0	R	SECONDS_C	00000000	RTC seconds counter C

Table 145: SECOND_D

Register Address	Bit	Type	Label	Default	Description
R125 SECOND_D	7:0	R	SECONDS_D	00000000	RTC seconds counter D (MSBs)

20.5 Register page 1

Table 146: PAGE_CON_P1

Register Address	Bit	Type	Label	Default	Description
R128 PAGE_CON_P1	6:0	R		0000000	
	7	RW	REG_PAGE	0	0: Selects Register R1 to R127 1: Selects Register R129 to R255

Table 147: CHIP_ID

Register Address	Bit	Type	Label	Default	Description
R129 CHIP_ID	3:0	R	TRC	Note 1	Read back of OTP trimming release code (TRC) – starts with a code 0
	7:4	R	MRC	Note 2	Read back of mask revision code (MRC) – code 0 for AA release

Note 1 This register allows read back of the revision. Variants that are shipped with different OTP defaults will be identified via a TRC number (loaded from OTP).

Note 2 Changes due to mask design changes will increment the MRC number

Table 148: CONFIG_ID

Register Address	Bit	Type	Label	Default	Description
R130 CONFIG_ID	2:0	R	CONF_ID	000	ID for customer variant of start-up voltages and sequencer configuration, written during production of variant
	7:3	R	CUSTOMER_ID	00000	ID for customer, written during production of variant

20.5.1 Customer OTP

Table 149: OTP_CONT

Register Address	Bit	Type	Label	Default	Description
R131 OTP_CONT	0	R/W	OTP_TRANSFER	0	0: No transfer in progress 1: Writing '1' to this bit initiates the fusing of selected OTP cells with the content from corresponding registers 1: Reading '1' indicates the transfer is still ongoing
	1	R/W	OTP_RP	0	0: Transfer is Read 1: Transfer is Programming
	2	R/W	OTP_GP	0	0: No action 1: Transfer includes configuration registers R132 to R142 (plus GP_WRITE_DIS and OTP_GP_LOCK)
	3	R/W	OTP_CONF	0	0: No action 1: Transfer includes configuration R10 to R106 (plus OTP_CONF_LOCK)
	4	R		0	
	5	R	OTP_GP_LOCK	0	0: OTP not locked after programming 1: OTP will be locked during programming (no further fusing possible) Note 1
	6	R/W	OTP_CONF_LOCK	1	0: OTP registers R10 to R106 not locked after programming (only for unmarked evaluation samples) 1: OTP registers R10 to R106 will be locked during programming (set for all marked parts, no further fusing possible) Note 1
	7	R/W	GP_WRITE_DIS	0	0: Enables write access to GP_ID registers 1: GP_ID registers are read only Note 1

Note 1 Write access for fusing only, control state is loaded from OTP defaults after POR

Table 150: OSC_TRIM

Register Address	Bit	Type	Label	Default	Description
R132 OSC_TRIM	7:0	R/W	TRIM_32K	00000000	Bits for correction of the 32 kHz oscillator frequency: 10000000: -244.1 ppm … 11111111: -1.9 ppm 00000000: off 00000001: 1.9 ppm (1/(32768*16)) … 01111111: 242.2 ppm

21 Register Map

Table 151: Register map

Register	Function	7	6	5	4	3	2	1	0
PAGE 0									
System control and event registers (SYSMON)									
R0	PAGE_CON	REG_PAGE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
R1	STATUS_A	VDAT_DET	VBUS_SEL		VBUS_DET				nONKEY
R2	STATUS_B	COMP_DET	SEQUENCING	GP_FB2	CHG_TO	CHG_END	CHG_LIM	CHG_PRE	CHG_ATT
R3	STATUS_C							GPI1	GPI0
R4	STATUS_D	GPI15	GPI14	GPI13	GPI12		GPI10	GPI9	GPI8
R5	EVENT_A	M_COMP_1V2	M_SEQ_RDY	E_ALARM	E_VDD_LOW	E_VBUS_REM		E_VBUS_DET	Reserved
R6	EVENT_B			E_ADC_EOM	E_TBAT	E_CHG_END			E_nONKEY
R7	EVENT_C							E_GPI1	E_GPI0
R8	EVENT_D	E_GPI15	E_GPI14	E_GPI13	E_GPI12		E_GPI10	E_GPI9	E_GPI8
R9	FAULT_LOG	WAIT_SHUT	nSD_SHUT	KEY_SHUT	Not used	TEMP_OVER	VDD_START	VDD_FAULT	
R10	IRQ_MASK_A	M_COMP_1V2	M_SEQ_RDY	M_ALARM	M_VDD_LOW	M_VBUS_REM		M_VBUS_VLD	Reserved
R11	IRQ_MASK_B			M_ADC_EOM	M_TBAT	M_CHG_END			M_nONKEY
R12	IRQ_MASK_C							M_GPI1	M_GPI0
R13	IRQ_MASK_D	M_GPI15	M_GPI14	M_GPI13	M_GPI12		M_GPI10	M_GPI9	M_GPI8
R14	CONTROL_A	GPI_V	PM_O_TYPE		PM_I_V		PWR1_EN	PWR_EN	SYS_EN
R15	CONTROL_B	SHUTDOWN	DEEP_SLEEP	WRITE_MODE		OTPREAD_EN	AUTO_BOOT	ACT_DIODE	BUCK_MERGE
R16	CONTROL_C	BLINK_DUR	BLINK_FRQ	DEBOUNCING	PM_FB2_PIN	PM_FB1_PIN			

Register	Function	7	6	5	4	3	2	1	0
R17	CONTROL_D		0 - Reserved	GPI14_15_SD	nONKEY_SD				
R18	PD_DIS	PM-CONT_PD	OUT_32K_PD		CHG_PD	HS-2-wire_PD	PM-IF_PD	GP-ADC_PD	GPIO_PD
R19	INTERFACE	IF_BASE_ADDR	nCS_POL	R/W_POL	CPHA	CPOL	IF_TYPE		
R20	RESET	RESET_EVENT	RESET_TIMER						
GPIO control registers (GPIO)									
R21	GPIO_0-1	GPIO1_MODE	GPIO1_TYPE	GPIO1_PIN		GPIO0_MODE	GPIO0_TYPE	GPIO0_PIN	
R22		1- Reserved	1 - Reserved	10 - Reserved		1 - Reserved	1 - Reserved	10 - Reserved	
R23		1 - Reserved	1 - Reserved	10 - Reserved		1 - Reserved	1- Reserved	10 - Reserved	
R24		1 - Reserved	1 - Reserved	10 - Reserved		1 - Reserved	1 - Reserved	10 - Reserved	
R25	GPIO_8-9	GPIO9_MODE	GPIO9_TYPE	GPIO9_PIN		GPIO8_MODE	GPIO8_TYPE	GPIO8_PIN	
R26	GPIO_10-11	1 - Reserved	1 - Reserved	10 - Reserved		GPIO10_MODE	GPIO10_TYPE	GPIO10_PIN	
R27	GPIO_12-13	GPIO13_MODE	GPIO13_TYPE	GPIO13_PIN		GPIO12_MODE	GPIO12_TYPE	GPIO12_PIN	
R28	GPIO_14-15	GPIO15_MODE	GPIO15_TYPE	GPIO15_PIN		GPIO14_MODE	GPIO14_TYPE	GPIO14_PIN	
Power sequencer control registers (SEQ)									
R29	ID_0_1	LDO1_STEP				Not used		DEF_SUPPLY	nRES_MODE
R30	ID_2_3	LDO3_STEP							
R32	ID_6_7	LDO7_STEP							
R34	ID_10_	LDO9_STEP							
R34	ID_10_11	PD_DIS_STEP				LDO10_STEP			
R36	ID_14_15	BUCKPRO_STEP				BUCKCORE_STEP			

Register	Function	7	6	5	4	3	2	1	0
R37	ID_16_17	BUCKPERI_STEP				BUCKMEM_STEP			
R38	ID_18_19	GP_RISE2_STEP				GP_RISE1_STEP			
R39	ID_20_21	GP_FALL2_STEP				GP_FALL1_STEP			
R40	SEQ_STATUS	SEQ_POINTER				WAIT_STEP			
R41	SEQ_A	POWER_END				SYSTEM_END			
R42	SEQ_B	PART_DOWN				MAX_COUNT			
R43	SEQ_TIMER	SEQ_DUMMY				SEQ_TIME			
Power supply control registers (REG)									
R44	BUCK_A	BPRO_ILIM		BPRO_MODE		BCORE_ILIM		BCORE_MODE	
R45	BUCK_B	BPERI_ILIM		BPERI_MODE		BMEM_ILIM		BMEM_ MODE	
R46	BUCKCORE	BCORE_CONF	BCORE_EN	VBCORE					
R47	BUCKPRO	BPRO_CONF	BPRO_EN	VBPRO					
R48	BUCKMEM	BMEM_CONF	BMEM_EN	VBMEM					
R49	BUCKPERI	BPERI_CONF	VBPERI	BPERI_HS	VBPERI				
R50	LDO1	LDO1_CONF	LDO1_EN	VLDO1					
R51		0 - Reserved	0 - Reserved						
R52	LDO3	LDO3_CONF	LDO3_EN	VLDO3					
R53		0 - Reserved	0 - Reserved						
R54		0 - Reserved	0 - Reserved						
R55		0 - Reserved	0 - Reserved						
R56	LDO7	LDO7_CONF	LDO7_EN	VLDO7					
R57		0 - Reserved	0 - Reserved						
R58	LDO9	LDO9_CONF	LDO9_EN	VLDO9					
R59	LDO10	LDO10_CON	LDO10_EN	VLDO10					

Register	Function	7	6	5	4	3	2	1	0
		F							
R60	SUPPLY	V_LOCK			VLDO3_GO		VB_MEM_GO	VB_PRO_GO	VB_CORE_GO
R61	PULLDOWN	Not used	Not used			LDO1_PD_DIS	MEM_PD_DIS	PRO_PD_DIS	CORE_PD_DIS
Charging control registers (CHARGE)									
R62	CHG_BUCK	CHG_TEMP	0 - Reserved	CHG_BUCK_LP	CHG_BUCK_EN	ISET_BUCK			
R63	WAIT_CONT	WAIT_DIR	RTC_CLOCK	WAIT_MODE	EN_32KOUT	DELAY_TIME			
R64	ISET	ISET				ISET_USB			
R65	BAT_CHG	ICHG_PRE		ICHG_BAT					
R66	CHG_CONT	VCHG_BAT				VCH_THR			
R67	INPUT_CONT	TCTR_MODE	VCHG_DROP		VBUS_SUSP	TCTR			
R68	CHG_TIME	CHG_TIME							
LED driver control registers (LED)									
R70						0 - Reserved	0 - Reserved	0 - Reserved	
R71			0 - Reserved	0 - Reserved	0 - Reserved	0 - Reserved	0 - Reserved	0 - Reserved	0 - Reserved
R79	LED4_CONT	LED4_DIM	LED4_PWM						
R80	LED5_CONT	LED5_DIM	LED5_PWM						
GP-ADC control registers (GPADC)									
R81	ADC_MAN	Not used	Not used	Not used	MAN_CONV	MUX_SEL			
R82	ADC_CONT	COMP1V2_EN	ADC_MODE	TBAT_ISRC_EN	AD4_ISRC_EN	0 - Reserved	AUTO_AD5_EN	AUTO_AD4_EN	AUTO_VDD_EN
R83	ADC_RES_L	Not used	Not used	Not used	Not used	Not used	Not used	ADC_RES_LSB	
R84	ADC_RES_H	ADC_RES_MSB							
R85	VDD_RES	VDDOUT_RES							

Register	Function	7	6	5	4	3	2	1	0
R86	VDD_MON	VDDOUT_MON							
R87	ICHG_AV	ICHG_AV							
R88	ICHG_THD	ICHG_THD							
R89	ICHG_END	ICHG_END							
R90	TBAT_RES	TBAT_RES							
R91	TBAT_HIGHP	TBAT_HIGHP							
R92	TBAT_HIGHN	TBAT_HIGHN							
R93	TBAT_LOW	TBAT_LOW							
R94	T_OFFSET	T_OFFSET							
R95	ADCIN4_RES	ADCIN4_RES							
R96	AUTO4_HIGH	AUTO4_HIGH							
R97	AUTO4_LOW	AUTO4_LOW							
R98	ADCIN5_RES	ADCIN5_RES							
R99	AUTO5_HIGH	AUTO5_HIGH							
R100	AUTO5_LOW	AUTO5_LOW							
R104	TJUNC_RES	TJUNC_RES							
RTC calendar and alarm (RTC)									
R111	COUNT_S	Not used	MONITOR	COUNT_SEC					
R112	COUNT_MI	Not used	Not used	COUNT_MIN					
R113	COUNT_H	Not used	Not used	Not used	COUNT_HOUR				
R114	COUNT_D	Not used	Not used	Not used	COUNT_DAY				
R115	COUNT_MO	Not used	Not used	Not used	Not used	COUNT_MONTH			
R116	COUNT_Y	Not used	Not used	COUNT_YEAR					
R117	ALARM_MI	TICK_TYPE	ALARM_TYPE	ALARM_MIN					

Register	Function	7	6	5	4	3	2	1	0
R118	ALARM_H	Not used	Not used	Not used	ALARM_HOUR				
R119	ALARM_D	Not used	Not used	Not used	ALARM_DAY				
R120	ALARM_MO	Not used	Not used	Not used	Not used	ALARM_MONTH			
R121	ALARM_Y	TICK_ON	ALARM_ON	ALARM_YEAR					
R122	SECOND_A	SECONDS_A							
R123	SECOND_B	SECONDS_B							
R124	SECOND_C	SECONDS_C							
R125	SECOND_D	SECONDS_D							
PAGE 1									
Customer OTP (MEM)									
R128	PAGE_CON	REG_PAGE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
R129	CHIP_ID	MRC				TRC			
R130	CONFIG_ID	CUSTOMER_ID					CONF_ID		
R131	OTP_CONT	GP_WRITE_DIS	OTP_CONF_LOCK	OTP_GP_LOCK	Not used	OTP_CONF	OTP_GP	OTP_RP	OTP_TRANSFER
R132	OSC_TRIM	TRIM_32K							

22 Package information

22.1 Package outlines

WLBGA 64B (3.94x4.12 mm) 0.5 mm pitch

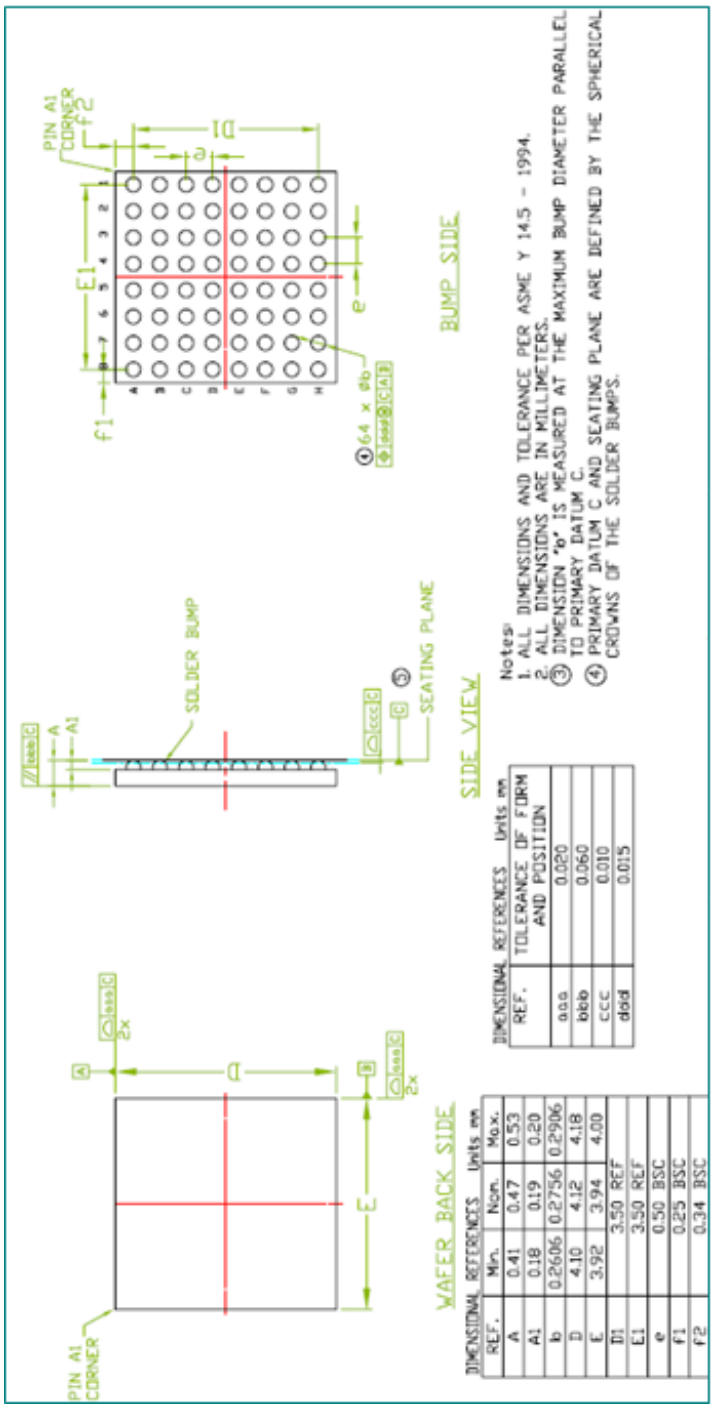

Figure 48: DA9021/22 package outline drawing

23 External component selection

23.1 Capacitor selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails.

When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account. On the VDDOUT main supply rail a minimum distributed capacitance of 30 µF with the following split is recommended:

- 10 µF close to VDDOUT pin
- 10 µF close to VDDMEM_PERI, VDD_CORE_PRO buck supply pins
- 10 µF close to boost converter input (coil)
- 2x 1 µF close to VDD_LDOx pins

Table 152: Recommended capacitor types

Application	Value	Size	Temp. char.	Tolerance	Rated voltage	Type
VLD01, VLD09 output bypass	4x 1 µF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A105KE15D
VLD03, VLD07, LD010 output bypass	6x 2.2 µF	0402	X5R +/-15 %	+/-20 %	6.3 V	Murata GRM155R60J225ME95D
VDDCORE output bypass	1x 100 nF	0402	X7R +/-15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
VBUCKMEM, VBUCKPERI output bypass	2x 10 µF	0805	X5R +/-15 %	+/-10 %	6.3 V	Murata GRM21BR60J106KE19L
VBUCKPRO, BUCKCORE output bypass (also in merged mode)	2x 22 µF	0805	X5R +/-15 %	+/-20 %	6.3 V	Murata GRM21BR60J226ME39L
VBUS bypass	2x 2.2 µF	0603	X5R +/-15 %	+/-10 %	16 V	Murata GRM188R61C225KE15
VBUS_PROT bypass	2x 4.7 µF	0603	X5R +/-15 %	+/-10 %	6.3 V	Murata GRM188R71J475KE19D
VCENTER bypass	1x 10 µF	0805	X7R +/-15 %	+/-10 %	10 V	Murata GRM21BR70J106KE76L
VDDOUT bypass	3x 10 µF	0805	X7R +/-15 %	+/-10 %	10 V	Murata GRM21BR70J106KE76L
	2x 1 µF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A105KE15D
VBAT bypass	1x 10 µF	0805	X7R +/-15 %	+/-10 %	10 V	Murata GRM21BR70J106KE76L
VDD_REF bypass	1x 2.2 µF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A225ME95D
VREF bypass	1x 100 nF	0402	X7R +/-15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
XIN, XOUT bypass to VSS	2x 12 pF	0402	U2J	+/-5 %	50 V	Murata GRM1557U1H120JZ01D

23.2 Inductor selection

Inductors should be selected based upon the following parameters:

- rated max. current (usually a coil provides two current limits):
  - the first limit specifies the maximum current at which the inductance derating (due to saturation effects) is limited to be within a specified tolerance (typical 20 % or 30 %) of the peak current
  - the second limit is defined by the maximum power dissipation and is applied to the effective current
- DC resistance
  - critical to converter efficiency and should therefore be minimised
- inductance
  - given by converter electrical characteristics; is 4.7 µH for all DA9021 switched mode converters

Table 153: Recommended inductor types

Application	Value	Size	Imax	Tolerance	DC res.	Type
BUCKMEM, BUCKPRO, BUCKCORE	3x 4.7 µH	3x3x1.2 mm	1.2 A	+/-20 %	0.13 Ω typ.	TDK VLS3012T-4R7M1R0
Merged BUCKCORE/BUCKPRO	1x 2.2 µH	3x3x1.2 mm	1.7 A	+/-20 %	0.08 Ω typ.	TDK VLS3012T-2R2M1R5
CHARGER BUCK	1x 4.7 µH	3x3x1.2 mm	1.2 A	+/-20 %	0.13 Ω typ.	TDK VLS3012T-4R7M1R0

23.3 Resistors

Table 154: Recommended resistor types

Application	Value	Size	Tolerance	P max	Type
IREF bias current reference	200kΩ	0402	+/-1 %	100 mW	Panasonic ERJ2RKF2003x

23.4 External pass transistors and Schottky diodes

Table 155: Example FETs:

Application	Package	Type
VBUS overvoltage protection FET	SOT-23	CSD25301W1015, PMV65XP
VBUS/dual overvoltage protection FET	PowerPAK1212-8 3.3x3.3x1 mm	Vishay Siliconix Si7911DN
System load switch (active diode) FET	SOT-23 3x2.6x1 mm	Vishay Siliconix Si2333CDS

23.5 Battery pack temperature sensor (NTC)

In order to achieve reasonable accuracy over the relevant temperature range (for example, 0 °C to 50 °C for charging) by using the internal 50 µA current source, the recommended NTC should have a nominal resistance of 10 kΩ at 25 °C and its resistance should not exceed 50 kΩ within this range.

Table 156: Example NTC

Type	Size	Manufacturer
NCP15XH103J03RC	0402	Murata

23.6 Crystal

The RTC module requires an external 32.768 kHz crystal.

For crystal selection the effective load capacitance has to be taken into account. It includes both external capacitors on pins XIN and XOUT in series combination and the PCB and DA9021 stray capacitances.

For example, if 2x12 pF external capacitors are used, which gives a series combination of 6 pF, and the stray capacitance is 3 pF, then the crystal type specified for a load capacitance of 9 pF should be chosen.

Different stray capacitances may require different external capacitors and/or a different crystal type.

Furthermore the series resistance of the crystal must not exceed 100 kΩ.

Table 157: Example crystal

Type	Size	Manufacturer
CC7V-T1A 32.768 kHz 9.0 pF +/- 30 ppm	3.2x1.5x0.9 mm	Micro Crystal

24 Layout guidelines

24.1 General recommendations

- Appropriate trace width and amount of vias should be used for all power supply paths.
- Too high trace resistances can prevent the system from proper operation, for example efficiency and current ratings of switch mode converters and charger might be degraded. Furthermore the PCB might be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.
- Special care must be taken to the DA9021 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row connection in an inner layer is recommended (depending on the maximum current two or more vias might be required).
- A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references like the VREF capacitor and IREF resistor should be referred to a silent ground which is connected at a star point underneath or close to the DA9021 main ground connection.
- Generally all power tracks with discontinuous and / or high currents should be kept as short as possible.
- Noise sensitive analogue signals like feedback lines or crystal connections should be kept away from traces carrying pulsed analogue or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.

24.2 System supply and charger

- Trace resistance of the VBUS_PROT bypass capacitor to VCENTER must be minimised to allow proper operation of the charge and system current control.
- If an external pMOS transistor is used to bypass the internal active diode, its connection trace resistance has to be kept to a minimum.
- The placement of the distributed capacitors at VDDOUT must ensure that all VDD inputs, especially to the buck converters and LDOs, are connected to a bypass capacitor close to the pads. It is recommended to place at least two 1 µF capacitors close to the LDO supply pads and at least one 10 µF close to the buck VDD rail.
- Using a local power plane underneath the chip for VDDOUT can be considered.
- Adequate heat sink areas should be used for at least one terminal of the external overvoltage protection and / or active diode FETs.

24.3 LDOs and switched mode supplies

- Transient current loops area of the switched mode converters should be minimised.
- The common references (VREF capacitor, IREF resistor) should be placed close to DA9021, cross coupling to any noisy digital or analogue trace must be avoided.
- Output capacitors of the LDOs should be placed close to the output pins. Small capacitors (for example 100 nF) are also required to be close to the input pins of the supplied devices.
- Care must be taken that no current is carried on feedback lines (VBUCKxx).

24.4 Crystal oscillator

- The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetric traces.
- The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines are buried between two ground layers, surrounded by additional ground traces.

24.5 DA9021 thermal connection, land pad and stencil design

- The DA9021 provides a centre ground plane, which is soldered directly to the PCB's centre ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.
- Solder mask openings for the ground pad must be split by following a certain pattern like stripes or round shapes or squares, as a solid square would apply too much solder paste and the signal pads might not be connected properly.
- As DA9021 also provides different sizes of the signal pads, some adaption of the mask openings might be required as well (generally small pads a bit larger, large pads a bit smaller than the pad itself). Vias inside or next to the pads should be filled. An appropriately fine solder paste is required.

25 Definitions

25.1 Power dissipation and thermal design

When designing with the DA9021/22 consideration must be given to power dissipation as the level of integration of the device can result in high power dissipation when all functions are operating with high battery voltages. Exceeding the package power dissipation will result in the internal thermal sensor shutting down the device until it has cooled sufficiently.

The package includes a thermal management paddle to enable improved heat spreading on the PCB.

Linear regulators operating with a high current and high differential voltage between input and output will dissipate the following power:

$$P_{diss} = (V_{in} - V_{out}) * I_{out}$$

Example

A regulator supplying 150 mA @ 2.8 V from a fully charged lithium battery (VDD = 4.1 V):

$$P_{diss} = (4.1\,V - 2.8\,V) * 0.15\,A = 195\,mW$$

For switching regulators:

$$P_{out} = P_{in} * efficiency$$

Therefore:

$$P_{diss} = P_{in} - P_{out}$$

Example

An 85 % efficient buck converter supplying 1.2 V@ 400 mA:

$$P_{diss} = 1.2\,V * 0.4\,A * \left(\frac{1}{0.85} - 1\right) = 85\,mW$$

As the DA9021/22 is a multiple regulator configuration each supply must be considered and summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

25.2 Regulator parameters

25.2.1 Dropout voltage

In the DA9021/22 a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and when entering the dropout condition the transistor is fully turned on and therefore cannot provide any further voltage control.

When the transistor is fully turned on the output voltage tracks the input voltage and regulation ceases. As the DA9021/22 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the ON resistance of the device. In the device the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm process Dialog Semiconductor are able to achieve very small pass transistor sizes for superior performance. $Vdropout = Vin - Vout = Rdson * Iout$

When defining dropout voltage it is specified in relation to a minimum acceptable change in output voltage. For example all Dialog regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest ON resistance for internal device) and maximum current load.

25.2.2 Power supply rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 A before reaching a steady state of 1.4 A (see below). Due to the battery having a finite internal resistance (typically 0.5 Ω) these current peaks induce ripple on the battery voltage of up to 500 mV. As the supplies to the audio and RF are derived from this supply it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions when the battery is at its minimum operating voltage, when there is minimum headroom available due to dropout.

25.2.3 Line regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage ΔVreg (regulator operating with a constant load current) in response to a change in the input voltage ΔVin. Transient line regulation is a measurement of the peak change ΔVreg in regulated voltage seen when the line input voltage changes.

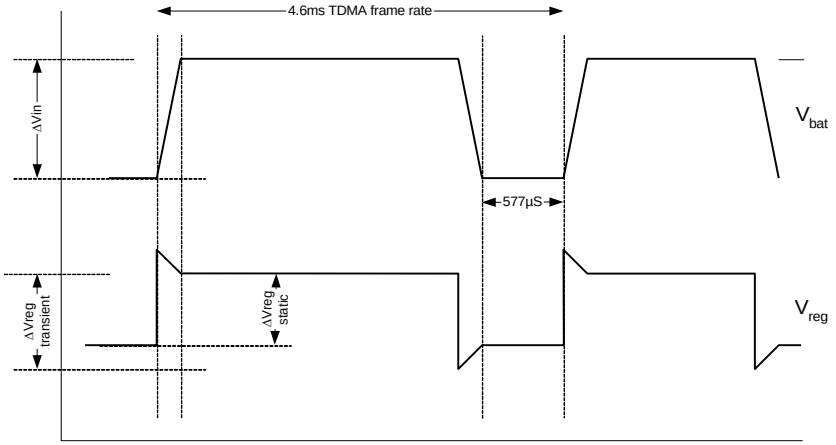

Figure 49: Line regulation

25.2.4 Load regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage ΔVreg in response to a change in the regulator loading Δload whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage ΔVreg seen when the regulator load changes.

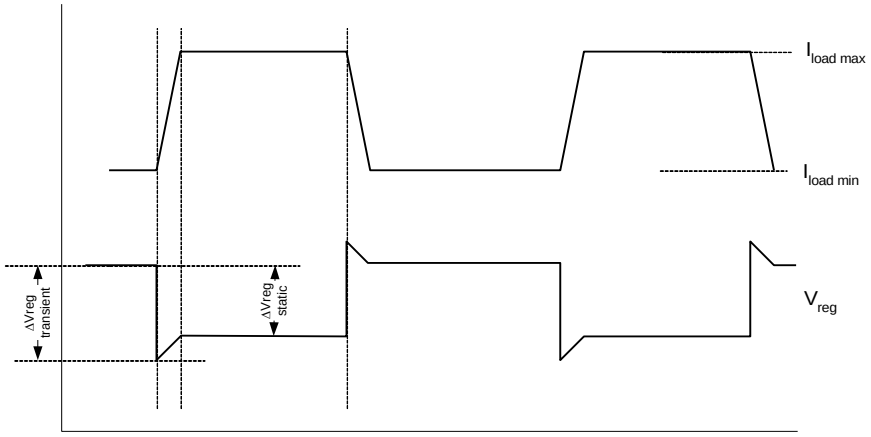

Figure 50: Load regulation

26 Ordering information

Part number	Package	Shipment	Pack quantity
DA9021-xxUE2	4x4 64 bump WLCSP	T&R	5000
DA9021-xxUE6	4x4 64 bump WLCSP	Waffle pack	320
DA9022-xxUE2	4x4 64 bump WLCSP	T&R	5000
DA9022-xxUE6	4x4 64 bump WLCSP	Waffle pack	320

26.1 Additional applications information

Please contact Dialog Semiconductor for latest application information on the DA9021/22 and other power management devices.

Revision history

Revision	Date	Description
2.5	17-Feb-2017	Minor update to General Description for uniformity, align revisioning
2.0	17-March-2016	Conversion to new template (CFR0011-120-00 Rev 5) and reformatting to current guidelines
Change details: ● Many minor formatting changes, such as the use of non-breaking spaces. Rewording of text from US to UK English and rewording of some confusing grammar and vocabulary to plain English.		

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.

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