Using Dialog Semiconductor* DA903x Advanced Power Management Controllers with the Intel® PXA27x Processor Family

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Revision History

Date	Revision	Reason for Changes
May 2004	1.0	Initial release of this document

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1.0 Introduction

This document explains how to use the Dialog Semiconductor* DA903x Advanced Power Management Controllers (DA903x PMIC) with the Intel® PXA27x Processor Family (PXA27x processor)-based platform to design power supply, battery management, and sleep-mode functions. The Dialog Semiconductor* DA903x Advanced Power Management Controllers consists of two devices:

- DA9030 Power Management Integrated Circuit (PMIC)
- DA9031 Power Management Integrated Circuit

The new DA903x PMIC is a highly integrated chip that supports the Wireless Intel SpeedStep® technology, enabling significant power savings by intelligently managing voltage and frequency changes similar to the technology used in Intel notebook processors. As a result of its highly integrated features, the DA903x PMIC reduces overall system cost and size significantly when compared to an equivalent discrete solution. This document addresses only the power-supply related features; addressing all of the features and functions of the optimized PMIC is beyond the scope of this document. The DA9030 PMIC and DA9031 PMIC datasheets describe all the features of the devices in detail.

1.1 Purpose of this Document

This document:

- Briefly introduces the DA9030 PMIC and its variants.
- Contains information about power domains, component selection, schematics of the PXA27x processor and DA903x PMIC interconnection, and on the other hardware related issues.
- Concentrates on the different power modes of the PXA27x processor and the DA9030 PMIC power-supply features.
- Briefly describes the charger concept and modes of operation.
- Contains concluding remarks.

1.2 DA9030 PMIC Variants

The Dialog Semiconductor DA9030 PMIC was developed in close cooperation with Intel to achieve the most optimized PMIC for mobile handsets using an Intel communication processor together with the PXA27x processor. All functions can be evaluated by using the Dialog Semiconductor evaluation board together with the control software. The DA9031 is the first variant to address PXA27x processor stand-alone applications. For systems using stacked memory or larger amounts of external memory (greater than 256 Mb), the second buck converter can be programmed to provide a 1.8V supply with currents up to 600mA. Customized versions of the existing PMIC to adapt it to specific customer requirements are also available through Dialog Semiconductor.

1.2.1 Main Features of DA9030 PMIC

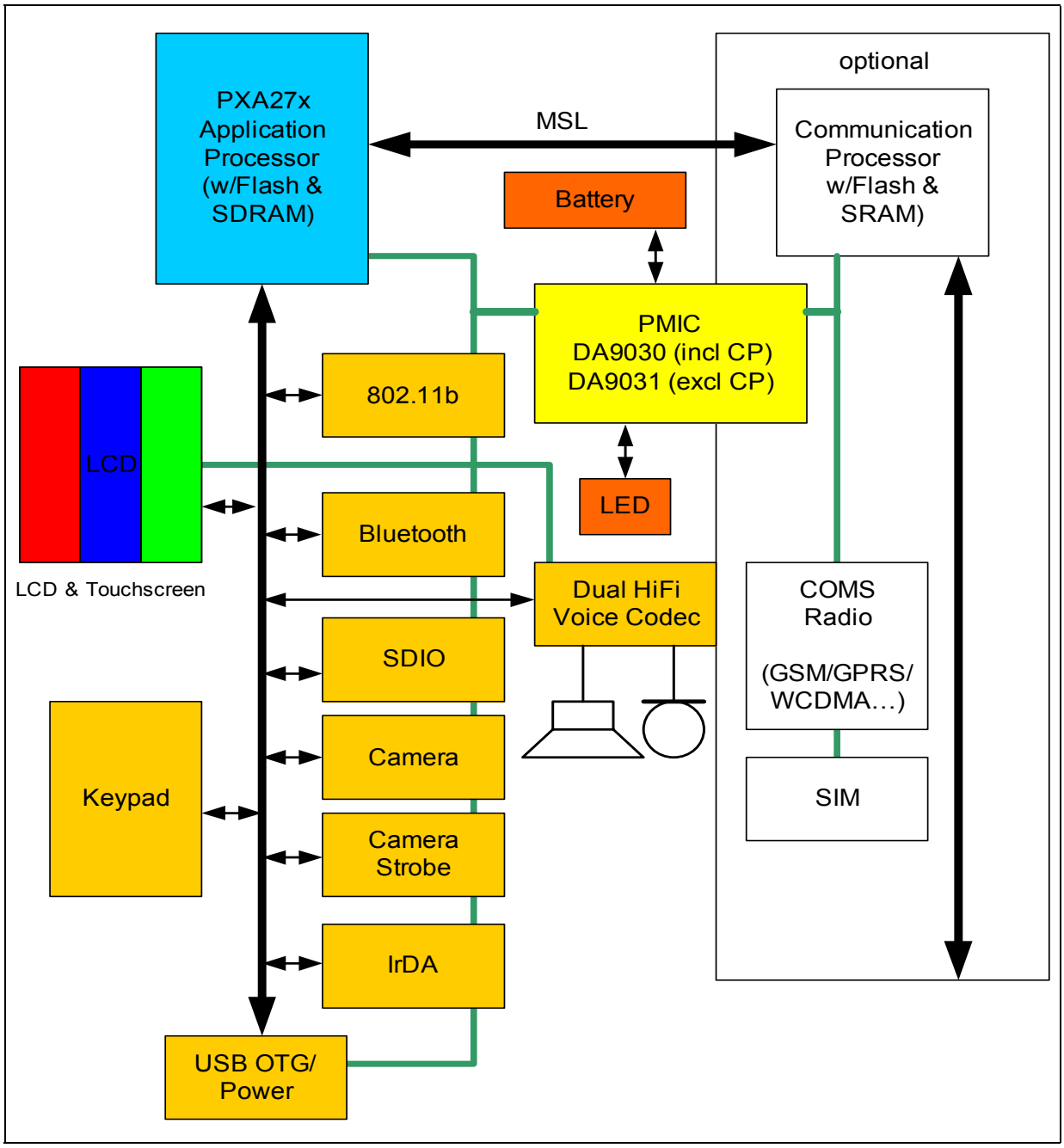
The DA9030 PMIC is an highly integrated power management controller and includes the following main features:

- Integrated, single-chip solution for battery charge control and power supply management
- Programmable low-dropout linear voltage regulators with over 65-dB power-supply rejection ratio (PSRR) from 10 Hz to 10 kHz
- High efficiency DC-to-DC converter (buck) with programmable output voltage
- High efficiency DC-to-DC converter (buck) with programmable output voltage and dynamic voltage control (DVC)
- One step-up low-current charge pump DC-to-DC converter with external capacitors
- System over-voltage and under-voltage shutdown
- Power on/off and reset control logic
- Five individually selectable LED drivers with PWM control
- Boost converter for two parallel strings of up to four white LEDs each
- Vibrator driver with PWM control
- Internal 8-bit analog-to-digital converter with auxiliary inputs; an automatic mode of operation allows monitoring of charger operation
- 8-Ohm 500mW speaker driver with volume control
- Linear or pulse-mode charger for single-cell Li-Ion or Li-Polymer packs
- Integrated control over pre-charge, constant-current, and constant-voltage charging phases; pulse-mode charging with programmable on/off time
- Programmable charging current and voltage
- Programmable charge termination by time
- Battery temperature sensing
- Battery pack wake up
- Serial 400 kHz I^2C-compatible interface to transfer the control data between the PMIC and the host controller (with two I^2C addresses)
- Internal current controlled oscillator (CCO) generates the internal high clock frequency
- Interrupt signal (IRQ) that generates the interrupt request for the host controller
- Super capacitor back-up charger
- Enhanced ESD protection on all pins that connect to the main battery pack
- USB OTG charge pump with session detection
- USB detection via EXTON pin enables automatic start-up including linear charging at 100mA.

2.0 System Application Block Diagram

Figure 1 depicts a system application block diagram.

Figure 1. Block Diagram



The system-application block diagram outlines a mobile handset using the PXA27x processor. The Dialog Semiconductor DA9030 PMIC handles all required power supplies for the PXA27x processor within such a system and also controls an (optional) communications processor (referred to in the remainder of this document as CProc) as well as the application processor, independently.

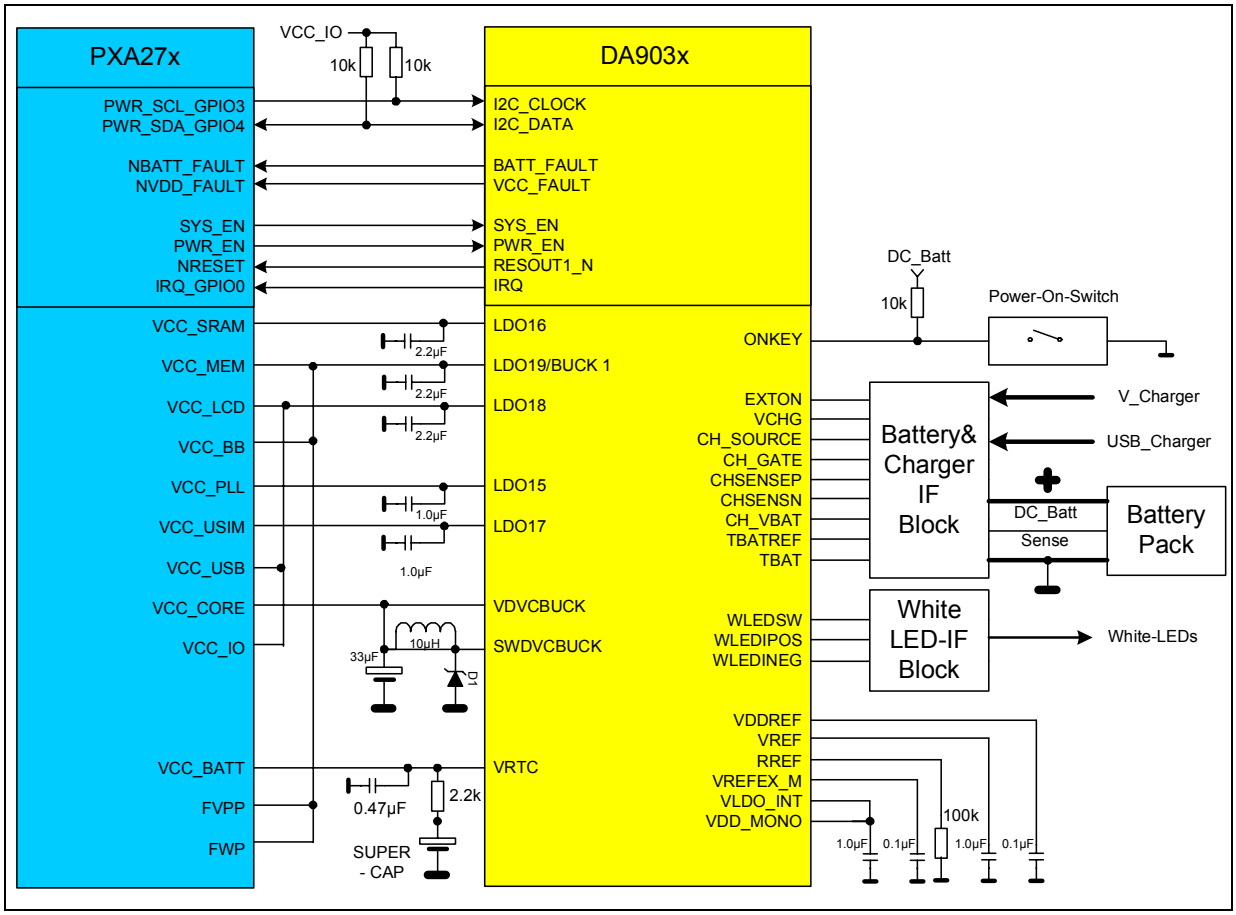
The applications processor controls all system-related peripheral functions whereas the communication controller predominantly focuses on the radio-communication part. The inter-processor communication occurs through the high-speed mobile serial-link interface (MSL).

The communication processor and its associated parts are optional. In this case, when only using the application processor PXA27x, the Dialog Semiconductor PMIC derivate DA9031 may be selected to reduce overall system cost.

2.1 System Power Connection Diagram

Connecting the Intel® PXA27x Processor Family and DA903x PMIC is shown in Figure 2.

Figure 2. Intel® PXA27x Processor Family and DA903x PMIC Interconnection



The schematic diagram in Figure 1 shows how the PXA27x processor and the DA903x can be interconnected to build an efficient power-supply system with few additional components. This configuration is set up for dynamic-voltage management as well as for supporting sleep mode. The white LED backlight circuit is optional.

Not all the pins of the DA903x PMIC and the PXA27x processor are shown. The diagram is described in more detail throughout the remainder of this section and is also referred to in other sections. Refer to the device data sheets for the use and description of the other pins.

2.2 PXA27x Processor Family Power Domain

Table 1 describes the PXA27x processor power domain and the related PMIC power sources. Two options are shown for driving internal or external memory.

Table 1. PXA27x Processor Power Domains, Connections and Descriptions

PXA27x Processor	DA903x PMIC	Description
VCC_BATT	VRTC	The RTC LDO features a very low quiescent current (<10uA) since this LDO is running all the time, even when the handset is switched off. The typical output voltage is 2.65V.
VCC_CORE	DVCBUCK	A DC to DC buck converter that supplies 0.85V - 1.625V at 600mA with a +/- 3% accuracy. The converter operates at a high frequency (1MHz) to allow the use of a small external inductor.
VCC_PLL	LDO15	A 25mA low-noise LDO with programmable output voltage (1.1V to 2.65V in steps of 50mV) from the I^2C bus. The default value at power up for this LDO is 1.3V.
VCC_MEM	LDO19	A 110mA "digital" LDO with programmable output voltage (1.8V to 3.2V in steps of 100mV) from the I^2C bus. This LDO can be used to supply other external peripheral devices connected to the BB. The default value at power up for this LDO is 1.8V.
VCC_BB		
FVPP		
FWP		
VCC_MEM	Buck 1	A 600mA DC-to-DC converter suitable for large memory configurations and MCP options. The voltage can be set to 1.8V. (can be used instead of LDO19)
VCC_IO	LDO 18	A 100mA low dropout digital LDO with programmable output voltage (1.8V to 3.2V in steps of 100mV) from the I^2C bus. The default value at power up for this LDO is 2.8V.
VCC_USB		
VCC_LCD		
VCC_USIM	LDO 17	A 30mA low noise LDO with programmable output voltage (1.8V to 3.2V in steps of 100mV) from the I^2C bus. The default value at power up for this LDO is 1.8V.
VCC_SRAM	LDO 16	A 40mA low noise LDO with programmable output voltage (1.1V to 2.65V in steps of 50mV) from the I^2C bus. The default value at power up for this LDO is 1.1V.

2.3 Digital Signals

Table 2 describes the digital signals.

Table 2. Digital Signal Descriptions (Sheet 1 of 2)

PXA27x Processor	DA903x PMIC	Description
PWR_SCL_GPIO3	I2C_CLOCK	I^2C clock connection
PWR_SDA_GPIO4	I2C_DATA	I^2C bi-directional serial data
NBATT_FAULT	BATT_FAULT	Battery fault signal to PXA27x processor
NVDD_FAULT	VCC_FAULT	Indicates a fault condition on the PXA27x processor LDOs

Table 2. Digital Signal Descriptions (Sheet 2 of 2)

PXA27x Processor	DA903x PMIC	Description
SYS_EN	SYS_EN	Enable signal from PXA27x processor
PWR_EN	PWR_EN	Enable signal from PXA27x processor
NRESET	RESOUT1	Reset output to PXA27x processor
IRQ_GPIO0	IRQ	Interrupt request from PMIC – N-channel open drain output, active low

NOTE: Refer to the *Intel® PXA27x Processor Family Electrical, Mechanical and Thermal Specifications* (EMTS) for detailed information about each signal.

2.4 Component Selection

2.4.1 Components

The components shown in Table 3 are used in the reference design (other equivalent parts can be used as well). Refer to the datasheets for more details.

Table 3. Components

Reference	Description	Value	Type	Manufacturer
D1	Schottky	—	CUS02	Panasonic
L	Inductor	10µH	C4-Y1.2R 4.7uH	Mitsumi
1µF	Capacitor X5R	1µF	ECJ1VB1C105K	Panasonic
2.2µF	Capacitor X5R	2.2µF	ECJ1VB1C225K	Panasonic
0.22uF	Capacitor X7R	220nF	C1608X7R1C224K	TDK
0.3F	Supercap		414R-S-VA5R	Kanebo
RREF	Resistor 1%	100k		Any
RVRTC	Resistor 1%	2.2k		Any

2.4.2 Decoupling Capacitors

Use additional decoupling capacitors, depending on layout as common practice in electronic engineering (that is, close to power-supply input pins; in particular, near VIN pins of the DC-to-DC converters; not shown in the previous diagram).

3.0 System Startup and Operating Modes

Most handheld systems need to operate with the lowest possible power consumption to keep the operating time high. The PXA27x processor as well as the DA903x offer several operating and power-save modes to accommodate these requirements.

3.1 PXA27x Processor Power Modes

The PXA27x processor provides the following power modes: run, turbo, idle, standby, sleep, and deep sleep.

- ***Run mode*** is the normal execution mode. The other power modes must be entered from run mode. The other power modes return to run mode when being exited.
- ***Turbo mode*** is for use in peak processing and is a multiple of run-mode frequency. The core voltage must allow for the turbo frequency, so a dynamic voltage change can be considered.
- ***Idle mode*** is the first level of reduced power consumption defined by the PXA27x processor. The CPU clock is stopped in idle mode only. There are no consequences for the DA903x.
- ***Sleep mode*** significantly reduces the power consumption of the PXA27x processor since most of the internal processor state is not clocked and, therefore, not preserved. Only the real-time clock (RTC) and the power manager are clocked while a PXA27x processor is in sleep mode. The DA903x PMIC pulls the core voltage down to VSS during sleep mode. (see sections 3.2 and 3.3).
- ***Deep sleep mode*** is where all power domains except the VCC_BATT can be powered down. External low-voltage and high voltage power supplies can be disabled.
- ***Standby mode*** is similar to sleep except CPU state is preserved. All activity inside the processor stops. RTC operational, OS timer are optionally operational.

The initial core frequency is low after boot up. The frequency-change sequence changes the processor clock frequency for run mode and turbo mode (see the *Intel® PXA27x Processor Family Developer's Manual* for details).

3.2 DA903x Operating Modes Overview

3.2.1 Power-Down Mode

The power-down mode of the DA903x has the minimum current consumption. The only active blocks are the internal power-on-reset block, the RTC LDO and its ultra low-power bandgap reference, and the input-detection circuit for the charger VCHG_DETECT. All other blocks are disabled to avoid draining the external battery when the equipment is switched off.

When the battery voltage is below the VPORLOWER (VRTC + 0.075V) threshold voltage, the DA903x is held in a reset state. During this time, the current consumption is at an absolute minimum with the only active circuits being the RTCLDO bandgap (used by the POR generator) and the charger detection comparator. While the internal POR is asserted, the DA903x is held in the power-down state and cannot be turned on until the POR has negated.

3.2.2 Power-On-Start-up Mode

The start-up mode is entered from the power-down mode initiated by the ONKEY_N, PWREN1, EXTON or VCHG_DETECT signals. This mode sequentially starts up the internal references, internal oscillator, voltage supervision, buck converter, followed by the LDO regulators—all under the control of an internal state machine. When a fault is detected (battery under-voltage, battery over-voltage or watchdog time out of the CProc response), the state machine terminates the start-up mode and returns to the power-down mode; otherwise, the state machine completes the start-up sequence, at which point the DA903x switches to the active mode.

3.2.3 Active Mode

The active mode is entered after a successful start-up or pre-charge mode. During this operating mode, the PXA27x processor takes over control of the system power management. Status information is passed to the control processor via the I^2C bus. The DA903x can flag interrupt requests to the control processor via a dedicated interrupt pin (IRQ).

Additionally, the temperature and voltages inside the DA903x are monitored and any fault conditions are flagged to the control processor.

3.2.4 Sleep Mode

Certain parts of the DA903x can be switched to a power-saving mode under the control of the SLEEP_N pin (active low), via the I^2C register bit SLEEP, or via the PWR_EN and SYS_EN pins. This sleep mode is entered only when the DA903x was in active mode.

In sleep mode, the charger block for fast charging is powered down, the buck switches to a low-power mode, and the external master clock can be disconnected (the DA903x switches to an internal oscillator when the external master is not present). The battery under-voltage detection (via auto-ADC), reference generators, and internal oscillator are still enabled in this mode. The LDO for each processor can be programmed to one of the states when sleep mode is active (off, on, or high-Z state).

3.3 Power ON/OFF and Reset Control

3.3.1 Internal Power-On-Reset Generator (POR)

To guarantee the correct startup of the DA903x, a power-on-reset (POR) is generated for the first connection of either the charger supply or the battery supply voltage. An internal shunt regulator supplied from the charger input is implemented that allows the DA903x to operate when the primary battery is completely discharged. This regulated supply is switched to the VDDREF pin of the DA903x. The POR is asserted while the voltage on VDDREF is less than the VPORUPPER threshold voltage. The VDDREF pin is also the supply for the VRTC LDO. The VDDREF pin is internally switched back to the main battery supply when the charger is not present.

The internal POR is negated when the VDDREF voltage rises above the VPORUPPER threshold voltage. The DA903x starts the bandgap reference circuit and the internal oscillator reads the contents of the fuse trim block, after which it returns to the power-down mode.

The DA903x is held in a reset state while the POR is asserted, during which the current consumption is at an absolute minimum, with the only active circuits being the RTCLDO bandgap (used by the POR generator) and the charger detection comparator. The DA903x cannot be turned on until the POR has negated. RESOUT1_N is held low in this state.

3.3.2 Switch On and Watchdog

There are four different ways to switch on the DA903x chip:

- Pulling the ONKEY_N input signal low (falling edge event)
- Pulling the PWREN1 high from the control processor interrupt alarm signal (rising-edge event)
- Pulling the EXTON input signal high from the external peripheral (rising-edge event)

- The DA903x sensing that the charger external adapter is connected by means of an internal signal VCHG_DETECT being asserted.

Pulling the ONKEY_N signal low is the normal way of turning on the device, which (1) turns on most of the LDO regulators and the buck converter inside the DA903x, and (2) asserts the RESOUT_N and RESOUT_N_OD signal to the (optional) baseband processor and RESOUT1_N for the PXA27x processor. Once the RESOUT1_N is released (goes high), the PXA27x processor starts an activation sequence via the I^2C bus communication with the DA903x, at which point the ONKEY_N can be released. The RESOUT_N_OD output is provided for use with external peripheral circuits, and can be OR'ed with an external-reset pin to generate a reset toward the (optional) baseband processor on RESOUT_N. PWREN1 going high also turns on the device; for example, when the alarm in the RTC module expires and when the ALARM signal from the processor is asserted.

An external device can also turn on the handset with the auxiliary EXTON signal, and initiate automatic linear charging at 100mA. With suitable external components, the DA903x can detect an external USB power source being connected, from which automatic linear charging at 100mA can be started.

3.3.3 Start-up Sequence with ONKEY_N or EXTON or PWREN1

When a start-up condition is detected on one of these pins and the VBAT voltage is above the VPORUPPER threshold voltage (that is, the internal POR is not asserted), the master band-gap reference and the internal oscillator is enabled. The DA903x returns to power-down mode when the signal has been released after a period of Tdelay1 (32ms, to allow for debouncing of the input signal and the bandgap reference to settle). If the signal is still asserted, the DA903x continues the start-up sequence and proceeds by comparing the VBAT with the VBATGOOD threshold. The PXA27x boot sequence starts performing the following sequence if the battery level is "good":

- The DA903x de-asserts the RESOUT1_N (high) after a minimum 50 ms from powerup of the RTC LDO after POR (this resets the PMU unit in the PXA27x processor).
- Once the VBAT has risen above the VBATUNDER threshold, the DA903x de-asserts (high) BATT_FAULT signal to the PXA27x processor (indicating that VBAT is OK).
- The DA903x waits for the PXA27x processor to assert (high) SYS_EN and powers up the LDOs associated with this signal (described in this section).
- The DA903x waits for the PXA27x processor to assert PWR_EN (minimum 125 ms after asserting SYS_EN) and powers up the sources associated with this signal (described in this section).
- After all sources are stable for the PXA27x processor, the DA903x de-asserts (high) VCC_FAULT (so the PXA27x processor can continue with its power-up sequence).

The SYS_EN signal controls these LDOs:

- LDO18
- LDO19
- LDO17
- Plus LDO10/LDO11 if enabled

These LDOs are in charge of these PXA27x processor power domains:

- VCC_IO

- VCC_LCD
- VCC_MEM
- VCC_BB
- VCC_USIM
- VCC_USB.

When SYS_EN is asserted, the power-up sequence of the different LDOs begins with LDO18 then all other LDOs. The order in which these LDOs are powered up does not matter with the exception of VCC_IO. The VCC_IO supply must be the highest potential in the system (excluding VCC_BATT and VCC_USB) and must be sequenced on at the same time or before the other supplies enabled by SYS_EN.

The PWR_EN signal controls these sources:

- DC/DC converter with DVC, LDO15, LDO16. (Plus LDO10/LDO11 if enabled)
- These sources are in charge of these PXA27x processor power domains:
  - VCC_CORE
  - VCC_PLL
  - VCC_SRAM
- When PWR_EN is asserted, the power-up sequence of the different sources is as follows:
  - DC/DC with DVC
  - All other LDOs at the same time or in interval timing.

There is no importance in which order these LDOs are powered up.

Once the RESOUT1_N to the PXA27x processor or RESOUT_N to the baseband processor is released, the baseband processor or the PXA27x processor must write a logic 1 to a dedicated I^2C Watchdog register bit during the next 8s period. This write moves the DA903x into the active mode and starts the continuous watchdog monitoring circuit. Failure to issue the initial watchdog write results in shutdown of the DA903x to the power-down state.

All other I/Os of the DA903x to the PXA27x processor are released after the rising of RESOUT1_N. The I/O includes these I/O signals:

- PWR_EN
- SYS_EN
- I^2C
- USB OTG signals
- IRQ.

3.3.4 PXA27x Processor Sleep Mode

The PXA27x processor sleep mode is triggered via PWR_EN and SYS_EN. The PXA27x processor has two sleep stages. The first one is sleep mode where only the low voltage sources are shut down (PWR_EN low). The other is deep sleep where all sources are shut down (high and low voltages, PWR_EN and SYS_EN low).

When PWR_EN is lowered, all low-voltage sources to the PXA27x processor are shut down (DVM DC/DC, LDO15 and LDO16). There is no significant order to shut down; the only constraint is that they must be shut down within a maximum of 100msec.

When SYS_EN is lowered, all high-voltage sources to the PXA27x processor must be shut down. (LDO17, 18 and 19). There is no constraint regarding the shut-down order with the exception of VCC_IO. The VCC_IO supply must be the highest potential in the system (excluding VCC_BATT and VCC_USB). The only other constraint is that the SYS_EN shut-down sequence cannot occur before PWR_EN shut down has completed (this is handled by the PXA27x processor).

The opposite operations occur when exiting from sleep mode. When entering sleep mode, then exiting sleep mode is accomplished through the rising PXA27x processor PWR_EN signal causing the DA903x to power up all low-voltage sources to the PXA27x processor (DVM DC/DC, LDO15, and LDO 16).

When exiting deep sleep, the PXA27x processor raises SYS_EN first causing the DA903x to power up all high-voltage LDOs to the PXA27x processor (LDO 17,18,19). The DA903x first powers up LDO18 and then all others in no special order; the time constraint for all high-voltage LDOs to be stable is 100msec.

Next, the PXA27x processor raises PWR_EN (125 msec after raising SYS_EN), causing the low power sources to power up (DVM DC/DC, LDO15 and LDO16).

Note: The DA903x power supplies can be enabled user the signals (PWR_EN and SYS_EN) or by programming a register control through the I^2C. By default, the power suplies within the DA903x are enabled using the external signals driven by PWR_EN and SYS_EN. When using the PXA27x application processor together with a communication processor, the communication processor can be used to control the power for the PXA27x application processor via I^2C commands.

3.4 PMIC Control Software Interface

The DA903x PMIC can be controlled and read through a serial interface using the control software included in the Power Management Evaluation Kit. The DA903x PMIC is controllable at several levels, including chip, module, register, and bit levels. Using the control software allows the Dialog Semiconductor DA903x PMIC to power the PXA27x processor at the correct voltages and sequences required for a successful boot up. Refer to the *DA903x Power Management Evaluation Kit* for full functionality and capabilities of the control software.

3.5 Dynamic Voltage Management (DVM)

There are a number of features on the PXA27x processor that enable the dynamic management of power consumption. Using these features, the core frequency voltage of the processor can be modified during operation, dynamically matching the computing performance to the current computing workload. The Dialog Semiconductor PMIC combined with the PXA27x processor and DVM software can run a wide range of applications using only a fraction of the battery power that would be required running at the fixed frequency and voltage needed for the peak computing workload.

Supporting DVM in the Dialog Semiconductor DA903x allows the following features to be fully used:

- The buck converter output voltage is programmable over the I^2C bus in the range 0.85V to 1.625V in 25mV steps. Additionally, the output voltage can be fixed at 1.8V for use with memory.
- The buck converter output voltage ramp rate is programmable over the I^2C bus in the range of 1.6mV/us to 25mV/us with a 4 bit register.

3.6 System Programming

System programming covers the power-related issues from a software perspective. The proposed methods typically are part of the operating system or a basic input/output system.

The PXA27x processor registers and the DA903x PMIC registers are being read and written at power up, when the system enters/exits sleep mode, or when the core voltage changes dynamically. Using the I^2C link, the PXA27x processor has full control to the DA903x registers.

4.0 Battery Charger Control

The battery-charger control block controls the charging of the battery and allows a startup independent of the battery voltage. The charging block contains the following:

- An internal regulator, which is active when the battery voltage is too low to allow normal operation; this regulator is supplied from the VCHG pin
- Current regulation, which is needed for constant current charging
- Voltage regulation, which is needed for constant voltage charging
- Current monitoring, which is always active when the charger is on
- Over voltage monitoring, which is always active when the charger is on
- Temperature monitoring, which is needed to turn off charging when the battery temperature is too high or too low.

The battery charger supports the following battery chemistries:

- Single-cell Li-Ion at 4.1V
- Single-cell Li-Ion at 4.2V
- Li-Polymer pack

Charging is separated into three different modes. One is the standalone *pre-charge* mode; the second is the *fast-linear charge* mode, which is controlled by the control processor. A third *fast-pulse charge* mode can also be used, where the charging current is limited by the “wall-cube” power supply rather than the external FET. In this mode, the external FET acts solely as a switch, allowing high current charging of the battery.

Refer to the DA903x documentation for more information on battery charging capabilities and functionality.

5.0 Conclusion

This application note provides basic information for connecting the Dialog Semiconductor DA903x advanced power management controller to the Intel® PXA27x processor family. Dialog Semiconductor can design a variant PMIC to address specific needs for other applications, if required.

For more detailed information on the PMIC circuits, contact Dialog Semiconductor directly (www.dialog-semiconductor.com).

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