Flexible system PMIC with USB power manager

General description

DA9052 is a highly integrated power management integrated circuit (PMIC) subsystem with supply domain flexibility to support a wide range of application processors, associated peripherals and user interface functions.

Combining a dual input switched-mode USB compatible charger, full power path management and multiple sleep modes, the device offers an energy-optimized solution suitable for portable handheld, wireless, industrial and infotainment applications.

The high-efficiency Li-Ion/Polymer switching charger supports precise current/voltage charging as well as pre-charge and USB modes without processor interaction. During charging, the die temperature is thermally regulated enabling high-capacity batteries to be rapidly charged at currents up to 1.26 A with minimum thermal impact to space-constrained PCBs. USB suspend mode operation is supported and, for robustness, the power inputs are protected against over-voltage conditions.

The autonomous power-path controller seamlessly detects and manages energy flow between an AC adaptor, USB cable, and battery while maintaining USB power specification compliance. The internally-generated system power rail supports power scenarios such as instant-on with a fully discharged battery. A reverse-protected backup battery charger is also integrated into the powerpath function.

Controlled by a programmable digital power manager the 14 user programmable switched/linear regulators may be configured to meet the start-up sequence, voltage, and timing requirements for most applications. The power manager includes supply-rail qualification and system reset management. For optimal processor energy-per-task performance dynamic voltage scaling is available on up to five supply domains. Dialog Semiconductor's patented **SmartMirror™** dynamic biasing is implemented on all linear regulators.

An integrated 10-channel general purpose ADC includes support for a touch screen controller with pen down detect, programmable high/low thresholds, an integrated current source for resistive measurements and system voltage monitoring with a programmable low voltage warning. The ADC has 8-bit resolution in auto mode and 10-bit resolution in manual conversion mode.

Key features

- Switched DC/USB charger with power path management
- Four buck converters (three have DVC)
  0.5 V to 3.6 V, up to 1.6 A (combined)
- 10 programmable LDOs
  High PSRR, 1 % accuracy
- Low power backup charger
  1.1 V to 3.1 V, up to 6 mA
- 10 channel general purpose ADC with touch screen interface
- 32 kHz RTC oscillator
- High voltage white LED driver boost, three strings
- 16-bit GPIO bus for enhanced wakeup and peripheral control
- 2-wire and 4-wire control interfaces
- USB supply detection and charge current selection
- 7x7 mm 169 VFBGA, 0.5 mm pitch package

Applications

- Personal media players
- Smartphone handsets
- Personal navigation devices
- Consumer infotainment devices
- IoT

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3 Terms and definitions

ADC	Analog to Digital Converter
DVC	Dynamic Voltage Control
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GND	Ground
GSM	Global System for Mobile Communication
IRQ	Interrupt Request
LDO	Low Dropout Voltage Regulator
LED	Light Emitting Diode
NTC	Negative Temperature Coefficient
OTP	One Time Programmable
OV	Overvoltage
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMIC	Power Management Integrated Circuit
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RTC	Real Time Clock
TDMA	Time Division Multiple Access
TRC	Trimming Release Code
USB	Universal Serial Bus

4 Block diagram

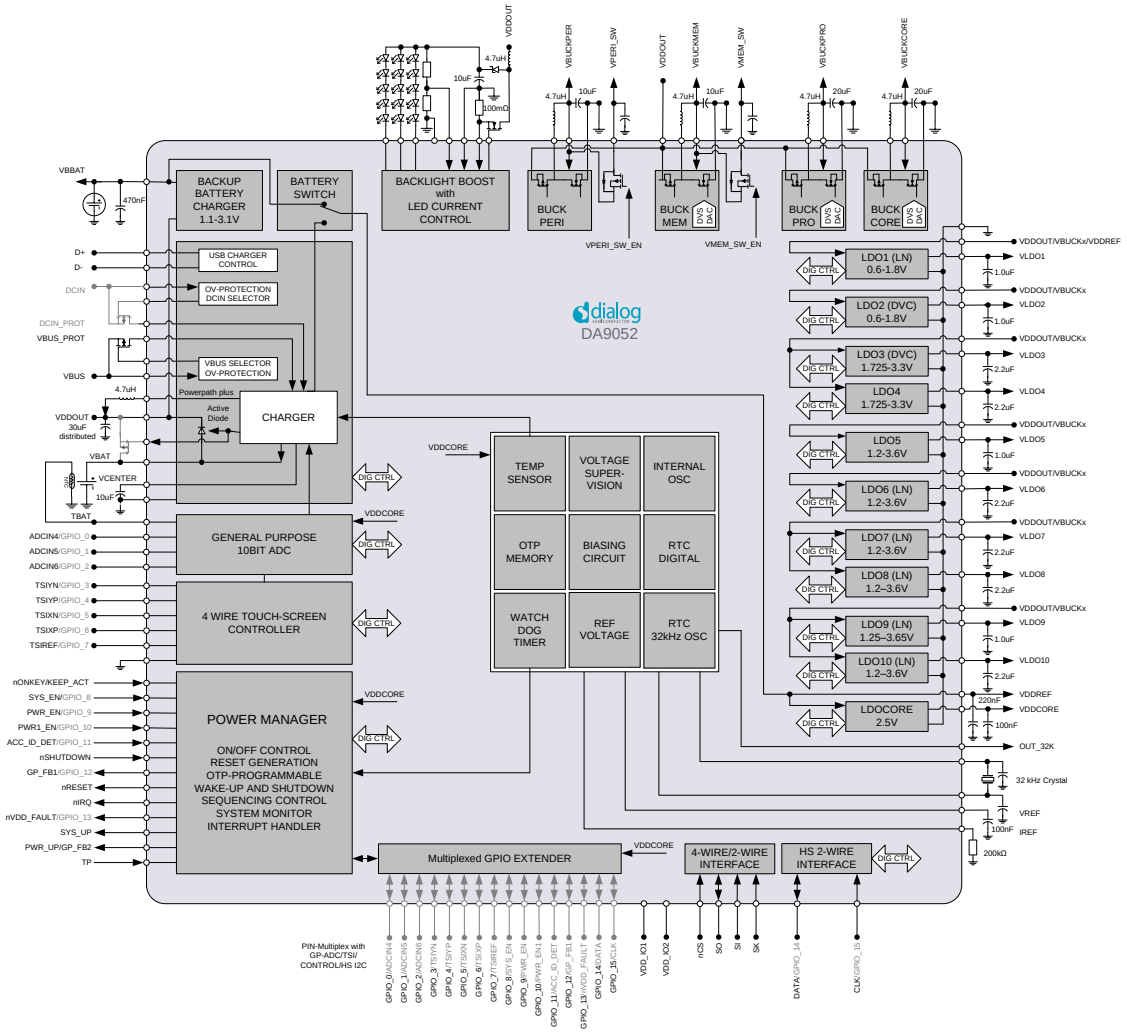


Figure 1: Block diagram

5 Generated supply domains

The default voltages shown in Table 1 indicate the voltages obtained from an unprogrammed device.

Table 1: Regulator overview

Regulator	Supplied pins	Supplied voltage (V)	Supplied max. current (mA)	External component	Notes
BUCKCORE Note 1	VBUCKCORE	0.5 to 2.075 ±3 % accuracy default 1.8	700	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off
			800		Between DVC transitions
BUCKPRO Note 1	VBUCKPRO	0.5 to 2.075 ±3 % accuracy default 1.2	700	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate, can be combined with BUCKCORE, pull-down resistor switch off, common supply with BUCKMEM
			800		Between DVC transitions
BUCKMEM	VBUCKMEM; VMEM_SW	0.95 to 2.525 ±3 % accuracy default 2.0	650	2.2 µH to 4.7 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; second output with sequencer controllable switch, pull-down resistor switch off, common supply with BUCKPRO
			750		< 2.075 V and between DVC transitions
BUCKPERI	VBUCKPERI VPERI_SW	1.8 to 3.6 ±3 % accuracy default 3.3	650	2.2 µH to 4.7 µH	2 MHz, 50/100 mV steps At low input voltages the buck switches to a follower mode (100 % duty cycle), second output with sequencer controllable switch
			750		< 2.1 V
BOOST	Ext. FET	5 to 25, regulated via current feedback	78	4.7 µH	Current controlled boost converter for three strings of up to six serial white LEDs. Overvoltage protection via a voltage feedback pin
LDO1	VLDO1	0.6 to 1.8 ±3 % accuracy default 1.2	40	1.0 µF	High PSSR, low noise LDO, 50 mV steps, pull-down resistor switch off
LDO2	VLDO2	0.6 to 1.8 ±3 % accuracy default 1.2	100	1.0 µF	DVC, digital LDO, 25 mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
LDO3	VLDO3	1.725 to 3.3 ±3 % accuracy default 2.85	200	2.2 µF	DVC, digital LDO, 25 mV steps, DVC with controlled slew rate, common supply with LDO4

Regulator	Supplied pins	Supplied voltage (V)	Supplied max. current (mA)	External component	Notes
LDO4	VLDO4	1.725 to 3.3 ± 3% accuracy default 2.85	150	2.2 µF	Digital LDO, 25 mV steps, optional hardware control from GPI1, common supply with LDO3
LDO5	VLDO5	1.2 to 3.6 ±3 % accuracy default 3.1	100	1.0 µF	Digital LDO, 50 mV steps, pull-down resistor switch off, optional hardware control from GPI2,
LDO6	VLDO6	1.2 to 3.6 ±3 % accuracy default 1.2	150	2.2 µF	High PSRR, low noise, 50 mV steps
LDO7	VLDO7	1.2 to 3.6 ±3 % accuracy default 3.1	200	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO8
LDO8	VLDO8	1.2 to 3.6 ±3 % accuracy default 2.85	200	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO7
LDO9	VLDO9	1.25 to 3.65 ±1 % accuracy (Note 2) default 2.5	100	1.0 µF	High PSRR, low noise, 50 mV steps, OTP trimmed, optional hardware control from GPI12, common supply with LDO10
LDO10	VLDO10	1.2 to 3.6 ±3 % accuracy default 1.8	250	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO9
BACKUP	VBBAT	1.1 to 3.1 default 3.0	6	470 nF	Programmable Voltage, configurable current limit between 100 µA and 6000 µA, reverse current protection
LDOCORE	Internal PMIC supply	2.5 ±2 % accuracy	4	100 nF	Not for external use

Note 1 For higher output current applications BUCKCORE and BUCKPRO may be combined to provide 1.6 A.

Note 2 At default voltage (1 % accuracy requires VLDO9 > 1.5 V).

6 Pad description

6.1 DA9052 BGA ball-out

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	VREF	DCIN_PROT	DCIN_PROT	VBUS_PROT	VBUS_PROT	VCENTER_A VCENTER_B	VSW	VSW	VDDOUT	VDDOUT	VBAT	VBAT
B	XOUT	VBBAT	DCIN_SEL	DCIN	VBUS_SEL	VBUS	NC	NC	NC	GP_FB1_GPIO_12	AD_CONT	VMEM_SW	DMINUS
C	XIN	VDD_REF	NC	ADCIN6_GPIO_2	ADCIN5_GPIO_1	ADCIN4_GPIO_0	NC	NC	NC	PWR_EN_GPIO_9	nVDD_FAULT_GPIO_13	VBUCKMEM	DPLUS
D	VLDO1	VDDCORE	NC	NC	IREF	N	N	N	N	SYS_EN_GPIO_8	nSHUTDOWN	VPERI_SW	VBUCKPERI
E	VDD_LDO2	VDD_LDO1	NC	NC	N	N	N	N	N	nIRQ	NC	NC	VDD_PERI
F	VLDO5	VLDO2	NC	NC	NC*	NC*	NC*	N	N	nRESET	NC	NC	SVBUCKPERI
G	VLDO6	VDD_LDO5	NC	NC	Q	Q	NC*	N	N	NC	NC	NC	SVBUCKPRO
H	VLDO4	VDD_LDO6	NC	NC	Q	Q	NC*	N	N	NC	NC	NC	VDD_COR_PRO
J	VLDO3	VDD_LDO3_4	NC	NC	Q	Q	NC*	N	N	PWR_UP_GP_FB2	NC	NC	VDD_COR_PRO
K	VLDO7	VDD_LDO7_8	NC	VDD_IO2	TSIXN_GPIO_5	TSIYN_GPIO_3	TSIXP_GPIO_6	TSIYP_GPIO_4	TSIREF_GPIO_7	SI	NCS	OUT32K	SVBUCKCORE
L	VLDO8	PWR1_EN_GPIO_10	ACC_ID_DET_GPIO_11	VDD_IO1	TP	TBAT	LED3_IN	LED2_IN	NC	SO	SK	SYS_UP	SVBUCKMEM
M	VLDO9	CLK_GPIO_15	VDD_LDO9_10	NC	NC	NC	NC	NC	LED1_IN	SW_BOOST	nONKEY_KEEP_ACT	VBUCKCORE	VDD_MEM
N	DATA_GPIO_14	VLDO10	NC	NC	NC	NC	NC	NC	BOOST_SENSE_N	BOOST_SENSE_P	BOOST_PROT	VBUCKPRO	NC

Figure 2: PCB board DA9052 BGA pad arrangement (view from the top)

Note 1 Connect NC* to GND plane for thermal enhancement.

Table 2: Pin description

NBA pad	Ball	Type (Table 3)	Pin name	Alternate port	Pin description
Power manager					
29	M11	DI	nONKEY _KEEP_ACT	KEEP_ACT	On/off key with optional long press shutdown/hardware input for watchdog supervision
82	D10	DI/DIO	SYS_EN_GPIO_8	GPIO_8	Hardware enable of power domain SYSTEM/GPIO_8
81	C10	DI/DIO	PWR_EN_GPIO_9	GPIO_9	Hardware enable of power domain POWER/GPIO_9
16	L2	DI/DIO	PWR1_EN _GPIO_10	GPIO_10	Hardware enable of power domain POWER1/GPIO_10 with high power output and blinking feature, input for power sequencer WAIT ID
64	L3	DI/DIO	ACC_ID_DET _GPIO_11	GPIO_11	ACC_ID_DET accessory detection circuitry/GPIO_11 with high power output and blinking feature
78	D11	DI	nSHUTDOWN		Active low input from switch or error indication line from host to initiate shutdown
76	F10	DO	nRESET		Active low RESET towards host
80	B10	DO/DIO	GP_FB1_GPIO_12	GPIO_12	Status indication towards host for a valid Wakeup event (EXT_WAKEUP) or indicator for ongoing power mode transition (READY) /GPIO_12, enables hardware control of LDO9
77	E10	DO	nIRQ		Active low IRQ line towards host
79	C11	DO/DIO	nVDD_FAULT _GPIO_13	GPIO_13	Active low indication for low supply voltage/GPIO_13
73	L12	DO	SYS_UP		Sequencer status indicator: All SYSTEM IDs powered up
74	J10	DO/DO	PWR_UP_GP_FB2	GP_FB2	Sequencer status indicator: All POWER IDs powered up (PWR_UP) or programmable level controlled from the power sequencer (GP_FB2)
17	L4	PS	VDD_IO1		First supply I/O voltage rail
18	K4	PS	VDD_IO2		Alternate supply I/O voltage rail
67	L5	DIO	TP		Test pin, enables POWER COMMANDER mode
4-wire/2-wire Interfaces					
25	L10	DIO	SO		4-wire data output/2-wire data
70	K10	DI	SI		4-wire data input
26	L11	DI	SK		4-wire/2-wire clock
27	K11	DI	nCS		4-wire chip select

NBA pad	Ball	Type (Table 3)	Pin name	Alternate port	Pin description
15	N1	DIO	DATA_GPIO_14	GPIO_14	HS-2-wire Data/GPIO_14 (enables reset if long press in parallel with GPI15) with high power output and PWM LED control
63	M2	DI	CLK_GPIO_15	GPIO_15	HS-2-wire Clock/GPIO_15 (enables reset if long press in parallel with GPI14)) with high power output and PWM LED control
Voltage Regulators					
5	D1	AO	VLDO1		Output voltage from LDO1
6	E2	PS	VDD_LDO1		Supply voltage for LDO1
7	F2	AO	VLDO2		Output voltage from LDO2
56	E1	PS	VDD_LDO2		Supply voltage for LDO2
11	J1	AO	VLDO3		Output voltage from LDO3
10	H1	AO	VLDO4		Output voltage from LDO4
59	J2	PS	VDD_LDO3_4		Supply voltage for LDO3 and LDO4
8	F1	AO	VLDO5		Output voltage from LDO5
57	G2	PS	VDD_LDO5		Supply voltage for LDO5
9	G1	AO	VLDO6		Output voltage from LDO6
58	H2	PS	VDD_LDO6		Supply voltage for LDO6
12	K1	AO	VLDO7		Output voltage from LDO7
61	L1	AO	VLDO8		Output voltage from LDO8
60	K2	PS	VDD_LDO7_8		Supply voltage for LDO7 and LDO8
13	M1	AO	VLDO9		Output voltage from LDO9
14	N2	AO	VLDO10		Output voltage from LDO10
62	M3	PS	VDD_LDO9_10		Supply voltage for LDO9 and LDO10
55	D2	AO	VDDCORE		Supply for internal circuitry
4	C2	AO	VDD_REF		Switched supply from VBAT, VBUS or VBACKUP
DC/DC buck converters					
32	M12	PS	VBUCKCORE		Output voltage from DVC DC/DC BUCKCORE
34	K13	PS	SWBUCKCORE		Switching node for BUCKCORE
31	N12	PS	VBUCKPRO		Output voltage from DVC DC/DC BUCKPRO
35	G13	PS	SWBUCKPRO		Switching node for BUCKPRO
39	C12	PS	VBUCKMEM		Output voltage from DVC DC/DC BUCKMEM
40	B12	PS	VMEM_SW		Second output from BUCKMEM
33	L13	PS	SWBUCKMEM		Switching node for BUCKMEM

NBA pad	Ball	Type (Table 3)	Pin name	Alternate port	Pin description
37	D13	PS	VBUCKPERI		Output voltage from DC/DC BUCKPERI
38	D12	PS	VPERI_SW		Second output from BUCKPERI
36	F13	PS	SWBUCKPERI		Switching node for BUCKPERI
75	M13	PS	VDD_MEM		Supply voltage for BUCKMEM
75	H13, J13	PS	VDD_COR_PRO		Supply voltage for BUCKCORE and BUCKPRO
75	E13	PS	VDD_PERI		Supply voltage for BUCKPERI
Reference Voltage Generation					
86	A2	AOI	VREF		Reference voltage output
54	D5	AO	IREF		Connection for bias setting
Internal Oscillator					
52	C1	AIO	XIN		32 kHz Crystal connection
51	B1	AIO	XOUT		32 kHz Crystal connection
30	K12	DO	OUT_32K		32 kHz Oscillator buffer output
Charger					
49	B5	PS	VBUS_SEL		Control for external overvoltage protection and input selection of VBUS
47	A5, A6	PS	VBUS_PROT		Overvoltage protected VBUS charger input
84	B6	PS	VBUS		USB or wall charger input
50	B3	PS	DCIN_SEL		Control for external overvoltage protection and input selection of DCIN
48	A3, A4	PS	DCIN_PROT		Overvoltage protected DCIN charger input
85	B4	PS	DCIN		Wall charger input
83	A7	PS	VCENTER		Protected input for switching charger (decouple with 10 µF)
46	A8, A9	PS	VSW		Switching node for charger buck
45	A10, A11	PS	VDDOUT		System power supply output
43	B11	PS	AD_CONT		Active diode controller output
44	A12, A13	PS	VBAT		Connection to main battery
Boost converter and LED current sinks					
24	M10	AO	SW_BOOST		Boost switching output
28	N10	AI	BOOST_SENSE_P		High side sense
71	N9	AI	BOOST_SENSE_N		Low side sense
72	N11	AI	BOOST_PROT		Overvoltage protection input
69	M9	AI	LED1_IN		Connection to LED string 1
23	L8	AI	LED2_IN		Connection to LED string 2

NBA pad	Ball	Type (Table 3)	Pin name	Alternate port	Pin description
68	L7	AI	LED3_IN		Connection to LED string 3
USB charger control					
41	C13	AIO	DPLUS		USB D+
42	B13	AIO	DMINUS		USB D-
General purpose ADC and touch screen interface					
22	L6	AI	TBAT		Connection to battery NTC resistor
1	C6	AI/DIO	ADCIN4_GPIO_0	GPIO_0	Connection to GP ADC auto channel 4 with threshold IRQ and resistor measurement option/GPIO_0
53	C5	AI/DIO	ADCIN5_GPIO_1	GPIO_1	Connection to GP ADC channel 5 with 1.2 V hardware comparator IRQ/GPIO_1, enables hardware control of LDO4
2	C4	AI/DIO	ADCIN6_GPIO_2	GPIO_2	Connection to GP ADC channel 6/GPIO_2
65	K6	AIO/DIO	TSIYN_GPIO_3	GPIO_3	TSI interface connection to YN terminal of touch screen
66	K8	AIO/DIO	TSIYP_GPIO_4	GPIO_4	TSI interface connection to YP terminal of touch screen
19	K5	AIO/DIO	TSIXN_GPIO_5	GPIO_5	TSI interface connection to XN terminal of touch screen
20	K7	AIO/DIO	TSIXP_GPIO_6	GPIO_6	TSI interface connection to XP terminal of touch screen
21	K9	PS	TSREF_GPIO_7	GPIO_7	TSI interface reference voltage
Backup Battery charger					
3	B2	AIO	VBBAT		Backup battery connection
VSS					
	D6..E9, E5, F8..J9	VSS	VSS_NOISY		Die VSS_NOISY
	G5..J6	VSS	VSS_QUIET		Die VSS_QUIET

Table 3: Type definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
Ps	Power supply	VSS	Ground connection

7 Absolute maximum ratings

The maximum continuous charger voltage must be less than 5.5 V. The overvoltage protection (OVP) circuit will help protect against transients above this level minimizing effects on operation lifetime.

VDDOUT must not be driven from an external supply if the charger buck is used.

Table 4: Absolute maximum ratings

Parameter	Symbol/Pin	Conditions (Note 1)	Min	Typ	Max	Unit
Storage temperature			-40		+95	°C
Junction temperature	T_J		-40		+150 Note 3	°C
Power supply input	VBAT, VBUS_PROT, DCIN_PROT		-0.3		5.5	V
Supply voltage charger	VBUS, DCIN		-0.3		12	V
Supply voltage LDO and buck input pins except listed below			-0.3		V_{DDOUT} + 0.3 V, 5 V Max	V
Supply voltage all pins except listed above			-0.3		V_{DDOUT} + 0.3 V, 5 V Max	V
Maximum power dissipation BGA package		Derating factor above T_A = 70 °C: 21 mW/°C			1.14	W
Package thermal resistance				Note 2	48	K/W
ESD susceptibility		Human body model			2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 JEDEC 4 layer board, still air, influenced by PCB technology and layout. The numbers of supplies that can be used at the same time at maximum dissipation power is limited by the thermal resistance of the package and the PCB layout.

Note 3 See Table 13.

8 Recommended operating conditions

Table 5: Recommended operating conditions

Parameter	Symbol/Pin	Conditions	Min	Typ	Max	Unit
Operating temperature	T_J		-25		+125	°C
Supply voltage	V_{BAT}		0		4.4	V
Supply voltage charger	V_{BUS}, DCIN		0		5.5	V
Supply voltage IO	V_{DD_IO1}, V_{DD_IO2}		1.2		3.6 Note 1	V

Note 1 V_{DDIO} is not allowed to be higher than VDDOUT.

9 Current consumption

Table 6: Current consumption

Operating mode	Conditions	Min	Typ	Max	Unit
NO-POWER mode	Detection circuits running, oscillator off			15	µA
RESET mode	VDDREF > 2.2 V, bucks and LDOs off (beside LDOCORE), RTC unit on			45 Note 1	µA
POWER-DOWN mode (Standby)	VDDREF > 2.8 V, supplies off (beside LDOCORE), all blocks in POWER_DOWN mode, RTC unit on			45	µA
POWER-DOWN mode (Hibernate)	BUCKCORE, LDOCORE, LDO2, 4, 5 enabled, RTC and GPIO unit on			155 Note 2	µA
ACTIVE mode	All supplies, GPIO, RTC and GPADC on			375 Note 2	µA

Note 1 VDDREF > 2.5 V if not supplied from backup battery.

Note 2 Enabled bucks are set to forced sleep mode, setting ‘00’.

10 Electrical characteristics

10.1 Digital I/O characteristics

Table 7: Digital I/O electrical characteristics, VDDREF ≥ 2.8 V

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
GPI0 – GPI15, nONKEY, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN Input High Voltage	VIH	VDDCORE mode	1.0			V
		VDD_IO2 mode	0.7*VDD_IO2			
GPI0 – GPI15, nONKEY, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN Input Low Voltage	VIL	VDDCORE mode			0.4	V
		VDD_IO2 mode			0.3*VDD_IO2	
CLK, DATA Input High Voltage	VIH	VDDCORE mode	0.7*VDDCORE			V
		VDD_IO2 mode	0.7*VDD_IO2			
CLK, DATA Input Low Voltage	VIL	VDDCORE mode			0.3*VDDCORE	V
		VDD_IO2 mode			0.3*VDD_IO2	
SK, nCS, SI Input High Voltage	VIH		0.7*VDDCORE			V
			0.7*VDD_IOx			
SK, nCS, SI Input Low Voltage	VIL		-0.3		0.3*VDD_IOx	V
GPO0 – GPO15, nVDD_FAULT, SO, nRESET, nIRQ, SYS_UP, PWR_UP, GP_FB2, OUT_32K Output High Voltage	VOH @1 mA VDD_IO1/2 ≥1.5 V	VDD_IO1 mode	0.8*VDD_IO1			V
		VDD_IO2 mode	0.8*VDD_IO2			
GPO0 – GPO15, DATA, SO, nRESET, nIRQ (open drain mode) Output High Voltage	VOH		0	OPEN DRAIN	VDDOUT	V
GPO0 – GPO15, DATA, SO, nVDD_FAULT, nRESET nIRQ, SYS_UP, PWR_UP, GP_FB2, OUT_32K Output Low Voltage	VOL@1 mA				0.3	V

10.2 GPIO characteristics

Table 8: GPIO electrical characteristics, VDDREF ≥ 2.8 V

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Sink current capability GPO 14, 15		VGPIO = 0.1 V		30		mA
Sink current capability GPO 10,11		VGPIO = 0.5 V		15		mA
Source current capability GPO 10,11,14,15		VGPIO = 0.8 * VDD_IO1/2		-4 Note 1		mA
Sink current capability GPO 0…9, 12…13		VGPIO = 0.3 V		1		mA
Source current capability GPO 0…9, 12…13		VGPIO = 0.8 * VDD_IO1/2		-1 Note 2		mA
GPO pull-up resistor Note 3		=1.5 V	100	180	30	kΩ
		VDD_IO1/2 = 1.8 V	65	120	175	
		=3.3 V	25	40	60	
D+/D- input impedance			10			MΩ
					2	pF

Note 1 For Vsupply < 1.5 V the source current for min 0.8 x VDD is limited to 0.8 mA.

Note 2 For Vsupply < 1.5 V the source current for min 0.8 x VDD is limited to 0.5 mA.

Note 3 V(PAD) = 0 V.

10.3 Power on reset

Table 9: Power on reset electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Deep discharge lockout lower threshold	VPOR_LOWER			2.0		V
Deep discharge lockout upper threshold	VPOR_UPPER			2.3		V
Under voltage lower threshold	VDD_FAULT_LOWER Note 1		2.4	2.9	3.15	V
Under voltage lower threshold accuracy	VDD_FAULT_LOWER Accuracy Note 1			±2		%
Under voltage upper threshold	VDD_FAULT_UPPER			VDD_FAULT_LOWER + 0.15		V
Charger buck under voltage	VDDOUT_MIN		3.35	3.40	3.45	V

Note 1 During production VDD_FAULT_LOWER voltage is trimmed via OTP over the range 2.8 V to 3.15 V in 50 mV steps (min 2.4 V for test).

10.4 Watchdog

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Minimum watchdog time	T_{WDMIN}		0.18	0.256	0.33	s
Maximum watchdog time	T_{WDMAX}		1.44	2.048	2.64	s

10.5 2-wire control bus

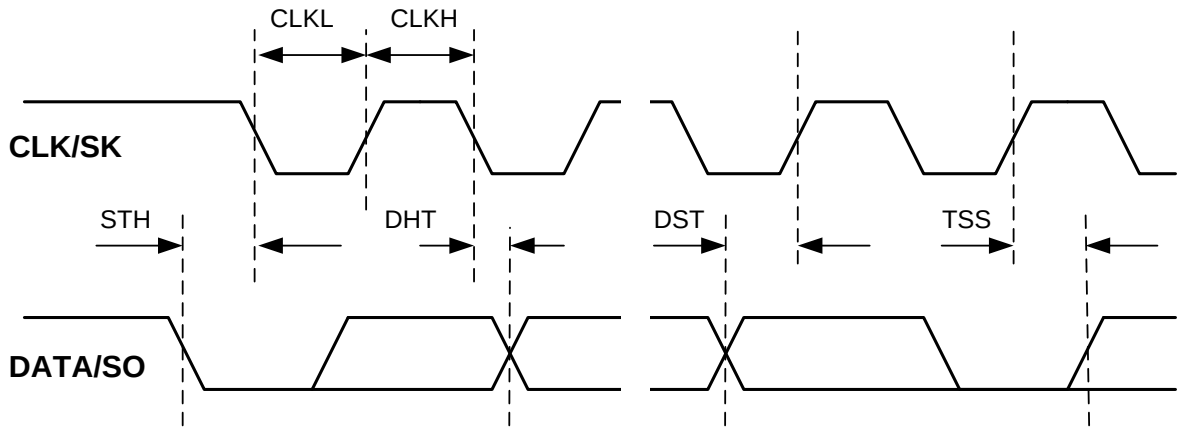


Figure 3: Power manager and HS-2-wire control bus timing diagram

Table 10: 2-wire control bus electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Bus free time STOP to START			1.3			µs
Bus line capacitive load					100	pF
Standard/Fast mode						
CLK clock frequency			1		400	kHz
Bus free time STOP to START			1.3			µs
Start condition set-up time			0.6			µs
Start condition hold time	STH		0.6			µs
CLK low time	CLKL		1.3			µs
CLK high time	CLKH		0.6			µs
2-wire CLK and DATA rise/fall time					300	ns
Data set-up time	DST		100			ns
Data hold-time	DHT		0			ns
Stop condition set-up time	TSS		0.6			µs
High Speed mode						
CLK clock frequency			1		1700	kHz
Start condition set-up time			160			ns

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Start condition hold time	STH		160			ns
CLK low time	CLKL		160			ns
CLK high time	CLKH		60			ns
HS-2-wire CLK rise/fall time					40	ns
HS-2-wire DATA rise/fall time					80	ns
Data set-up time	DST		10			ns
Data hold-time	DHT		10			ns
Stop condition set-up time	TSS		16			ns

10.6 4-wire control bus

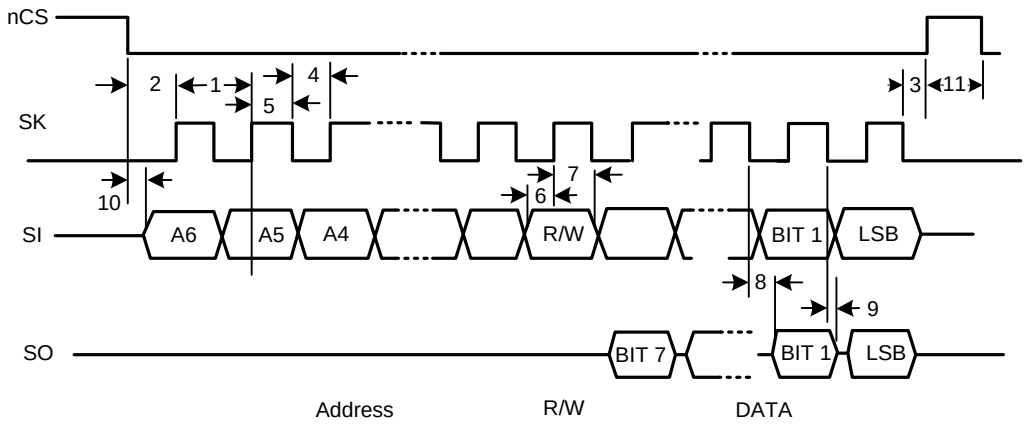


Figure 4: 4-wire control bus timing diagram

Note 1 The above timing is valid for active low and high CS

Table 11: 4-wire control bus electrical characteristics

Parameter	Symbol	Label in plot	Min	Typ	Max	Unit
Cycle Time	t_C	1	70			ns
Enable lead time	t_{CSS}	2, from CS active to first SK edge	20			ns
Enable lag time	t_{SCS}	3, from last SK edge to CS idle	20			ns
Clock low time	t_{CL}	4	0.4 x t_C			ns
Clock high time	t_{CH}	5	0.4 x t_C			ns
Data In setup time	t_{SIS}	6	5			ns
Data In hold time	t_{SIH}	7	5			ns
Data Out valid time	t_{SOV}	8			22	ns
Data Out hold time	t_{SOH}	9	6			ns
Data access time	t_H	10			22	ns
CS inactive Time	t_{WCS}	11	20			ns

10.7 Oscillator

Table 12: Oscillator electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Internal oscillator frequency		before trimming	1.4	2.0	2.6	MHz
		after trimming	1.9	2.0	2.1	

10.8 Reference voltage generation and temperature supervision

Table 13: Reference voltage generation and temperature supervision electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Reference Voltage	VREF pin		-1 %	1.2	+1 %	V
VREF decoupling capacitor				100		nF
Reference Current resistor	IREF pin		-1 %	200	+1 %	kΩ
Thermal Shutdown	T_{OVER}		125	140	155	ºC
Charge current reduction	$T_{CHARGELOW}$		75	90	115	ºC
Charge suspend	$T_{CHARGESUSPEND}$		105	120	135	ºC
Hysteresis				10		ºC

10.9 LDO voltage regulators

10.9.1 LDO1

Table 14: LDO1 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.0		VDDOUT + 0.3 V, 5 V Max	V
		(If supplied from buck)	(1.5)			
Output voltage	VLDO1	$I_{OUT} = I_{MAX}$	0.6	Note 1	1.8	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3	Note 2	+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO1)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	40	Note 3		mA
Short circuit current	I_{SHORT}			80		mA
Dropout voltage	$V_{DROPOUT}$	VDD > 2.15 V $I_{OUT} = I_{MAX}$		200	350	mV
		(VDD = 2.0 V, I_{OUT} = 0.4 x I_{MAX} or VDD = 1.5 V, I_{OUT} = 0.25 x I_{MAX})		100	150	
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	50	60		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 4		8 µA + 1.25 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			300	µs

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO1_PD_DIS		100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Sourced from LDOCORE band gap.

Note 3 Max. current is 10 mA if supplied from VDDREF.

Note 4 Internal regulator current flowing to ground.

10.9.2 LDO2

Table 15: LDO2 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO2	$I_{OUT} = I_{MAX}$	0.6	Note 1	1.8	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO2)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.6 % of I_{OUT}		µA
Quiescent current	IQ_{OFF}				1	µA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
in OFF mode						
Turn on time	t_{ON}	10 % to 90 %			500	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO2_PD_DIS		100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.3 LDO3

Table 16: LDO3 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.9)			
Output voltage	VLDO3	$I_{OUT} = I_{MAX}$	1.725	Note 1	3.3	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO3)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}		200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.9 V, $I_{OUT} = I_{MAX}$ *2/3)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ tr = tf = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} tr = tf = 1 µs		20	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.3 % of I_{OUT}		µA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			300	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.4 LDO4

Table 17: LDO4 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.9)			
Output voltage	VLDO4	$I_{OUT} = I_{MAX}$	1.725	Note 1	3.3	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO4)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}		150			mA
Short circuit current	I_{SHORT}			300		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.9 V, $I_{OUT} = I_{MAX} * 2/3$)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.5 % of I_{OUT}		µA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			300	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.5 LDO5

Table 18: LDO5 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO5	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO5)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	200	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.7 % of		µA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
				I_{OUT}		
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			200	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO5_PD_DIS		100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.6 LDO6

Table 19: LDO6 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO6	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO6)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	150			mA
Short circuit current	I_{SHORT}			300		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V, $I_{OUT} = I_{MAX}/3$		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.5 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			200	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.7 LDO7

Table 20: LDO7 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO7	I_{OUT} = I_{MAX}	1.2	Note 1	3.6	V
Output accuracy		I_{OUT} = I_{MAX}	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO7)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = I_{MAX} (for VDD = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V I_{OUT} = I_{MAX}		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V I_{OUT} = I_{MAX} t_r = t_f = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX}		20	50	mV

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
		$t_r = t_f$ = 1 µs				
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	IQ_{ON}	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{OFF}	Note 2		8 µA + 0.4 % of I_{OUT}		µA
Quiescent current in OFF mode	t_{ON}				1	µA
Turn on time	t_{OFF}	10 % to 90 %			600	µs
Turn off time	ROFF	90 % to 10 %			10	ms
Pull down resistance in OFF mode				100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.8 LDO8

Table 21: LDO8 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO8	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO8)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		20	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 11 MHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.4 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			200	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.9 LDO9

Table 22: LDO9 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO9	$I_{OUT} = I_{MAX}$	1.25	Note 1	3.65	V
Output accuracy		$I_{OUT} = I_{MAX}$	-1		+1	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO9)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA + 0.7 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			200	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.10 LDO10

Table 23: LDO10 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8		VDDOUT + 0.3 V, 5 V Max	V
		(if supplied from buck)	(1.5)			
Output voltage	VLDO10	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO10)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	250			mA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Short circuit current	I_{SHORT}			500		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD < 1.8 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	VDD = 3.0 to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	VDD = 3.0 to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	VDD = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		30	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz VDD = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz VDD = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.3 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	t_{ON}	10 % to 90 %			300	µs
Turn off time	t_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by VDD - dropout voltage.

Note 2 Internal regulator current flowing to ground.

10.9.11 LDOCORE

Table 24: LDOCORE electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Output voltage	VDDCORE	I_{OUT} = 0 mA to I_{MAX}	2.45	2.5	2.55	
		When supplied from BBAT	2.15	2.2	2.25	V
Decoupling capacitor	C_{IN}	On VDDREF	-35 %	220	+35 %	nF
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ 2.5 V)	-55 %	100	+35 %	nF
ESR resistance		f > 1 MHz			0.1	Ω
Dropout voltage	$V_{DROPOUT}$	I_{OUT} < 10 µA , follower mode		0.05	0.1	V
Max output current	I_{MAX}		4			mA
Maximum quiescent current	IQ	POWER-DOWN mode: I_{OUT} < 20 µA		13	17	µA

10.10 DC/DC buck converters

10.10.1 BUCKCORE

Table 25: BUCKCORE electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps and track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBCORE	$I_{OUT} = I_{MAX}$	0.725	Note 2	2.075	V
Output voltage accuracy		Incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		$I_{OUT} = I_{MAX}$		5		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA to 500 mA, dI/dt = 50 mA/µs		15	35	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 500 mA $t_r = t_f$ = 10 µs		3	8	mV
Output current	I_{MAX}	During DVC transitions	700			mA
		Between DVC transitions	800 Note 4			
Current limit (programmable)	I_{LIM} Note 5	BUCKCORE_ILIM=00	-20 %	700	20 %	mA
		BUCKCORE_ILIM=01	-20 %	800	20 %	mA
		BUCKCORE_ILIM=10	-20 %	1000	20 %	mA
		BUCKCORE_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	F			2		MHz
Switching duty cycle			10		95	%
Turn on time	t_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via CORE_PD_DIS			200	Ω
Efficiency	η	I_{OUT} = 30 mA to I_{MAX} VDD < 4.2 V		85		%

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
On resistance pMOS	R_{pMOS}	Incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	Incl. pin and routing			0.3	Ω
PFM mode						
Output voltage	VBCORE	I_{OUT} < 70 mA	0.5	Note 6	2.075	V
Typical mode switching current				40		mA
Output current	I_{MAX}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		25	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 to 70 mA		80		%
Mode transition time				16	18	µs

Note 1 Must be in the range of VDDOUT +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/us while slewing.

Note 3 Minimum tolerance is +/-30 mV.

Note 4 VDD > 3.0 V, using Coilcraft LPS3015-222ML.

Note 5 The current limits will be automatically doubled when BUCKCORE is merged with BUCKPRO.

Note 6 Max. VDD – 1.0 V.

10.10.2 BUCKPRO

Table 26: BUCKPRO electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBPRO	I_{OUT} = I_{MAX}	0.725	Note 2	2.075	V
Output voltage accuracy		Incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		5		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA to 500 mA dI/dt = 50 mA/µs		15	35	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 to 3.6 V I_{OUT} = 500 mA t_r = t_f = 10 µs		3	8	mV
Output current	I_{MAX}	During DVC transitions	700			mA

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
		Between DVC transitions	800 Note 4			
Current limit (programmable)	I_{LIM}	BUCKPRO_ILIM=00	-20 %	700	20 %	mA
		BUCKPRO_ILIM=01	-20 %	800	20 %	mA
		BUCKPRO_ILIM=10	-20 %	1000	20 %	mA
		BUCKPRO_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	F			2		MHz
Switching duty cycle			10		90	%
Turn on time	t_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via PRO_PD_DIS			200	Ω
Efficiency	η	I_{OUT} = 30 mA to I_{MAX} VDD < 4.2 V		85		%
On resistance pMOS	R_{pMOS}	Incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	Incl. pin and routing			0.3	Ω
PFM mode						
Output voltage	VBPRO	I_{OUT} < 70 mA	0.5	Note 5	2.075	V
Typical mode switching current				40		mA
Output current	I_{MAX}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		20	35	µA
Frequency of operation			0		5	MHz
Efficiency	H	I_{OUT} = 10 to 70 mA		80		%
Mode transition time				16	18	µs

Note 1 Must be in the range of VDDOUT +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing.

Note 3 Minimum tolerance is +/-30 mV.

Note 4 VDD > 3.0 V, using Coilcraft LPS3015-222ML.

Note 5 Max. VDD – 1.0 V.

10.10.3 BUCKMEM

Table 27: BUCKMEM electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	10	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBMEM	$I_{OUT} = I_{MAX}$	0.95	Note 2	2.525	V
Output voltage accuracy		Incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		$I_{OUT} = I_{MAX}$		10		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA to 300 mA dI/dt = 30 mA/µs		20	40	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 to 3.6 V I_{OUT} = 300 mA tr=tf=10 µs		5	10	mV
Output current	I_{MAX}	During DVC transitions	650			mA
		Between DVC transitions, VBMEM < 2.075 V	750 Note 4			
Current limit (programmable)	I_{LIM}	BUCKMEM_ILIM=00	-20 %	700	20 %	mA
		BUCKMEM_ILIM=01	-20 %	800	20 %	mA
		BUCKMEM_ILIM=10	-20 %	1000	20 %	mA
		BUCKMEM_ILIM=11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.2		mA
Switching frequency	f			2		MHz
Switching duty cycle			10		90	%
Turn on time	t_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via MEM_PD_DIS			250	Ω
Efficiency	η	I_{OUT} =30 mA to I_{MAX} VDD < 4.2 V		85		%
On resistance pMOS	R_{pMOS}	Incl. pin and routing			0.5	Ω
On resistance nMOS	R_{nMOS}	Incl. pin and routing			0.3	Ω

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
PFM mode						
Typical mode switching current				40		mA
Output current	I_{MAX}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		20	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 to 70 mA	80			%
Mode transition time				16	18	µs
VMEM_SW switch RON		VBMEM = 1.8 V V_{DROP} = 200 mV			0.5	Ω
VMEM_SW switch Turn on time		VBMEM = 1.8 V C_{LOAD} = 10 µF max		200	400	µs
VMEM_SW switch $R_{pull-down}$		VBMEM = 1.8 V V_{OUT} = 100 mV		200		Ω

Note 1 Must be in the range of VDDOUT +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing.

Note 3 Minimum tolerance is +/-35 mV.

Note 4 VDD > 3.0 V, using Coilcraft LPS3015-222ML.

10.10.4 BUCKPERI

Table 28: BUCKPERI electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VDD		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	10	+30 %	µF
Output capacitor ESR		f > 100 kHz all cap's + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}			100	150	mΩ
Output voltage	VBPERI	I_{OUT} = I_{MAX}	1.8	Note 2	3.6	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		10		mV
Load regulation transient	VTR_{LOAD}	VDD = 3.6 V, VBPERI < 3.0 V I_{OUT} = 0 mA to 500 mA, dI/dt = 50 mA/µs		20	40	mV
	VTR_{LOAD}	VDD = 3.6 V, VBPERI = 3.3 V		40	80	mV

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
		I_{OUT} = 0 mA to 500 mA, dI/dt = 50 mA/µs				
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 300 mA tr = tf = 10 µs		10	20	mV
Output current	I_{MAX}	During DVC transitions	650			mA
		Between DVC transitions, VBMEM < 2.1 V	750 Note 4			
Current limit (programmable)	I_{LIM}	BUCKPERI_ILIM = 00	-20 %	700	20 %	mA
		BUCKPERI_ILIM = 01	-20 %	800	20 %	mA
		BUCKPERI_ILIM = 10	-20 %	1000	20 %	mA
		BUCKPERI_ILIM = 11	-20 %	1200	20 %	mA
Quiescent current in OFF mode	IQ_{FF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			3		mA
Switching frequency	f			2		MHz
Switching duty cycle			20		100	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V			200	Ω
Efficiency	η	I_{OUT} < I_{MAX} VDD <4.2 V		80	85	%
Efficiency (half pass device Note 5)	$η_2$	I_{OUT} = 50 mA to 300 mA VDD < 4.2 V		90	95	%
On resistance pMOS	R_{pMOS}	incl. pin and routing			0.25	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
Bypass resistance	R_{Bypass}	at VDDPERI = 3.6 V			1.0	Ω
PFM mode						
Typical mode switching current				40		mA
Output current	I_{MAX}		70			mA
Current limit	I_{LIM}		-20 %	150	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		25	35	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 70 mA		80		%
Mode transition time				16	18	µs
VPERI_SW switch RON		VBPERI = 1.8 V Vdrop = 200 mV			0.5	Ω
VPERI_SW switch		VBPERI = 1.8 V		200	400	µs

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Turn on time		C_{LOAD}=10 µF max				
VPERI_SW switch Rpull-down		VBPERI=1.8 V V_{OUT}=100 mV		200		Ω

Note 1 Must be in the range of VDDOUT +/- 0.3 V.

Note 2 Programmable in 100/50 mV increments, maximum output voltage is less than VDD.

Note 3 Minimum tolerance is +/-35 mV.

Note 4 VDD > 3.0 V, using Coilcraft LPS3015-222ML.

Note 5 See control BPERI_HS.

10.11 Battery charger

10.11.1 Charger supply modes

Table 29: Charger supply modes

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
VBUS	VUSB		4.4		5.5	V
USB2.0 host/hub mode (default)	ISET_USB		70	Note 1	1300	mA
DCIN (Wall Brick, 1000 mA)	VDCIN		4.8		5.5	V
	ISET_DCIN		70	Note 1	1300	mA

Note 1 Programmable in 10 mA increments from 70 mA to 120 mA and 100 mA increments from 400 mA to 1300 mA.

10.11.2 Charger buck

Table 30: Charger buck electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	VCENTER		4.4		5.6	V
Output capacitor	C_{OUT}		30			µF
ESR of output capacitor		F > 100 kHz			20	mΩ
Inductor value	L_{BUCK}		-30 %	4.7	+30 %	µH
Inductor resistance	R_{ESR}	F = 1 MHz		100	150	mΩ
Output voltage	VDDOUT	I_{OUT}= 1000 mA	3.6	VBAT + 200 mV		V
Ripple voltage		I_{OUT} = 1000 mA		10		mV
Line regulation transient	VTR_{LINE}	VBUS_PROT=4.4 V to 5.5 V, I_{OUT}=1000 mA tr = tf = 10 µs		10		mV
Output current	I_{MAX}		1300			mA
Current limitation	I_{LIM}	2-wire programmable (different step sizes for different ranges)	70		1300	mA
Quiescent current in OFF mode					1	µA
Quiescent current in synchronous rectification mode				5		mA
F_BUCK Frequency of operation				2		MHz
Switching duty cycle			10		100	%
Ton Turn on time					2.2	ms

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Efficiency		I_{OUT} = 1000 mA VBUS_PROT = 5 V	85	90		%
R_PMOS PMOS on resistance		including pin and routing	0.08	0.15	0.2	Ω
R_NMOS NMOS on resistance		including pin and routing	0.15	0.25	0.3	Ω
R_VBUS_PROT internal switch on resistance		including pin and routing, VBUS_PROT= 4.8 V	0.05	0.1	0.15	Ω
Sleep mode – PFM mode						
Sleep mode output current	$I_{OUTSLEEP}$		100			mA
Current limitation			300	tbd	550	mA
IQ_ SLEEP – No load supply current in SLEEP mode		I_{OUT} = 0 mA (due to high precision current limit)		80	100	µA
F_BUCK Frequency of operation			0		3	MHz
Efficiency		I_{OUT} = 10 mA to 100 mA	85			%
Efficiency		I_{OUT} = 1 mA to 50 mA VDD =4.8 V	75			%
Mode transition time				16	18	µsec

10.11.3 Voltage levels on VBAT

Table 31: Voltage levels on VBAT

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
BAT_FAULT				2.9		V
ICHG_BAT (ICHG_PRE over-ride)		VBAT < BAT_FAULT	20	40	60	mA

10.11.4 Charging modes

Table 32: Charging modes

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
CC mode output current		6-bits ICHG_BAT (20 mA steps)	0	200	1260	mA
CC absolute accuracy		ICHG_BAT <100 mA	-10		+10	mA
CC absolute accuracy		ICHG_BAT >100 mA	-10		+10	%
CV mode output voltage		VCHG_BAT (25 mV steps)	3.65	4.2	4.425	V
CV output voltage accuracy		VCHG_BAT	-25		+25	mV

10.11.5 Charger detection circuit

Table 33: Charger detection circuit electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Charger detect threshold	VCH_DET		4.25	4.35	4.4	V
Charger current limit reduction threshold		VCHG_THR (configurable)	3.7	3.8	4.35	V
Charger insertion debounce time	VCHG_INS_DEB			10		ms
VBUS, DCIN excess voltage threshold	VCHG_EXCESS		5.5	5.6	5.8	V

10.11.6 VBUS charge control

Table 34: VBUS charge control electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Data Source Voltage	V_{DAT_SRC}	@IDAT_SRC	0.5		0.7	V
Data Source Current	I_{DAT_SRC}		0		200	µA
Data Detect Voltage	V_{DAT_REF}	@IDAT_SINK	0.25		0.4	V
Data Sink Current	I_{DAT_SINK}		50		150	µA
D+ source on time	$T_{DP\_SRC\_ON}$		100			ms
D+ source off to high current	T_{DPSRC_HICRNT}		40			ms
VBUS load in low power Suspend mode	$I_{VBUS\_SUSPEND}$	0 V ≤ VBUS ≤ 5.25 V T_{AVG} = <1 s, no spikes higher than 100 mA			500	µA

10.11.7 Charge timer

Table 35: Charge timer

Parameter	Register	Test conditions	Min	Step	Max	Step
Total Charging Timer setting	TCTR	30 min total charge time is defined as the total charge time from when the charger was enabled (both for LINEAR and PRE-CHARGE mode charging). If the timer expires, the CHG_TO flag is set in the EVENT register, an IRQ is issued and the charging is disabled. The default TCTR setting is 0x0A. Setting the TCTR to 0x00 disables the timer.	0	30	450	min
Read back of current timer value	CHG_TIME	This register can be used to read back the current value of the charge time counter, counting down from the value loaded by the TCTR	0	2	510	Min

10.11.8 DCCC and active diode

Table 36: DCCC and active diode electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Active diode R_{on}		VBAT=3.6 V I=500 mA Including pin and routing		0.14		Ω
Circuit activation voltage		VBAT - VDDOUT	10	20	40	mV
Maximum diode current	ID_{max}			2.2		A

10.11.9 Backup battery charger

Table 37: Backup Battery Charger electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Backup battery charging current	BCHARGER_ISET	VIN = 3.6 V, VDDBBAT = 2.5 V	100	Note 1	6000	µA
Charger termination voltage	BCHARGER_VSET	VIN = 3.6 V	1.1	Note 2	3.1	V
Backup battery short circuit current		VDDBBAT = 0 V		9		mA
Stabilization capacitor	C_{OUT}		-55 %	470	+35 %	nF
ESR of capacitor		F > 1 MHz			0.1	Ω
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = 5 mA		150	200	mV
Quiescent current	IQ	I_{OUT} > 50 µA		5.25+ 1.75 % of I_{OUT}		µA
		I_{OUT} < 50 µA		5.25+ 1.5 % of I_{OUT}		µA

Note 1 Programmable in 100 µA increments from 100 µA to 1000 µA and 1 mA increments from 1 mA to 6 mA.

Note 2 Programmable.

10.12 Boost converter

Table 38 shows parameters using external components shown.

Table 38: Boost converter electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Output Voltage	VBOOST	2.8 V < V_{IN} < 4.5 V 0.03 mA < I_{LOAD} <50 mA	4.6		25	V
Efficiency		1 MHz, VBOOST = 20 V I_{LOAD} = 50 mA;		80		%
Output Voltage Ripple		I_{LOAD} = 26 mA C_{OUT} = 2 µF (@max V_{OUT})		200		mV_{p-p}
Operating Quiescent Current		I_{LOAD} = 0 mA; automatically changed to discontinuous mode		250	350	µA
Shutdown Quiescent Current		Leakage of ext. transistor and feedback resistors excluded			1	µA
Switching Frequency		Programmable 1 MHz or 2 MHz	-10 %	1/2	+10 %	MHz
Programmable output current (Reg. 0x24/0x25)		LEDx_IN	0.05		26	mA
Inductor			-20 %	4.7	+20 %	µH
Inductor Current Limitation		Tolerance without external resistor	-20 %	1100 Note 1	+20 %	mA
Decoupling capacitor	C_{boost}	Ceramic capacitor recommended; figure w/ 25 V voltage bias, may correspond to 10 µF nom. value w/o bias	1	2		µF
ESR C_{boost}		F > 100 kHz		100		mΩ
Current monitoring resistor Rsense		External connection from sense resistor to BOOST_SENSEP input		0.1		Ω
Output voltage overshoot		Max overshoot over shutdown threshold		1	2.5	V
Over-voltage threshold		Voltage at BOOST_PROT pin		1.38		V

Note 1 For reduced backlight power requirements a lower current limitation of 710 mA can be selected via control BOOST_ILIM.

10.13 WLED driver

Table 39: WLED driver electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
absolute output current accuracy (LED1_IN1 / LED2_IN / LED3_IN)		Full scale tolerance	-20		+20	%
		Linearity 1 mA to 26 mA	-10		+10	
		Linearity 0.1 mA to 1 mA	-20		+20	
relative output current accuracy (IOUT1 - IOUT2) / (IOUT1+IOUT2)		I_{out}1/2/3 = 5 mA to 25 mA	-3.25		+3.25	%
		I_{out}1/2/3 = <5 mA	-4.5		+4.5	
Current sink VDSAT		@I_{OUT}=25 mA		0.6		V
LED current sink VDMAX		Max. voltage drop at current source			5.5	V
Ramp step rate		TSTEP-UP		1		ms
IDAC step size		LEDx_CURRENT = 0 to 255		0.212		dB

10.14 ADC

Table 40: ADC electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
ADC reference voltage		VDDCORE/ TSIREF	1.8 Note 1	2.5	2.6 Note 1	V
Off current					1	µA
ADC operating current		During conversion		100		µA
ADC resolution				10		bit
ADC integral non linearity				+/-2		LSB
ADC differential non linearity				+/-0.8		LSB
ADC absolute accuracy			12		15	mV
ADC conversion clock				1.0		MHz
Auto-zero time				5		µs
Conversion time				29		µs
Total ADC conversion Time				34		µs
Internal MUX-resistance	R_{int}			5		kΩ
Maximum source impedance	R_{source} Note 2			100		kΩ
Internal sampling capacitor.		C_{array}		10		pF

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Acquisition time		~7*τ=~7*(R_{int}+R_{source}) *C_{int}	10	12	14	µs
Input capacitance (C_{int})		Total input capacitance		10.5		pF
VDDOUT voltage range Channel 0		VDDOUT minus VDDCORE Gain of 1.25 ADC=[(VDDOUT-2.5 V)*0.5] *1023	2.5		4.5	V
ICH current measurement using an internal current mirror device. Channel 1, used for dynamic safety timer and EOC detection		Equivalent to 3.9 mA/bit	0	Note 3	1000	mA
TBAT voltage range Channel 2		Voltage across a NTC resistor in the battery pack, 50 µA biasing	0		VDDCORE	V
VBAT voltage range Channel 3		VBAT minus VDDCORE Gain of 1.25 ADC=[(VBAT-2.5 V)*0.5] * 1023	2.5		4.5	V
ADCIN4 to 6 voltage range Channel 4 to 6		ADC = [VIN/2.5 V] * 1023	0		2.5	V
VBBAT voltage range Channel 9		Gain of 0.5 ADC=[(VBBAT/2.5 V)*0.5] * 1023	0		5.0	V
ADCIN4 current source Channel 4		If enabled		15		µA
ADCIN5 comparator threshold Channel 5		Disabled during ADCIN5 conversion		1.2		V
R_{ON}, TSI X-Y switches				5		Ω
MUX cross talk isolation				60		dB

Note 1 TSIREF voltage range.

Note 2 R_{source} is the impedance of the external source the ADC is sampling.

Note 3 ICH measurement range is internally restricted to around 100 mA (~2.5 V across 50 kΩ sense resistor) to protect the ADC from overvoltage.

11 Accessory identity detection

This block detects the status of the accessory identity detection (ACC_ID_DET) pin. It is capable of detecting three different states:

- Floating (USB peripheral device connected)
- Shorted to ground (USB host device connected)
- Connected to ground via resistor (accessory asserted)

The sensing can be turned on or off, ID_FLOAT and ID_GND asserts an interrupt at both (rising and falling) edges. The sensing can be debounced. If a mini-USB or an accessory is connected to the ACC_ID_DET pin in POWER-DOWN mode a wakeup event will be initiated (only at falling edge of ID_FLOAT).

If the accessory coding requires the detection of an impedance of less than 40 kΩ an external resistor has to be placed between VDDCORE and ACC_ID_DET.

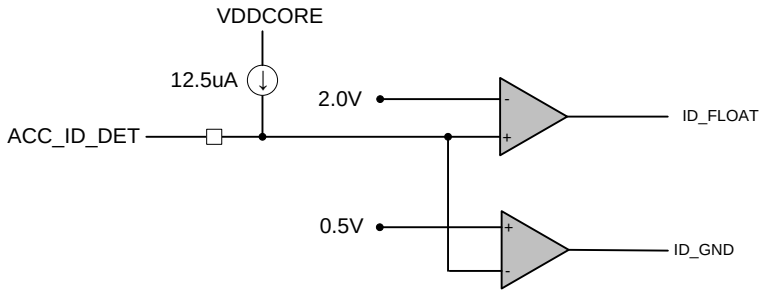


Figure 5: ID detection circuitry

Table 41: Accessory detection states

External resistance to GND	ACC_ID_DET state	ID_Float	ID_GND
R > 160 kΩ	Floating open pin. USB B-Device connected (peripheral)	High	Low
40 kΩ < R < 160 kΩ	High via resistor to ground. Accessory connected	Low	Low
R < 40 kΩ	Low < 10 Ω to ground. USB A-Device connected (host)	Low	High

12 Real time clock and 32 kHz oscillator

The real time clock (RTC) block keeps track of the RTC counter and alarm function. The RTC block will operate from the LDO_CORE power supply.

12.1 32 kHz oscillator

The clock oscillator cell is used to drive the RTC counter. It works with an external piezoelectric oscillator crystal at 32.768 kHz.

In order to achieve typically the desired crystal frequency an external capacitor (10 pF to 20 pF, depending on the parasitic capacitance of the board) is connected to ground from each of the crystal pins. The start-up time of the oscillator is typically 0.5 s over the voltage range. When the crystal is not mounted the XTAL pins should be grounded. The 32 kHz clock signal is made available at the OUT_32K pin and the buffer can be disabled from the sequencer during POWER-DOWN mode.

The timekeeping error from the frequency variance of crystal oscillators (typ. +/-20 ppm) can be trimmed individually by +/- 242 ppm with a resolution of 1.9 ppm (1/(32768 * 16)). The timekeeping correction will be applied only towards the on-chip RTC block. To avoid potential clock jitter issues the 32 kHz clock signal at the OUT_32K pin provides the original frequency of the crystal.

NOTE
The oscillator inputs will be able to withstand a leakage current, corresponding to at least a 10 MΩ connected between the pin and any signal level between VDDOUT and GND.

12.2 RTC counter and alarm

The RTC counter counts the number of 32 kHz clock periods, providing a seconds, minutes, hours, day, month, and year output. Year 0 corresponds to 2000 and it can count up to 63 years. The value of the RTC calendar is read-/write-able via the power manager communication. The calendar is reset to zero when VDDCORE is lost.

There is an alarm register containing minutes, hours, day, month, and year. When the RTC counter register value corresponds to the value set in the alarm an IRQ event will be triggered and a wakeup if DA9052 is in POWER-DOWN mode. The trigger will also set a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_TYPE, is either asserted every second or minute. In the case the host has enabled both alarms it can determine from the status of ALARM_TYPE whether the IRQ/wakeup was caused by the timer or the tick.

The power manager registers ALARM_ON and TICK_ON enable/disable the alarm/tick. The power manager register bit MONITOR will be set to 0 each time the RTC is powered up. Software shall set this bit to ‘1’ when setting the time and date, which will allow software to detect a subsequent loss of the clock.

NOTE
Values written into the RTC calendar and alarm registers have to be valid regarding the allowed value range (see register description, for example maximum 60 for seconds or minutes).

The RTC seconds registers define a 32-bit seconds counter (approximately 136 years), that can only be reset via the nPOR and starts counting seconds after nPOR is released. Using the RTC input clock the output port GPO10 and GPO11 can be toggled with a configurable periodic pulse. In this mode GPO10 or GPO11 offer blinking LED drivers that are able to run in POWER-DOWN mode.

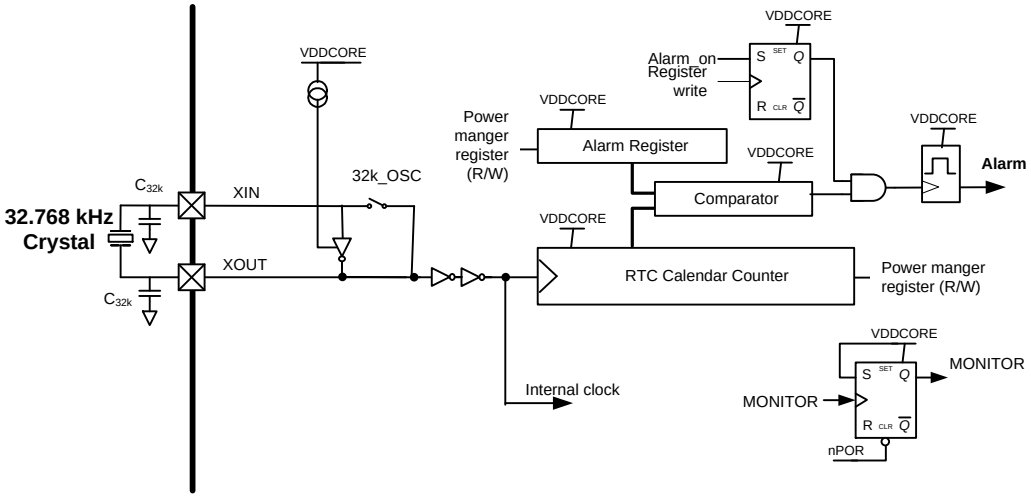


Figure 6: Schematics of the RTC oscillator and counter functionality

12.3 RTC oscillator electrical characteristics

Table 42: Oscillator electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Supply voltage	VDDCORE		2.0	2.5	2.55	V
Oscillator crystal frequency	f_{OSC}			32.768		kHz
Crystal series resistance	R_{OSC}				100	kΩ
Output frequency	f_{OUT}			32.768		kHz
Start-up time for cell over the voltage range	T_{START}			0.5	2.0	s
Current consumption POWER-DOWN mode				1	5	µA
Current consumption ACTIVE mode				3	5	µA
Input duty cycle	D_{XTAL1}	Bypass mode	40	50	60	%
OUT_32K clock jitter		cycle to cycle		20	30	ns

13 ID code/scratch pad

DA9052 offers 10 general purpose registers, which can be configured from OTP cells. The OTP cells can be programmed during test/production with an individual code and so can provide a device specific serial number as required for music and media applications supporting DRM. The general purpose registers are loaded from OTP when DA9052 starts-up from RESET-mode and can be 'read only' protected during fusing. If writing is enabled the registers can be used by the application to store up to 10 bytes of data that a host processor can use for example after powering up from low power modes.

13.1 Programming the ID code/scratch pad

The ID Code/Scratch pad OTP cells can be programmed only once and cannot be erased. Programming can only take place when:

- DA9052 is in Boot Commander mode
- DA9052 has reached the ACTIVE mode operational state.
- There is no charger attached
- The supply voltage for the programming VPP has been provided at the VBUS node
- The range modifiers have been set to select the correct addresses (OTP_GP = 1)
- The write access enable bit GP_WRITE_DIS has been set to program the intended GP register mode (after being programmed once to 'read only' registers R133 to R142 can only be written for fusing). The content received from a read can no longer be modified just by writing in to the registers.
- The lock bit in the OTP is in the correct state (OTP_GP_LOCK = 0)

NOTE
Connecting TP to VDDCORE enables POWER COMMANDER mode.

The data intended to be programmed into the OTP must be first loaded into the related GP_ID registers using the HS 2-wire interface. The contents of the GP_ID registers are then transferred into the OTP cells by setting OTP_TRANSFER = OTP_RP = 1. Once started the transfer cannot be stopped. During an ongoing programming transfer the device will not react to any external events that otherwise would make it transition to other states. Upon completion of a transfer the OTP_TRANSFER bit will be reset automatically. So the end of the transfer can be determined by polling this bit.

If the lock bit OTP_GP_LOCK is set any further programming of the ID code/scratch pad is suppressed. If the write access control bit GP_WRITE_DIS is set, then the GP_ID registers become 'read-only' (reading content will be always a 100 % mirror of the related OTP cells).

In a production environment it is mandatory to check the success of the programming of the GP_ID registers by reading back the OTP contents. DA9052 defaults to performing a margin mode read which allows the reliability of the stored information to be assessed.

To initiate a read transfer from the OTP cells into the related GP_ID registers, firstly set OTP_GP =1 to access the correct addresses, and then OTP_RP=0 and OTP_TRANSFER = 1 to start the read operation. Read transfers are unaffected by the state of the lock or write enable bits.

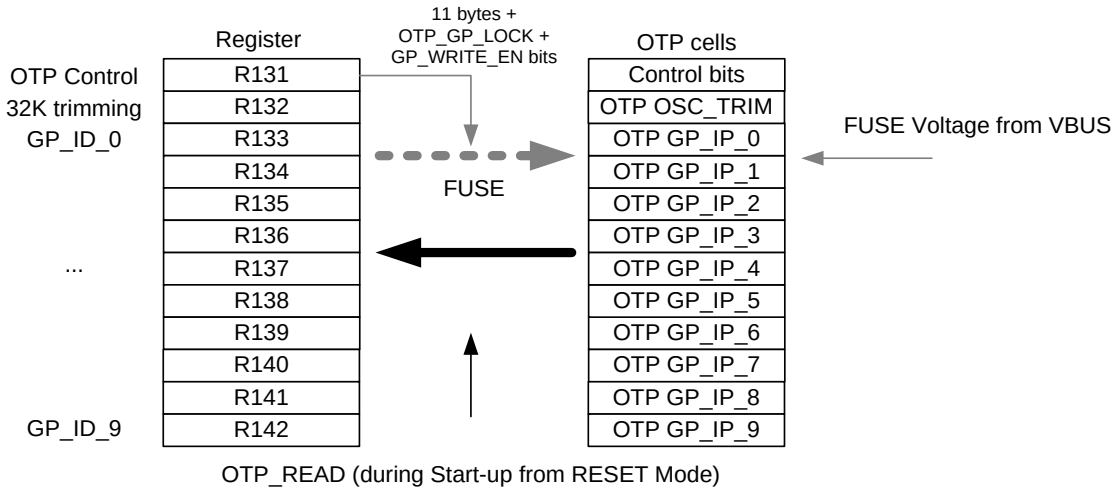


Figure 7: OTP scratch pad block diagram

13.2 GP_ID

Table 43: GP_ID

Supply mode	Symbol	Test conditions	Min	Typ	Max	Unit
Number of bits				88		bits
Programming time GP_ID					5	ms
Voltage limit for OTP fusing		VBUS voltage as the programming voltage	7.0	7.5	7.8	V

14 Typical characteristics

14.1 Buck regulator performance

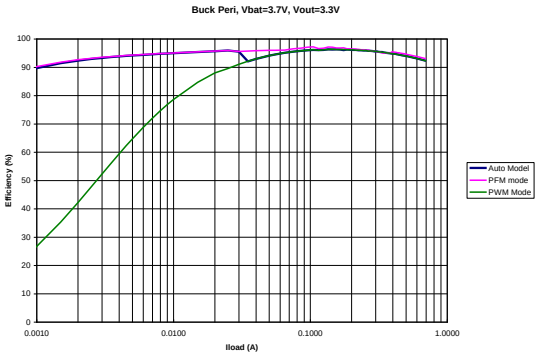


Figure 8: BUCKPERI efficiency curves

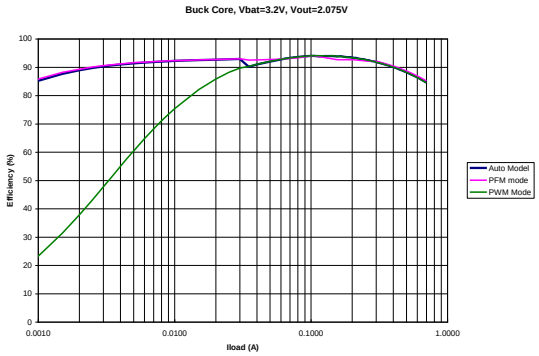


Figure 9: BUCKCORE efficiency curves

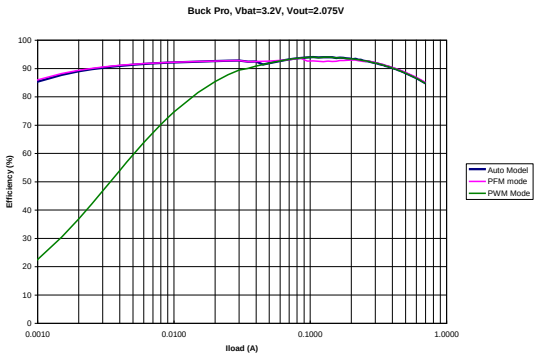


Figure 10: BUCKPRO efficiency curves

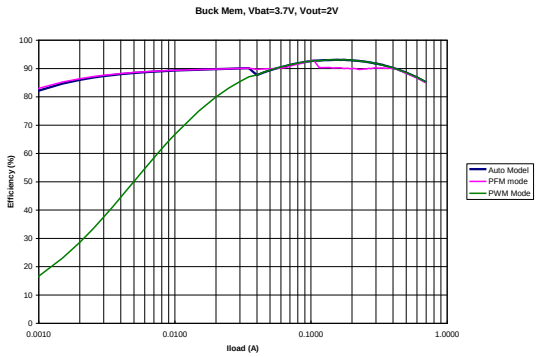


Figure 11: BUCKMEM efficiency curves

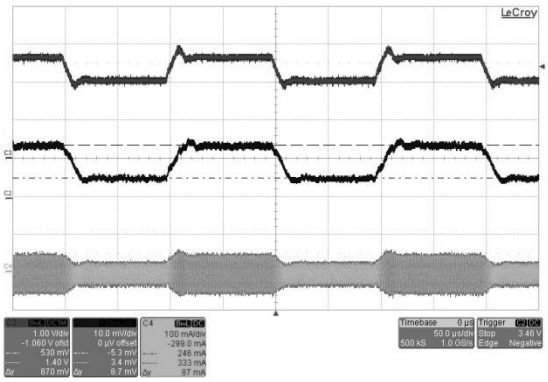


Figure 12: Typical buck line transient

Ch2: V_{BAT}, Ch3: V_{OUT}, Ch4: I_{COIL}
V_{OUT} = 2.5 V, no load, V_{BAT} = 3.0 V to 3.6 V step, t_rise=t_fall = ~10 µs

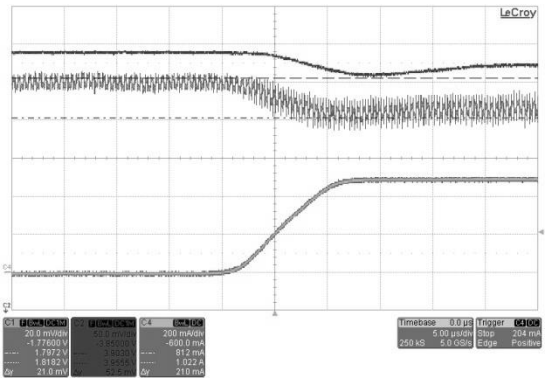


Figure 13: Typical buck load transient

Ch1: I_{COIL}, Ch2: V_{OUT}, Ch4: I_{LOAD}
V_{OUT} = 1.8 V, V_{BAT} = 4 V, I_{LOAD} = 0 mA to 500 mA, dI/dt~50 mA/µs, rising

14.2 Linear regulator performance

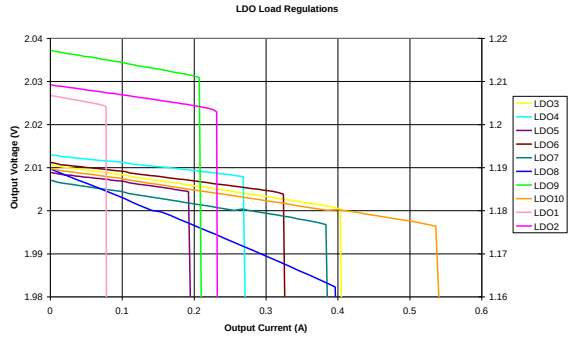


Figure 14: Typical LDO load regulation

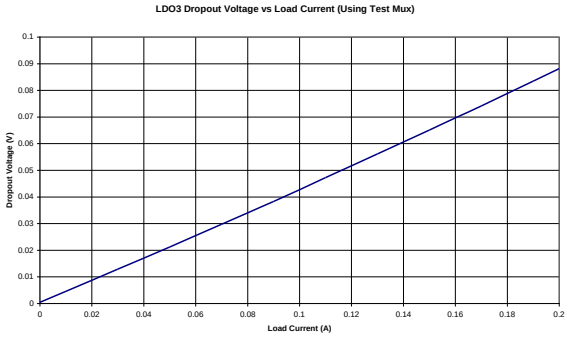


Figure 15: Typical LDO drop-out voltage

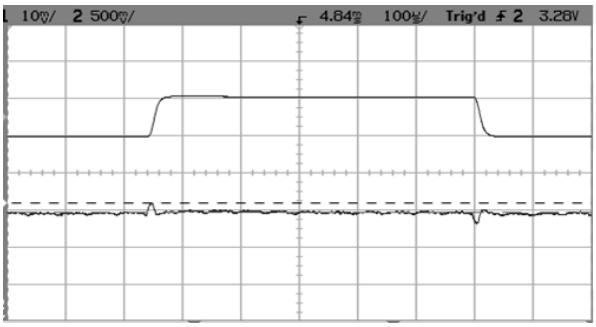


Figure 16: Typical LDO line transient (transient of 3.6 V to 4.2 V at VBAT)

Top trace=VBAT, bottom trace=VLDO1

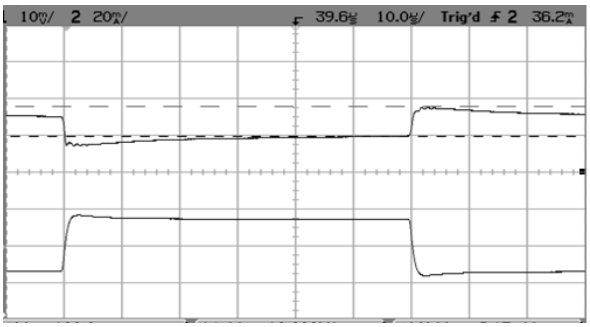


Figure 17: LDO load transient (1 mA to I_{MAX} of 40 mA) VLDO = 1.2 V

Top trace=VLDO1, bottom trace=Load

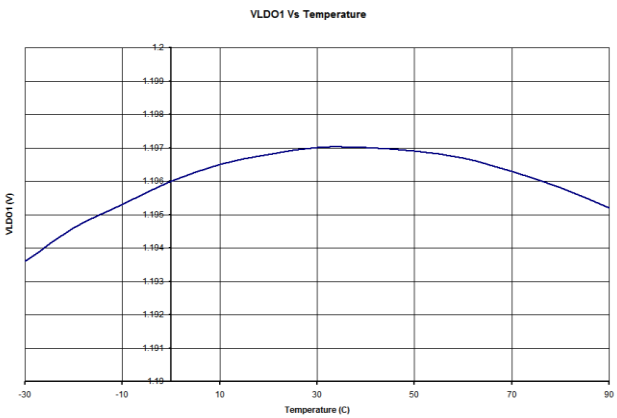


Figure 18: Typical LDO voltage vs temperature

14.3 ADC performance

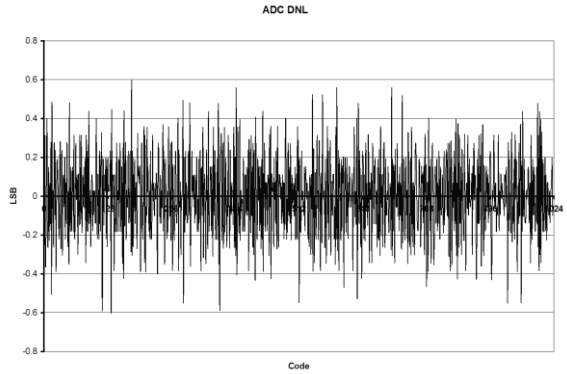


Figure 19: ADC DNL performance

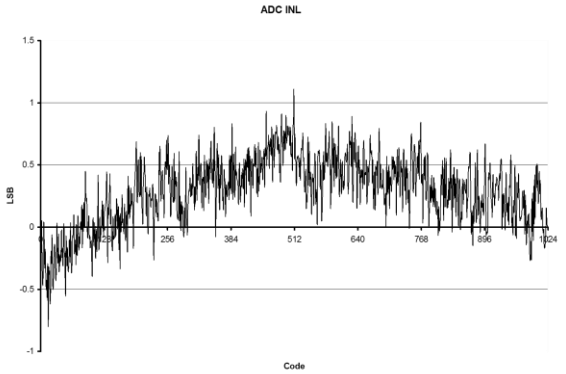


Figure 20: ADC INL performance

14.4 Power path performance

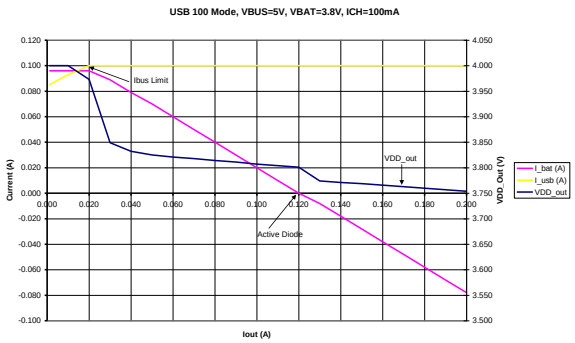


Figure 21: Power path behaviour USB100 mode

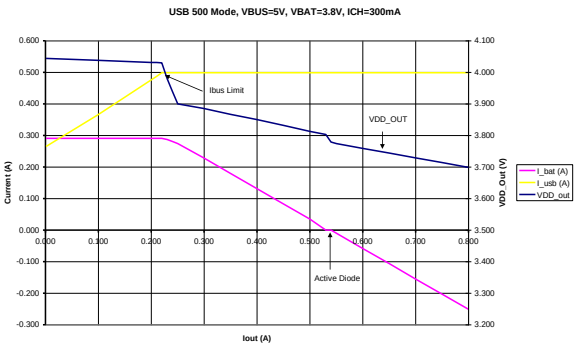


Figure 22: Power path behaviour USB500 mode

Figure 21 and Figure 22 show increasing load current supplied from VBUS, power path loop reduces ICH until active diode turns on which then allows current from battery to supply system load current via VDDOUT.

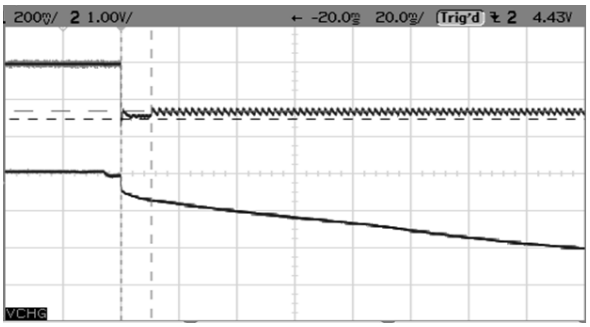


Figure 23: Transitioning supply from VCHG (via DCIN) to VBAT

Top trace = VDDOUT, bottom trace = DCIN

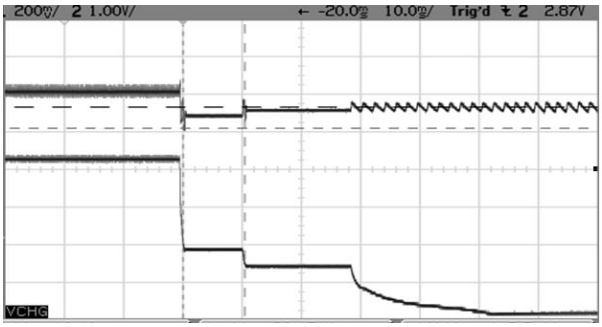


Figure 24: Transitioning supply from USB 5 V (via VBUS) to VBAT

Top trace = VDDOUT, bottom trace = VBUS

14.5 Boost and LED current control performance

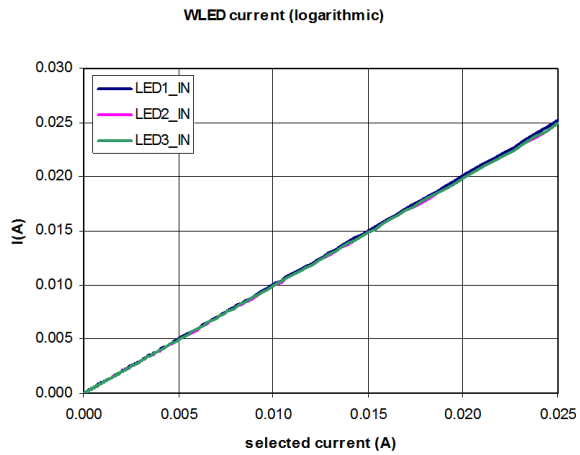


Figure 25: WLED current (logarithmic)

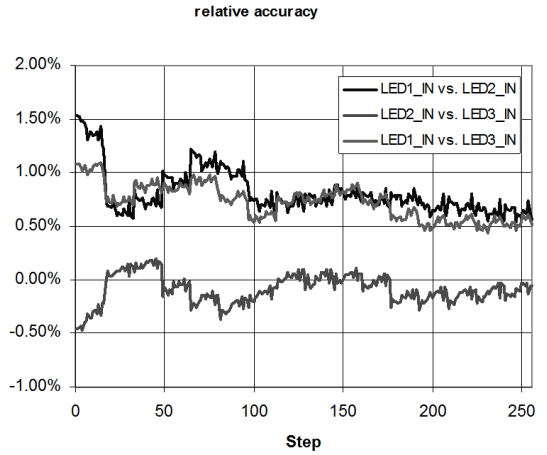


Figure 26: Relative accuracy

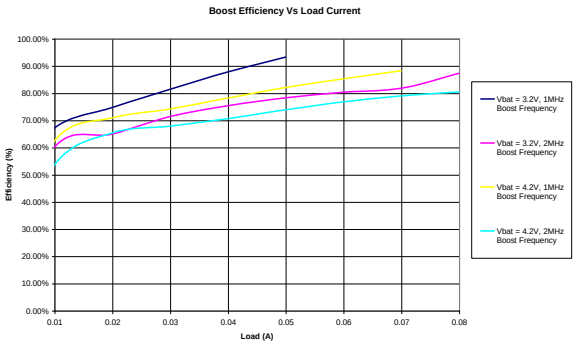


Figure 27: Boost converter efficiency curves

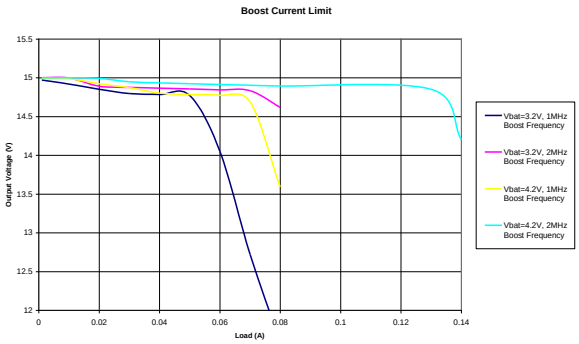


Figure 28: Boost regulation voltages

15 Functional description

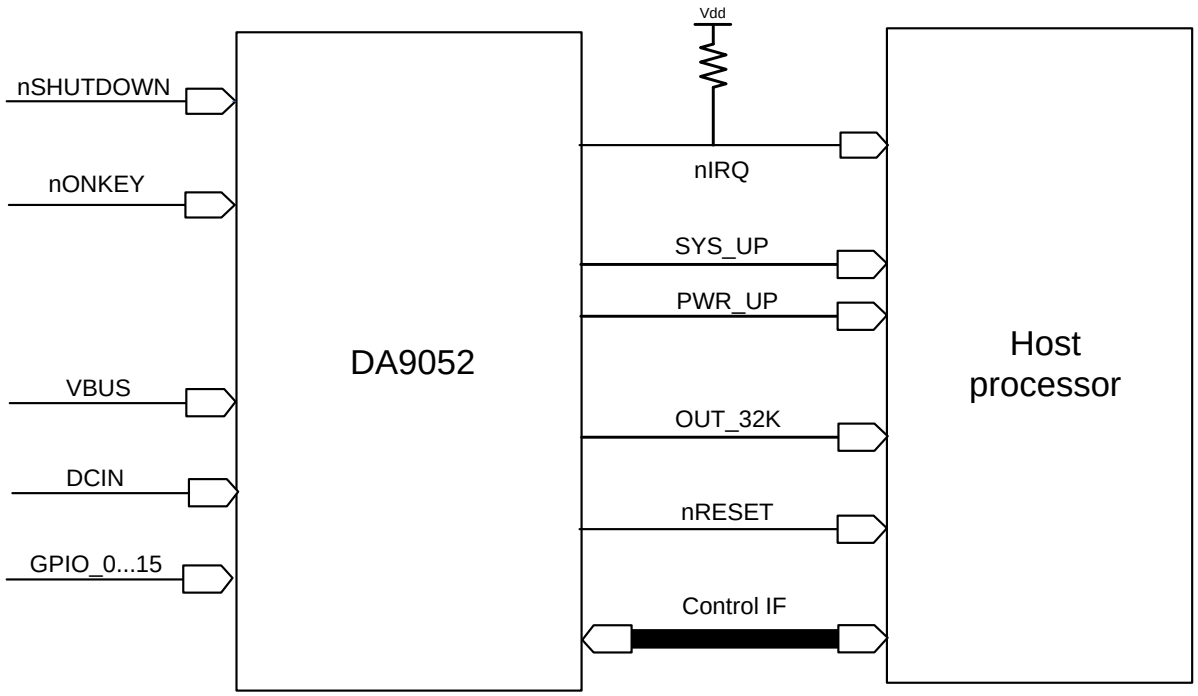


Figure 29: Control ports and interface

15.1 Power manager IO ports

The power manager input ports are supplied either from the internal rail VDDCORE or VDD_IO2, selected via PM_I_V. The output ports are supplied from VDD_IO1 or VDD_IO2, selected via PM_O_V. Apart from nRESET, nIRQ, SYS_UP, PWR_UP/GP_FB2 during the initial start-up sequence the power manager IO ports are in ‘tri-state’ mode until being configured from OTP when leaving RESET mode. Output ports are push-pull type except for nRESET and nIRQ, which can also be configured to open drain.

15.2 On/off and hardware-watchdog port (nONKEY/KEEP_ACT)

The nONKEY signal is an edge triggered high to low wakeup interrupt/event intended to switch-on the DA9052 supplied application. nONKEY is always enabled during POWER-DOWN mode, so that the application can be also switched-on with a disabled GPIO extender. The wakeup event can be disabled via the interrupt mask. This pin can be alternatively asserted to the watchdog unit, so that every assertion of the pin (rising edge sensitive) sets its bit similar to a write via the power manager bus. The host has to release KEEP_ACT in advance to the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 µs.

15.3 Hardware reset (nSHUTDOWN, nONKEY, GPIO14 and GPIO15)

A user-initiated hard reset at the DA9052 nSHUTDOWN is an active low input initiated typically by a push button switch or an asserted error detection line from a host processor. The sequencer then powers down all domains in reverse order down to step 0 and all supplies of DA9052 except LDOCORE are switched off.

DA9052 includes a second hardware reset that follows the nONKEY after being asserted for a period of 5 s +/-30 %. The same can be achieved by a parallel connection of GPI14 and GPI15 to ground for 5 s +-30 %.

If the WATCHDOG has been disabled, this feature provides the ability to emergency turn-off the application in the event of a software lock-up without the need for a dedicated RESET hardware switch or removing the battery.

After a minimum time-out of 500 ms DA9052 will start to power up again. It will wait for a valid wakeup event (for example key press) or will start the power sequencer automatically. By asserting EXT_WAKEUP it can request the host processor to control the subsequent start-up. Alternatively the power up sequence can be performed autonomously by the PMIC following OTP pre-configurations. A detection of a hard reset forces the assertion of nRESET to low when the sequencer returns from POWER-DOWN mode to RESET-mode.

This type of reset is typically used only for severe or unrecoverable hardware or software problems, because it completely resets the processor and can result in data loss.

15.4 Reset output (nRESET)

The nRESET signal is an active-low output signal from DA9052 to the host processor, which tells the host to enter the hardware-reset state. nRESET is always asserted at the beginning of a DA9052 cold start from NO-POWER mode and when the DA9052 returns to RESET mode. nRESET can also be asserted as a soft reset after the sequencer finishes powering down without progressing to RESET-mode.

The reset timer trigger signal can be configured to be EXT_WAKEUP, SYS_UP or PWR_UP. After being asserted nRESET remains low until the reset timer is started from the selected trigger signal and expires. The expiry time can be configured from 1 ms to 1024 ms.

15.5 Accessory and ID detect (ACC_ID_DET)

In ACTIVE and POWER-DOWN mode the detector can track the condition of the USB ID line and differentiates between the following three conditions:

1. Floating (USB peripheral device connected)
2. Shorted to ground (USB host device connected)
3. Connected to ground via resistor (accessory asserted)

If the ACC_ID_DET pin stops floating (falling edge) during POWER-DOWN mode a wakeup event is triggered.

15.6 System enable (SYS_EN)

SYS_EN is an input signal from the host processor to DA9052 (or can be default enabled via OTP settings), which initiates enabling the system power supplies. The control SYS_EN will be initialized from OTP if the related port is configured as GPI or GPO. The register bit SYS_EN can be read and changed via the control interfaces. DA9052 will not accept any power mode transition commands until the sequencer has stopped processing IDs. De-asserting SYS_EN informs the DA9052 that the host processor is going into a standby/hibernate mode. When the port is changing from active to passive state there is no IRQ or wakeup event trigger. With the exception of supplies that are configured in ACTIVE mode with a voltage preset before powering down all regulators and buck converters in power domain POWER1, POWER and SYSTEM will be sequentially disabled in reverse order.

15.7 Power enable (PWR_EN)

PWR_EN is an input signal from the host processor to DA9052 or is configured via OTP or host commands. Initialization, IRQ assertion and register bit PWR_EN control is similar to SYS_EN. To ensure the correct sequencing SYS_EN has to be active before asserting PWR_EN. When de-asserting SYS_EN the sequencer will sequentially power down POWER1, POWER and SYSTEM domains respectively.

15.8 Power1 enable (PWR1_EN)

PWR1_EN is an input signal from a host to DA9052 and is configured via OTP or host commands. Initialization, IRQ assertion and register bit PWR1_EN control is similar to SYS_EN. The domain POWER1 is a sub power domain for general purpose.

15.9 General purpose feedback signal 1 (GP_FB1: EXT_WAKEUP/READY)

The feedback GP_FB1 supports two different modes. If configured as EXT_WAKEUP it is an active high output signal to the host processor that indicates a valid wakeup event during POWER-DOWN mode. External signals that are causing wakeup events are debounced before DA9052 assert the EXT_WAKEUP signal. EXT_WAKEUP is released when entering the ACTIVE mode. If configured as READY signal it indicates ongoing DVC or power sequencer activities. The signal is active low and is asserted from DA9052 as long as the power sequencer processes IDs or DVC voltage transitions are ongoing.

15.10 Power domain status (SYS_UP, PWR_UP/GP_FB2)

The power domain status indicators are active high and assigned after the sequencer has processed all IDs of a power domain (all assigned supplies are up). When domains are disabled during power mode transitions the status indicator is released before the DA9052 sequencer processes the last step of a domain.

PWR_UP is one mode of the general purpose indicator GP_FB2 that can also be used as a configurable feedback signal that is level/time controlled from the power sequencer.

15.11 Supply rail fault (nVDD_FAULT)

nVDD_FAULT is an active low output signal to the host processor to indicate a VDDOUT low status. The assertion of nVDD_FAULT indicates that the main battery and the supply input voltage is low and therefore informs the host processor that the power will shut down very soon. After that the processor may operate for a limited time from the backup battery, which can provide power to the processor for a few cycles. In the event of nVDD_FAULT assertion the processor may be programmed to enter an emergency mode, where for example, external memory data refresh is no longer performed.

15.12 Interrupt request (nIRQ)

The nIRQ is an active low output signal which indicates that an interrupt causing event has occurred and that the event and status information is available in the related registers. States information includes data such as temperature and voltage of the PMIC, fault conditions, charging status, status changes at GPI ports. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ will not be released until the event registers have been cleared.

15.13 Real time clock output (OUT_32K)

The OUT_32K is an output signal that generates a buffered signal of the DA9052 32 kHz oscillator. The 32 kHz oscillator will always run on the DA9052 following the initial start-up from NO-POWER mode until the device has reached NO-POWER mode again. The signal output buffer can be disabled during POWER-DOWN mode with bit OUT_32K_PD.

15.14 IO_Supply voltage (VDD_IO1 and VDD_IO2)

VDD_IO1 and VDD_IO2 are two independent IO supply rail inputs of DA9052 that can be individually assigned to the power manager interface, power manager IOs and GPIOs. The rail assignment determines the IO voltage levels and logical. The selection of the supply rail for GPIOs is also partially used for their alternate functions. GPOs configured in open drain mode have to use the VDD_IO1 rail if an internal pull-up resistor is required.

16 Control interfaces

The DA9052 is completely SW-controlled from the host by registers. DA9052 offers two independent serial control interfaces to access these registers. The communication via the main power manager interface is selectable to be either a 2-wire or a 4-wire connection (I^2C or SPI compliant). The alternate interface is fixed towards a 2-wire bus. Data is shifted in to or out from DA9052 under the control of the host processor that also provides the serial clock.

16.1 Power manager interface (4-wire and 2-wire control bus)

This is the dedicated power control interface from the primary host processor. In 4-wire mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

16.2 4-wire communication

In 4-wire mode the DA9052 register map is split into two pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after reset includes registers R1 to R127. Writing to the page control register changes the active page for all subsequent read/write operations. After modifying the active page it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

The 4-wire interface features a half-duplex operation (data can be transmitted and received with in a single 16-bit frame) at enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.

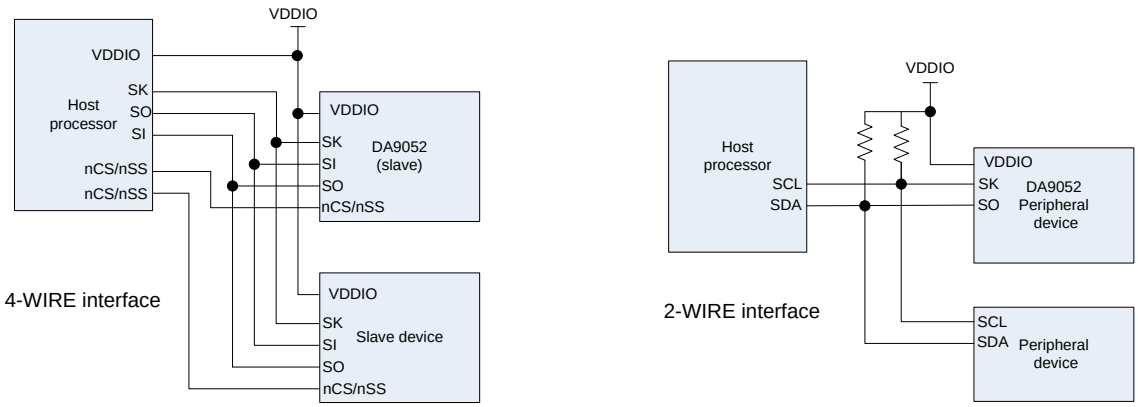


Figure 30: Schematic of 4-wire and 2-wire power manager bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0 to 127, decimal) which will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which specifies the direction of the following data exchange. During register writing the host continues sending out data during the following 8 SK clocks. For reading the host stops transmitting and the 8-bit register is clocked out of DA9052 during the consecutive 8 SK clocks of the frame. Address and data are transmitted with MSB first. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9052 is normally in high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 44: 4-wire clock configurations

CPOL clock polarity	CPHA clock phase	Output data is updated at SK edge	Input data is registered at SK edge
0 (idle low)	0	falling	rising
0 (idle low)	1	rising	falling
1 (idle high)	0	rising	falling
1 (idle high)	1	falling	rising

The DA9052 4-wire interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0 setting DA9052 latches data on the SK rising edge. If the CPHA is set to 1 the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9052 must be set to the same CPOL and CPHA states to communicate with each other.

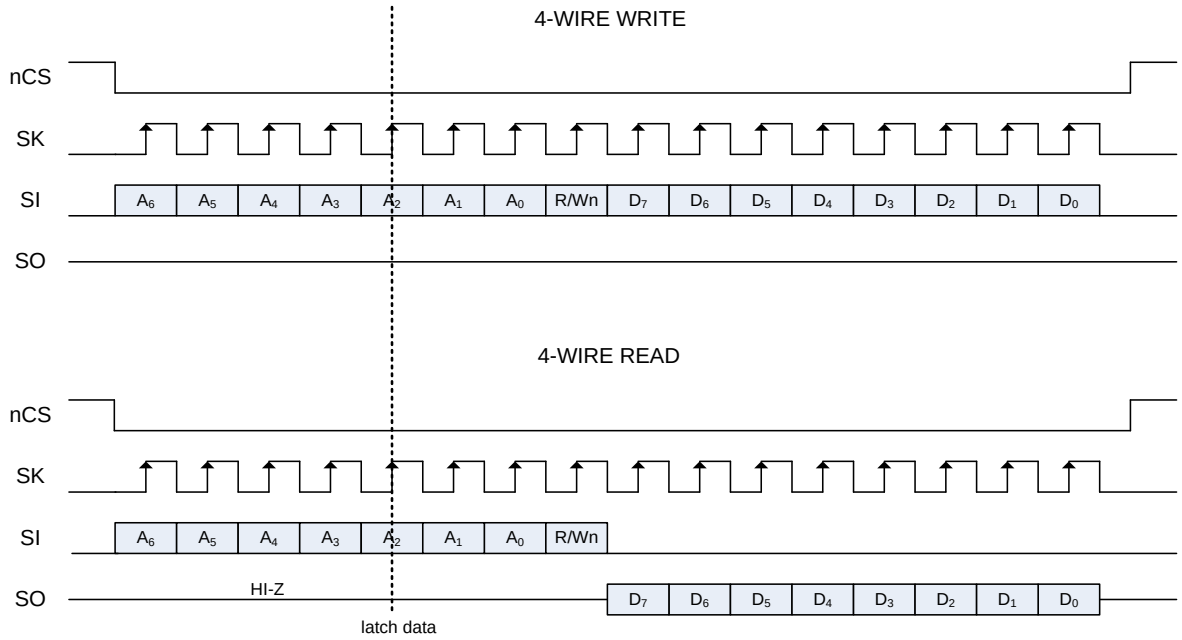


Figure 31: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '0')

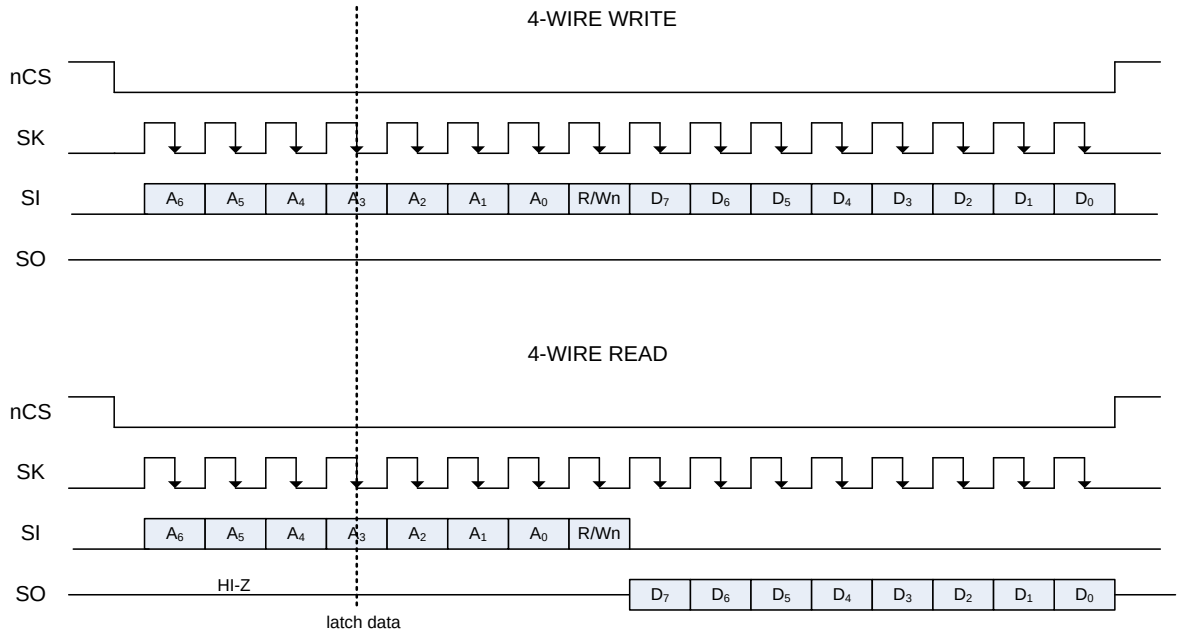


Figure 32: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '1')

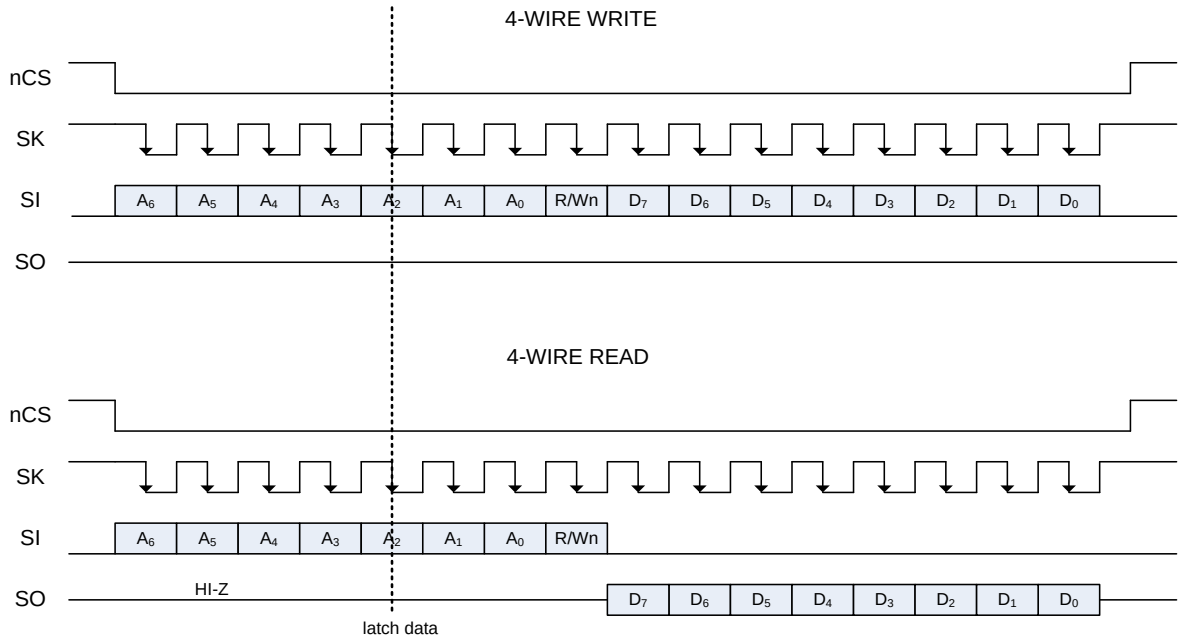


Figure 33: 4-wire host write and read timing (nCS_POL = '0', CPOL = '1', CPHA = '0')

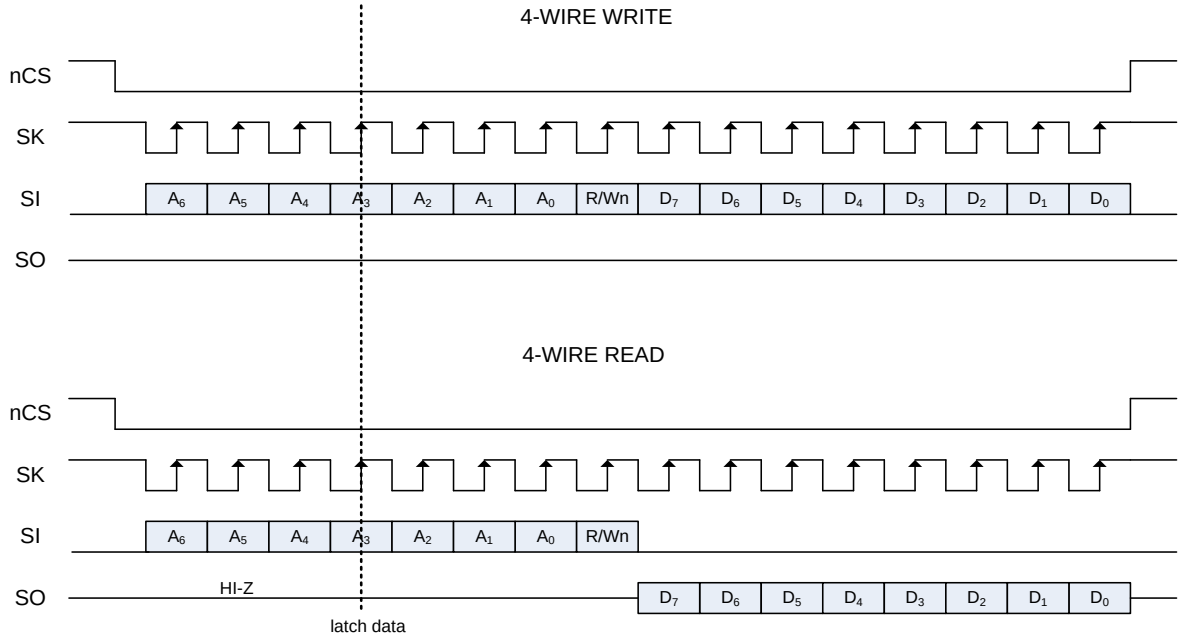


Figure 34: 4-wire host write and read timing (nCS_POL = '0', CPOL = '1', CPHA = '1')

Table 45: 4-wire interface summary

PARAMETER		
Signal Lines	nCS	Chip select
	SI Serial input data	Master out Slave in
	SO Serial output data	Master in Slave out
	SK	Transmission clock
Interface	Push-pull with tristate	
Supply voltage	Selected from VDD_IO1/VDD_IO2	1.6 V to 3.3 V
Data rate	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16-bit cycles	7-bit address, 1-bit read/write, 8-bit data
Configuration	CPOL	clock polarity
	CPHA	clock phase
	nCS_POL	nCS is active low/high

NOTE
Reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example, by writing/reading another register address in between).

16.3 2-wire communication

The power manager interface can be configured for a 2-wire serial data exchange. It has a configurable SLAVE write address (default: 0x90) and a configurable SLAVE read address (default: 0x91).

SK provides the 2-wire clock and SO carries all the power manager bidirectional 2-wire data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict, if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and do not have any relation to the DA9052 internal clock signals. DA9052 will follow the host clock speed with in the described limitations and does not initiate any clock arbitration or slow down.

In high speed mode the maximum frequency of the bus may be increased towards 1.7 MHz. This mode is supported if the SK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SO pin to decrease the rise time of the data. In this mode the SO line on DA9052 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave. The DA9052 will only operate as a slave. As opposed to the 4-wire mode the 2-wire interface has direct (linear) access to the whole DA9052 register space (except R0 and R128). This is achieved by using the MSB of the 2-wire 8-bit register address as a selector of the register page (this does not modify the page control register R0/R128 that is accessible only in 4-wire mode).

16.3.1 Details of the 2-wire control bus protocol

All data is transmitted across the 2-wire bus in groups of 8 bits. To send a bit the SO line is driven towards the independent state while the SK is LOW (a low on SO indicates a zero bit). Once the SO has settled the SK line is brought HIGH and then LOW. This pulse on SK clocks the SO bit into the receivers shift register.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SO line while the SK is in the high state (a STOP condition is indicated by a low to high transition on the SO line while the SK is in the high state).

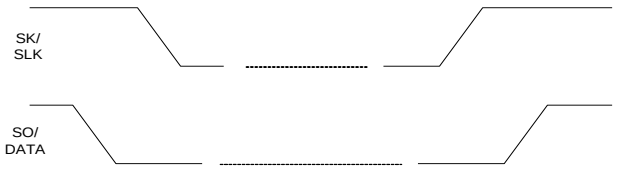


Figure 35: Timing of 2-wire START and STOP condition

The 2-wire bus will be monitored by DA9052 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. These acknowledge is done by pulling the SO line low during the following clock cycle (white blocks marked with 'A' in Figure 36 to Figure 39).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded by DA9052 with Acknowledge):

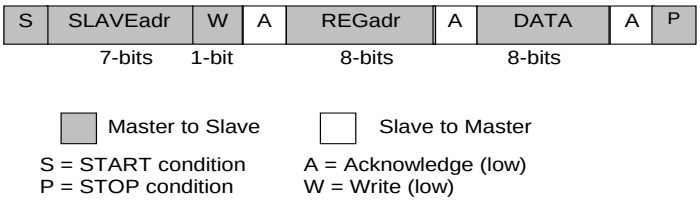


Figure 36: 2-wire byte write (SO/DATA line)

When the host reads data from a register it first has to write access DA9052 with the target register address and then read access DA9052 with a Repeated START or alternatively a second START condition. After receiving the data the host sends Not acknowledge and terminates the transmission with a STOP condition:

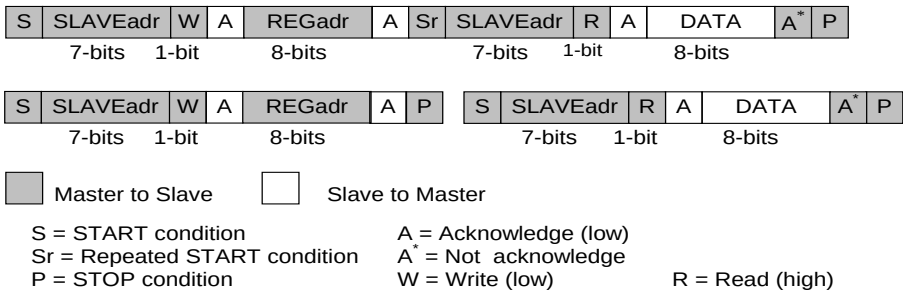


Figure 37: Examples of 2-wire byte read (SO/DATA line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-wire control block then increments the address pointer to the next 2-wire address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then the DA9052 will return code zero:

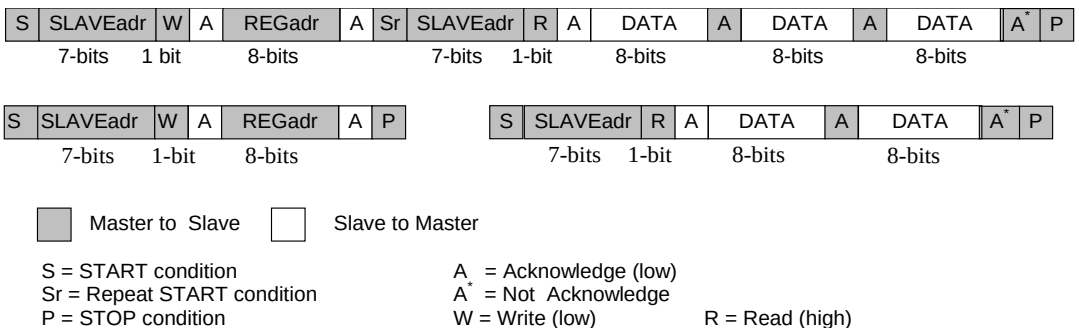


Figure 38: Examples of 2-wire page read (SO/DATA line)

NOTE
The slave address after the repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an acknowledge until the master sends the STOP condition.

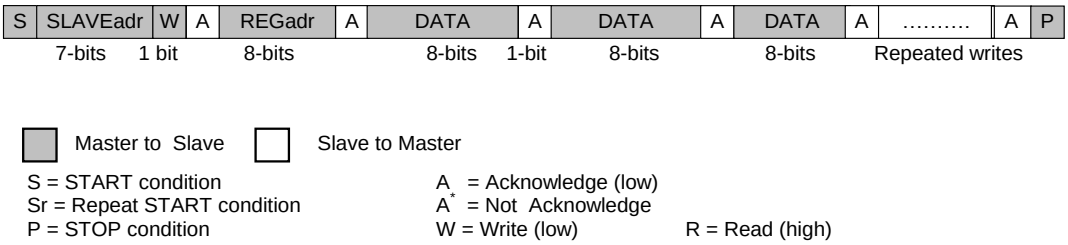


Figure 39: 2-wire page write (SO/DATA line)

An alternate write mode receiving alternated register address and data can be configured to support host repeated write operations that access several but nonconsecutive registers. Data will be stored at the previously received register address:

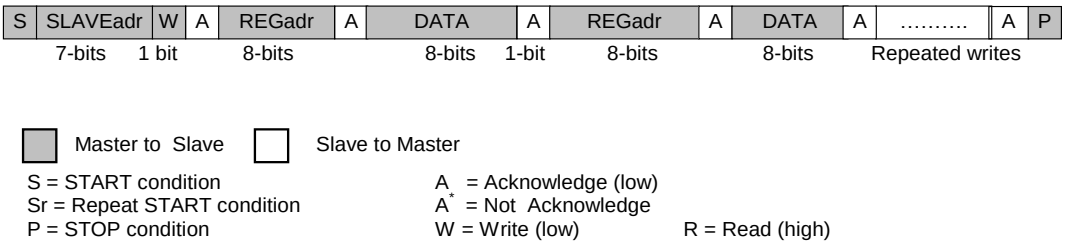


Figure 40: 2-wire repeated write (SO/DATA line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

16.3.2 Alternate high speed 2-wire interface

The high speed 2-wire (HS-2-wire) interface is the alternate serial control bus, which consists of a DATA (data line) and a CLK (clock line) that can be used as an independent control interface for data transactions between DA9052 and a second host processor. The DA9052 high speed 2-wire interface has a configurable 8-bit SLAVE write address (default: 0x92) and a configurable SLAVE read address (default: 0x93).

The interface is enabled if DATA was selected via configuration GPIO14_PIN. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). GPIO15_TYPE defines the supply rail of the interface (used for input logic levels and the internal pull-up resistors). The controls GPIO15_PIN and GPIO15_ MODE are disabled when the interface was enabled via GPIO14_PIN. Whenever the interface receives a READ or WRITE command that includes a matching slave address it is able to trigger the assertion of a nIRQ including an optional wakeup event (enabled via GPIO14_ MODE).

NOTE
If the nIRQ assertion from interface access is enabled (E_GPI4) it may by masked as long as the HS-2-wire is in use (this nIRQ cannot be cleared via the HS-2_wire interface because every interface access will trigger a re-assertion).

Beside the interface base address and the optional wakeup the characteristics of the HS-2-wire interface is identical to the power manager 2-wire interface (see above).

NOTE
By connecting TP to VDDCORE DA9052 (POWER COMMANDER mode) will load the register default values via the HS 2-wire interface instead of from OTP cells. In this mode the interface will be supplied from VDDCORE (independent to the settings at GPIO15_TYPE).

17 DA9052 operating modes

17.1 ACTIVE mode

DA9052 enters ACTIVE mode after the host processor has performed at least one initial ‘alive’ watchdog write (or alternatively an initial assertion of the KEEP_ACT pin) within the target time window (this watchdog condition can be disabled).

A running application is typically in ACTIVE mode in this mode the PMIC core functions (for example, LDOCORE, BCD counter, internal oscillator) as well as a supplies for features like battery charger and GP-ADC are enabled. In ACTIVE mode the host processor can take over the control of the automatic battery charging block if necessary and is able to respond to any faults that have been detected. Status information can be read from the host processor via the power manager bus the DA9052 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ). Temperature and voltages inside and outside the DA9052 can be monitored and any fault conditions flagged to the host processor.

17.2 POWER-DOWN mode

DA9052 is in POWER-DOWN mode whenever the power domain SYSTEM is disabled (even partially). This can be achieved when progressing from RESET mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low power mode instructions from the host or happens as an interim state during an application shutdown to RESET mode.

During POWER-DOWN mode the LDOCORE, the band-gap, the nONKEY and the BCD counter are active. Dedicated power supplies can be kept enabled during POWER-DOWN mode if power down voltages has been pre-configured during ACTIVE mode. In addition , for example, GPIO-ports, the GP-ADC, battery charger and the control interfaces keep on running if not disabled via register PD_DIS. Disabling blocks during POWER-DOWN mode will save quiescent current especially if all blocks are disabled that require an oscillator clock. If the host will no longer communicate during POWER-DOWN mode the control interfaces may be temporally disabled too (see controls PM-IF_PD/HS-2-wire_PD). Also dedicated power supplies can be enabled in POWER-DOWN mode if power down voltages has been pre-configured during ACTIVE mode. The internal oscillator (2 MHz) will only run on demand (for example for a running GP-ADC or enabled bucks are enabled that are not forced to PFM mode). The application supervision by WATCHDOG timer is discontinued in POWER-DOWN mode. Via clock gating the digital control logic of disabled features from DA9052 (such as regulators, bucks, chargers, boosts and GP-ADC) will be disconnected from the clock tree, so that the device will offer an optimized dissipation power in POWER-DOWN mode.

Following the next wakeup event all supplies are re-configured with their default voltage values from OTP and the sequencer timers are set to their default OTP values. If the POWER-DOWN mode was caused by releasing SYS_EN the sequencer pointer is located at position 0 that allows default enabling and disabling of supplies (beside LDOCORE).

17.3 RESET mode

DA9052 is in RESET mode whenever a complete application reset is required. The RESET mode happens after cold start when progressing from NO-POWER mode or can be forced by the user via a pressed reset switch that is connected to port nSHUTDOWN, a long press of nONKEY (if its RESET feature was enabled) or a long parallel assertion of GPIO14 and GPIO15 (if this RESET feature was enabled), from the host processor by asserting port nSHUTDOWN or via an error detection from DA9052.

DA9052 error conditions that force a RESET mode:

- A Watchdog write from the host outside of the watchdog time window (if watchdog was enabled)
- An under-voltage detected at VDDOUT (VDDOUT < VDD_FAULT_LOWER)
- An internal die over-temperature detected
- An overvoltage or over current at the boost

In order to allow the host to determine the reason for the RESET a FAULTLOG register records the cause.

When returning from POWER-DOWN mode the RESET mode will be achieved after powering down domain SYSTEM completely and continue towards a state with absolute minimum current consumption, with the only active circuits being LDOCORE, the BCD counter, the band gap and the VDDREF, VBUS, DCIN, ACC_ID_DET and VDDOUT comparators. Beside LDO1 and the backup battery charger other supplies and blocks on DA9052 such as the backlight boost are automatically disabled to avoid draining the battery. During DA9052 RESET mode also the host processor can be held in a RESET state via port nRESET that is always asserted to low when DA9052 progresses from RESET mode (for example, after cold start from NO-POWER mode) and can be asserted (depending on configuration of sequencer step 0) when the sequencer has finished powering down domain SYSTEM (even partially) .

Beside E_B_FAULT and E_ALARM all asserted events will automatically be cleared and the DA9052 register configuration will be re-loaded from OTP when leaving RESET mode (with the exception of AUTO_BOOT in case of emergency charging).

NOTE
FAULT_LOG and other non OTP loaded registers such as. the RTC calendar and alarm will not be changed when leaving RESET mode.

Some RESET conditions like the SHUTDOWN via register bit, WATCHDOG error, over-temperature will automatically expire. Other conditions like asserting the port nSHUTDOWN need to be released to enable a progress from RESET to POWER-DOWN mode. If the RESET was initiated by a hardware reset from user keys or port nSHUTDOWN a 500 ms time out will be inserted before trying to power up again. When the RESET condition has disappeared DA9052 requires either a connected good main battery (VDDOUT > VDD_FAULT_UPPER) or a detected supply (VBUS/DCIN > VCH_THR) that is able to provide enough power to VDDOUT (VDDOUT > VDDOUT_MIN) to start-up to POWER-DOWN mode.

17.4 NO-POWER mode

DA9052 will enter the NO-POWER mode when VDDCORE drops below VPOR_LOWER (for example, during continued discharge of main and backup battery). As long as VDDCORE is now lower than VPOR_UPPER the core supply LDOCORE, the 32 kHz oscillator and the BCD counter are switched off, an internal power-on-reset (nPOR) is asserted and only the VDDCORE comparator is active and checks for a condition that allows DA9052 to turn on again. When DA9052 detects either a good main battery or a connected supply charger which rises VDDCORE > VPOR_UPPER it will reset the BCD counter and FAULT_LOG register and progress to RESET mode.

17.5 POWER COMMANDER mode

This is a special mode for evaluation and configuration. In POWER COMMANDER mode DA9052 is configured to load the control register default values from the HS 2-wire interface instead of from the OTP cells so that unprogrammed DA9052 samples will power up and allow a PC running power commander software to load all the configuration registers.

POWER COMMANDER mode is enabled by connecting TP to VDDCORE.

In RESET-mode DA9052 will do an initial OTP read to setup the trim values. However, if the OTP values loaded into these registers are not as required they can be updated during the subsequent power commander programming sequences.

NOTE
In POWER COMMANDER mode GPI14/15 will be configured for HS-2-wire interface operation (with VDDCORE as the supply) and GPO13 will be configured as an output for nVDD_FAULT. Any register writes or OTP loads which can change this configuration are ignored until DA9052 has exited from POWER COMMANDER mode.

After the initial OTP read has completed DA9052 informs the system that it is waiting for a programming sequence by driving nVDD_FAULT low. The software running on the PC monitors nVDD_FAULT and responds by downloading the values into the configuration registers within DA9052. nVDD_FAULT is automatically released after the release register was loaded.

There are two programming sequences performed in POWER COMMANDER mode. The first takes place between RESET and POWER-DOWN modes and the second takes place between POWER-DOWN and SYSTEM modes. Two release registers are used support these two programming sequences:

- A write to register R106 will end the first programming sequence
- A write to register R61 will end the second programming sequence

During these programming sequences any registers can be written too in any order, but the sequence will terminate after the appropriate release register has been written to.

NOTE
To correctly configure DA9052 registers, R10 to R105 should be programmed during the first sequence and FAULT LOG register (R9) bit VDD_FAULT has to be cleared by writing a ‘1’. Registers R14 and R43 to R61 should be programmed during the second sequence.

The host can determine whether DA9052 is in the first or second programming sequence by reading the FAULT LOG register. If a read of the FAULT LOG register bit VDD_FAULT returns a zero, then the DA9052 is in the second programming sequence otherwise it is in the first.

After the first programming sequence has been completed DA9052 will be in POWER-DOWN mode. Progression from this mode is determined by the values programmed for SYS_EN and AUTO_BOOT. If DA9052 has been directed to progress from POWER-DOWN mode then it will drive pin nVDD_FAULT low for a second time to request that the SW performs the second programming sequence.

Once the second programming sequence has completed the progress of the power-up sequence will be controlled by the values loaded during the programming sequence.

The programmed configuration can be identified by reading the fuse register CONFIG_ID.

NOTE
During POWER COMMANDER mode the fault detection status bit VDD_FAULT and the level at the related pin nVDD-FAULT do not match and does not indicate a low voltage level at VDDOUT. An enabled shutdown from the 5 s assertion of GPIO14/15 will be ignored during POWER COMMANDER mode.

17.6 DA9052 start-up from NO-POWER mode

17.6.1 Power-on-reset

To guarantee the correct start-up of DA9052 an internal power-on-reset nPOR (active low) is generated for the initial connection of either a supply or a good battery following a phase of not being supplied with sufficient power. To allow DA9052 to start-up even if the main battery is completely discharged an internal VDDREF rail is used to supply the charger blocks, comparators and the control logic. If no charger is present VDDREF is switched to the main battery or backup battery, which ever provides the higher voltage level. If the backup battery was connected to the application before main power, DA9052 remains off and draws no current. This allows the application to wait for its initial activation without discharging the backup battery.

While VDDCORE < VPOR_UPPER the internal nPOR is asserted and DA9052 will not switch on (NO-POWER mode). When VDDCORE rises above VPOR_UPPER the nPOR is negated, LDOCORE will be switched on, the BCD counter and FAULT_LOG register is reset and DA9052 progresses to RESET mode.

When an external charger is detected (rising edge on DCIN_DET or VBUS_DET) having no or only a deep discharged main battery connected to DA9052 the internal charger, oscillator and band-gap are enabled and the whole OTP trim block is read and stored to the register bank. If the supply voltage is below the charger detection threshold (VCH_THR) after a debouncing period of Tdelay (10 ms, to allow for de-bouncing of the input signal and the band-gap reference to settle) the device returns to RESET mode.

If the external charger is still present and the CHG_ATT comparator flags a minimum of 100 mV head room from charger input VCENTER to VDDOUT DA9052 starts-up the charger buck to supply VDDOUT at the default current limit (loaded from OTP) and starts supplying power to VDDOUT, which enables an application start-up also with a flat battery. When VDDOUT rises above VDDOUT_MIN DA9052 enters the POWER-DOWN mode. If this does not happen within 128 ms it will return to RESET mode.

From POWER-DOWN mode DA9052 will continue with powering up supplies if the power domain SYSTEM was asserted via input port (or set via OTP settings) and AUTO_BOOT was enabled (or a valid wakeup event has happened). The below simplified flow diagram shows the start-up events and an example of a typical initial sequence. If DA9052 causes a RESET from an under voltage detected within 10 s after releasing nRESET (the start-up initiating supply is not strong enough to supply the application) DA9052 will assert VDD_START inside the FAULTLOG register and temporally disable AUTO_BOOT for the consecutive start-up (enabling only the battery charger and start waiting for a valid wakeup event). Only events generated from user inputs (GPIs or nONKEY) trigger a wakeup event during this emergency charging but a flashing LED connected to GPIO 11 or 11 can be automatically enabled via control BLINK_FRQ. AUTO_BOOT is set back to its default value when the battery voltage VBAT > VCHG_BAT -– VCHG_DROP.

A similar start-up to POWER-DOWN mode will be performed when a pre-charged battery was inserted (VDDOUT>VDD_FAULT_UPPER) following a state where DA9052 has not been provided with any supply voltage as shown in Figure 41.

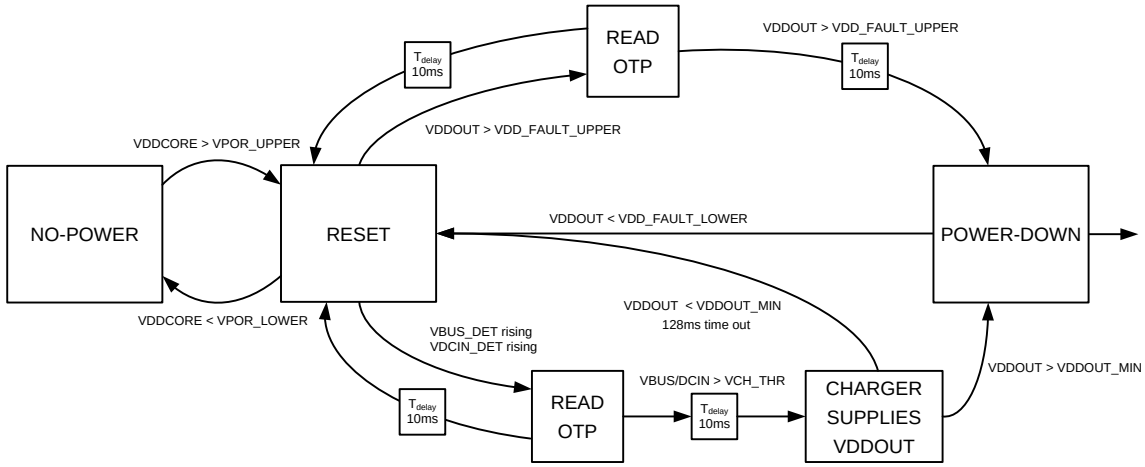


Figure 41: Start-up from NO-POWER to POWER-DOWN mode

17.6.2 Application wakeup

A valid wakeup event (for example nONKEY, SYS_EN, RTC-Alarm or a trigger from GPIOs) initiates an application power up from POWER-DOWN mode. The wakeup event from GPIOs (or selected alternate features, that uses a shared GPI event) has to be enabled via GPIx_MODE and can be masked in addition with the related nIRQ mask. After a wakeup condition is detected the OTP trim block for all supplies and the sequencer timer is read (R14 and R43-R61) and the values reconfigure the supplies and the sequencer timer. If the POWER-DOWN mode was reached by progressing from RESET mode the power sequencer can also be started without waiting for a wakeup event if AUTO_BOOT was asserted.

DA9052 will assert the EXT_WAKEUP signal toward the host processor and if the power domains are not pre-enabled by OTP the host processor has to control the further application start-up (for example via the power domain enable lines). Alternatively DA9052 continues stand-alone powering up the OTP enabled domains via the power domain sequencer. By that a start-up from RESET mode powers up the application automatically only if SYS_EN is asserted from the host processor or was default set from OTP.

Continuation into ACTIVE mode requires an assertion of PWR_EN (from the host via port PWR_EN, register write or enabled from OTP). After starting the WATCHDOG timer the host processor has the configured time window to assert the WATCHDOG timer via the power manager bus (if Watchdog is enabled). If this does not happen the state-machine will terminate the ACTIVE mode at the end of the time window and return to the RESET mode.

Table 46: Wakeup events

Signal / condition	Wakeup	User event	System event	IRQ
Charger attach: E_DCIN_DET	X		X	X
Charger attach: E_VBUS_DET	X		X	X
Charger removal: E_DCIN_REM	X		X	X
Charger removal: E_VBUS_REM	X		X	X
VDDOUT low pre-warning: E_VDD_LOW	X		X	X
RTC alarm: E_ALARM	X		X	X

Signal / condition	Wakeup	User event	System event	IRQ
Sequencing finished: E_SEQ_RDY			X	X
Voltage comparator: E_COMP_1V2	X		X	X
Pressed On-key: E_nONKEY	X	X		X
Accessory and USB ID detect (ID_FLOAT falling edge)	X		X	X
Accessory and USB ID detect (ID_FLOAT rising edge)			X	X
End of battery charging: E_CHG_END	X		X	X
Battery temperature: E_TBAT			X	X
Manual ADC result ready: E_ADC_EOM			X	X
Pen down detection from TSI: E_PEN_DOWN	X	X		X
Measurement ready from TSI: E_TSI_READY			X	X
GPIOs: E_GPIx	X	X		X
ADC 4, 5, 6 threshold: via GPI0, 1, 2	X		X	X
SYS_EN, PWR_EN, PWR1_EN (passive to active transition): via GPIO8, 9, 10	X		X	X
HS-2-wire interface: via GPIO14	X		X	X

17.6.3 Power supply sequencer

The start-up of DA9052 supplies is performed with a sequencer that contains a programmable step timer, a variable ID array of time slot pointers and four predefined pointers (SYSTEM_END, POWER_END, MAX_COUNT and PART_DOWN). The sequencer is able to control up to 22 IDs (4 buck converter, 2 rail switches VCOREVPERI_SW_EN/VMEM_SW_EN, 10 LDOs, 4 feedback pin level controls, a Wait ID (GPI10) and a POWER-DOWN register), which can be grouped in three power domains. The power domains have configurable size and their borders are described by the location pointers SYSTEM_END, POWER_END and MAX_COUNT.

The lowest level power domain SYSTEM starts at step 1 and ends at the step that is described by the location pointer SYSTEM_END. The second level domain POWER starts at the successive step and ends at POWER_END. The third level domain POWER1 starts at the consecutive step and ends at MAX_COUNT. The values of pointer SYSTEM_END, POWER_END and MAX_COUNT are predefined in OTP registers. and should be configured to be SYSTEM_END < POWER_END < MAX_COUNT.

The domain SYSTEM by can be understood as a basic set of supplies that are mandatory to keep the application at least inside a standby/hibernate mode. If enabled via control OTPREAD_EN all supplies of DA9052 and the sequencer timer (registers R14 and R43-R61) are configured with the default value from OTP before powering up the domain SYSTEM. This will cause a reconfiguration of all supplies that have been powered down with a preset voltage level. The second level domain POWER includes supplies that are required in addition to get the application ‘alive’ and set DA9052 in to ACTIVE mode. POWER1 can be understood as a sub domain of POWER that can be used for additional hardware/software initiated control of supply blocks during ACTIVE mode (for example for a sub-application like WLAN or GSM baseband). Supplies in domain POWER and POWER1 can be voltage preconfigured and by that sequentially changed during powering down, but will not be reset to their default values from OTP unless there is a power-up from domain SYSTEM.

NOTE
Running applications should be configured to ACTIVE mode (domain POWER is up) and pointer POWER_END has to be at least one time slot higher than SYSTEM_END.

All buck converter and 10 LDOs of DA9052 have received a unique sequencer ID. The power-up sequence is then defined by an OTP register bank that contains a series of supplies (and other features), which are pointing towards a sequencer time slot. Several supplies can point in to the same time slot and by that will be enabled by the sequencer in parallel. Time slots that have no IDs pointing towards it are dummy steps that do nothing but insert a configurable time delay (marked as 'D' in Figure 43). Supplies that are not pointing towards a sequencer time slot (with a step number greater than zero and less than MAX_COUNT) will not be enabled by the power sequencer and have to be controlled individually by the host (via the power manager bus).

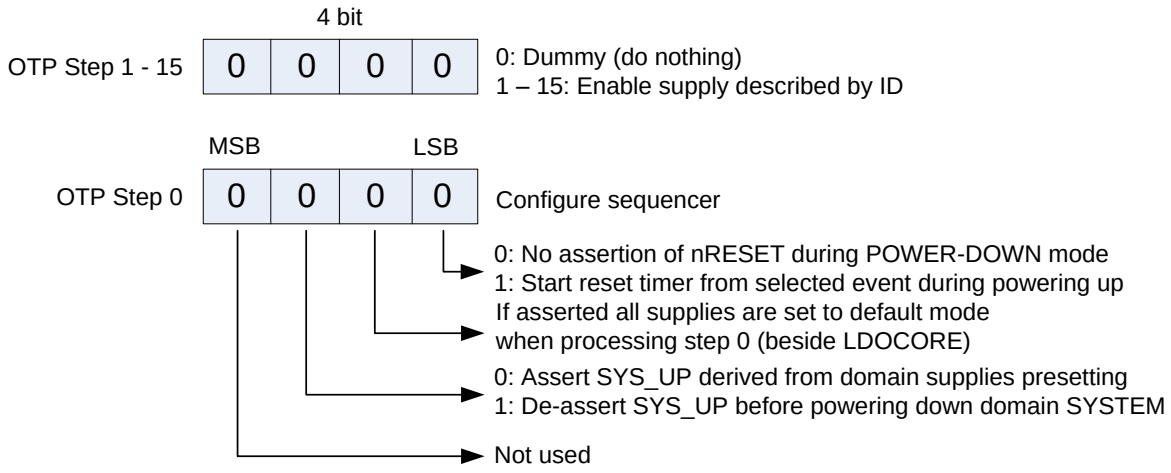


Figure 42: Content of OTP power sequencer register cell

During powering up the sequencer will start at step 0 where the sequencer behavior is configured. If DEF_SUPPLY is asserted this includes an optional enabling of supplies (depending on the OTP default settings of the supplies). If SYS_EN was asserted via port or OTP) the sequencer will assert the READY signal (if selected for the feedback pin) and continue with step 1 that enables all supplies (features) from the OTP register bank that are pointing towards step 1, and so on. .

The sequencer will progress until it has reached the position of pointer SYSTEM_END. Now all supplies of the first power domain SYSTEM are enabled and DA9052 will assert the output signal SYS_UP, release the READY signal and assert the E_SEQ_RDY interrupt.

NOTE
It is recommended that supplies having an asserted enable bit in the OTP are not controlled via IDs of the power sequencer if DEF_SUPPLY is asserted (IDs of these supplies should point into time slot 0).

Table 47: Power sequencer controlled actions

Action	Sequencer time slot
Step 0: Configure power sequencer (Note 1)	ID_0
LDO1_EN	LDO1_STEP
LDO2_EN	LDO2_STEP
LDO3_EN	LDO3_STEP

Action	Sequencer time slot
LDO4_EN	LDO4_STEP
LDO5_EN	LDO5_STEP
LDO6_EN	LDO6_STEP
LDO7_EN	LDO7_STEP
LDO8_EN	LDO8_STEP
LDO9_EN	LDO9_STEP
LDO10_EN	LDO10_STEP
PD_DIS	PD_DIS_STEP
VCOREVPERI_SW_EN	VPERICORE_SW_STEP
VMEM_SW_EN	VMEM_SW_STEP
BCORE_EN	BUCKCORE_STEP
BPRO_EN	BUCKPRO_STEP
BMEM_EN	BUCKMEM_STEP
BPERI_EN	BUCKPERI_STEP
Assert/Release GP_FB2	GP_RISE1_STEP
Assert/Release GP_FB2	GP_RISE2_STEP
Release/Assert GP_FB2	GP_FALL1_STEP
Release/Assert GP_FB2	GP_FALL2_STEP
Wait for active state at GPI 10	WAIT_STEP

Note 1 ID's not controlled by the sequencer (or enabled via DEF_SUPPLY in step 0) should point into step 0.

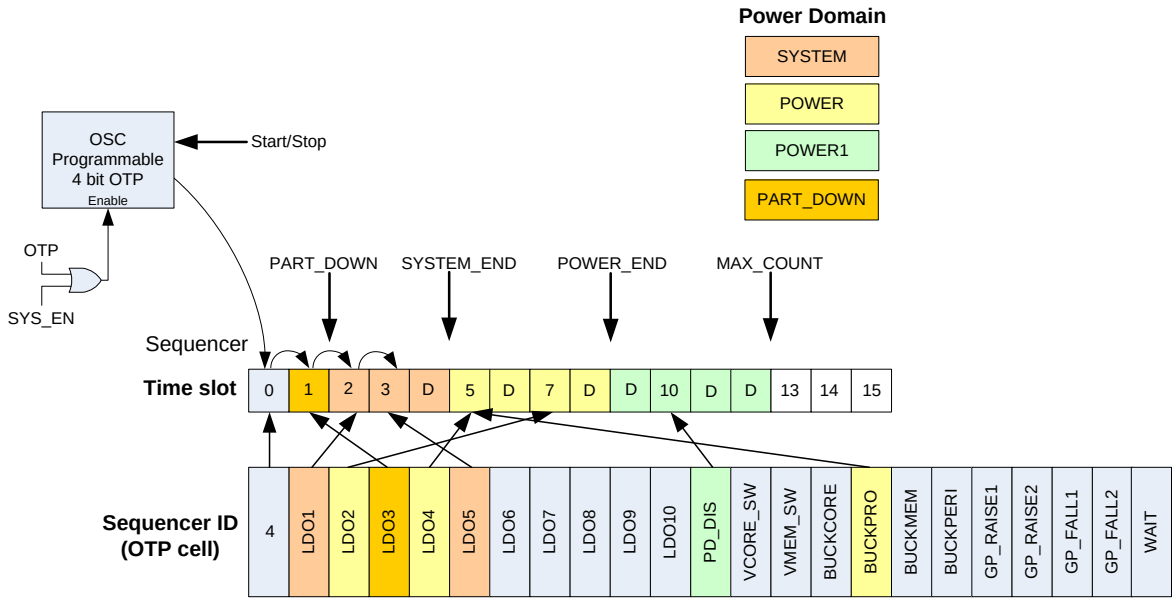


Figure 43: Allocation of supplies (IDs) into to the sequencer time slots

To continue the sequencer checks for PWR_EN to be asserted (via PWR_EN port, register write or OTP). When this is available the feedback signal READY will be asserted and supplies of domain POWER will be enabled sequentially. The sequencer stops at step POWER_END, releases the READY signal, asserts PWR_UP, asserts the E_SEQ_RDY interrupt, enables the initial WATCHDOG timer and waits for an 'alive' feedback from the host processor, which starts the ACTIVE mode of DA9052 and releases an asserted EXT_WAKEUP signal.

A third power domain POWER1 can be enabled from PWR1_EN (asserted via PWR1_EN port, register write or OTP). It will enable all consecutive supplies until step MAX_COUNT has been reached, assert PWR1_UP and assert the E_SEQ_RDY interrupt. The READY signal will be asserted as long as IDs are processed (if enabled). The domain POWER1 offers no dedicated status indicator, but the end of its power-up sequence can be selected to start the RESET timer.

The delay between the steps of a sequence is controlled via a 4-bit OTP programmable timer unit SEQ_TIME with a default delay of 1285 µs per step (minimum 32 µs and max. 816 ms). The delay time between individual supplies can be extended by leaving consecutive steps having no IDs pointing to it (dummy supply), which provides an independent delay configured via control SEQ_DUMMY. The delay timers are configured with their default values from OTP (R43) every time before powering up inside domain SYSTEM.

NOTE
During entering and leaving a power domain a 32 µs delay will always be inserted.

When DA9052 is powering down the sequencer will disable the supplies in reverse order and timing. Supplies that are configured with a preset value (LDOx_CONF or BUCKxxx_CONF bit is set) will not be disabled but configured with their preset voltage when the related time slot/ID is processed. If a domain contains at least one supply with an assigned preset, the power domain status indicator (PWR1_UP, PWR_UP and SYS_UP) will not be released. Otherwise the indicator will be released before the first supply of a power domain will be disabled (a de-assertion of SYS_UP can be forced via step 0 configuration).

If powering down was initiated from releasing PWR_EN1 the sequencer will stop to modify supplies when the domain pointer POWER_END was reached. If PWR_EN was disabled the domain POWER1 will be powered down followed by POWER until the sequencer reaches pointer SYSTEM_END. If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0. If the low power mode was initiated by asserting the control register DEEP_SLEEP the sequencer will first power down POWER1 and POWER continue with SYSTEM and stop when pointer PART_DOWN has been reached (PART_DOWN has to point into domain SYSTEM). If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0 (ignoring the PART_DOWN pointer).

The sequencer asserts the E_SEQ_RDY interrupt whenever reaching the target pointer position. During processing step 0 all supplies (beside LDOCORE) can be set to their OTP default state (if bit DEF_SUPPLY of step 0 is asserted), but the voltage levels are unchanged. It is not recommended to default enable more than a single supply at step 0 due to adding rush currents on the battery.

Asserting control register bit SHUTDOWN will first power down to step 0 and then forces DA9052 to RESET mode. DA9052 features, for example the 32 kHz output buffer or an Auto ADC measurement, can be disabled temporarily in POWER-DOWN mode via register PD_DIS. The timing for processing PD_DIS can be defined by the placement of PD_DIS inside the sequence. The temporary disable will be discontinued. Features asserted in PD_DIS are enabled when PD_DIS is processed during the next power-up sequence. If the READY signal is enabled, it will be asserted during processing of the IDs for powering down.

NOTE
Any reconfiguration of supplies from the host in ACTIVE mode will not affect the domain status indicators (SYS_UP, and PWR_UP) and by that has to be performed carefully. The sequencer will later only check for supplies with an assigned preset configuration bit; others will keep their actual voltage level unchanged during power mode transitions. Powering up from domain SYS_EN will configure all supplies and the sequencer timer with the default values from OTP (R14 and R43-R61). During sequencing (indicated from DA9052 via signal READY or the E_SEQ_RDY interrupt) the host is not allowed to send additional power mode transition requests (via power manger interface or power domain enable lines).

A conditional mode transition can be achieved using ID WAIT_STEP. If pointing into the sequence the progress of an initiated mode transition can be synchronized, for example with the state of a host, and indicated via a signal connected to GPI10. A security time-out of 500 ms can be selected via GPIO10_ MODE, that will trigger a power down to RESET mode (including the assertion of WAIT_SHUT inside register FAULT_LOG) if E_GPI10 was not asserted during the 500 ms period.

NOTE
In the case of a shutdown sequence towards RESET mode (or POWER-DOWN from fault condition) any waiting from ID WAIT_STEP will be skipped.

When powering up from NO_POWER mode ID WAIT_STEP can alternatively be used as a configurable delay to allow the 32 kHz oscillator to stabilize before the TTL signal is provided at the 32 kHz output pin (see register WAIT_CONT).

The configuration at sequencer step 0 (nRES_MODE) enables the assertion of nRESET at the end of a power down sequence and starting the reset timer during the consecutive powering up. This is also true for partial POWER-DOWN mode, when the sequencer powers down to pointer position PART_DOWN. The reset timer will start to run from the selected event RESET_EVENT and release the nRESET port after the reset timer has expired (see also description for powering up from NO-POWER/RESET mode).

NOTE
By connecting TP to VDDCORE DA9052 can be configured to load control register default values from the HS 2-wire interface instead from OTP cells. During start-up the power sequencer will then assert pin nVDD_FAULT (set to zero) and wait until an external device has loaded default values into the control registers R10 to R106 after RESET mode (if VDD_FAULT is asserted), R14 and R43 to R61 when leaving POWER-DOWN mode (if VDD_FAULT is not asserted) via HS 2-wire interface. The host has to clear the FAULT_LOG register after loading R10 to R106. When the last register has been loaded nVDD_FAULT will be released and the start-up sequence is continued. During this mode the settings of GPI14 and 15 will be ignored (pins are assigned as 2-wire interface supplied from VDDCORE).

17.7 System monitor (Watchdog)

After powering up domain POWER DA9052 can initiate an initial Watchdog monitor function (if this feature is enabled via control TWDSCALE). If the WATCHDOG is enabled the host processor has to write logic ‘1’ within a configured TWDMAX time to bit WATCHDOG in DA9052 register R17 to indicate that it is ‘alive’ after PWR_UP was asserted. If the host does not write ‘1’ to the watchdog bit within the TWDMAX time DA9052 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode.

After this first write to the WATCHDOG the host must write to the watchdog bit within a configured time window or DA9052 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode. The WATCHDOG error condition is cleared when entering the RESET mode. The time window has a minimum time TWDMIN fixed at 256 ms and a maximum time TWDMAX of nominally 2.048 s. The TWDMAX value can be extended by multiplying the nominal TWDMAX by the register bits TWDSCALE. TWDSCALE is used to extend the TWDMAX time by x1, x2, x4, x8, x16, x32 or x64.

Changing the maximum value of the time window or the state of KEEPACT_EN bit requires TWDSCALE to be zero (WATCHDOG is disabled) for a minimum of 100 µs. This requires the host to first switch off the WATCHDOG for at least 150 µs before configuring it with a new timing window scale value (TWDSCALE).

The WATCHDOG bit can also be asserted from the host via hardware by asserting KEEP_ACT. This is mode selected via control KEEPACT_EN, which disables the control of the WATCHDOG bit via the host control interface. The in time assertion of nONKEY will then also enable DA9052 to transfer into ACTIVE mode.

Once in the ACTIVE state DA9052 will continue to monitor the system unless it is disabled via setting TWDSCALE to zero. If the WATCHDOG register bit is set to a ‘1’ within the time window the Watchdog monitor resets the timer, sets the WATCHDOG bit back to zero (bit is always read as zero) and waits for the next Watchdog signal.

17.8 Register page control

Register address	Bit	Type	Label	Default	Description
R0 to R128 PAGE_CON_P0	6:0	R		0000000	
	7	RW	REG_PAGE	0	0: Selects Register R1 to R127 1: Selects Register R129 to R255

17.9 Register page 0

17.9.1 Power manager control and monitoring

The STATUS register reports the current value of the various signals at the time that it is read out. All the status bits have the same polarity as their corresponding signals.

Table 48: STATUS_A

Register address	Bit	Type	Label	Default	Description
R1 STATUS_A	0	R	nONKEY	1	Current nONKEY state
	1	R	ID_FLOAT	0	Current ID_FLOAT detector value
	2	R	ID_GND	0	Current ID_GND detector value
	3	R	DCIN_DET	0	0: DCIN voltage not detected (@ DCIN pin) 1: DCIN voltage detected
	4	R	VBUS_DET	0	0: VBUS voltage not detected (@ VBUS pin) 1: VBUS voltage detected
	5	R	DCIN_SEL	0	0: No valid charger at DCIN (overvoltage) 1: DCIN charger selected
	6	R	VBUS_SEL	0	0: No valid charger at VBUS (overvoltage) or DCIN charger received priority 1: VBUS charger selected
	7	R	VDAT_DET	0	0: USB host/hub detected (100 mA) 1: Dedicated or host/hub charger detected

Table 49: STATUS_B

Register address	Bit	Type	Label	Default	Description
R2 STATUS_B	0	R	CHG_ATT	0	0: No charger attached (drop from VCENTER to VDDOUT < 100 mV) 1: Charger attached (drop from VCENTER to VDDOUT > 100 mV)
	1	R	CHG_PRE	0	Charging mode when CHG_END is not asserted 0: Charger is in fast CC/CV mode 1: Charger is in pre-charge mode

Register address	Bit	Type	Label	Default	Description
	2	R	CHG_LIM	0	0: Charging as configured 1: Charge current in constant current mode reduced to less than ICHG_THD
	3	R	CHG_END	0	0: Battery charging 1: Battery charging completed Cleared automatically when starting charging/re-charging
	4	R	CHG_TO	0	0: Battery charging timer OK or disabled 1: Battery charging timeout caused charging finished Cleared automatically when starting charging/re-charging and when loading TCTR
	5	R	GP_FB2	0	Status of GP_FP2 pin: configured from power sequencer
	6	R	SEQUENCING	0	0: Sequencer is idle 1: Sequencer is processing IDs
	7	R	COMP_DET	0	0: Comparator at ADCIN5 (1.2 V) not asserted 1: Comparator asserted

Table 50: STATUS_C

Register address	Bit	Type	Label	Default	Description
R3 STATUS_C	0	R	GPI0	0	GPI0 level or ADCIN4 threshold indicator (‘1’ when overriding high limit)
	1	R	GPI1	0	GPI1 level or ADCIN5 threshold indicator (‘1’ when overriding high limit)
	2	R	GPI2	0	GPI2 level or ADCIN6 threshold indicator (‘1’ when overriding high limit)
	3	R	GPI3	0	GPI3 level
	4	R	GPI4	0	GPI4 level
	5	R	GPI5	0	GPI5 level
	6	R	GPI6	0	GPI6 level
	7	R	GPI7	0	GPI7 level

Table 51: STATUS_D

Register address	Bit	Type	Label	Default	Description
R4 STATUS_D	0	R	GPI8	0	GPI8/SYS_EN level
	1	R	GPI9	0	GPI9/PWR_EN level
	2	R	GPI10	0	GPI10/PWR1_EN level
	3	R	GPI11	0	GPI11 level
	4	R	GPI12	0	GPI12/EXT_WAKEUP/READY level
	5	R	GPI13	0	GPI13 level
	6	R	GPI14	0	GPI14 level
	7	R	GPI15	0	GPI15 level

The EVENT registers hold information about events that have occurred in DA9052. Events are triggered by a change in the status registers that contains the status of monitored signals. When an EVENT bit is set in the event register the nIRQ signal shall be asserted (unless the nIRQ is to be masked by a bit in the IRQ mask register). The nIRQ is also masked during the power-up sequence and will not be released until the event registers have been cleared. The IRQ triggering event register will be cleared from the host by writing a byte containing a '1' at the bit to be reset (bits written containing a zero will leave the related event register bits unchanged and by that keep later events be asserted). The event registers may be read in page/repeated mode. New events that occur during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Table 52: EVENT_A

Register address	Bit	Type	Label	Default	Description
R5 EVENT_A	0	R Note 1	E_DCIN_DET	0	DCIN detection caused event
	1	R Note 1	E_VBUS_DET	0	VBUS 4.4 V detection caused event
	2	R Note 1	E_DCIN_REM	0	DCIN removal caused event
	3	R Note 1	E_VBUS_REM	0	VBUS removal caused event
	4	R Note 1	E_VDD_LOW	0	VDDOUT less than VDDOUT_MON threshold caused event
	5	R Note 1	E_ALARM	0	RTC alarm caused event
	6	R Note 1	E_SEQ_RDY	0	Sequencer reached stop position caused event
	7	R Note 1	E_COMP_1V2	0	1.2 V comparator caused event

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Table 53: EVENT_B

Register address	Bit	Type	Label	Default	Description
R6 EVENT_B	0	R Note 1	E_nONKEY	0	nONKEY caused event
	1	R Note 1	E_ID_FLOAT	0	Accessory detection change caused event (rising and falling edge of ID_FLOAT, only falling edge during POWER-DOWN mode)
	2	R Note 1	E_ID_GND	0	Accessory detection change caused event (rising and falling edge of ID_GND)
	3	R Note 1	E_CHG_END	0	Battery charging complete caused event
	4	R Note 1	E_TBAT	0	Battery over/ under temp caused event
	5	R Note 1	E_ADC_EOM	0	ADC manual conversion result ready caused event
	6	R Note 1	E_PEN_DOWN	0	Pen down detection caused event
	7	R Note 1	E_TSI_READY	0	TSI sequence (XP, XYP, XYZP) finished caused event

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Table 54: EVENT_C

Register address	Bit	Type	Label	Default	Description
R7 EVENT_C	0	R Note 1	E_GPI0	0	GPI event according to active state setting/ ADCIN4 high / low threshold exceeded caused event
	1	R Note 1	E_GPI1	0	GPI event according to active state setting/ ADCIN5 high / low threshold exceeded caused event
	2	R Note 1	E_GPI2	0	GPI event according to active state setting/ ADCIN6 high / low threshold exceeded caused event
	3	R Note 1	E_GPI3	0	GPI event according to active state setting
	4	R Note 1	E_GPI4	0	GPI event according to active state setting
	5	R Note 1	E_GPI5	0	GPI event according to active state setting
	6	R Note 1	E_GPI6	0	GPI event according to active state setting
	7	R Note 1	E_GPI7	0	GPI event according to active state setting

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Table 55: EVENT_D

Register address	Bit	Type	Label	Default	Description
R8 EVENT_D	0	R Note 1	E_GPI8	0	GPI event according to active state setting/SYS_EN assertion caused event
	1	R Note 1	E_GPI9	0	GPI event according to active state setting/PWR_EN assertion caused event
	2	R Note 1	E_GPI10	0	GPI event according to active state setting/PWR1_EN assertion caused event
	3	R Note 1	E_GPI11	0	GPI event according to active state setting
	4	R Note 1	E_GPI12	0	GPI event according to active state setting
	5	R Note 1	E_GPI13	0	GPI event according to active state setting
	6	R Note 1	E_GPI14	0	GPI event according to active state setting/Event caused from host addressing HS-2-wire interface
	7	R Note 1	E_GPI15	0	GPI event according to active state setting

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

The nIRQ line will be released only when all events have been cleared from the host processor by writing a '1' to each asserted event bit (to prohibit missing events it is recommended to clear event bits individually).

Table 56: FAULT_LOG

Register address	Bit	Type	Label	Default	Description
R9 FAULT_LOG Note 1	0	R Note 2	TWD_ERROR	0	Watchdog time violated
	1	R Note 2	VDD_FAULT	1	Power down by VDDOUT under voltage detect
	2	R Note 2	VDD_START	0	Power down by VDDOUT under voltage detect within 10 s from releasing nRESET
	3	R Note 2	TEMP_OVER	0	Junction over temperature detected
	4	R Note 2			
	5	R Note 2	KEY_SHUT	0	Power down by a long press of the nONKEY or GPI14 and GPI15 in parallel
	6	R Note 2	nSD_SHUT	0	Power down by assertion of port nSHUTDOWN
	7	R Note 2	WAIT_SHUT	0	Power down by time out of ID WAIT_STEP

Note 1 The FAULT_LOG register has to be cleared from the host after reading by writing '11111111'.

Note 2 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Table 57: IRQ_MASK_A

Register address	Bit	Type	Label	Default	Description
R10 IRQ_MASK_A	0	R/W	M_DCIN_VLD	0	Mask DCIN detection caused nIRQ
	1	R/W	M_VBUS_VLD	0	Mask VBUS 4.4 V detection caused nIRQ
	2	R/W	M_DCIN_REM	0	Mask DCIN removal caused nIRQ
	3	R/W	M_VBUS_REM	0	Mask VBUS removal caused nIRQ
	4	R/W	M_VDD_LOW	0	Mask VDDOUT low caused nIRQ
	5	R/W	M_ALARM	0	Mask RTC alarm caused nIRQ
	6	R/W	M_SEQ_RDY	0	Mask Sequencer reached stop position caused nIRQ
	7	R/W	M_COMP_1V2	0	Mask 1.2 V comparator caused nIRQ

Table 58: IRQ_MASK_B

Register address	Bit	Type	Label	Default	Description
R11 IRQ_MASK_B	0	R/W	M_nONKEY	0	Mask nONKEY caused nIRQ
	1	R/W	M_ID_FLOAT	0	Mask ID_FLOAT accessory detection change caused nIRQ
	2	R/W	M_ID_GND	0	Mask ID_GND accessory detection change caused nIRQ
	3	R/W	M_CHG_END	0	Mask battery charging complete caused nIRQ
	4	R/W	M_TBAT	0	Mask Battery over / under temp caused nIRQ
	5	R/W	M_ADC_EOM	0	Mask ADC manual conversion result ready caused nIRQ
	6	R/W	M_PEN_DOWN	0	Mask Pen down detection caused nIRQ
	7	R/W	M_TSI_READY	0	Mask TSI sequence (XP, XYP, XYZP) finished caused nIRQ

Table 59: IRQ_MASK_C

Register address	Bit	Type	Label	Default	Description
R12 IRQ_MASK_C	0	R/W	M_GPI0	0	Mask GPI caused/ ADCIN4 high / low threshold exceeded caused nIRQ
	1	R/W	M_GPI1	0	Mask GPI caused/ ADCIN5 high / low threshold exceeded caused nIRQ, should be asserted for LDO H/W control
	2	R/W	M_GPI2	0	Mask GPI caused/ ADCIN6 high / low threshold exceeded caused nIRQ, should be asserted for LDO H/W control
	3	R/W	M_GPI3	0	Mask GPI caused nIRQ
	4	R/W	M_GPI4	0	Mask GPI caused nIRQ
	5	R/W	M_GPI5	0	Mask GPI caused nIRQ
	6	R/W	M_GPI6	0	Mask GPI caused nIRQ
	7	R/W	M_GPI7	0	Mask GPI caused nIRQ

Table 60: IRQ_MASK_D

Register address	Bit	Type	Label	Default	Description
R13 IRQ_MASK_D	0	R/W	M_GPI8	0	Mask GPI/SYS_EN caused nIRQ
	1	R/W	M_GPI9	0	Mask GPI/PWR_EN caused nIRQ
	2	R/W	M_GPI10	0	Mask GPI/PWR1_EN caused nIRQ
	3	R/W	M_GPI11	0	Mask GPI caused nIRQ
	4	R/W	M_GPI12	0	Mask GPI caused nIRQ, should be asserted for LDO H/W control
	5	R/W	M_GPI13	0	Mask GPI caused nIRQ
	6	R/W	M_GPI14	0	Mask GPI/HS-2-wire caused nIRQ
	7	R/W	M_GPI15	0	Mask GPI caused nIRQ

Table 61: CONTROL_A

Register address	Bit	Type	Label	Default	Description
R14 CONTROL_A	0	R/W	SYS_EN Note 1	1	Target status of power domain SYSTEM: State of GPI8 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_8_PIN)
	1	R/W	PWR_EN Note 2	1	Target status of power domain POWER: State of GPI9 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_9_PIN)

Register address	Bit	Type	Label	Default	Description
	2	R/W	PWR1_EN Note 3	0	Target status of power domain POWER1: State of GPI10 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_10_PIN)
	3	R/W	PM_IF_V	0	**0: Power manager IF (4-wire/2-wire) supplied from VDD_IO1** 1: Power manager IF (4-wire/2-wire) supplied from VDD_IO2
	4	R/W	PM_I_V	0	nONKEY, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN are supplied from: **0: VDDCORE** 1: VDD_IO2
	5	R/W	PM_O_V	0	SYS_UP, PWR_UP, GP_FB2, OUT_32K, nRESET, nIRQ are supplied from: **0: VDD_IO1** 1: VDD_IO2
	6	R/W	PM_O_TYPE	0	nRESET, nIRQ output are: **0: Push-pull** 1: Open drain
	7	R/W	GPI_V	0	GPIs (not configured as PM control inputs) are supplied from: **0: VDDCORE** 1: VDD_IO2

Note 1 SYS_EN hardware control can be configured as high or low active via GPIO_8_TYPE.

Note 2 PWR_EN hardware control can be configured as high or low active via GPIO_9_TYPE.

Note 3 PWR1_EN hardware control can be configured as high or low active via GPIO_10_TYPE.

Table 62: CONTROL_B

Register address	Bit	Type	Label	Default	Description
R15 CONTROL_B	0	R/W	BUCK_MERGE	0	Has to be set if the outputs of BUCKCORE and BUCKPRO are merged towards a single coil; the control from BUCKPRO registers is disabled
	1	R/W	ACT_DIODE	0	Battery provides power **0: through internal active diode path (mandatory, if no external FET connected!)** 1: through internal active diode and external power FET
	2	R/W	AUTO_BOOT	1	0: Start-up of power sequencer after progressing from RESET mode requires a valid wakeup event **1: PMIC automatically starts power sequencer after progressing from RESET mode**

Register address	Bit	Type	Label	Default	Description
	3	R/W	OTPREAD_EN	1	0: Partial OTP read after POWER-DOWN mode disabled **1: Power supplies are configured with OTP values when leaving POWER-DOWN mode**
	4	R/W	BBAT_EN	0	**0: Disables supply from backup battery** 1: Automatic switch of VDDREF to backup battery enabled
	5	R/W	WRITE_MODE	1	2-wire multiple write mode (setting used for both 2-wire interfaces) 0: Page write mode **1: Repeated write mode**
	6	R/W	DEEP_SLEEP	0	If set to '1' DA9052 goes to deep sleep mode (sequencer stops at pointer PART_DOWN). The bit is cleared back to '0' automatically before powering up from POWER-DOWN mode
	7	R/W	SHUTDOWN	0	If set to '1' the sequencer powers down to RESET mode The bit is cleared back to '0' automatically before leaving the RESET mode

Table 63: CONTROL_C

Register address	Bit	Type	Label	Default	Description
R16 CONTROL_C	0	R/W	PM_FB1_PIN	0	**0: Feedback pin indicates EXT_WAKEUP events (active high)** 1: Feedback pin is used as READY indicator, signaling ongoing power mode transitions (power sequencer and DVC) (active low)
	1	R/W	PM_FB2_PIN	0	**0: Feedback pin indicates the status of domain POWER1 (active high PWR1_UP)** 1: Feedback pin is used as a configurable GP_FB indicator, that is asserted from the power sequencer
	4:2	R/W	DEBOUNCING	001	GPI, nONKEY and nSHUTDOWN debounce time 000: no debounce time **001: 10.24 ms** 010: 20.48 ms 011: 40.96 ms 100: 102.40 ms 101: 1024 ms 110: 2048 ms 111: 5120 ms

Register address	Bit	Type	Label	Default	Description
	6:5	R/W	BLINK_FRQ	11	GPO10/GPO11 flashing frequency 00: no blinking 01: every 1 s 10: every 2 s **11: every 2 s enabled during PRE-CHARGE mode and emergency charging**
	7	R/W	BLINK_DUR	0	GPO10/GPO11 flashing on-time **0:10 ms** 1:40 ms

Table 64: CONTROL_D

Register address	Bit	Type	Label	Default	Description
R17 CONTROL_D	2:0	R/W	TWDSCALE	000	**000: Watchdog disabled** 001: 1x scaling applied to TWDMAX period 010: 2x 011: 4x 100: 8x 101: 16x 110: 32x 111: 64x
	3	R/W	KEEPACT_EN	0	**0: nONKEY is enabled** 1: nONKEY is disabled, pin asserted to KEEPACT (hardware-assertion of bit WATCHDOG)
	4	R/W	nONKEY_SD	0	**0: Disables shutdown via nONKEY** 1: Enables shutdown via nONKEY
	5	R/W	GPI14_15_SD	0	**0: Disables shutdown via parallel assertion of GPI14 and GPI15** 1: Enables shutdown via GPI14 & GPI15
	6	R/W	ACC_DET_EN	0	Enables ACC_DET circuitry when set to ‘1’
	7	R/W	WATCHDOG	0	If set to ‘1’ watchdog timer is reset. The bit is cleared back to ‘0’ automatically.

Table 65: PD_DIS

Register address	Bit	Type	Label	Default	Description
R18 PD_DIS	0	R/W	GPIO_PD	0	**0: GPIO extender enabled during POWER-DOWN** 1: Auto-disable of features configured as GPIO pins during POWER-DOWN mode and force the detection of a pending ACTIVE state on GPIs by re-enabling the pin through a passive state of the related GPI status register
	1	R/W	GP-ADC_PD	1	0: ADC/TSI measurements continue during POWER-DOWN as configured **1: Auto-disable auto measurements on A4, A5, A6, A7(TSI) and manual measurement on all channels during POWER-DOWN mode; if no auto measurements for charging and on A0 are required switch off the ADC completely**
	2	R/W	PM-IF_PD	1	0: Power manager interface not disabled during POWER-DOWN mode **1: Auto-disable of power manager interface during POWER-DOWN mode**
	3	R/W	HS-2-wire_PD	1	0: HS-2-wire not disabled during POWER-DOWN mode **1: Auto-disable of HS-2-wire interface during POWER-DOWN mode**
	4	R/W	CHG_PD	0	**0: Enables battery charging during POWER-DOWN** 1: Auto-disable battery charging during POWER-DOWN mode
	5	R/W	CHG_BBAT_PD	0	**0: Enables backup battery charger during POWER-DOWN mode** 1: Auto-disable backup battery charger during POWER-DOWN
	6	R/W	OUT_32K_PD	1	0: Enables OUT_32K during POWER-DOWN **1: Auto-disable OUT_32K output buffer during POWER-DOWN mode and auto-enable during power-up from NO-POWER mode when executing this ID**
	7	R/W	PM-CONT_PD	0	**0: SYS_EN, PWR_EN, PWR1_EN enabled during POWER-DOWN** 1: Auto-disable of SYS_EN, PWR_EN and PWR_EN during POWER-DOWN mode and force the detection of a pending ACTIVE state by re-enabling the pin through a passive state of the related GPI status register

Table 66: INTERFACE

Register address	Bit	Type	Label	Default	Description
R19 INTERFACE	0	R Note 1	IF_TYPE	0	**0: Power manager IF is 4-wire** 1: Power manager IF is 2-wire
	1	R Note 1	CPOL	0	4-wire IF clock polarity **0: SK is low during idle** 1: SK is high during idle
	2	R Note 1	CPHA	0	4-wire IF clock phase (see Table 44 4-wire clock configurations)
	3	R Note 1	R/W_POL	1	4-wire: Read/Write bit polarity 0: Host indicates reading access via R/W bit = '0' **1: Host indicates reading access via R/W bit = '1'**
	4	R Note 1	nCS_POL	1	4-wire chip select polarity 0: nCS is low active **1: nCS is high active**
	7:5	R Note 1	IF_BASE_ADDR	100	3 MSB of 2-wire control interfaces base address XXX10000 **100**10000 = 0x90 write address of PM 2-wire interface **100**10001 = 0x91 read address of PM 2-wire interface **100**10010 = 0x92 write address of HS-2-wire interface **100**10011 = 0x93 read address of HS-2-wire interface

Note 1 The base address can be written/modified for unmarked samples having the control OTP_CONF_LOCK not been asserted/fused.

Table 67: RESET

Register address	Bit	Type	Label	Default	Description
R20 RESET	5:0	R/W	RESET_TIMER	000101	000000: RESET disabled 000001: 1.024 ms 000010: 2.048 ms 000011: 3.072 ms 000100: 4.096 ms **000101: 5.120 ms** …. 011110: 30.720 ms 011111: 31.744 ms 100000: 32.768 ms 100001: 65.536 ms 100010: 98.304 ms ….. 111101: 983.040 ms 111110: 1015.808 ms 111111: 1048.576 ms
	7:6	R/W	RESET_EVENT	01	RESET timer started by 00: EXT_WAKEUP **01: SYS_UP** 10: PWR_UP 11: PWR1_UP (internal signal)

18 GPIO extender

The DA9052 includes a GPIO extender that offers up to 16 VDDOUT-tolerant (5.5 V max) general purpose input/output pins; each controlled by registers from the host.

NOTE
The input voltage has to be lower than the VDDIO level selected for the port.

The GPIO ports are pin-shared with ports from GP-ADC, TSI-interface, HS-2-wire-interface and signals from the power manager and can be individually assigned. Configuration settings and events from several GPIx ports are shared with alternate features. If, for example, ADCIN5 was selected overriding the configured thresholds will trigger a GPI1 event that generates a maskable GPI1 interrupt. The GPI active High/Low setting from GPIOx_TYPE register and the selection of supply rail (and pull-up resistor) is also valid for the alternate port features selected via GPIOx_PIN (for example SYS_EN, PWR_EN and PWR1_EN). The same is true for GPIOx_MODE to enable triggering a wakeup event (ADCIN4, ADCIN5, SYS_EN, PWR_EN, PWR1_EN, HS-2-wire interface) for the alternate features.

In ACTIVE and POWER-DOWN modes the GPIO extender can continuously monitor the level of ports that are selected as general purpose inputs. GPIs are supplied from the internal rail VDDCORE or VDD_IO2 and can be configured to trigger events in active high or active low mode. The input signals can be debounced or directly change the state of the assigned status register GPIx to high or low. Whenever the status has changed to its configured active state (edge sensitive) the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked inside the nIRQMASK register). GPI 0, 3 to 11 and 13 to 15 will generate a system wakeup if debouncing is enabled. In debouncing off mode GPI 12 enables/disables LDO9, the minimum enable time is 100 µs. The same feature is available at GPI 1 for LDO4_EN and GPI 2 for LDO5_EN. Events on GPI10 can be used to control the progress of the power sequencer. Processing ID WAIT_STEP will cause the sequencer to wait until GPI 10 changes into active state.

If defined as an output the GPO can be configured as open-drain or push-pull. The supply rail can be individually selected from either VDD_IO1 or VDD_IO2. When selecting VDD_IO1 in open-drain mode, there is an internal pull-up resistor against this rail, otherwise an external pull-up resistor towards the target voltage level is required. The output state will be assigned as configured by the GPIO register bit GPIOx_MODE.

GPO 10, 11 are high power GPO ports, where the maximum sink current is rated to be 15 mA and the maximum source current will be 4 mA. This enables driving LEDs with optional RTC timer controlled flashing.

GPO 14 and 15 are high power GPO ports able to sink up to 30 mA and include an optional PWM control. The PWM control can also be made to dim the brightness between its current value and a new value at a rate of 32 ms per step. In conjunction with the LED3 drive, which offers a similar PWM mode, this creates a common anode tricolor LEDs brightness control.

18.1 GPIO control

Table 68: GPIO_0-1

Register address	Bit	Type	Label	Default	Description
R21 GPIO_0-1 Note 1	1:0	R/W	GPIO0_PIN	00	PIN assigned to **00: ADCIN4** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO0_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO0_ MODE	1	0: GPI/ADCIN4: debouncing off GPO: Sets output to low level **1: GPI/ADCIN4: debouncing on and generate wakeup** GPO: Sets output to high level
	5:4	R/W	GPIO1_PIN	00	PIN assigned to **00: ADCIN5/1.2 V comparator** 01: GPI (LDO4 hardware control) 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO1_TYPE	0	**0: GPI: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO1_ MODE	1	0: GPI/ADCIN5: debouncing off, Set LDO4_EN when GPI transfers to active state (reset when GPI gets to passive state) 1.2 V comparator: (debouncing off), Set LDO4_EN when GPI transfers to active state (reset when GPI gets to passive state) GPO: Sets output to low level **1:** GPI: debouncing on, no LDO4_EN control **ADCIN5/1.2 V comparator: debouncing on and generate wakeup** GPO: Sets output to high level

Note 1 If GPIO1 pin = 01 and GPIO1 mode = 00 then bit 1 of register R12 should also be set to avoid small nIRQ pulse generation.

Table 69: GPIO_2-3

Register address	Bit	Type	Label	Default	Description
R22 GPIO_2-3 Note 1	1:0	R/W	GPIO2_PIN	01	PIN assigned to 00: ADCIN6 **01: GPI (LDO5 hardware control)** 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO2_TYPE	1	**0: GPI: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO2_MODE	1	0: GPI/ADCIN6: (debouncing off), **Set LDO5_EN when GPI transfers to active state (reset when GPI gets to passive state)** GPO: Sets output to low level **1: GPI: debouncing on, no LDO5_EN control** ADCIN6: debouncing on and generate wakeup GPO: Sets output to high level
	5:4	R/W	GPIO3_PIN	00	PIN assigned to **00: TSIYN** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO3_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO3_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Note 1 If GPIO2 pin = 01 and GPIO2 mode = 00 then bit 2 of register R12 should also be set to avoid small nIRQ pulse generation.

Table 70: GPIO_4-5

Register address	Bit	Type	Label	Default	Description
R23 GPIO_4-5	1:0	R/W	GPIO4_PIN	00	PIN assigned to **00: TSIYP** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO4_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO4_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level
	5:4	R/W	GPIO5_PIN	00	PIN assigned to **00: TSIXN** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO5_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO5_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Table 71: GPIO_6-7

Register address	Bit	Type	Label	Default	Description
R24 GPIO_6-7	1:0	R/W	GPIO6_PIN	00	PIN assigned to **00: TSIXP** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO6_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO6_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level
	5:4	R/W	GPIO7_PIN	00	PIN assigned to **00: TSIREF** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO7_TYPE	0	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO7_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Table 72: GPIO_8-9

Register address	Bit	Type	Label	Default	Description
R25 GPIO_8-9	1:0	R/W	GPIO8_PIN	01	PIN and status register bit assigned to 00: SYS_EN **01: GPI** 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO8_TYPE	0	**0: GPI/SYS_EN: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/SYS_EN: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO8_ MODE	1	0: GPI only (not SYS_EN): debouncing off GPO: Sets output to low level **1: GPI/SYS_EN: debouncing on and generate wakeup** GPO: Sets output to high level
	5:4	R/W	GPIO9_PIN	01	PIN and status register bit assigned to 00: PWR_EN **01: GPI** 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO9_TYPE	0	**0: GPI/PWR_EN: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/PWR_EN: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO9_ MODE	1	0: GPI/PWR_EN: debouncing off GPO: Sets output to low level **1: GPI/PWR_EN debouncing on and generate wakeup** GPO: Sets output to high level

Table 73: GPIO_10-11

Register address	Bit	Type	Label	Default	Description
R26 GPIO_10-11	1:0	R/W	GPIO10_PIN	01	PIN and status register bit assigned to 00: PWR1_EN **01: GPI** 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO10_TYPE	0	**0: GPI/PWR1_EN: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/PWR1_EN: active high GPO: blinking from RTC counter, supplied from VDD_IO2/ external pull-up in open-drain mode
	3	R/W	GPIO10_ MODE	1	0: GPI/PWR1_EN: debouncing off GPO: Sets output to low level **1: GPI/PWR1_EN: debouncing on and generate wakeup, time out from processing ID WAIT_STEP after 500 ms** GPO: Sets output to high level
	5:4	R/W	GPIO11_PIN	00	PIN assigned to **00: ACC_ID_DET** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO11_TYPE	0	**0: GPI: active low** GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: blinking from RTC counter, supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO11_ MODE	1	0: GPI: : debouncing off / ACC_ID_DET: debouncing off GPO: Sets output to low level **1: GPI: : debouncing on and generate wakeup** / ACC_ID_DET: debouncing on and generate wakeup (for ACC_ID_DET only at ID_FLOAT falling edge) GPO: Sets output to high level

Table 74: GPIO_12-13

Register address	Bit	Type	Label	Default	Description
R27 GPIO_12-13 Note 1	1:0	R/W	GPIO12_PIN	11	PIN and status register bit assigned to 00: GP_FB1 (EXT_WAKEUP/READY) 01: GPI (LDO9 hardware control) 10: GPO (Open drain) **11: GPO (Push-pull)**
	2	R/W	GPIO12_TYPE	0	0: GPI: active low **GPO/GP_FB1: supplied from VDD_IO1/internal pull-up for open-drain** 1: GPI: active high GPO/GP_FB1: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO12_ MODE	0	0: GPI: debouncing off, Set LDO9_EN when GPI transfers to active state (reset when GPI gets to passive state) **GPO: Sets output to low level** 1: GPI: debouncing on, no LDO9_EN control GPO: Sets output to high level
	5:4	R/W	GPIO13_PIN	00	PIN assigned to **00: nVDD_FAULT** 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO13_TYPE	0	0: GPI: active low **GPO/nVDD_FAULT: supplied from VDD_IO1/internal pull-up for open-drain** 1: GPI: active high GPO/nVDD_FAULT: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO13_ MODE	0	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Note 1 If GPIO12 pin = 01 and GPIO12 mode = 0 then bit 4 of register R13 should also be set to avoid small nIRQ pulse generation.

Table 75: GPIO_14-15

Register address	Bit	Type	Label	Default	Description
R28 GPIO_14-15	1:0	R/W	GPIO14_PIN	11	PIN assigned to 00: DATA (assigns GPIO15_PIN to CLK) 01: GPI 10: GPO (Open drain, PWM control) **11: GPO (Push-pull)**
	2	R/W	GPIO14_TYPE	0	0: GPI: active low **GPO: supplied from VDD_IO1/internal pull-up in open-drain mode** 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO14_ MODE	0	0: GPI: debouncing off, no wakeup HS-2-wire: no wakeup **GPO: Sets output to low level** 1: GPI:debouncing on and generate wakeup HS-2-wire: generate wakeup when interface was accessed GPO: Sets output to high level
	5:4	R/W	GPIO15_PIN	11	PIN assigned to 00: CLK (see GPIO14_PIN) 01: GPI 10: GPO (Open drain, PWM control) **11: GPO (Push-pull)**
	6	R/W	GPIO15_TYPE	0	0: GPI: active low **GPO: supplied from VDD_IO1/internal pull-up in open-drain mode** DATA/CLK supplied from VDD_IO1 (Note 1) 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode DATA/CLK supplied from VDD_IO2 (Note 1)
	7	R/W	GPIO15_ MODE	0	0: GPI: debouncing off **GPO: Sets output to low level** 1: GPI: debouncing on and generate wakeup GPO: Sets output to high level

Note 1 In POWER COMMANDER mode the HS-2-wire IF is always supplied from VDDCORE.

19 Power supply sequencer

The start-up of DA9052 supplies is performed with a sequencer. The sequencer is able to control up to 22 IDs (four buck converter, two rail switches, 10 LDOs, four feedback pin level controls, a Wait ID and a POWER-DOWN register), which can be grouped in three power domains. The power sequences for each domain have configurable size.

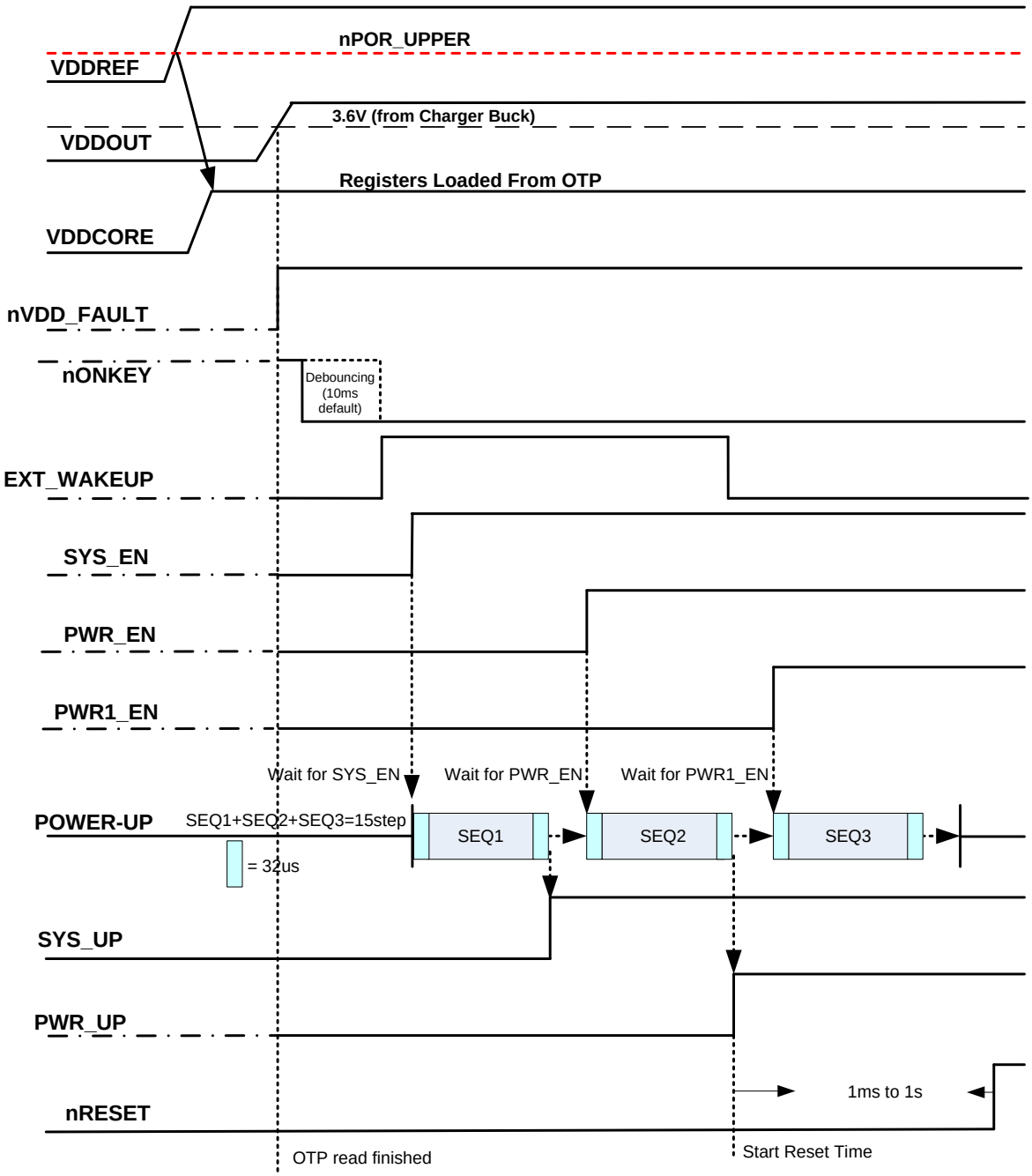


Figure 44: Typical power-up timing

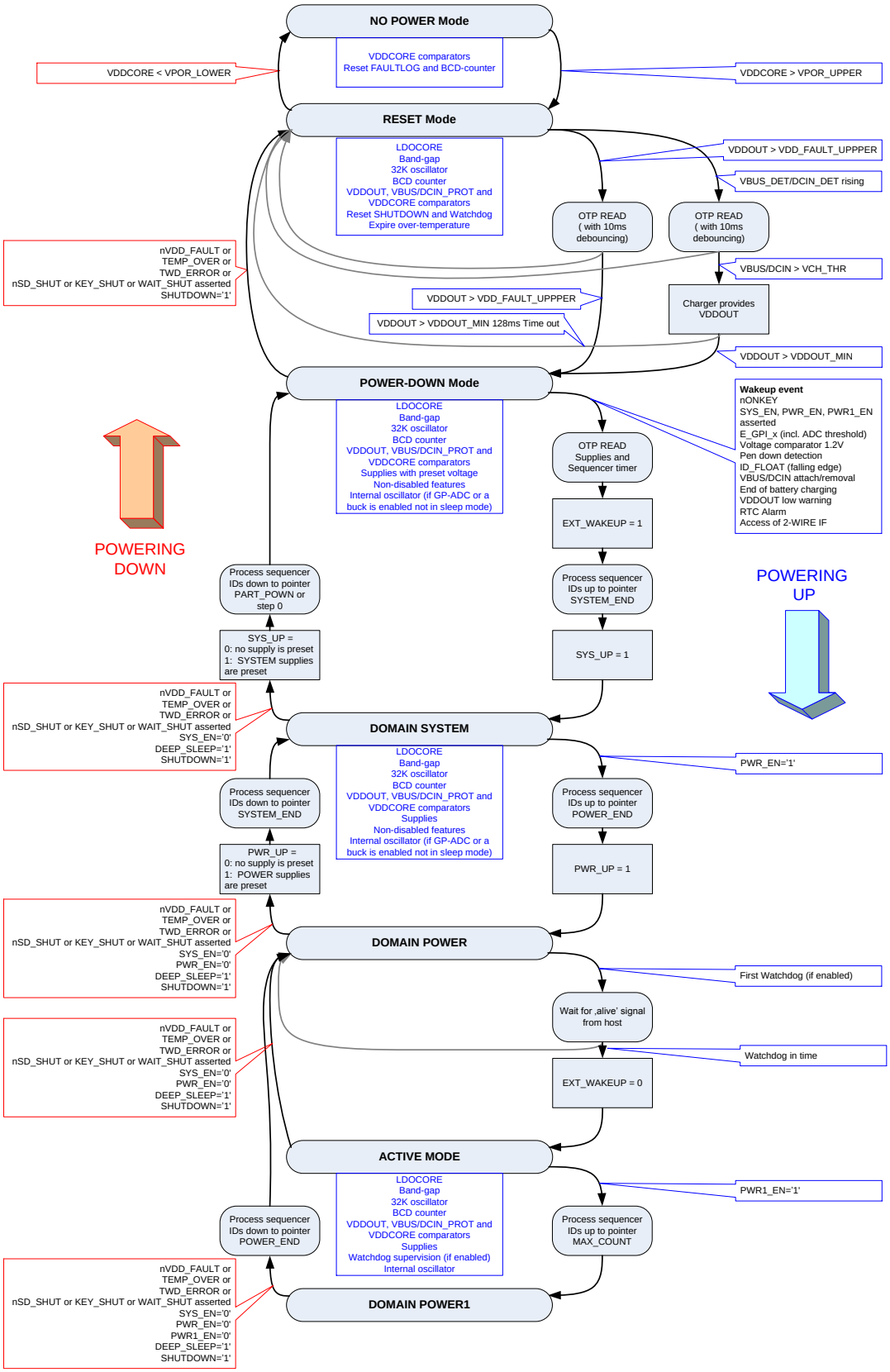


Figure 45: Power mode transitions

19.1 Power sequencer

Table 76: ID_0_1

Register address	Bit	Type	Label	Default	Description
R29 ID_0_1	0	R/W	nRES_MODE	1	0: No assertion of nRESET during POWER-DOWN mode **1: Assert nRESET when entering POWER-DOWN mode (release after leaving POWER-DOWN mode)**
	1	R/W	DEF_SUPPLY	0	When asserted all supplies (beside LDOCORE) are enabled/disabled from OTP default mode
	2	R/W	SYS_PRE	0	**0: Set SYS_UP as configured from supplies presettings** 1: Always de-assert SYS_UP before powering down domain SYSTEM
	3	R			
	7:4	R/W	LDO1_STEP	1001	Power sequencer time **slot 9**

Table 77: ID_2_3

Register address	Bit	Type	Label	Default	Description
R30 ID_2_3	3:0	R/W	LDO2_STEP	0100	Power sequencer time **slot 4**
	7:4	R/W	LDO3_STEP	1000	Power sequencer time **slot 8**

Table 78: ID_4_5

Register address	Bit	Type	Label	Default	Description
R31 ID_4_5	3:0	R/W	LDO4_STEP	0010	Power sequencer time **slot 2**
	7:4	R/W	LDO5_STEP	0011	Power sequencer time **slot 3**

Table 79: ID_6_7

Register address	Bit	Type	Label	Default	Description
R32 ID_6_7	3:0	R/W	LDO6_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	LDO7_STEP	0000	**Not controlled** by power sequencer

Table 80: ID_8_9

Register address	Bit	Type	Label	Default	Description
R33 ID_8_9	3:0	R/W	LDO8_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	LDO9_STEP	0000	**Not controlled** by power sequencer

Table 81: ID_10_11

Register address	Bit	Type	Label	Default	Description
R34 ID_10_11	3:0	R/W	LDO10_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	PD_DIS_STEP	0101	Power sequencer time **slot 5**

Table 82: ID_12_13

Register address	Bit	Type	Label	Default	Description
R35 ID_12_13	3:0	R/W	VPERICORE_SW_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	VMEM_SW_STEP	0000	**Not controlled** by power sequencer

Table 83: ID_14_15

Register address	Bit	Type	Label	Default	Description
R36 ID_14_15	3:0	R/W	BUCKCORE_STEP	0001	Power sequencer time **slot 1**
	7:4	R/W	BUCKPRO_STEP	0111	Power sequencer time **slot 7**

Table 84: ID_16_17

Register address	Bit	Type	Label	Default	Description
R37 ID_16_17	3:0	R/W	BUCKMEM_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	BUCKPERI_STEP	0000	**Not controlled** by power sequencer

Table 85: ID_18_19

Register address	Bit	Type	Label	Default	Description
R38 ID_18_19	3:0	R/W	GP_RISE1_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	GP_RISE2_STEP	0000	**Not controlled** by power sequencer

Table 86: ID_20_21

Register address	Bit	Type	Label	Default	Description
R39 ID_20_21	3:0	R/W	GP_FALL1_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	GP_FALL2_STEP	0000	**Not controlled** by power sequencer

Table 87: SEQ_STATUS

Register address	Bit	Type	Label	Default	Description
R40 SEQ_STATUS	3:0	R/W	WAIT_STEP	0000	**Not controlled** by power sequencer
	7:4	R/W	SEQ_POINTER	0000	Actual pointer position (time slot) of power sequencer

Table 88: SEQ_A

Register address	Bit	Type	Label	Default	Description
R41 SEQ_A	3:0	R/W	SYSTEM_END	0110	OTP pointer to last supply of domain SYSTEM
	7:4	R/W	POWER_END	1001	OTP pointer to last supply of domain POWER

Table 89: SEQ_B

Register address	Bit	Type	Label	Default	Description
R42 SEQ_B	3:0	R/W	MAX_COUNT	1001	OTP pointer to last supply of domain POWER1
	7:4	R/W	PART_DOWN	0100	OTP pointer for partial POWER-DOWN mode

Table 90: SEQ_TIMER

Register address	Bit	Type	Label	Default	Description
R43 SEQ_TIMER	3:0	R/W	SEQ_TIME	0011	0000: 32 µsec 0001: 64 µsec 0010: 96 µsec **0011: 128 µsec** 0100: 160 µsec 0101: 192 µsec 0110: 224 µsec 0111: 256 µsec 1000: 288 µsec 1001: 384 µsec 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms
	7:4	R/W	SEQ_DUMMY	0011	0000: 32 µs 0001: 64 µs 0010: 96 µs **0011: 128 µs** 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs

Register address	Bit	Type	Label	Default	Description
					1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms

20 Voltage Regulators

Three types of low dropout regulators are integrated on the DA9052, each optimized for performance depending on the most critical parameter of the circuitry supplied. For high performance analog supplies (for example, audio) the regulators have been designed to offer high PSRR and low noise, for the digital supplies PSRR is relaxed saving quiescent current and for the PMIC core/RTC supplies quiescent current has been optimized as the most important performance parameters. The regulators employ Dialog Semiconductor's SmartMirror™ dynamic biasing, removing the need for a low power operating mode and associated software or hardware overhead.

SmartMirror™ technology guarantees a high phase margin within the regulator control loop and has been designed to offer stable performance with small output capacitances over a wide range of output currents. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is also maintained across the full operating current range however quiescent current consumption is scaled to demand giving improved efficiency when current demand is low.

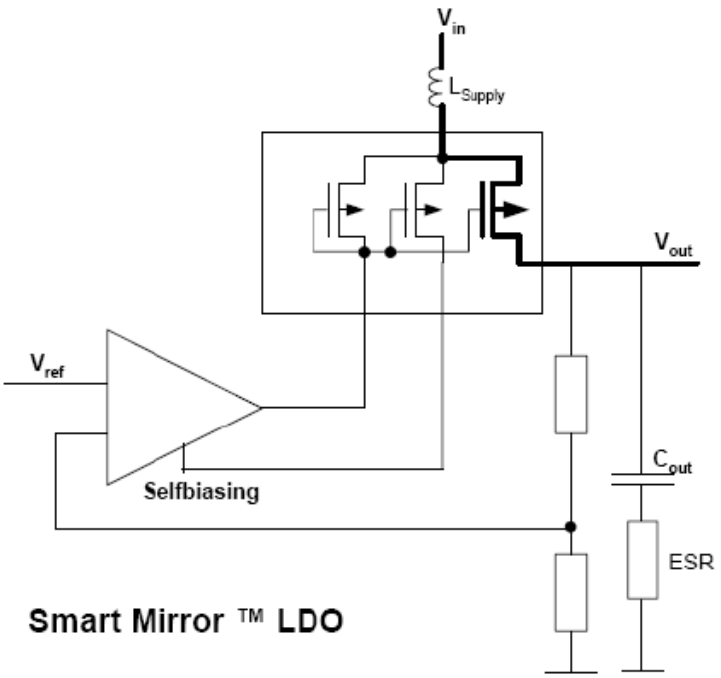


Figure 46: SmartMirror™ voltage regulator

The regulator output voltages are fully programmable via the control interface allowing optimization of the complete system for maximum performance and power efficiency. For security reasons the re-programming of output voltages from the control interfaces can be disabled. The default output voltage is loaded from after start-up from OTP. A power saving mode is not required for the LDOs due to the use of dynamic biasing in the LDO internal circuitry, so when operating at low current demands the quiescent current taken by the regulator is automatically minimized. LD01 to LDO10 can optionally be supplied from a buck output (VDD < 2.8 V). In this mode some specification parameters will change.

LDO1 to LDO10 can be controlled inside the power manager sequence. If enabled at sequencer step 0 (bit DEF_SUPPLY) supplies can be default enabled via OTP whenever the sequencer passes step 0 (OTP settings are used). To limit the battery rush current it is recommended to enable not more

than a single supply (including bucks) at step 0! When powering down (for example to POWER-DOWN mode) sequencer controlled supplies can be preconfigured with a new target voltage (LDOx_CONF bit is set). If LDOx_CONF was asserted in parallel with LDOx_EN also the supply enable is deferred until the sequencer is processing the related ID. The previous output voltage and enable state will be kept unchanged until the sequencer processes the related time slot/ID during powering down (ignoring any assertions of VLDOx_GO while LDOx_CONF is high). Before wakeup from POWER-DOWN mode (processing time slots from domain SYSTEM) the sequencer will configure all regulators with their default voltage values from OTP and by that also reset the LDOx_CONF bits. The regulators can also be enabled/disabled/configured via the power manager and HS-2-wire interface when the DA9052 is in the ACTIVE state. Voltage transitions on LDOs including DVC will always be ramped.

NOTE
Powering down to RESET mode will automatically disable all regulators beside LDO1.

LDO2 and LDO3 include dynamic DVC control to enable power savings on peripheral domains:

- The output voltage is programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.

The DVC control is handled by the following registers:

- Output voltage setting register VLDO2 and VLDO3 to configure the new target voltage
- Activate bit VLDO2_GO and VLDO3_GO will implement the changes on the LDO output (also used from the sequencer for deferred voltage changes). After being started DA9052 will block (not accept any re-programming of) the related voltage setting registers until slewing has been finished. If selected the READY signal will be asserted during ramping.

LDO4, LDO5 and LDO9 include an optional hardware enable/disable via GPIO1, GPIO2 and GPIO12 by selecting the GPI feature with ‘debouncing off’. After detecting an E_GPI1, E_GPI2 or E_GPI12 event DA9052 will configure LDO4_EN, LDO5_EN or LDO9_EN by the status of GPI1, GPI2 or GPI9 and the event bit E_GPI1, E_GPI2 or E_GPI12 is automatically cleared. A parallel write access to LDO4_EN, LDO5_EN or LDO9_EN from the control interfaces or the power sequencer is delayed and will later override the hardware configuration.

NOTE
It is recommended to assert the IRQ mask bit of GPIOs, which are configured for LDO hardware control, to prevent the host being disturbed by IRQ strobes from the automatically cleared events.

Disabling regulators LDO1, LDO2 and LDO5 can switch off their pull down resistor, which is required for usage in parallel to an alternate supply.

20.1 DA9052 core regulator LDOCORE

The LDOCORE will be used for running the DA9052 internal Real Time Clock module, internal state machine, GPIO pins with comparators, bias, reference, GPADC, OTP and power manager registers. It is supplied by the battery switch either from an external supply, VBAT or the backup battery (coin cell or super cap). If no backup battery exists or the backup battery charger is configured to a level below 2.0 V the automatic VDDREF switch to the backup battery can be disabled.

21 DC/DC buck converters

DA9052 includes four DC/DC buck converters, three with DVC (Dynamic voltage control) and one with fixed output voltage (programmable from OTP). The output voltages are fully programmable via the control interface allowing optimization of the complete system for maximum performance and power efficiency. For security reasons the re-programming of output voltages from the control interfaces can be disabled via control V_LOCK.

NOTE
Powering down to RESET mode will automatically disable all buck converters.

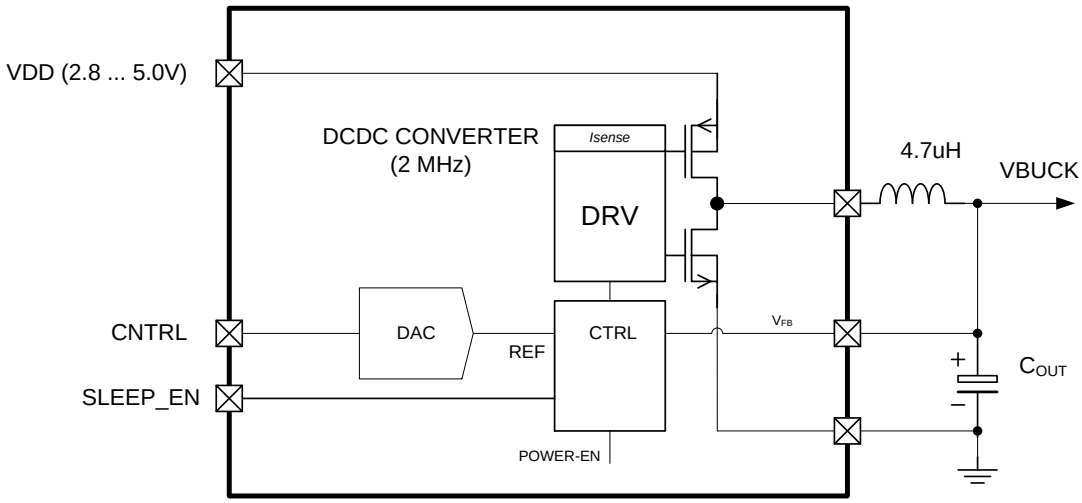


Figure 47: DCDC buck converter

21.1 Converters BUCKCORE, BUCKPRO and BUCKMEM with DVC

These converters are high efficiency synchronous step down regulators operating at a high frequency (2 MHz) supplying individual output voltages with +/- 3 % accuracy. Default output voltage is loaded from OTP and can be set in 25 mV steps.

The DVC controller allows the following features:

- The buck converter output voltage to be programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.
- Output voltages below 0.725 V will only be supported in pulse frequency modulation (PFM) mode. During a voltage reduction below 0.725 V the slew rate control ends at 0.725 V and the buck mode is automatically changed to sleep mode (with reduced maximum current capability). The timing of voltage transitions between 0.5 V and 0.725 V depends on the load.

The DVC control is handled by the following registers:

- Output voltage setting register VBCORE, VBPRO and VBMEM to configure the new target voltage
- Activate bit VB_CORE_GO, VB_PRO_GO and VB_MEM_GO will implement the changes at the buck output (also used from the sequencer for deferred voltage changes). After being started DA9052 will block (not accept any re-programming of) the related voltage setting registers until slewing has been finished. If selected the READY signal will be asserted during ramping.

The supply current during PWM (synchronous rectification) operation is in the order of 2.2 mA (quiescent current and charge/discharge current) and drops to <1 µA in shutdown. Switching frequency is chosen to be high enough to allow the use of a small 4.7 µH inductor.

The operating mode of the buck converter is selected via the buck control register bits. The buck converter can be forced to operate in either Synchronous mode or Sleep mode. Additionally the buck converter has an automatic mode where it will switch between Synchronous and Sleep modes depending on the load current. In Sleep mode the buck converter works in PFM mode. An internal zero crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode.

All buck converters can be controlled via an ID from the power manager sequencer. If enabled at sequencer step 0 (bit DEF_SUPPLY) buck converters can be default enabled via OTP whenever the sequencer passes step 0 (OTP default settings are used). To limit the battery rush current it is recommended to enable not more than a single supply (including LDOs) at step 0! During powering down supplies can be preconfigured with a new target value (Bxxx_CONF bit is set). If Bxxx_CONF was asserted in parallel with BUCKx_EN also the supply enable is deferred until the sequencer is processing the related ID. The output voltage and enable state will be kept unchanged until the sequencer processes the related time slot/ID during powering down (ignoring any assertions of VB_xxx_GO while Bxxx_CONF is high). When powering up from POWER-DOWN mode (processing time slots in domain SYSTEM) the sequencer will configure bucks with their default voltage values from OTP and by that reset the BUCKxxx_CONF bits. The bucks can also be enabled/disabled/configured via the power manager and HS-2-wire interface when the DA9052 is in the ACTIVE state. Voltage transitions on bucks including DVC will always be ramped. Disabled bucks BUCKCORE, BUCKPRO and BUCKMEM can switch off their pull down resistor (required for usage in parallel to an alternate supply).

NOTE
Powering down to RESET mode will automatically disable all buck converters.

The converters BUCKPERI and BUCKMEM provide additional power path switches that can be controlled from the sequencer. This enables a partial power down of IO and power rails for optimized application quiescent currents during standby/hibernate modes. The embedded soft start (approx. 200 µs) enables a usage as power manager controlled hot swap power switches with a maximum capacitive load up to 10 µF (for example for SD-cards). If a switch is open, the associated pin will be discharged to VSS by a pull down resistor.

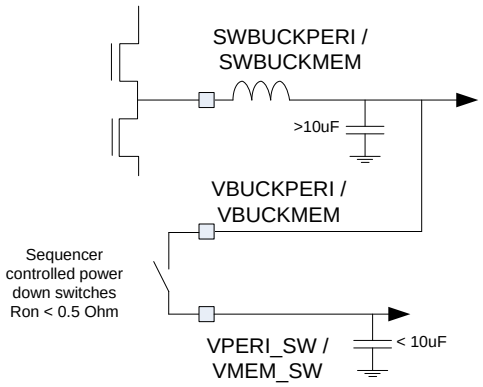


Figure 48: BUCKCORE / BUCKMEM output switches

The converter BUCKCORE can additionally be merged with BUCKPRO towards a single DCDC converter with a maximum output current of 1.4 A. The routing of the switcher output pins towards the common inductor has to be symmetrical and the feedback signal VBUCKPRO should be connected to GND (if PRO_PD_DIS is asserted VBUCKCORE can alternatively be connected to

VBUCKCORE). The inductor and the output capacitor have to be selected according to the intended increased output current. Please notice that configuration controls of BUCKPRO are automatically disabled by asserting the bit BUCK_MERGE and the selected current limits of BUCKCORE will be automatically doubled.

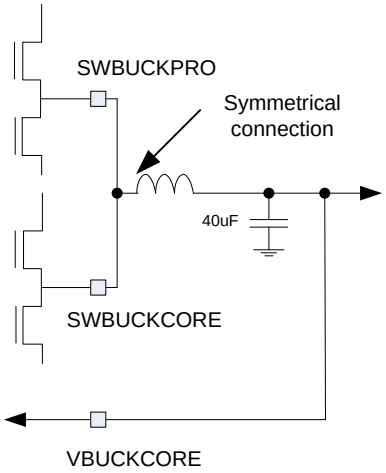


Figure 49: BUCKCORE merged with BUCKPRO

21.2 Converter BUCKPERI with OTP programmable output voltage and bypass mode

The BUCKPERI Converter is a high efficiency synchronous step down regulator operating at a high frequency (2 MHz). The default output voltage is loaded from OTP and can be set from 1.8 V - 3.6V in 50/100 mV steps.

NOTE
Changes of the output voltage have to be executed in DISABLED mode as this regulator does not offer DVC.

The supply current during PWM operation is in the order of 3 mA (quiescent current and charge/discharge current) and drops to <1 µA in shutdown. Switching frequency is chosen to be high enough to allow the use of a small 4.7 µH inductor.

The buck converter can be forced to operate in either Synchronous mode or Sleep mode. Additionally the buck converter has an automatic mode where it will switch between Synchronous and Sleep mode depending on the load current. If the application requires a fast transition from Synchronous to Automatic mode it is recommended to use the ‘Automatic forcing to Synchronous mode’, because it already prepares the control signal that will be required in the later Automatic mode. In Sleep mode, the buck converter works in PFM mode. An internal zero crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode.

If reduced output power is required for improved efficiency it can run with a smaller pass device. BUCKPERI is able to operate up to a duty cycle of 100 %, where a by-pass switch across the coil will be enabled to prevent L-C-oscillations introduced by load-current spikes.

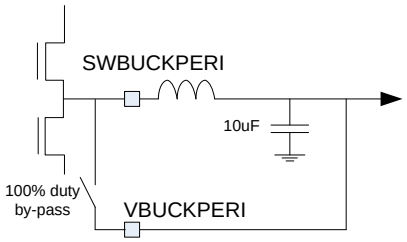


Figure 50: BUCKPERI bypass mode

Table 91: Selection of buck current limit from coil parameters

Min. ISAT (mA)	Frequency (MHz)	Buck current limit (mA)
1450	2	1200
1200	2	1000
960	2	800
840	2	700

21.3 Supplies

Table 92: BUCK_A

Register address	Bit	Type	Label	Default	Description
R44 BUCK_A	1:0	R/W	BCORE_MODE	01	00: BUCKCORE always operates in Sleep mode **01: BUCKCORE operates in Automatic mode** 10: BUCKCORE always operates in Synchronous mode 11: BUCKCORE in Automatic forcing to Synchronous mode
	3:2	R/W	BCORE_ILIM	10	00: BUCKCORE current limit 700 mA (1400 mA in merged mode) 01: BUCKCORE current limit 800 mA (1600 mA in merged mode) **10: BUCKCORE current limit 1000 mA (2000 mA in merged mode)** 11: BUCKCORE current limit 1200 mA (2400 mA in merged mode)
	5:4	R/W	BPRO_MODE	01	00: BUCKPRO always operates in Sleep mode **01: BUCKPRO operates in Automatic mode** 10: BUCKPRO always operates in Synchronous mode 11: BUCKPRO in Automatic forcing to Synchronous mode
	7:6	R/W	BPRO_ILIM	10	00: BUCKPRO current limit 700 mA 01: BUCKPRO current limit 800 mA **10: BUCKPRO current limit 1000 mA** 11: BUCKPRO current limit 1200 mA

Table 93: BUCK_B

Register address	Bit	Type	Label	Default	Description
R45 BUCK_B	0:1	R/W	BMEM_ MODE	01	00: BUCKMEM always operates in Sleep mode **01: BUCKMEM operates in Automatic mode** 10: BUCKMEM always operates in Synchronous mode 11: BUCKMEM in Automatic forcing to Synchronous mode
	2:3	R/W	BMEM_ILIM	10	00: BUCKMEM current limit 700 mA 01: BUCKMEM current limit 800 mA **10: BUCKMEM current limit 1000 mA** 11: BUCKMEM current limit 1200 mA
	4:5	R/W	BPERI_ MODE	01	00: BUCKPERI always operates in Sleep mode **01: BUCKPERI operates in Automatic mode** 10: BUCKPERI always operates in Synchronous mode 11: BUCKPERI in Automatic forcing to Synchronous mode
	7:6	R/W	BPERI_ILIM	10	00: BUCKPERI current limit 700 mA 01: BUCKPERI current limit 800 mA **10: BUCKPERI current limit 1000 mA** 11: BUCKPERI current limit 1200 mA

Table 94: BUCKCORE

Register address	Bit	Type	Label	Default	Description
R46 BUCKCORE	5:0	R/W	VBCORE	110100	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V … 011011: 1.175 V 011100: 1.200 V 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V

Register address	Bit	Type	Label	Default	Description
					100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V 101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V 110010: 1.750 V 110011: 1.775 V **110100: 1.800 V** 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V 111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BCORE_EN	0	**0: BUCKCORE disabled** 1: BUCKCORE enabled
	7	R/W	BCORE_CONF	0	**0: Voltage ramped after assertion of VB_CORE_GO** 1: Supply voltage preset

Table 95: BUCKPRO

Register address	Bit	Type	Label	Default	Description
R47 BUCKPRO	5:0	R/W	VBPRO	011100	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V …

Register address	Bit	Type	Label	Default	Description
					011011: 1.175 V **011100: 1.200 V** 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V 100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V 101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V 110010: 1.750 V 110011: 1.775 V 110100: 1.800 V 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V 111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BPRO_EN	**0**	**0: BUCKPRO disabled** 1: BUCK PRO enabled
	7	R/W	BPRO_CONF	0	**0: Voltage ramped after assertion of VB_PRO_GO** 1: Supply voltage preset

Table 96: BUCKMEM

Register address	Bit	Type	Label	Default	Description
R48 BUCKMEM	5:0	R/W	VBMEM	101011	000000: 0.950 V 000001: 0.975 V 000010: 1.000 V 000011: 1.025 V 000100: 1.050 V … 010110: 1.500 V 010111: 1.525 V 011000: 1.550 V 011001: 1.575 V 011010: 1.600 V 011011: 1.625 V 011100: 1.650 V 011101: 1.675 V 011110: 1.700 V 011111: 1.725 V 100000: 1.750 V 100001: 1.775 V 100010: 1.800 V 100011: 1.825 V 100100: 1.850 V 100101: 1.875 V 100110: 1.900 V 100111: 1.925 V 101000: 1.950 V 101001: 1.975 V 101010: 2.000 V **101011: 2.025 V** 101100: 2.050 V 101101: 2.075 V 101110: 2.100 V 101111: 2.125 V 110000: 2.150 V 110001: 2.175 V 110010: 2.200 V 110011: 2.225 V 110100: 2.250 V 110101: 2.275 V 110110: 2.300 V 110111: 2.325 V 111000: 2.350 V 111001: 2.375 V 111010: 2.400 V

Register address	Bit	Type	Label	Default	Description
					111011: 2.425 V 111100: 2.450 V 111101: 2.475 V 111110: 2.500 V 111111: 2.525 V
	6	R/W	BMEM_EN	0	**0: BUCKMEM disabled** 1: BUCKMEM enabled
	7	R/W	BMEM_CONF	0	**0: Voltage ramped after assertion of VB_MEM_GO** 1: Supply voltage preset

Table 97: BUCKPERI

Register address	Bit	Type	Label	Default	Description
R49 BUCKPERI	4:0	R/W	VBPERI	11011	00000: 1.8 V 00001: 1.85 V 00010: 1.9 V 00011: 1.95 V 00100: 2.0 V 00101: 2.05 V 00110: 2.1 V 00111: 2.15 V 01000: 2.2 V 01001: 2.25 V 01010: 2.3 V 01011: 2.35 V 01100: 2.4 V 01101: 2.45 V 01110: 2.5 V 01111: 2.55 V 10000: 2.6 V 10001: 2.65 V 10010: 2.7 V 10011: 2.75 V 10100: 2.8 V 10101: 2.85 V 10110: 2.9 V 10111: 2.95 V 11000: 3.0 V 11001: 3.1 V 11010: 3.2 V **11011: 3.3 V** 11100: 3.4 V 11101: 3.5 V

Register address	Bit	Type	Label	Default	Description
					11110: 3.6 V >11110: 3.6 V
	5	R/W	BPERI_HS	0	0: BUCK_PERI PMOS pass device is full size 1: BUCK_PERI PMOS pass device is half size
	6	R	BPERI_EN	0	**0: BUCKPERI disabled** 1: BUCKPERI enabled
	7	R/W	BPERI_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 98: LDO1

Register address	Bit	Type	Label	Default	Description
R50 LDO1	4:0	R/W	VLDO1	01100	00000: 0.600 V 00001: 0.650 V 00010: 0.700 V 00011: 0.750 V 00100: 0.800 V 00101: 0.850 V 00110: 0.900 V 00111: 0.950 V 01000: 1.000 V 01001: 1.050 V 01010: 1.100 V 01011: 1.150 V **01100: 1.200 V** 01101: 1.250 V 01110: 1.300 V 01111: 1.350 V 10000: 1.400 V 10001: 1.450 V 10010: 1.500 V 10011: 1.550 V 10100: 1.600 V 10101: 1.650 V 10110: 1.700 V 10111: 1.750 V 11000: 1.800 V >11000: 1.800 V
	5	R		0	
	6	R/W	LDO1_EN	0	**0: LDO1 disabled** 1: LDO1 enabled

Register address	Bit	Type	Label	Default	Description
	7	R/W	LDO1_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 99: LDO2

Register address	Bit	Type	Label	Default	Description
R51 LDO2	5:0	R/W	VLDO2	011000	000000: 0.600 V 000001: 0.625 V 000010: 0.650 V 000011: 0.675 V 000100: 0.700 V 000101: 0.725 V 000110: 0.750 V 000111: 0.775 V 001000: 0.800 V 001001: 0.825 V 001010: 0.850 V 001011: 0.875 V 001100: 0.900 V 001101: 0.925 V 001110: 0.950 V 001111: 0.975 V 010000: 1.000 V 010001: 1.025 V 010010: 1.050 V 010011: 1.075 V 010100: 1.100 V 010101: 1.125 V 010110: 1.150 V 010111: 1.175 V **011000: 1.200 V** 011001: 1.225 V 011010: 1.250 V 011011: 1.275 V 011100: 1.300 V 011101: 1.325 V 011110: 1.350 V 011111: 1.375 V 100000: 1.400 V 100001: 1.425 V 100010: 1.450 V 100011: 1.475 V 100100: 1.500 V

Register address	Bit	Type	Label	Default	Description
					100101: 1.525 V 100110: 1.550 V 100111: 1.575 V 101000: 1.600 V 101001: 1.625 V 101010: 1.650 V 101011: 1.675 V 101100: 1.700 V 101101: 1.725 V 101110: 1.750 V 101111: 1.775 V 110000: 1.800 V >110000: 1.800 V
	6	R/W	LDO2_EN	0	**0: LDO2 disabled** 1: LDO2 enabled
	7	R/W	LDO2_CONF	0	**0: Voltage ramped after assertion of VLDO2_GO** 1: Supply voltage preset (ramping activated during power down)

Table 100: LDO3

Register address	Bit	Type	Label	Default	Description
R52 LDO3	5:0	R/W	VLDO3	101101	000000: 1.725 V 000001: 1.750 V 000010: 1.775 V 000011: 1.800 V 000100: 1.825 V … 010110: 2.275 V 010111: 2.300 V 011000: 2.325 V 011001: 2.350 V 011010: 2.375 V 011011: 2.400 V 011100: 2.425 V 011101: 2.450 V 011110: 2.475 V 011111: 2.500 V 100000: 2.525 V 100001: 2.550 V 100010: 2.575 V 100011: 2.600 V 100100: 2.625 V

Register address	Bit	Type	Label	Default	Description
					100101: 2.650 V 100110: 2.675 V 100111: 2.700 V 101000: 2.725 V 101001: 2.750 V 101010: 2.775 V 101011: 2.800 V 101100: 2.825 V **101101: 2.850 V** 101110: 2.875 V 101111: 2.900 V 110000: 2.925 V 110001: 2.950 V 110010: 2.975 V 110011: 3.000 V 110100: 3.025 V 110101: 3.050 V 110110: 3.075 V 110111: 3.100 V 111000: 3.125 V 111001: 3.150 V 111010: 3.175 V 111011: 3.200 V 111100: 3.225 V 111101: 3.250 V 111110: 3.275 V 111111: 3.300 V
	6	R/W	LDO3_EN	0	**0: LDO3 disabled** 1: LDO3 enabled
	7	R/W	LDO3_CONF	0	**0: Voltage ramped after assertion of VLDO3_GO** 1: Supply voltage preset

Table 101: LDO4

Register address	Bit	Type	Label	Default	Description
R53 LDO4	5:0	R/W	VLDO4	101101	000000: 1.725 V 000001: 1.750 V 000010: 1.775 V 000011: 1.800 V 000100: 1.825 V … 010110: 2.275 V 010111: 2.300 V

Register address	Bit	Type	Label	Default	Description
					011000: 2.325 V 011001: 2.350 V 011010: 2.375 V 011011: 2.400 V 011100: 2.425 V 011101: 2.450 V 011110: 2.475 V 011111: 2.500 V 100000: 2.525 V 100001: 2.550 V 100010: 2.575 V 100011: 2.600 V 100100: 2.625 V 100101: 2.650 V 100110: 2.675 V 100111: 2.700 V 101000: 2.725 V 101001: 2.750 V 101010: 2.775 V 101011: 2.800 V 101100: 2.825 V **101101: 2.850 V** 101110: 2.875 V 101111: 2.900 V 110000: 2.925 V 110001: 2.950 V 110010: 2.975 V 110011: 3.000 V 110100: 3.025 V 110101: 3.050 V 110110: 3.075 V 110111: 3.100 V 111000: 3.125 V 111001: 3.150 V 111010: 3.175 V 111011: 3.200 V 111100: 3.225 V 111101: 3.250 V 111110: 3.275 V 111111: 3.300 V
	6	R/W	LDO4_EN	0	**0: LDO4 disabled** 1: LDO4 enabled

Register address	Bit	Type	Label	Default	Description
	7	R/W	LDO4_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 102: LDO5

Register address	Bit	Type	Label	Default	Description
R54 LDO5	5:0	R/W	VLDO5	100110	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V

Register address	Bit	Type	Label	Default	Description
					100101: 3.05 V **100110: 3.10 V** 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO5_EN	0	**0: LDO5 disabled** 1: LDO5 enabled
	7	R/W	LDO5_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 103: LDO6

Register address	Bit	Type	Label	Default	Description
R55 LDO6	5:0	R/W	VLDO6	000110	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V **000110: 1.50 V** 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V

Register address	Bit	Type	Label	Default	Description
					010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO6_EN	0	**0: LDO6 disabled** 1: LDO6 enabled
	7	R/W	LDO6_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 104: LDO7

Register address	Bit	Type	Label	Default	Description
R56 LDO7	5:0	R/W	VLDO7	001100	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V

Register address	Bit	Type	Label	Default	Description
					000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V **001100: 1.80 V** 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V

Register address	Bit	Type	Label	Default	Description
	6	R/W	LDO7_EN	0	**0: LDO7 disabled** 1: LDO7 enabled
	7	R/W	LDO7_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 105: LDO8

Register address	Bit	Type	Label	Default	Description
R57 LDO8	5:0	R/W	VLDO8	001100	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V **001100: 1.80 V** 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V

Register address	Bit	Type	Label	Default	Description
					100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO8_EN	0	**0: LDO8 disabled** 1: LDO8 enabled
	7	R/W	LDO8_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 106: LDO9

Register address	Bit	Type	Label	Default	Description
R58 LDO9	5:0	R/W	VLDO9	011001	000000: 1.25 V 000001: 1.30 V 000010: 1.35 V 000011: 1.40 V 000100: 1.45 V 000101: 1.50 V 000110: 1.55 V 000111: 1.60 V 001000: 1.66 V 001001: 1.70 V 001010: 1.75 V 001011: 1.80 V 001100: 1.85 V 001101: 1.90 V 001110: 1.95 V 001111: 2.00 V 010000: 2.05 V 010001: 2.10 V 010010: 2.15 V 010011: 2.20 V

Register address	Bit	Type	Label	Default	Description
					010100: 2.25 V 010101: 2.30 V 010110: 2.35 V 010111: 2.40 V 011000: 2.45 V **011001: 2.50 V** 011010: 2.55 V 011011: 2.60 V 011100: 2.65 V 011101: 2.70 V 011110: 2.75 V 011111: 2.80 V 100000: 2.85 V 100001: 2.90 V 100010: 2.95 V 100011: 3.00 V 100100: 3.05 V 100101: 3.10 V 100110: 3.15 V 100111: 3.20 V 101000: 3.25 V 101001: 3.30 V 101010: 3.35 V 101011: 3.40 V 101100: 3.45 V 101101: 3.50 V 101110: 3.55 V 101111: 3.60 V 110000: 3.65 V >110000: 3.65 V
	6	R/W	LDO9_EN	0	**0: LDO9 disabled** 1: LDO9 enabled
	7	R/W	LDO9_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 107: LDO10

Register address	Bit	Type	Label	Default	Description
R59 LDO10	5:0	R/W	VLDO10	100001	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V **100001: 2.85 V** 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V

Register address	Bit	Type	Label	Default	Description
					101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO10_EN	0	**0: LDO10 disabled** 1: LDO10 enabled
	7	R/W	LDO10_CONF	0	**0: Supply voltage immediate change** 1: Supply voltage preset (activated during power down sequence instead of disable)

Table 108: SUPPLY

Register address	Bit	Type	Label	Default	Description
R60 SUPPLY	0	R/W	VB_CORE_GO	0	**0: Hold VBUCKCORE at current setting.** 1: Ramp BUCKCORE to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKCORE_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	1	R/W	VB_PRO_GO	0	**0: Hold VBUCKPRO at current setting.** 1: Ramp BUCKPRO to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKPRO_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	2	R/W	VB_MEM_GO	0	**0: Hold VBUCKMEM at current setting.** 1: Ramp BUCKMEM to configured voltage. While the voltage is ramping, write access is blocked to BUCKMEM register. VBUCKMEM_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM

Register address	Bit	Type	Label	Default	Description
	3	R/W	VLDO2_GO	0	**0: Hold LDO2 at current setting.** 1: Ramp LDO2 to configured voltage. While the voltage is ramping, write access is blocked to LDO2 register. VLDO2_GO is cleared when the target voltage is reached (ignored if LDO2_CONF was asserted)
	4	R/W	VLDO3_GO	0	**0: Hold VLDO3 at current setting.** 1: Ramp VLDO3 to configured voltage. While the voltage is ramping, write access is blocked to LDO3 register. VLDO3_GO is cleared when the target voltage is reached (ignored if LDO3_CONF was asserted)
	5	R/W	VCOREVPERI_SW_EN	1	0: Disconnects VPERICORE_SW pin from buck **1: VPERICORE_SW closed (controllable from sequencer)**
	6	R/W	VMEM_SW_EN	1	0: Disconnects VMEM_SW pin from buck **1: VMEM_SW closed (controllable from sequencer)**
	7	R/W	V_LOCK	0	**0: Allows writing new values into buck and LDO voltage registers** 1: Disables voltage re-programming from the host (enable/disable, DVC ramping, power sequencing including deferred update still possible)

Table 109: PULLDOWN

Register address	Bit	Type	Label	Default	Description
R61 PULLDOWN	0	R/W	CORE_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	1	R/W	PRO_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	2	R/W	MEM_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	3	R/W	LDO1_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	4	R/W	LDO2_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	5	R/W	LDO5_PD_DIS	0	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	7:6	R/W		00	

22 Programmable battery charger

The system power and charger control block contains the following functions:

- 3-way power path switch with automatic selection of the system power source (VDDOUT) from either the wall charger DCIN, VBUS or VBAT with preference given to DCIN. Battery disconnection switch to allow instant-on system start-up with discharged main battery.
- Embedded active diode plus external active diode controller provide a low loss power path seamless switching in whenever input power is limited or unavailable
- VBAT tracking switching regulator supplying system power out of USB port and wall charger with an efficiency > 85 % @ 1000 mA load current
- Full featured autonomous Li-Ion/Polymer battery charger with pre-configurable current limits and programmable EOC voltages (4.1 V to 4.4 V), current monitoring (always active when charger is on) and OTP programmable EOC currents. Integrated control over battery pre-charge (including battery pack wakeup), constant-current (CC) and constant-voltage (CV) charging phases.
- Automatic charge current reduction via dynamic charger current control (DCCC), maintaining VDDOUT system power at minimum 3.5 V without exceeding the supply current limits. Individual programmable current limits for the USB and DCIN supply input.
- Automatic USB Battery Charging Specification Rev.1.0 compliant charger type detection, USB Suspend mode support
- Battery temperature qualified charging (using GP-ADC) with default threshold settings loaded from OTP
- Battery charging termination by current (using GP-ADC) with default threshold setting loaded from OTP
- Extended battery life by protection against continuous top charging (configurable re-charge hysteresis)
- Thermal limiting of charge current by IC temperature (using GP-ADC)
- Programmable charge termination by timer for safety

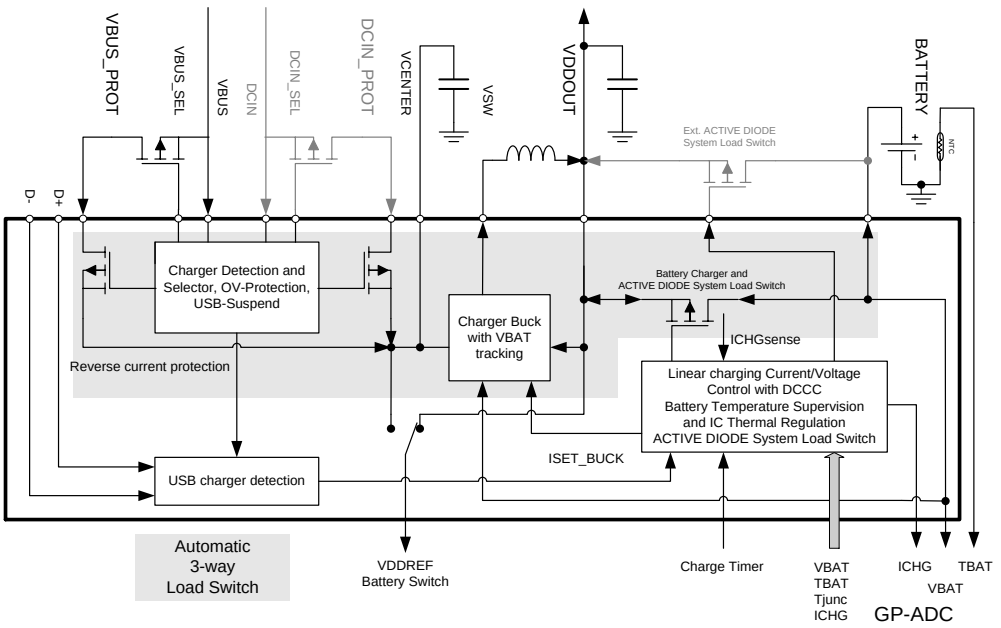


Figure 51: Charger block diagram

22.1 High efficiency charger DC-DC buck converter

In order to minimize the total system power loss at high input currents, DA9052's main system power VDDOUT is supplied out of a high efficient DCDC converter, which is able to track VBAT+200 mV (with minimum VDDOUT = 3.6 V).

When powering up VDDOUT the DC-DC converter provides a soft-start circuitry and the current limit is implemented to meet the USB 2.0 specification for currents spikes where charge peaks are always less than an equivalent bypass capacitive load of 10 µF. An integrated overvoltage protection and supply selection controls the behavior of these power paths.

The buck converter operates at a high frequency (2 MHz). This switching frequency is chosen to be high enough to allow the use of a small 4.7 µH inductor. To guarantee high efficiency at high load currents the series resistance of the coil is limited to 100 mΩ (at 1000 mA). Under light load conditions the buck converter can be forced by the host to a low current PFM mode.

22.2 Charger supply detection/VBUS monitoring

DA9052 provides a dual mode charger input VBUS, which can be supplied either from a USB host/hub, a USB type host/hub charger or a dedicated wall charger. To protect DA9052 against destruction from invalid supplies an overvoltage protection circuitry will disconnect every charger that supplies more than 5.6 V.

At the VBUS input a connected USB 2.0 compliant host/hub will supply 5 V and is able to provide maximum 100 mA whenever it is operational. A dedicated wall charger or USB host/hub charger has to be differentiated from a USB host/hub because it usually provides charging currents greater 100 mA. DA9052 has therefore a built-in circuitry to detect the attached charger type at VBUS. For a dedicated charger DA9052 has to detect a short between D+ and D- (with a maximum resistance of 200 Ω). From then on the USB charger specification allows the connected charger to charge the device with a current up to 1500 mA. If alternatively the voltage on D- was detected to be less than VDAT_REF (0.25 V to 0.4 V) DA9052 will keep the current limit at 100 mA.

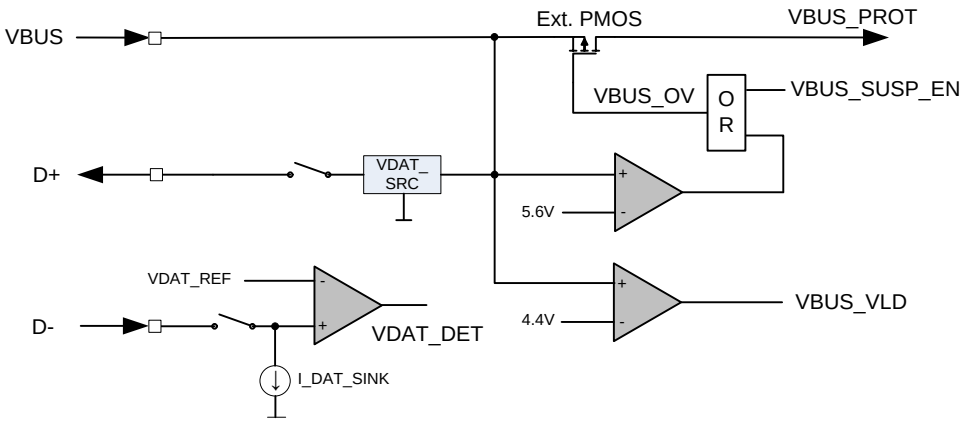


Figure 52: USB charger detection

In addition to the combined charger input VBUS DA9052 provides a second charger input DCIN that allows a wall charger to be connected in parallel. This supply will receive priority as soon as it is detected. VCENTER will then be connected to DCIN.

NOTE
The configured default maximum current values have to allow the application being powered completely from the external supply (in the case of a deep discharged battery) but at the same time have to secure that all potential chargers are able to provide the automatically selected maximum average current.

The charger initial insertion is detected when the voltage comparators indicate that VBUS_PROT/DCIN_PROT is still present after a debounce time of 10 ms. At this time the charger buck converter will be enabled via a soft start up to the appropriate current limitation (see above) if the chargers attach comparator flags with enough voltage headroom from VDDOUT to VCENTER to allow the buck converter to operate. The battery is disconnected from VDDOUT as the charger supply takes over. This is done by enabling an active diode function as part of the battery P-FET, giving a clean transfer of power.

The differential charger attach comparator (CHG_ATT) detects a typical drop of 100 mV across VCENTER to VDDOUT and acts together with the charge detection comparators as an under voltage lock out, which is performed in two phases. In the first phase a falling voltage at the charger input (DCIN or VBUS) towards VCH_THR will force the charger buck state machine to reduce the charger buck current limitation step by step down to its minimum value. If the input voltage will not recover and the CHG_ATT comparator flags a voltage drop from VCENTER to VDDOUT is below 85 mV, the charger buck is disabled as soon the current limit reaches its minimum value. If the input voltage will recover, the state machine starts increasing the current limit again until it reaches its programmed value using a slow attach time.

If during normal operation the CHG_DET signals a valid input voltage, but the CHG_ATT comparator flags a low drop across VCENTER to VDDOUT, the buck current limit is ramped down in the same way as mentioned before. The charger buck will be disabled if the voltage drop across VCENTER to VDDOUT will not rise towards a minimum of 100 mV.

NOTE
CHG_DET is either DCIN_DET or VBUS_DET depending on the selected charger source.

22.3 VBUS overvoltage protection and USB suspend

DA9052 includes an over-voltage protection circuit that disconnects VBUS or DCIN from the VBUS_PROT/DCIN_PROT inputs via the external P-FETs whenever the VBUS/DCIN voltage is above the VCHG_EXCESS threshold. If both inputs are connected to valid supplies DCIN will receive priority and VBUS will be disconnected via the P-FET. This circuit supports a USB low power suspend mode enabled via the control bit VBUS_SUSP where the VBUS_PROT path is switched off and the VDD_OUT main supply is switched to the battery disabling charging (similar to removing the VBUS supply). VBUS_SUSP is cleared when the USB charger is removed. DCIN_PROT may also be temporally disconnected via DCIN_SUSP register bit. This function has a similar behavior to VBUS_SUSP. DA9052 supports in addition a BUS powered low current mode which is enabled via control bit CHG_BUCK_LP. In this mode the charger buck is forced to a PFM mode to ensure the system is backed up with minimum power dissipation when being supplied from an external supply. Charging will be suspended, but (with appropriate configurations of the regulators) power to, for example, an idle USB PHY can be supplied (USB high power suspend mode allows maximum 2.5 mA).

NOTE
Circuit layout is critical to avoid low levels of back powering during suspend mode when a DC charger is connected. The VCENTER decoupling capacitor must be fitted as close as possible to the IC to minimize this effect and be fully USB2.0 compliant. With some layouts it may sometimes be necessary to add a resistor (around 5 kΩ)between VBUS_PROT and GND.

Monitoring of the VBUS/DCIN voltage is always provided, allowing the host processor to detect a removal of the VBUS also in suspend mode (see DCIN/VBUS status bits).

The removal of supplies will issue E_DCIN_REM/E_VBUS_REM interrupt requests and trigger a wakeup in POWER-DOWN mode if is still present after a debounce time of 10 ms. Removing DCIN will automatically clear DCIN_SUSP, removing VBUS will clear VBUS_SUSP and removing the active supply also CHG_BUCK_LP is cleared.

22.4 Battery pre-charge mode

Battery PRE-CHARGE mode is started and controlled automatically by DA9052. This is needed to ensure that a completely empty battery can be charged without the intervention of the host processor. In the event of a heavily discharged battery the battery is disconnected from the VDDOUT supply so that the system may be started. The charger then powers the VDDOUT rail from one of the supply paths as described above, allowing the LDOs and buck converter to be switched on.

PRE-CHARGE mode is started when a charger has been detected and the VDDOUT voltage is greater than VBAT + 200 mV (or > 3.6 V). The PRE-CHARGE mode also handles the re-enable of a battery pack which has an internal safety switch been opened (from deep discharge). The safety switch will be reset by applying a current through the diode in the safety switch, charging the battery cell up to about 2.8 V where the switch will be closed again. DA9052 can optionally drive a flashing LED at GPIO 10 or 11 that will indicate the invisible battery charging until the application is able to power up.

Charging is suspended by writing 0 mA to ICHG_PRE in PRE-CHARGE mode.

22.5 Fast linear-charge mode

Battery LINEAR-CHARGE mode is initiated automatically once the battery voltage has exceeded the BAT_FAULT threshold for a minimum of 40 ms (to allow a battery safety switch to close)

The linear charge mode has two phases of operation:

- Constant current (CC) mode.
- Constant voltage (CV) mode.

If the battery voltage (VBAT) is less than the target voltage, the charging starts in CC mode.

Temperature supervision of the battery by the GP-ADC channel 2 is started and charging is only allowed if the battery temperature is in the correct range. If a TBAT fault condition is detected while charging the battery, charging will be suspend until the battery temperature is back in the correct range, except in the case that the charging end point has been reached.

The CC mode has 64 possible current settings ranging from 20 mA to 1260 mA, controllable by the host processor via the power manager bus. When the battery voltage approaches the target regulation voltage level the charger control loop changes over to CV mode.

NOTE
The CC and CV mode actually operate in parallel, with the CC loop limiting the charging current and the CV loop limiting the charging voltage.

The charging current will be measured automatically by the GP-ADC, generating an average current reading over a 10 s period that will be used to determine the charging end point detection. This allows for flexibility in determining when to automatically stop charging for different sizes and types of battery.

22.6 Thermal charge current control

During charging the temperature of DA9052 (Tjunc) is continuously supervised by the GP-ADC against overheating. A thermal supervision circuit reduces the charge current via a current/temperature control whenever the die temperature attempts to rise above a preset value of TCHARGELOW (90 °C). It completely suspends charging when TCHARGESUSPEND (120 °C) has been reached. This protects DA9052 from excessive temperature but allows the application to push the limits of the power handling capability of a given circuit board without risk of damage. Another benefit of the thermal limit is that the charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Whenever the junction temperature (Tjunc, see chapter GP-ADC) overrides a threshold from below table the thermal control will raise the (internal) temperature class and reduce the battery charge current limit towards the related value. It will increase the charge current limit only if the temperature drops below the threshold of the actual class 1. This prohibits a continuous change of the charging current around a temperature threshold.

The thermal charge current control can be disabled but this will increase the risk for a complete thermal shutdown from the internal temperature supervision inside high power applications.

Table 110: Thermal charge current control

Tjunc (°C)	Class	Charge current limit (mA)	ICHG_BAT (Register value)
<90	0	1260	111111
>90	1	1100	110111
>95	2	900	101101
>100	3	700	100011
>105	4	500	011001
>110	5	300	001111
>115	6	Charging suspended	000000

22.7 Dynamic charging current control (DCCC) and active diode

If the combination of the system load plus the battery charging current (pre-charge or fast linear charging) exceeds the charger buck output current (which is limited by the current limitation of the buck) into the VDDOUT node, then the output voltage on VDDOUT will start to drop down to VBAT (which automatically reduces the charging current). When the VDDOUT voltage drops to 3.6 V and the charger buck is still in current limit, the charging current to the battery will be reduced until it reaches zero or the buck runs below its current limit. Once the VDDOUT is above 3.6 V or the buck runs below its current limit, the charging will be increased until it reaches the programmed setting.

The battery charging control includes an active diode circuit that will automatically provide current to the system if the VDDOUT voltage falls below the VBAT voltage. If large currents or very low resistance in series with the battery output is required the path can be extended by an external power FET using the external active diode controller.

Example of DCCC & active diode operation in USB high power mode

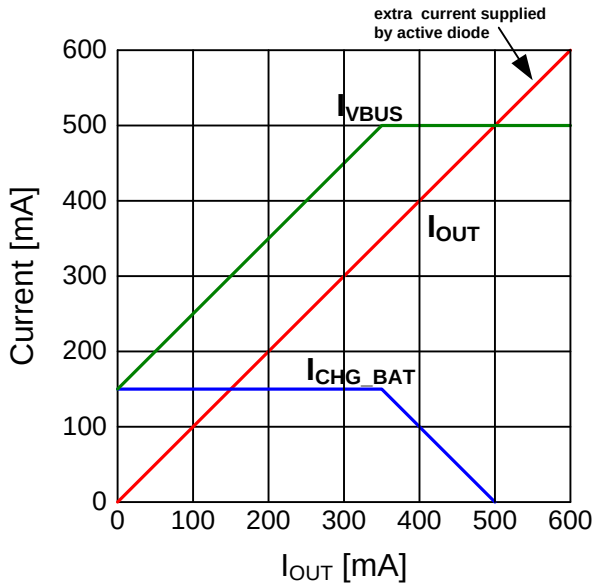


Figure 53: DCCC and active diode operation

22.8 Programmable charge termination by time

The battery charger block will provide a safety timer controlling the maximum time allowed for battery charging. The charge timer is programmable through the power manager bus. The total charge time is defined as the time from when the battery charging was enabled (both for FAST and PRE-CHARGE mode charging). During FAST charge mode the time is dynamically extended whenever the current into the battery is automatically reduced from DCCC or thermal regulation towards less than for example 50 % of the configured maximum charge current. This change in charge time is inversely proportional to the change in charge current. The dynamic safety timer is limited to eight times the programmed clock period and can alternatively be configured towards a fixed timer. If the timer expires (reaches zero) an interrupt request is issued and charging is disabled.

22.9 Backup battery charger and battery switch

The backup battery charger provides a constant charge current with a programmable top off charging voltage for charging of Lithium-Manganese coin cell batteries and super capacitors. Charging current is programmable from 100 µA to 1000 µA (in steps of 100 µA) and from 1 mA to 6 mA (in steps of 1 mA). Termination voltage is programmable in 100 mV steps from 1.1 V to 3.1 V. Charging is suspended whenever the termination voltage has been reached and the charging current drops below 50 µA. Charging is re-enabled whenever the backup battery voltage drops 0.2 V below the target termination voltage. It switches off automatically during NO-POWER mode (nPOR asserted).

The function of the battery switch is to provide power to VDDREF (LDOCORE) from the appropriate battery or supply, depending on conditions as described below.

- If only the backup battery is applied, the switch will automatically connect VDDREF to this battery. If the power path provides a voltage from the main battery or an external supply that is higher than VBBAT the switch will automatically connect to VDDOUT. During NO-POWER mode VDDREF will always be disconnected from the backup battery to prohibit a discharge in advance to the initial start-up of the application. If the target voltage of the backup battery is configured lower than VDDCORE the automatic connection of VBBAT to VDDREF is disabled.
- As the main battery is discharged the system will be warned via the VDDOUT Voltage Supervision with an interrupt. If no action is taken to restore the charge on the main battery and discharging is continued the battery switch will disconnect the input of the LDOCORE (VDDREF) from the main battery and connect to the backup battery when VDDOUT < VBBAT - 0.2 V. If the application includes no backup battery or the backup battery voltage is configured to be less than LDOCORE (intended to provide only a low voltage RTC supply to the host) the automatic switch to the backup battery can be disabled. Having a typical 3 V backup battery the main battery voltage at which is switched over from main to backup battery is 2.8 V. There is a hysteresis in this switch operation so VDDREF will not be reconnected to main battery until the main battery voltage is greater than VBBAT (3.0 V typically).
- The backup battery charger includes a reverse current protection against VDDREF and can also be used as an ultra-low quiescent ‘always on’ supply for low voltage/power rails (on during RESET mode).

22.9.1 Battery charger

Table 111: CHG_BUCK

Register address	Bit	Type	Label	Default	Description
R62 CHG_BUCK	3:0	R/W	ISET_BUCK	0010 Note 1	0000: 80 mA 0001: 90 mA **0010: 100 mA** 0011: 110 mA 0100: 120 mA 0101: 130 mA 0110: 400 mA 0111: 450 mA 1000: 500 mA 1001: 550 mA 1010: 600 mA 1011: 650 mA 1100: 700 mA 1101: 900 mA 1110: 1100 mA 1111: 1300 mA
	4	R/W	CHG_BUCK_EN	1	This bit is controlled by the charger state machine. If reset by the host only a charger removal and re-attach starts automatic charger control again. If set to 1 the automatic charger control is started immediately.
	5	R/W	CHG_BUCK_LP	0	When set to 1 the charger buck is forced to the PFM (sleep) mode and charging will be suspended. Automatically cleared when starting charging/re-charging
	6	R/W	CHG_USB_ILIM	0	**0: No automatic USB charger type detection (always use ISET_USB)** 1: Automatic USB supply current limit enabled (D+,D- sensing, start with ISET_BUCK)
	7	R/W	CHG_TEMP	1	0: Thermal charging control disabled **1: Thermal charging control enabled**

Note 1 The OTP value is used during manufacturing to trim the max. 100 mA current limit (USB default charge current).

Table 112: WAIT_CONT

Register address	Bit	Type	Label	Default	Description
R63 WAIT_CONT	3:0	R/W	DELAY_TIME	1011	0000: 0 µs 0001: 540 µs 0010: 1.0 ms 0011: 2.0 ms 0100: 4.1 ms 0101: 8.2 ms 0110: 16.4 ms 0111: 32.8 ms 1000: 65.5 ms 1001: 131 ms 1010: 262 ms **1011: 524 ms** 1100: 1.0 s 1101: 2.1 s 1110: 4.2 s 1111: Reserved
	4	R/W	EN_32KOUT	0	**0: 32K clock buffer off** 1: 32K clock buffer on
	5	R/W	WAIT_MODE	1	0: Wait for GPIO10 to be active **1: Delay timer mode (start timer and wait for expire)**
	6	R/W	RTC_CLOCK	1	0: No gating of RTC calendar clock **1: Clock to RTC counter is gated until WAIT is asserted**
	7	R/W	WAIT_DIR	0	**0: Wait during power-up sequence** 1: Wait during power-up and power-down sequence

Table 113: ISET

Register address	Bit	Type	Label	Default	Description
R64 ISET	3:0	R/W	ISET_USB	1000	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 130 mA 0110: 400 mA 0111: 450 mA **1000: 500 mA** 1001: 550 mA 1010: 600 mA 1011: 650 mA 1100: 700 mA 1101: 900 mA 1110: 1100 mA 1111: 1300 mA
	7:4	R/W	ISET_DCIN	1101	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 130 mA 0110: 400 mA 0111: 450 mA 1000: 500 mA 1001: 550 mA 1010: 600 mA 1011: 650 mA 1100: 700 mA **1101: 900 mA** 1110: 1100 mA 1111: 1300 mA

Table 114: BAT_CHG

Register address	Bit	Type	Label	Default	Description
R65 BAT_CHG	5:0	R/W	ICHG_BAT Note 1	001010	Battery charger current limit (CC) 000000: 0 mA (charging suspended) 000001: 20 mA 000010: 40 mA 000011: 60 mA 000100: 80 mA 000101: 100 mA 000110: 120 mA 000111: 140 mA 001000: 160 mA 001001: 180 mA **001010: 200 mA** 001011: 220 mA ... 110111: 1100 mA 111000: 1120 mA 111001: 1140 mA 111010: 1160 mA 111011: 1180 mA 111100: 1200 mA 111101: 1220 mA 111110: 1240 mA 111111: 1260 mA
	7:6	R/W	ICHG_PRE	10	Battery pre-charge current limit 00: 0 mA (charging suspended) 01: 20 mA **10: 40 mA** 11: 60 mA

Note 1 3-bit trimming are used to adjust the absolute value via OTP.

Table 115: CHG_CONT

Register address	Bit	Type	Label	Default	Description
R66 CHG_CONT	2:0	R/W	VCH_THR	001	Charger buck reduces the actual current limit if external supply voltage drops below: 000: 3.7 V **001: 3.8 V** 010: 3.9 V 011: 4.0 V 100: 4.1 V 101: 4.2 V 110: 4.3 V 111: 4.35 V (detection threshold)
	7:3	R/W	VCHG_BAT	10110	Battery charger voltage limit (CV) 00000: 3.650 V 00001: 3.675 V 00010: 3.700 V 00011: 3.725 V 00100: 3.750 V 00101: 3.775 V 00110: 3.800 V 00111: 3.825 V 01000: 3.850 V 01001: 3.875 V 01010: 3.900 V 01011: 3.925 V 01100: 3.950 V 01101: 3.975 V 01110: 4.000 V 01111: 4.025 V 10000: 4.050 V 10001: 4.075 V 10010: 4.100 V (Li-Polymer) 10011: 4.125 V 10100: 4.150 V 10101: 4.175 V **10110: 4.200 V (Li-Ion)** 10111: 4.225 V 11000: 4.250 V 11001: 4.275 V 11010: 4.300 V 11011: 4.3250 V 11100: 4.350 V 11101: 4.375 V 11110: 4.400 V 11111: 4.425 V

Table 116: INPUT_CONT

Register address	Bit	Type	Label	Default	Description
R67 INPUT_CONT	3:0	R/W	TCTR Note 1	1010	0000: Charge time out disabled 0001: 30 min remaining 0010: 60 min remaining 0011: 90 min remaining … **1010: 300 min remaining** ... 1111: 450 min remaining
	4	R/W	VBUS_SUSP	0	When set to 1, the USB charger path is set into suspend mode, where the power path from VBUS_PROT to VCENTER is switched off. Automatically cleared when USB supply is removed
	5	R/W	DCIN_SUSP	0	When set to 1, the DCIN charger path is set into disconnect mode, where the power path from DCIN_PROT to VCENTER is switched off. Automatically cleared when DCIN supply is removed
	6	R/W	VCHG_DROP	0	Charger re-enabled if VBAT drops below VCHG_BAT minus 0: 100 mV 1: 200 mV
	7	R/W	TCTR_MODE	0	**0: Total charge time is extended during periods with reduced charge current** 1: Total charge time is fixed

Note 1 Changing the value of TCTR sets the timer to the new value. The timer is paused whenever the ICHG_BAT=0 mA. The current timer value can be read from the CHG_TIME register. The timer counts down from the loaded value.

Table 117: CHG_TIME

Register address	Bit	Type	Label	Default	Description
R68 CHG_TIME	7:0	R	CHG_TIME	00000000	Remaining minutes until charging time out 00000000: Charging ended 00000001: 2 min remaining 00000010: 4 min remaining ... 11111111: 510 min remaining

22.9.2 Backup battery charger

Table 118: BBAT_CONT

Register address	Bit	Type	Label	Default	Description
R69 BBAT_CONT	3:0	R/W	BCHARGER_VSET	1110	0000: disabled 0001: 1.1 V 0010: 1.2 V 0011: 1.4 V 0100: 1.6 V 0101: 1.8 V 0110: 2.0 V 0111: 2.2 V 1000: 2.4 V 1001: 2.5 V 1010: 2.6 V 1011: 2.7 V 1100: 2.8 V 1101: 2.9 V **1110: 3.0 V** 1111: 3.1 V
	7:4	R/W	BCHARGER_ISET	0000	**0000: disabled** 0001: 100 µA 0010: 200 µA 0011: 300 µA 0100: 400 µA 0101: 500 µA 0110: 600 µA 0111: 700 µA 1000: 800 µA 1001: 900 µA 1010: 1 mA 1011: 2 mA 1100: 3 mA 1101: 4 mA 1110: 5 mA 1111: 6 mA

23 White LED driver and boost converter

DA9052 will provide the capability for supplying the power for at least five white LEDs in series. Using the components described in this datasheet to drive three independent strings of five LEDs the inductive boost converter will provide around 24 V at a forward current of max. 78 mA.

NOTE
To handle strings of greater than five LEDs higher voltages are possible by using lower voltages to driving fewer than five LEDs more than 50 mA will be possible by choosing different external components, contact your Dialog representative for specific cases.

The regulation scheme will ensure that the correct voltage is generated for the series connected LEDs. This is achieved by controlling the output voltage of the boost converter such that the lowest voltage at the control loop enabled pins LED1_IN / LED2_IN / LED3_IN exceeds a threshold voltage of approx. 0.7 V at the programmed current. The overvoltage protection will protect the block from a disconnected load, limiting the output voltage of the boost converter. The overvoltage protection threshold is defined by an external voltage divider compared with a reference voltage of 1.41 V. Whenever overvoltage is detected or the current through the inductor gets larger than the maximum configured limit, the boost switches off.

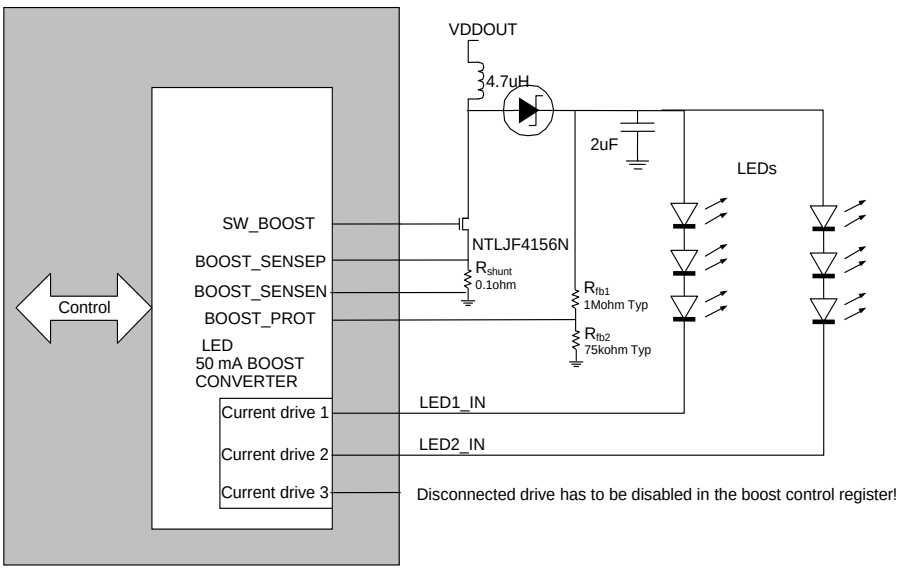


Figure 54: Example of white LED backlight application

Each white LED output driver will have a programmable logarithmic IDAC with 256 steps to set the output current. The dynamic range is 50 µA to 26 mA resulting towards a step multiplication of the “255th root of 520”. All three drivers will have individual controls to enable an LED current ramping with 1 ms per step. The relative matching of identical configured IDACs is designed to be within the range of +/-3.25 % at full current.

NOTE
All LEDx_IN ports that are connected (via LED) to a voltage rail potentially > 5.5 V have to be enabled at a current level that protects the port against high voltages. If a current drive input is not connected to the boost, its regulation has to be disabled in the control register allowing an enabled boost to stop increasing at the intended voltage level. Disabling the current sink without disabling it for the boost control will potentially damage the current drive. It is mandatory to prohibit voltages higher than 5.5 V at the current sink inputs. A balanced configuration is recommended with a similar type and number of LEDs and a similar current for the connected LED strings. Always enable all connected current sinks BEFORE enabling the boost.

The current sinks offer a PWM control. The generated PWM signal is of duty cycle from 16 % to 100 %, with a repetition frequency of 21 kHz and 95 steps (using 2 MHz clock for each step). A PWM ratio greater than 95 results in the output switch being permanently closed. During the duty cycle the current sinks use the individual configured current setting.

The low level current of the PWM controlled LED strings is common. The PWM control can also be made to dim between its actual value and a new value at a rate of 40 ms per step. When set to zero the PWM ratio will change immediately.

NOTE
It is strongly recommended that PWM controlled LED strings, which are enabled for the boost control loop are configured balanced with identical PWM duty cycle and high level current settings. If boost driven strings contain more than 4 LEDs small current deltas or a current ramping are highly recommended because an immediate switch to very low currents can already generate critical input voltages at the current sinks.

LED3 includes a PWM-only mode (no current control) which automatically disables the LED3 input towards the boost control with a duty cycle from 0 % to 100 %. In conjunction with GPIO 14 and GPIO 15 this offers a common anode tri-color LEDs brightness control. This mode is intended to drive a single LED from supply voltages below 5.5 V and requires an appropriate resistor in series.

Recommended components:

- Schottky diode: BAT54J or equivalent.
- FET: NTLJF4156N (includes Schottky) or FDC633N

NOTE
The efficiency of the boost converter is dominated by the external losses. To achieve a good efficiency, the coil, diode and transistor losses should be minimized.

23.1 Boost and LED driver

Table 119: BOOST

Register address	Bit	Type	Label	Default	Description
R70 BOOST	0	R/W	BOOST_EN	0	**0: Boost converter disabled** 1: Boost converter enabled
	1	R/W	LED1_IN_EN	0	**0: LED1 input is disabled for boost voltage control (mandatory, if not connected to boost)** 1: LED1 is included for lowest input voltage
	2	R/W	LED2_IN_EN	0	**0: LED2 input is disabled for boost voltage control (mandatory, if not connected to boost)** 1: LED2 is included for lowest input voltage
	3	R/W	LED3_IN_EN	0	**0: LED3 input is disabled for boost voltage control (mandatory, if not connected to boost)** 1: LED3 is included for lowest input voltage
	4	R/W	BOOST_ILIM	0	**0: 710 mA Boost current limitation** 1: 1000 mA Boost current limitation
	5	R/W	BOOST_FRQ	1	0: 1 MHz Boost switching frequency **1: 2 MHz Boost switching frequency**
	6	R/W	M_B_FAULT	0	Mask boost failure caused nIRQ
	7	R Note 1	E_B_FAULT	0	If set boost the overvoltage or over current limitation triggered an error event

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Table 120: LED_CONT

Register address	Bit	Type	Label	Default	Description
R71 LED_CONT	0	R/W	LED1_EN	0	**0: LED1 current sink disabled, LED1_IN_EN is automatically set to zero** 1: LED1 current sink enabled
	1	R/W	LED1_RAMP	0	**0: No LED1 current ramping** 1: New target LED1 current will be adjusted by ramping (1 step/1 ms)
	2	R/W	LED2_EN	0	**0: LED2 current sink disabled, LED2_IN_EN is automatically set to zero** 1: LED2 current sink enabled
	3	R/W	LED2_RAMP	0	**0: No LED2 current ramping** 1: New target LED2 current will be adjusted by ramping (1 step/1 ms)

Register address	Bit	Type	Label	Default	Description
	4	R/W	LED3_EN	0	**0: LED3 current sink disabled, LED3_IN_EN is automatically set to zero** 1: LED3 current sink enabled
	5	R/W	LED3_RAMP	0	**0: No LED3 current ramping** 1: New target LED3 current will be adjusted by ramping (1 step/1 ms)
	6	R/W	LED3_ICONT	1	0: LED3 is PWM-only controlled (GPIO14/15 mode), LEDMIN_CURRENT and LED3_CURRENT are not used, LED3_EN and LED3_IN_EN are automatically set to zero **1: LED3 is current controlled (LED1/2 mode)**
	7	R	Reserved	0	

Table 121: LEDMIN_123

Register address	Bit	Type	Label	Default	Description
R72 LEDMIN_123	7:0	R/W	LEDMIN_CURRENT	00000000	LED1/2/3 current value during PWM idle time: **00000000: 50.0 µA** 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Table 122: LED1_CONF

Register address	Bit	Type	Label	Default	Description
R73 LED1_CONF	7:0	R/W	LED1_CURRENT	00000000	LED1 current value: **00000000: 50.0 µA** 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Table 123: LED2_CONF

Register address	Bit	Type	Label	Default	Description
R74 LED2_CONF	7:0	R/W	LED2_CURRENT	00000000	LED2 current value: **00000000: 50.0 µA** 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Table 124: LED3_CONF

Register address	Bit	Type	Label	Default	Description
R75 LED3_CONF	7:0	R/W	LED3_CURRENT	00000000	LED3 current value: **00000000: 50.0 µA** 00000001: 51.2 µA (+0.213 dB) 0000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Table 125: LED1_CONT

Register address	Bit	Type	Label	Default	Description
R76 LED1_CONT	6:0	R/W	LED1_PWM	0000000	LED1 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) **0000000: off** 0000001: 1 % (not used) 0000010: 2 % (not used) 0000011: 3 % (not used) 0000100: 4 % (not used) 0000101: 5 % (not used) 0000110: 6 % (not used) 0000111: 7 % (not used) 0001000: 8 % (not used) 0001001: 9 % (not used) 0001010: 10 % (not used) 0001011: 11 % (not used) 0001100: 12 % (not used) 0001101: 13 % (not used) 0001110: 14 % (not used) 0001111: 15 % (not used) 0010000: 16 % .... 1011111: 100 % >1011111: 100 %

Register address	Bit	Type	Label	Default	Description
					LED1_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT.
	7	R/W	LED1_DIM	0	**0: LED1 PWM ratio changes instantly** 1: LED1 ramps between changes in PWM ratio with 40 ms per step

Table 126: LED2_CONT

Register address	Bit	Type	Label	Default	Description
R77 LED2_CONT	6:0	R/W	LED2_PWM	0000000	LED2 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) **0000000: off** 0000001: 1 % (not used) 0000010: 2 % (not used) 0000011: 3 % (not used) 0000100: 4 % (not used) 0000101: 5 % (not used) 0000110: 6 % (not used) 0000111: 7 % (not used) 0001000: 8 % (not used) 0001001: 9 % (not used) 0001010: 10 % (not used) 0001011: 11 % (not used) 0001100: 12 % (not used) 0001101: 13 % (not used) 0001110: 14 % (not used) 0001111: 15 % (not used) 0010000: 16 % .... 1011111: 100 % >1011111: 100 % LED2_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT.
	7	R/W	LED2_DIM	0	**0: LED2 PWM ratio changes instantly** 1: LED2 ramps between changes in PWM ratio with 40 ms per step

Table 127: LED3_CONT

Register address	Bit	Type	Label	Default	Description
R78 LED3_CONT	6:0	R/W	LED3_PWM	0000000	LED3 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) **0000000: off** 0000001: 1 % (not used if current controlled) 0000010: 2 % (not used if current controlled) 0000011: 3 % (not used if current controlled) 0000100: 4 % (not used if current controlled) 0000101: 5 % (not used if current controlled) 0000110: 6 % (not used if current controlled) 0000111: 7 % (not used if current controlled) 0001000: 8 % (not used if current controlled) 0001001: 9 % (not used if current controlled) 0001010: 10 % (not used if current controlled) 0001011: 11 % (not used if current controlled) 0001100: 12 % (not used if current controlled) 0001101: 13 % (not used if current controlled) 0001110: 14 % (not used if current controlled) 0001111: 15 % (not used if current controlled) 0010000: 16 % .... 1011111: 100 % >1011111: 100 % LED3_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT (LED1/2 mode). If LED3_ICONT is not asserted the current control with be disabled and the output will be just switched on and off (GPIO14/15 mode).
	7	R/W	LED3_DIM	0	0: LED3 PWM ratio changes instantly 1: LED3 ramps between changes in PWM ratio with 40 ms per step

Table 128: LED4_CONT

Register address	Bit	Type	Label	Default	Description
R79 LED4_CONT	6:0	R/W	LED4_PWM	0000000	GPIO14 LED on-time (low level at GPIO 14, period 21 kHz = 95 cycles of 0.5 µs) **0000000: off** 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 % 0001011: 11 % 0001100: 12 % 0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % .... 1011111: 100 % >1011111: 100 %
	7	R/W	LED4_DIM	0	**0: LED4 PWM ratio changes instantly** 1: LED4 ramps between changes in PWM ratio with 40 ms per step

Table 129: LED5_CONT

Register address	Bit	Type	Label	Default	Description
R80 LED5_CONT	6:0	R/W	LED5_PWM	0000000	GPIO15 LED on-time (low level at GPIO 15, period 21 kHz = 95 cycles of 0.5 µs) **0000000: off** 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 % 0001011: 11 %

Register address	Bit	Type	Label	Default	Description
					0001100: 12 % 0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % .... 1011111: 100 % >1011111: 100 %
	7	R/W	LED5_DIM	0	**0: LED5 PWM ratio changes instantly** 1: LED5 ramps between changes in PWM ratio with 40 ms per step

24 Monitoring ADC and touch screen interface

24.1 ADC overview

The DA9052 provides an Analog to Digital Converter (ADC) with 10-bit resolution and track and hold circuitry combined with an analog input multiplexer. The analog input multiplexer will allow conversion of up to 10 different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs:

- Channel 0: VDDOUT – measurement of the system voltage
- Channel 1: ICH – internal battery charger current measurement
- Channel 2: TBAT – output from the battery NTC
- Channel 3: VBAT – measurement of the battery voltage
- Channel 4: ADC_IN4 – high impedance input (0 V to 2.5 V)
- Channel 5: ADC_IN5 – high impedance input (0 V to 2.5 V)
- Channel 6: ADC_IN6 – high impedance input (input divider, 0 V to 2.5 V)
- Channel 7: XY– TSI interface to measure the X and Y voltage of the touch screen resistive potentiometers
- Channel 8: internal Tjunc sense (internal temp. sensor)
- Channel 9: VBBAT – measurement of the backup battery voltage

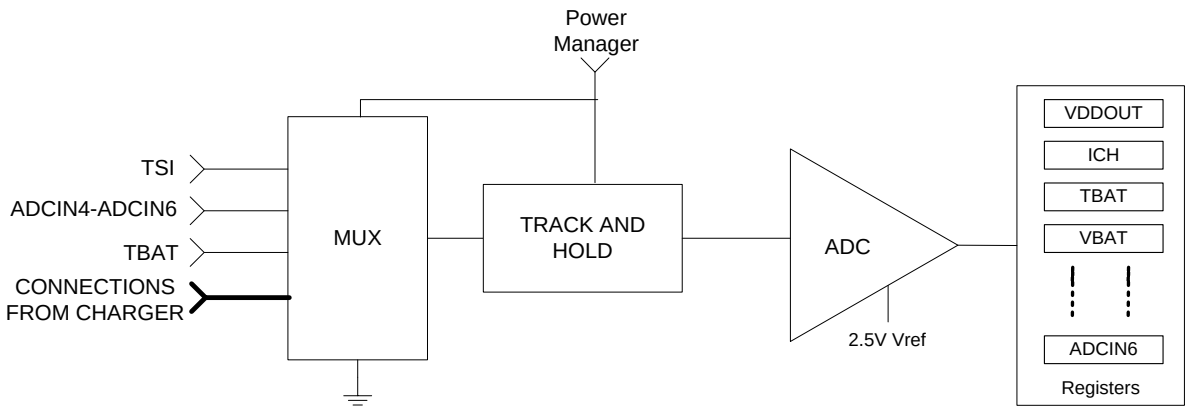


Figure 55: ADC block diagram

24.1.1 Input MUX

The MUX selects from and isolates the 10 inputs and presents the channel to be measured to the ADC input. When selected, an input amplifier on the VDDOUT (and VBAT) channel subtracts the VDDCORE reference voltage and scales the signal to the correct value for the ADC.

24.1.2 ADC

The ADC uses a sample and hold successive approximation switched capacitor architecture. It is supplied from internal core supply rail VDDCORE (2.5 V). It can be used either a high speed mode with measurements sequences repeated every 1 ms or in economy mode with sequences performed every 10 ms.

24.2 Manual conversion mode

For manual measurements the ADC powers up, one conversion is done on the specified channel and the 10-bit result is stored. After the conversion is completed, the ADC powers down again and an IRQ event flag is set (end of manual conversion). The generation of this IRQ can be masked by the IRQ mask.

24.3 Automatic measurements scheduler

The automatic measurement scheduler allows monitoring of the system voltage VDDOUT, the charging current ICH, the battery temperature TBAT and the touch screen interface XY. Additionally, the auxiliary channels, ADCIN4 to ADCIN6, are able to be automatically monitored with upper and low thresholds set by power manager registers to give a nIRQ event if a measurement is outside these levels. All measurements are handled by the scheduler system detailed below.

The scheduler performs a sequence of 10 slots continually repeated according to the configured mode. If the TSI is enabled the first half slot performs either an automatic or a manual conversion. The second half slot performs TSI actions and measurements. If the TSI measurement is disabled there is no split of the slot and only the first conversion is performed. A slot requires 100 µs. The pattern of measurements over the 10 slots depends upon the charging mode. Automatic measurements of VDDOUT, ICH and TBAT are made during charging. These cease when not charging. When automatic measurements are disabled, the manual measurements are made immediately and unused automatic measurements will handle manual conversion requests.

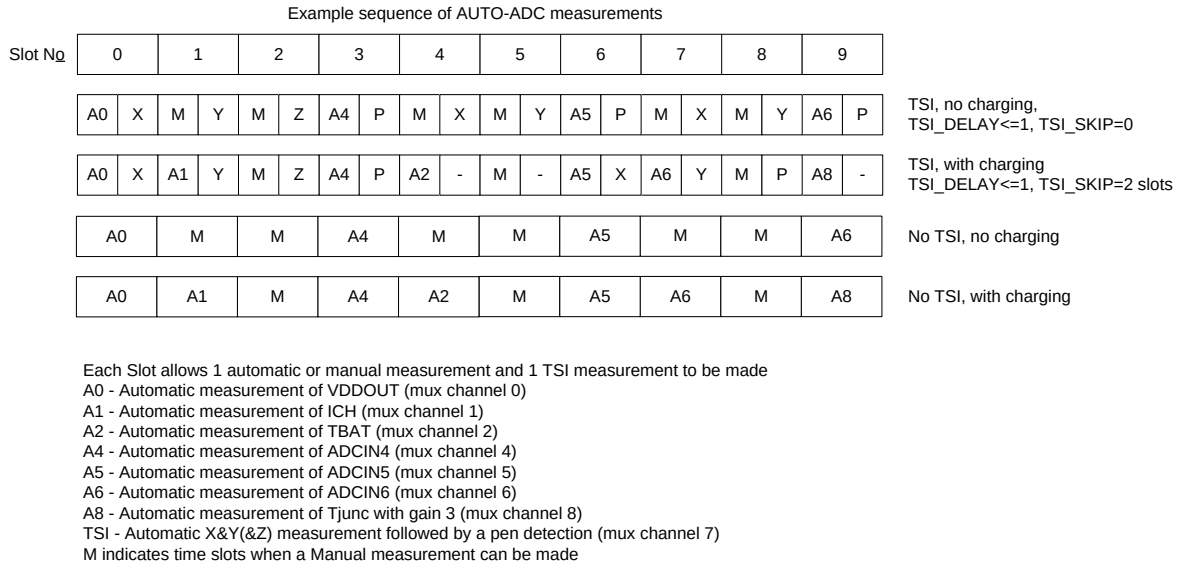


Figure 56: ADC sequence

The action of each automatic measurement follows. Beside the TSI automatic measurements only store the 8 MSB's of the ADC measurement.

24.3.1 A0: VDDOUT low voltage nIRQ measurement mode

VDDOUT is measured and compared with a threshold. If the reading is below this level for a number of three consecutive readings an error event is generated. After nIRQ assertion, the automatic measurement of channel VDDOUT is paused for reading, The host must clear the associated event flag (the event causing value is kept inside the result register) to re-enable the supervision of VDDOUT. If no action is taken to restore the VDDOUT voltage (discharging the battery is continued) the host may consider to switch off optional 'Always on' blocks (backup battery charger or supplies, that are not disabled when powering down to RESET mode) to save energy later on. The multiple reading provides a debouncing of the VDDOUT voltage before issuing a nIRQ. The assertion of nIRQ can be masked by IRQ mask.

24.3.2 A1: ICH and ICH_BAT average measurement mode

When the battery is being charged in FAST CHARGE mode the ICH current is measured automatically every 1 ms or 10 ms and an average value is determined by adding the result to an 18-bit accumulator and latching the top 8 bits every 1024 samples (during high speed mode nine measurements are ignored before performing an update). This provides an average charging current value every 10.24 s, as long as the system load current is less than the maximum current provided from the external supply. When the ICH_BAT falls below the value set (and the other requirements for charging end detect are met), an IRQ will be flagged. The IRQ can be masked.

24.3.3 A2: TBAT and battery temperature warning nIRQ measurement mode

When the battery is being charged, the TBAT voltage is measured automatically. During this measurement, a 50 µA current is sourced to the battery temperature sense resistor from the TBAT pin. During production testing, the TBAT high and low thresholds are programmed into the OTP memory, with adjustments made to correct for the accuracy of the 50 µA current source and the high and low temperature resistance of the NTC resistor.

The measurement result is used to protect the battery pack from damage during charging at too high temperatures. Temperature is flagged by three threshold levels held in the threshold registers (loaded from OTP at start-up). If three consecutive readings of TBAT are outside the configured range, then charging is disabled, an event flag is set and an interrupt is generated. The processor can then either service the IRQ and turn off charging or do nothing. If nothing is done, the FAST CHARGE block will start charging again as soon as the temperature readings are inside the programmed range. The generation of this IRQ can be masked.

24.3.4 A4, A5, A6: automatic measurement and high/low threshold warning nIRQ mode

The automatic measurement result of channel ADC_IN4 is stored. If a reading of A4 outside the programmed range then an event flag is set. If nIRQ was asserted the automatic measurement of channel ADC_IN4 is paused until the host has cleared the associated event flag (the event causing value is kept inside the result register). If debouncing is selected the event will only be asserted if two consecutive measurements override the same threshold. The assertion of nIRQ can be masked by IRQ mask. The same functionality is available at ADC_IN5 and ADC_IN6. In addition it is possible to use ADCIN_4 with a 15 µA current source that allows automatic measurement of a resistor value. During automatic measurements the enabled current source is dynamically switched off at the end of the conversion and switched on one slot prior to the next ADCIN_4 measurement (to enable minimum current consumption, but allow external capacitance to settle), otherwise its status is static.

24.3.5 A8: automatic measurement of internal temperature

Selection of channel 8 (Tjunc) will be used to measure the output of the internal temperature sensor generated out of a PTAT current from the BGR. The channel 8 measures the output of the temperature sensor with a gain of 3. An offset register can be used for a one point calibration of the temperature sensor.

24.3.6 A3, A9: manual measurement VBAT and VBBAT

Channel 3 will be used to measure manually the main battery voltage and channel 9 can be used to measure the voltage of the backup battery.

24.3.7 Fixed threshold non-ADC warning nIRQ mode

A comparator with a threshold of VDDREF (1.2 V) is connected to the input of channel 5. The comparator is asserted whenever the input voltage is excessing or dropping below 1.2 V for at least 10 ms (debouncing) when being enabled via COMP1V2_EN. A status-flag COMP_DET is indicating the actual state and a mask able interrupt request E_COMP_1V2 is generated at falling and rising edge state transitions. The comparator has to be disabled via COMP1V2_EN when auto measurements with high resolution are executed on ADCIN5.

24.3.8 A7: XY touch screen interface

The TSI operates as a sub-system within the scheduler, using the slots to step through tasks such as; pen down detection, matrix switching and settling, and X (one-dimensional resistor network) or XY measurements including pen pressure (Z).

Features:

- Compatible with 4-wire resistive touch screens and supports pen pressure measurement
- Unidirectional resistor network measurements (XP mode)
- X+, X-, Y+, Y- inputs can be alternatively used for multiplexed manual measurements on GP-ADC channel 7
- Pen detection, pen controlled automatic measurements and nIRQ generation with application wakeup
- Supports configurable low power schemes
- Includes TSI pre-charging (to compensate external noise reduction capacitors) and TSI settling to let mechanical vibration of TSI layer sheet stabilize prior to measurement

Maximum X&Y sample rate: 3 kHz (pen pressure: 1 kHz).

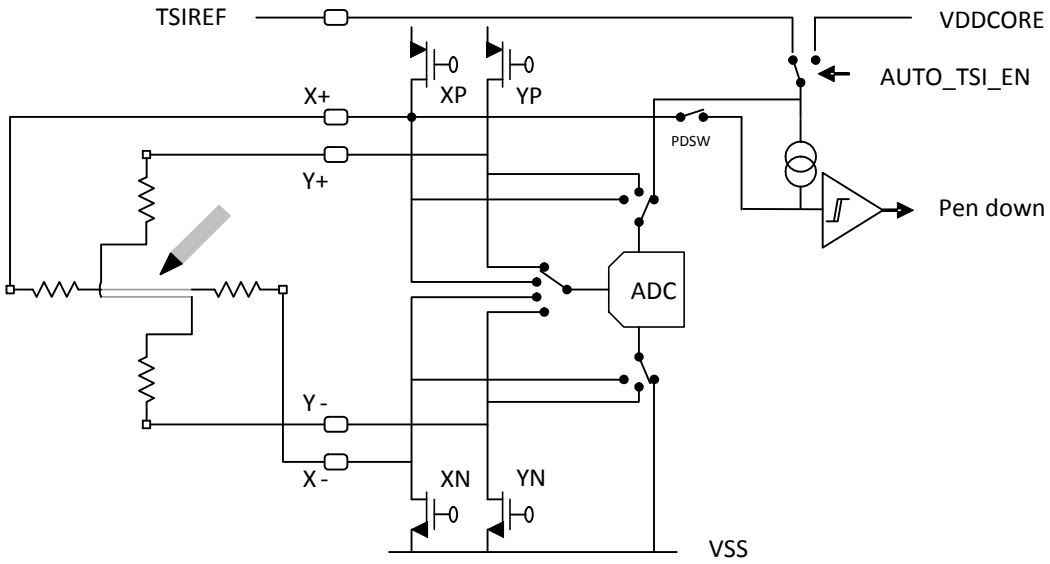


Figure 57: TSI switch matrix

24.3.9 Pen down detect

Whenever the screen is touched outside of autonomous TSI sequences (AUTO_TSI_EN is released) the pen detection will issue an interrupt and will trigger a wakeup from POWER-DOWN mode. An autonomous start of configured TSI sequences (XYZ or X mode) can be armed in parallel to PEN_DET_EN (requires a valid supply voltage at TSIREF), otherwise the host has to start the TSI measurements by asserting AUTO_TSI_EN. For a single sequence of X&Y&Z&P (or X&P) the host has to disable AUTO_TSI_EN when receiving the E_TSI_READY interrupt request.

For pen detection the YN switch is closed, grounding the Y plate. The XP signal is internally connected by switch PDSW to a current source. When the screen is touched, the formed conducting path steers the current to ground and a low voltage triggers an interrupt request. When pen detect is blocked the PDSW is opened to isolate the current from the resistor matrix and ADC. As long as only the pen detection is running the current source is supplied from VDDCORE (2.5 V). Otherwise the supply will be switched to TSIREF which should be connected to LDO9 or a similar high precision regulator.

24.3.10 TSI scheduler

The TSI measurement circuitry is supplied from TSIREF. When measuring the X position the X- switch is closed (grounding the X plane), the X+ switch is closed (charging the X plane) and later the Y+ signal is connected to the ADC input for measurement. When measuring the Y position the Y- switch is closed (grounding the Y plane), the Y+ switch is closed (charging the Y plane) and later the X+ signal is connected to the ADC input.

The TSI function operates every half-slot of the scheduler, performing automatic X, Y, Z (and pen detect) measurements of the touch screen resistive potentiometer. The resulting XYP or XYZP (XP) measurements are then available from the distributed TSI_X & TSI_Y (and (TSI_Z) registers. Whenever a XYP or XYZP (or alternatively XP) data block is ready an interrupt is generated to inform the host about new data to be read. The registers latch the results for all three/four values to ensure an autonomic data read, given that a new measurement may become available whilst reading the multiple registers.

Filtering of LCD noise is handled by external capacitors connected from each TSI pin to ground. A low pass filter is formed with the touch screen resistance that forces a longer settling time prior to ADC sampling. The time between switching and measurement conversion is handled by control bits.

To reduce power consumption the data block measurement can be made intermittently. The gap between actual measurements specifies a delay in multiples of slot time. A value of zero indicates the XYP, XYZP (or XP) block measurements are continually repeated. Otherwise the specified number of slots is skipped in advance to the next XYP, XYZP (or XP) measurement.

In summary a settling delay precedes an X measurement, followed by a settling delay preceding a Y measurement, which is performed identically to the Z and pen detection measurements. A number of slots are missed between a pair of XYP, XYZP (or XP) block measurements. Figure 58 shows an example sequence explaining TSI_DELAY (2 slots) and TSI_SKIP (2 slots) in XP mode.

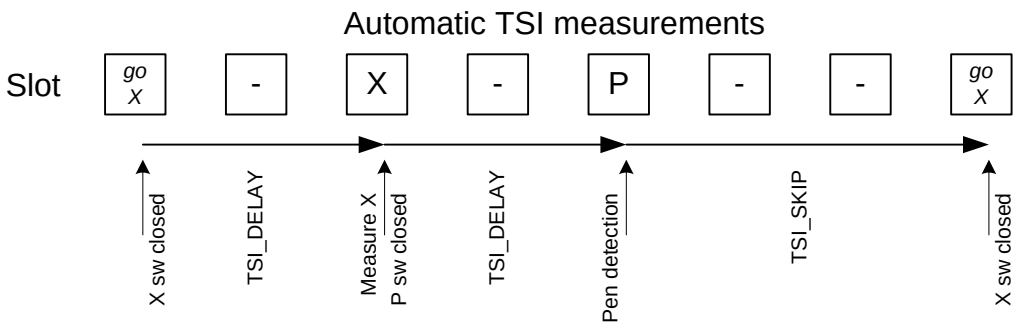


Figure 58: TSI_DELAY (2 slots) and TSI_SKIP (2 slots) in XP mode

24.3.11 Pen pressure

When measuring Z the X- switch is closed (grounding the X plane), the Y+ switch is closed (charging the Y plane) and the X+ signal is later then connected to the ADC input for measuring the value.

The pen pressure can then be estimated from the touch resistance Rpressure which has to be calculated by the host from the measured X, Y and Z values and the known resistance values of the TSI X- and Y-plates (Rx and Ry).

24.3.11.1 Manual measurements

Manual measurements can be executed by asserting TSI_MAN. If asserted in combination with AUTO_TSI_EN = 1 it forces the immediate single TSI measurement selected within TSI_MODE (not waiting for an activate pen detection). If AUTO_TSI_EN = 0 all TSI input channels can be used as further general purpose inputs routed via TSI_MUX to ADC channel 7. In combination with the assertion of TSI_SEL_0 to TSI_SEL_3 this interface mode supports a wide range of host controlled voltage/impedance measurements with ADC channel 7.

24.4 Registers summary

Table 130: Registers Summary

Name (bits)	Description
AUTO_TSI_EN	Touch screen block enable. Regular measurements of X-Y and pen detection are scheduled.
PEN_DET_EN	Enables pen detection mode.
TSI_MODE	0: XYZP mode (X&Y&Z plus two X&Y measurement, each followed by a pen detection) 1: XP mode (X measurements followed by a pen detection)
E_PEN_DOWN	Pen touch detected. Set when pen touch down, else reset. Flags nIRQ and wakeup with current value shown in status registers.
E_TSI_READY	Interrupt request. Cleared by reading event register.
M_TSI_READY	Interrupt request mask. Set to 1 to disable interrupt.
M_PEN_DOWN	Interrupt request mask. Set to 1 to disable interrupt.
TSI_XM, TSI_YM, TSI_XL,TSI_YL, TSI_ZL, PEN_DOWN TSI_Z	Touch screen X, Y and Z readings: R107: TSI_X bits 9:2 R107+1: TSI_Y bits 9:2 R107+2: TSI_X bits 1:0, TSI_Y bits 1:0, TSI_Z bits 1:0, PEN_DOWN R107+3: TSI_Z bits 9:2 (used to calculate the pen pressure) To ensure a synchronous data read, the assertion of the TSI_READY event latches the latest X and Y (and Z) measurements. The values at addresses R107, R107+1 and R107+2 (and R107+3 in XYZP mode) can then be safely read until the event is cleared by the host, even if another TSI measurement occurs in the elapsed time between reads. The addresses are sequential, allowing a three or four word page mode 2-wire read.
TSI_DELAY	Delay between closing X and Y switches and ADC conversion: 0=0 slot: Switches closed only for ADC conversion. This allows 6 µs for settling. 1=1 slot, 2=2 slots, 3=4 slots Switches are set at the end of ADC conversion, reading occurs in next slot and the pattern repeats. Delay of 1 slot enables continuous X,Y,Z (and P) readings.
TSI_SKIP	Delay between two measurements (X and Y or X and Y and Z) where no TC measurements are made (between X values for XP mode). During this period the switches are open and no current is flowing through the screen so reducing average current consumption 0 = Continuous operation 1 = 2 slot, 2 = 5 slot, 3 = 10 slot, 4 = 30 slot, 5 = 80 slot, 6 = 130 slot, 7 = 330 slot.
TSI_MAN	When set with AUTO_TSI_EN released, the following registers override the normal operation
TSI_SEL_0 TSI_SEL_1 TSI_SEL_2 TSI_SEL_3	Direct setting of XY switches: 0 = Open X+, 1 = Close X+ 0 = Open X-, 1 = Close X- 0 = Open Y+, 1 = Close Y+ 0 = Open Y-, 1 = Close Y-
TSI_MUX	Direct setting of MUX selecting which XY pin is routed to GPADC_IN7 input. Depending on the MUX settings the result will be available either in the TSI_X or TSI_Y registers named in brackets: 00 = X+ (TSI_XM, TSI_XL)

Name (bits)	Description
	01 = Y+ (TSI_YM, TSI_YL) 10 = X- (TSI_XM, TSI_XL) 11 = Y- (TSI_YM, TSI_YL)
ADCREF	ADC reference connection. 0 = TSIREF/VSS 1 = X+/X-, Y+/Y- or Y+/X- depending on the channel being measured (X/Y/Z)

24.5 GP-ADC

Table 131: ADC_MAN

Register address	Bit	Type	Label	Default	Description
R81 ADC_MAN	3:0	R/W	MUX_SEL	1000	0000: VDDOUT pin (channel 0) selected 0001: ICH (channel 1) selected 0010: TBAT pin (channel 2) selected 0011: VBAT pin (channel 3) selected 0100: ADCIN4 selected 0101: ADCIN5 selected 0110: ADCIN6 selected 0111: TSI (channel 7) selected) **1000: internal T-Sense using gain 1 (channel 8) selected** 1001: VBBAT-voltage
	4	R/W	MAN_CONV	0	Perform manual conversion. Bit is reset to 0 when conversion is complete.
	7:5	R		000	

Table 132: ADC_CONT

Register address	Bit	Type	Label	Default	Description
R82 ADC_CONT	0	R/W	AUTO_VDD_EN	0	**0: VDDOUT auto measurements disabled** 1: VDDOUT auto measurements enabled
	1	R/W	AUTO_AD4_EN	0	**0: ADCIN4 auto measurements disabled** 1: ADCIN4 auto measurements enabled
	2	R/W	AUTO_AD5_EN	0	**0: ADCIN5 auto measurements disabled** 1: ADCIN5 auto measurements enabled
	3	R/W	AUTO_AD6_EN	0	**0: ADCIN6 auto measurements disabled** 1: ADCIN6 auto measurements enabled
	4	R/W	AD4_ISRC_EN	0	**0: Disable ADCIN4 15 µA current source** 1: Enable ADCIN4 15 µA current source

Register address	Bit	Type	Label	Default	Description
	5	R/W	TBAT_ISRC_EN	0	**0: TBAT 50 µA current source enabled one slot before measurement (disabled after measurement)** 1: Enable TBAT 50 µA current source permanently
	6	R/W	ADC_MODE	0	**0: Measurement sequence interval 10 ms (economy mode)** 1: Measurement sequence interval 1 ms (recommended for TSI mode)
	7	R/W	COMP1V2_EN	0	**0: Disable 1.2 V comparator at ADCIN5** 1: Enable 1.2 V comparator

Table 133: ADC_RES_L

Register address	Bit	Type	Label	Default	Description
R83 ADC_RES_L	1:0	R	ADC_RES_LSB	00	10-bit manual conversion result (2 LSBs)

Table 134: ADC_RES_H

Register address	Bit	Type	Label	Default	Description
R84 ADC_RES_H	7:0	R	ADC_RES_MSB	000000	10-bit manual conversion result (8 MSBs)

Table 135: VDD_RES

Register address	Bit	Type	Label	Default	Description
R85 VDD_RES	7:0	R	VDDOUT_RES	00000000	0x00 – 0xFF: Auto VDDOUT conversion result (ADCIN0) **00000000 corresponds to 2.5 V** 11111111 corresponds to 4.5 V

Table 136: VDD_MON

Register address	Bit	Type	Label	Default	Description
R86 VDD_MON	7:0	R/W	VDDOUT_MON	00000000	VDDOUT_MON threshold setting (8-bit). **00000000 corresponds to 2.5 V** 11111111 corresponds to 4.5 V

Table 137: ICHG_AV

Register address	Bit	Type	Label	Default	Description
R87 ICHG_AV	7:0	R	ICHG_AV	00000000	Charger current average conversion result, 8 MSBs from an internal 18-bit accumulator, updated every 10.24 s: **00000000 corresponds to 0 mA,** 11111111 corresponds to 1000 mA

Table 138: ICHG_THD

Register address	Bit	Type	Label	Default	Description
R88 ICHG_THD	7:0	R/W	ICHG_THD	01000000	Reduced battery charging current detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Table 139: ICHG_END

Register address	Bit	Type	Label	Default	Description
R89 ICHG_END	7:0	R/W	ICHG_END	00000110	Battery charging end point current detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Table 140: TBAT_RES

Register address	Bit	Type	Label	Default	Description
R90 TBAT_RES	7:0	R	TBAT_RES	00000000	00000000 – 11111111: Auto ADC TBAT conversion result (ADCIN1)

Table 141: TBAT_HIGHP

Register address	Bit	Type	Label	Default	Description
R91 TBAT_HIGHP	7:0	R/W	TBAT_HIGHP	00000000	00000000 – 11111111: TBAT high temperature threshold

Table 142: TBAT_HIGHN

Register address	Bit	Type	Label	Default	Description
R92 TBAT_HIGHN	7:0	R/W	TBAT_HIGHN	00000000	00000000 – 11111111: TBAT high temperature resume charging threshold (typically 45 °C)

Table 143: TBAT_LOW

Register address	Bit	Type	Label	Default	Description
R93 TBAT_LOW	7:0	R/W	TBAT_LOW	11111111	00000000 – 11111111: TBAT low temperature threshold (typically 0 °C)

Table 144: T_OFFSET

Register address	Bit	Type	Label	Default	Description
R94 T_OFFSET	7:0	R/W	T_OFFSET	00000000	10000000 – 01111111: signed two's complement calibration offset for junction temperature measurement

Table 145: ADCIN4_RES

Register address	Bit	Type	Label	Default	Description
R95 ADCIN4_RES	7:0	R	ADCIN4_RES	00000000	00000000 – 11111111: Auto ADC ADCIN4 conversion result

Table 146: AUTO4_HIGH

Register address	Bit	Type	Label	Default	Description
R96 AUTO4_HIGH	7:0	R/W	AUTO4_HIGH	11111111	00000000 – 11111111: ADCIN4 high level threshold

Table 147: AUTO4_LOW

Register address	Bit	Type	Label	Default	Description
R97 AUTO4_LOW	7:0	R/W	AUTO4_LOW	00000000	00000000 – 11111111: ADCIN4 low level threshold

Table 148: ADCIN5_RES

Register address	Bit	Type	Label	Default	Description
R98 ADCIN5_RES	7:0	R	ADCIN5_RES	00000000	00000000 – 11111111: Auto ADC ADCIN5 conversion result

Table 149: AUTO5_HIGH

Register address	Bit	Type	Label	Default	Description
R99 AUTO5_HIGH	7:0	R/W	AUTO5_HIGH	11111111	00000000 – 11111111: ADCIN5 high level threshold

Table 150: AUTO5_LOW

Register address	Bit	Type	Label	Default	Description
R100 AUTO5_LOW	7:0	R/W	AUTO5_LOW	00000000	00000000 – 11111111: ADCIN5 low level threshold

Table 151: ADCIN6_RES

Register address	Bit	Type	Label	Default	Description
R101 ADCIN6_RES	7:0	R	ADCIN6_RES	00000000	00000000 – 11111111: Auto ADC ADCIN6 conversion result

Table 152: AUTO6_HIGH

Register address	Bit	Type	Label	Default	Description
R102 AUTO6_HIGH	7:0	R/W	AUTO6_HIGH	11111111	00000000 – 11111111: ADCIN6 high level threshold

Table 153: AUTO6_LOW

Register address	Bit	Type	Label	Default	Description
R103 AUTO6_LOW	7:0	R/W	AUTO6_LOW	00000000	00000000 – 11111111: ADCIN6 low level threshold

Table 154: TJUNC_RES

Register address	Bit	Type	Label	Default	Description
R104 TJUNC_RES	7:0	R	TJUNC_RES	00000000	00000000 – 11111111: Auto TJUNC conversion result (ADCIN8)

24.6 TSI control

Table 155: TSI_CONT_A

Register address	Bit	Type	Label	Default	Description
R105 TSI_CONT_A	0	R/W	AUTO_TSI_EN	0	**0: Auto TSI sequence disabled** 1: Auto TSI sequence measurements enabled (triggered from pen detection or manual measurement)
	1	R/W	PEN_DET_EN	0	**0: Pen detection (repeating sequences measurement) disabled** 1: Pen detect circuit (repeating sequences measurement) enabled
	2	R/W	TSI_MODE	0	Configures TSI to automatically measure sequence either XP or XYZP (XYP) values **0: XYZP mode: X and Y and Z plus two X and Y measurement, each followed by a pen detection** 1: XP mode: X measurements each followed by a pen detection. If PEN_DETECT_EN is asserted the sequences will be repeated until PEN_DOWN is released otherwise only one sequence is measured
	5:3	R/W	TSI_SKIP	000	Delay between two measurements of X and Y and P or X and Y and Z and P (or X and P) where no measurements are made. During this period the XY switches are open and no current is flowing through the screen so reducing average current consumption. **000: continuous operation (<= 3 kHz X and Y)** 001: 2 slots (<=1.875 kHz X and Y) 010: 5 slots (<=1.200 kHz X and Y) 011: 10 slots (<=750 Hz X and Y) 100: 30 slots (<=300 Hz X and Y) 101: 80 slots (<=120 Hz X and Y) 110: 130 slots (<=75 Hz X and Y) 111: 330 slots (<=30 Hz X and Y)
	7:6		TSI_DELAY	01	Delay between closing XY switches and ADC measurement to allow external decoupling capacitors to settle (extends the measurement interval in addition to TSI_SKIP). 00: 0 slot (Switches closed inside ADC conversion slot => 6 µs for settling) **01: 1 slots (Switches closed at end of previous slot => 56 µs for settling)** 10: 2 slots (> 156 µs for settling) 11: 4 slots (> 256 µs for settling)

Register address	Bit	Type	Label	Default	Description
					Switches are set at the end of previous TSI conversion, reading occurs in the slot following the specified number of delay slots and the pattern repeats. Delay of <= 1 slot provides continuous readings.

Table 156: TSI_CONT_B

Register address	Bit	Type	Label	Default	Description
R106 TSI_CONT_B	0	R/W	TSI_SEL_0	0	**0: X+ switch open** 1: X+ switch closed
	1	R/W	TSI_SEL_1	0	**0: X- switch open** 1: X- switch closed
	2	R/W	TSI_SEL_2	0	**0: Y+ switch open** 1: Y+ switch closed
	3	R/W	TSI_SEL_3	0	**0: Y- switch open** 1: Y- switch closed
	5:4	R/W	TSI_MUX	00	Direct setting of MUX selecting which XY pin is routed to ADC_IN7 input. **00: X+ (results will be stored in TSI_XM)** 01: Y+ (results will be stored in TSI_YM) 10: X- (results will be stored in TSI_XM) 11: Y- (results will be stored in TSI_YM)
	6	R/W	TSI_MAN	0	When set, starts manual operation of the TSI measurements: If AUTO_TSI_EN is zero an individual measurement configured by TSI_SEL_x and TSI_MUX will be performed. If AUTO_TSI_EN was asserted the content from TSI_SEL_x and TSI_MUX will be ignored and a single measurement sequence configured in TSI_MODE will be executed. This bit clears automatically at the end of the selected measurement.
	7	R/W	ADCREF	0	ADC reference connection for TSI measurements. **0: TSIREF/VSS** 1: X+/X-, Y+/Y- or Y+/X- (for X, Y or Z measurements)

Table 157: TSI_X_MSB

Register address	Bit	Type	Label	Default	Description
R107 TSI_X_MSB	7:0	R	TSI_XM	00000000	TSI X measurement result- 8 MSBs To ensure a synchronous data read, the act of reading TSI_X_MSB, latches the latest X and Y measurements. The values can then be safely read, even if another TSI measurement has occurred in the elapsed time between reads. The addresses are sequential, allowing a page mode read.

Table 158: TSI_Y_MSB

Register address	Bit	Type	Label	Default	Description
R108 TSI_Y_MSB	7:0	R	TSI_YM	00000000	TSI Y measurement result- 8 MSBs

Table 159: TSI_LSB

Register address	Bit	Type	Label	Default	Description
R109 TSI_LSB	1:0	R	TSI_XL	00	TSI X measurement result- 2 LSBs
	3:2	R	TSI_YL	00	TSI Y measurement result- 2 LSBs
	5:4	R	TSI_ZL	00	TSI Z measurement result- 2 LSBs
	6	R	PEN_DOWN	0	PEN_DOWN state: **0: Pen touch not detected** 1: Pen touch detected
	7	R		0	

Table 160: TSI_Z_MSB

Register address	Bit	Type	Label	Default	Description
R110 TSI_Z_MSB	7:0	R	TSI_ZM	00000000	TSI Z measurement result- 8 MSBs

24.7 GRTC calendar and alarm

Table 161: COUNT_S

Register address	Bit	Type	Label	Default	Description
R111 COUNT_S	5:0	R/W	COUNT_SEC	000000	0x00 – 0x3B: RTC seconds read-out. A read of this register latches the current RTC calendar count into the registers R111 to R116 (coherent for approx. 0.5 s).
	6	R/W	MONITOR	0	Read-out '0' indicates that the power was lost. Read-out of '1' indicates that the clock is OK Set to '1' when setting time to arm RTC monitor function.
	7	R		0	

Table 162: COUNT_MI

Register address	Bit	Type	Label	Default	Description
R112 COUNT_MI	5:0	R/W	COUNT_MIN	000000	0x00 – 0x3B: RTC minutes read-out
	7:6	R		00	

Table 163: COUNT_H

Register address	Bit	Type	Label	Default	Description
R113 COUNT_H	4:0	R/W	COUNT_HOUR	00000	0x00 – 0x17: RTC hours read-out
	7:5	R		000	

Table 164: COUNT_D

Register address	Bit	Type	Label	Default	Description
R114 COUNT_D	4:0	R/W	COUNT_DAY	00001	0x01 – 0x1F: RTC days read-out
	7:5	R		000	

Table 165: COUNT_MO

Register address	Bit	Type	Label	Default	Description
R115 COUNT_MO	3:0	R/W	COUNT_MONTH	0001	0x01 – 0x0C: RTC months read-out
	7:4	R		0000	

Table 166: COUNT_Y

Register address	Bit	Type	Label	Default	Description
R116 COUNT_Y	5:0	R/W	COUNT_YEAR	000000	0x00 – 0x3F: RTC years read-out (0 corresponds to year 2000). A write to this register latches the registers R111 to R116 into the current RTC calendar count
	7:6	R		00	

Table 167: ALARM_MI

Register address	Bit	Type	Label	Default	Description
R117 ALARM_MI	5:0	R/W	ALARM_MIN	000000	0x00 – 0x3B: Alarm minutes setting
	6	R/W	ALARM_TYPE	0	Alarm event caused by: **0: TICK** 1: Timer alarm
	7	R/W	TICK_TYPE	1	Tick alarm interval is: 0: 1 s **1: 1 min**

Table 168: ALARM_H

Register address	Bit	Type	Label	Default	Description
R118 ALARM_H	4:0	R/W	ALARM_HOUR	00000	0x00 – 0x17: Alarm hours setting
	7:5	R		000	

Table 169: ALARM_D

Register address	Bit	Type	Label	Default	Description
R119 ALARM_D	4:0	R/W	ALARM_DAY	00001	0x01 – 0x1F: Alarm days setting
	7:5	R		000	

Table 170: ALARM_MO

Register address	Bit	Type	Label	Default	Description
R120 ALARM_MO	3:0	R/W	ALARM_MONTH	0001	0x01 – 0x0C: Alarm months setting
	7:4	R		0000	

Table 171: ALARM_Y

Register address	Bit	Type	Label	Default	Description
R121 ALARM_Y	5:0	R/W	ALARM_YEAR	0000	0x00 – 0x3F: Alarm years setting (0 corresponds to year 2000). A write to this register latches the registers R117 to R121
	6	R/W	ALARM_ON	0	**0: Alarm function is disabled** 1: Alarm enabled
	7	R/W	TICK_ON	0	**0: Tick function is disabled** 1: Periodic tick alarm enabled

Table 172: SECOND_A

Register address	Bit	Type	Label	Default	Description
R122 SECOND_A	7:0	R	SECONDS_A	00000000	RTC seconds counter A (LSBs). A read of this register latches the current 32-bit counter into the registers R122 to R125 (coherent for approx. 0.5 s).

Table 173: SECOND_B

Register address	Bit	Type	Label	Default	Description
R123 SECOND_B	7:0	R	SECONDS_B	00000000	RTC seconds counter B

Table 174: SECOND_C

Register address	Bit	Type	Label	Default	Description
R124 SECOND_C	7:0	R	SECONDS_C	00000000	RTC seconds counter C

Table 175: SECOND_D

Register address	Bit	Type	Label	Default	Description
R125 SECOND_D	7:0	R	SECONDS_D	00000000	RTC seconds counter D (MSBs)

24.8 Register page 1

Table 176: PAGE_CON_P1

Register address	Bit	Type	Label	Default	Description
R128 PAGE_CON_P1	6:0	R		0000000	
	7	RW	REG_PAGE	0	**0: Selects Register R1 to R127** 1: Selects Register R129 to R255

Table 177: CHIP_ID

Register address	Bit	Type	Label	Default	Description
R129 CHIP_ID	3:0	R	TRC	Note 1	Read back of OTP Trimming release code (TRC) – starts with a code 0
	7:4	R	MRC	Note 2	Read back of mask revision code (MRC) – code 0 for AA release

Note 1 This register allows read back of the revision. Variants that are shipped with different OTP defaults will be identified via a TRC number (loaded from OTP).

Note 2 Changes due to mask design changes will increment the MRC number.

Table 178: CONFIG_ID

Register address	Bit	Type	Label	Default	Description
R130 CONFIG_ID	2:0	R	CONF_ID	000	ID for customer variant of start-up voltages and sequencer configuration, written during production of variant
	7:3	R	CUSTOMER_ID	00000	ID for customer, written during production of variant

24.9 Customer OTP

Table 179: OTP_CONT

Register address	Bit	Type	Label	Default	Description
R131 OTP_CONT	0	R/W	OTP_TRANSFER	0	**0: No transfer in progress** 1: Writing '1' to this bit initiates the fusing of selected OTP cells with the content from corresponding registers 1: Reading '1' indicates the transfer is still ongoing
	1	R/W	OTP_RP	0	**0: Transfer is Read** 1: Transfer is Programming
	2	R/W	OTP_GP	0	**0: No action** 1: Transfer includes configuration registers R132to R142(plus GP_WRITE_DIS and OTP_GP_LOCK)
	3	R/W		0	
	4	R		0	
	5	R	OTP_GP_LOCK	0	**0: OTP not locked after programming** 1: OTP will be locked during programming (no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR
	6	R/W	OTP_CONF_LOCK	1	0: OTP registers R10 to R106 not locked after programming (only for unmarked evaluation samples) **1: OTP registers R10 to R106 will be locked during programming (set for all marked parts, no further fusing possible)** Note: Write access for fusing only, control state is loaded from OTP defaults after POR
	7	R/W	GP_WRITE_DIS	0	**0: Enables write access to GP_ID registers** 1: GP_ID registers are 'read only' Note: Write access for fusing only, control state is loaded from OTP defaults after POR

Table 180: OSC_TRIM

Register address	Bit	Type	Label	Default	Description
R132 OSC_TRIM	7:0	R/W	TRIM_32K	00000000	Bits for correction of the 32K oscillator frequency: 10000000: -244.1 ppm … 11111111: -1.9 ppm **00000000: off** 00000001: 1.9 ppm (1/(32768*16)) … 01111111: 242.2 ppm

Table 181: GP_ID_0

Register address	Bit	Type	Label	Default	Description
R133 GP_ID_0	7:0	R/W Note 1	GP_0	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 182: GP_ID_1

Register address	Bit	Type	Label	Default	Description
R134 GP_ID_1	7:0	R/W Note 1	GP_1	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 183: GP_ID_2

Register address	Bit	Type	Label	Default	Description
R135 GP_ID_2	7:0	R/W Note 1	GP_2	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 184: GP_ID_3

Register address	Bit	Type	Label	Default	Description
R136 GP_ID_3	7:0	R/W Note 1	GP_3	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 185: GP_ID_4

Register address	Bit	Type	Label	Default	Description
R137 GP_ID_4	7:0	R/W Note 1	GP_4	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 186: GP_ID_5

Register address	Bit	Type	Label	Default	Description
R138 GP_ID_5	7:0	R/W Note 1	GP_5	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 187: GP_ID_6

Register address	Bit	Type	Label	Default	Description
R139 GP_ID_6	7:0	R/W Note 1	GP_6	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 188: GP_ID_7

Register address	Bit	Type	Label	Default	Description
R140 GP_ID_7	7:0	R/W Note 1	GP_7	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 189: GP_ID_8

Register address	Bit	Type	Label	Default	Description
R141 GP_ID_8	7:0	R/W Note 1	GP_8	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

Table 190: GP_ID_9

Register address	Bit	Type	Label	Default	Description
R142 GP_ID_9	7:0	R/W Note 1	GP_9	00000000	Data from fuse array (OTP)

Note 1 Write access disabled if GP_WRITE_DIS was once fused with '1'.

25 Register map

Most register bits (exceptions are for example FAULT_LOG or CHG_TIME), that are not loaded from OTP are reset to defaults (zero in most cases) when powering up from RESET mode. Register bits shown in blue are loaded from OTP.

R	Function	7	6	5	4	3	2	1	0
PAGE 0									
System control and event registers (SYSMON)									
R0	PAGE_CON	REG_PAGE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
R1	STATUS_A	VDAT_DET	VBUS_SEL	DCIN_SEL	VBUS_DET	DCIN_DET	ID_GND	ID_FLOAT	nONKEY
R2	STATUS_B	COMP_DET	SEQUENCING	GP_FB2	CHG_TO	CHG_END	CHG_LIM	CHG_PRE	CHG_ATT
R3	STATUS_C	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
R4	STATUS_D	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8
R5	EVENT_A	M_COMP_1V2	M_SEQ_RDY	E_ALARM	E_VDD_LOW	E_VBUS_REM	E_DCIN_REM	E_VBUS_DET	E_DCIN_DET
R6	EVENT_B	E_TSI_READY	E_PEN_DOWN	E_ADC_EOM	E_TBAT	E_CHG_END	E_ID_GND	E_ID_FLOAT	E_nONKEY
R7	EVENT_C	E_GPI7	E_GPI6	E_GPI5	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0
R8	EVENT_D	E_GPI15	E_GPI14	E_GPI13	E_GPI12	E_GPI11	E_GPI10	E_GPI9	E_GPI8
R9	FAULT_LOG52 F	WAIT_SHUT	nSD_SHUT	KEY_SHUT	Not used	TEMP_OVER	VDD_START	VDD_FAULT	TWD_ERROR
R10	IRQ_MASK_A	M_COMP_1V2	M_SEQ_RDY	M_ALARM	M_VDD_LOW	M_VBUS_REM	M_DCIN_REM	M_VBUS_VLD	M_DCIN_VLD
R11	IRQ_MASK_B	M_TSI_READY	M_PEN_DOWN	M_ADC_EOM	M_TBAT	M_CHG_END	M_ID_GND	M_ID_FLOAT	M_nONKEY
R12	IRQ_MASK_C	M_GPI7	M_GPI6	M_GPI5	M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0
R13	IRQ_MASK_D	M_GPI15	M_GPI14	M_GPI13	M_GPI12	M_GPI11	M_GPI10	M_GPI9	M_GPI8
R14	CONTROL_A	GPI_V	PM_O_TYPE	PM_O_V	PM_I_V	PM_IF_V	PWR1_EN55F	PWR_EN54F	SYS_EN53F
R15	CONTROL_B	SHUTDOWN	DEEP_SLEEP	WRITE_MODE	BBAT_EN	OTPREAD_EN	AUTO_BOOT	ACT_DIODE	BUCK_MERGE
R16	CONTROL_C	BLINK_DUR	BLINK_FRQ	DEBOUNCING	PM_FB2_PIN	PM_FB1_PIN			
R17	CONTROL_D	WATCHDOG	ACC_DET_EN	GPI14_15_SD	nONKEY_SD	KEEPACT_EN	TWDSCALE		
R18	PD_DIS	PM-CONT_PD	OUT_32K_PD	CHG_BBAT_PD	CHG_PD	HS-2-wire_PD	PM-IF_PD	GP-ADC_PD	GPIO_PD

R	Function	7	6	5	4	3	2	1	0
R19	INTERFACE	IF_BASE_ADDR	nCS_POL	R/W_POL	CPHA	CPOL	IF_TYPE		
R20	RESET	RESET_EVENT	RESET_TIMER						
GPIO control registers (GPIO)									
R21	GPIO_0-1	GPIO1_ MODE	GPIO1_TYPE	GPIO1_PIN	GPIO0_ MODE	GPIO0_TYPE	GPIO0_PIN		
R22	GPIO_2-3	GPIO3_ MODE	GPIO3_TYPE	GPIO3_PIN	GPIO2_MODE	GPIO2_TYPE	GPIO2_PIN		
R23	GPIO_4-5	GPIO5_ MODE	GPIO5_TYPE	GPIO5_PIN	GPIO4_ MODE	GPIO4_TYPE	GPIO4_PIN		
R24	GPIO_6-7	GPIO7_ MODE	GPIO7_TYPE	GPIO7_PIN	GPIO6_ MODE	GPIO6_TYPE	GPIO6_PIN		
R25	GPIO_8-9	GPIO9_ MODE	GPIO9_TYPE	GPIO9_PIN	GPIO8_ MODE	GPIO8_TYPE	GPIO8_PIN		
R26	GPIO_10-11	GPIO11_ MODE	GPIO11_TYPE	GPIO11_PIN	GPIO10_ MODE	GPIO10_TYPE	GPIO10_PIN		
R27	GPIO_12-13	GPIO13_ MODE	GPIO13_TYPE	GPIO13_PIN	GPIO12_ MODE	GPIO12_TYPE	GPIO12_PIN		
R28	GPIO_14-15	GPIO15_ MODE	GPIO15_TYPE	GPIO15_PIN	GPIO14_ MODE	GPIO14_TYPE	GPIO14_PIN		
Power sequencer control registers (SEQ)									
R29	ID_0_1	LDO1_STEP	Not used	SYS_PRE	DEF_SUPPLY	nRES_MODE			
R30	ID_2_3	LDO3_STEP	LDO2_STEP						
R31	ID_4_5	LDO5_STEP	LDO4_STEP						
R32	ID_6_7	LDO7_STEP	LDO6_STEP						
R34	ID_10_	LDO9_STEP	LDO8_STEP						
R34	ID_10_11	PD_DIS_STEP	LDO10_STEP						
R35	ID_12_13	VMEM_SW_STEP	VPERI_SW_STEP						
R36	ID_14_15	BUCKPRO_STEP	BUCKCORE_STEP						
R37	ID_16_17	BUCKPERI_STEP	BUCKMEM_STEP						
R38	ID_18_19	GP_RISE2_STEP	GP_RISE1_STEP						
R39	ID_20_21	GP_FALL2_STEP	GP_FALL1_STEP						
R40	SEQ_STATUS	SEQ_POINTER	WAIT_STEP						

R	Function	7	6	5	4	3	2	1	0
R41	SEQ_A	POWER_END	SYSTEM_END						
R42	SEQ_B	PART_DOWN	MAX_COUNT						
R43	SEQ_TIMER	SEQ_DUMMY	SEQ_TIME						
Power supply control registers (REG)									
R44	BUCK_A	BPRO_ILIM	BPRO_MODE	BCORE_ILIM	BCORE_MODE				
R45	BUCK_B	BPERI_ILIM	BPERI_ MODE	BMEM_ILIM	BMEM_ MODE				
R46	BUCKCORE	BCORE_CONF	BCORE_EN	VBCORE					
R47	BUCKPRO	BPRO_CONF	BPRO_EN	VBPRO					
R48	BUCKMEM	BMEM_CONF	BMEM_EN	VBMEM					
R49	BUCKPERI	BPERI_CONF	BPERI_EN	BPERI_HS	VBPERI				
R50	LDO1	LDO1_CONF	LDO1_EN	VLDO1					
R51	LDO2	LDO2_CONF	LDO2_EN	VLDO2					
R52	LDO3	LDO3_CONF	LDO3_EN	VLDO3					
R53	LDO4	LDO4_CONF	LDO4_EN	VLDO4					
R54	LDO5	LDO5_CONF	LDO5_EN	VLDO5					
R55	LDO6	LDO6_CONF	LDO6_EN	VLDO6					
R56	LDO7	LDO7_CONF	LDO7_EN	VLDO7					
R57	LDO8	LDO8_CONF	LDO8_EN	VLDO8					
R58	LDO9	LDO9_CONF	LDO9_EN	VLDO9					
R59	LDO10	LDO10_CONF	LDO10_EN	VLDO10					
R60	SUPPLY	V_LOCK	VMEM_SW_EN	VPERI_SW_EN	VLDO3_GO	VLDO2_GO	VB_MEM_GO	VB_PRO_GO	VB_CORE_GO
R61	PULLDOWN	Not used	Not used	LDO5_PD_DIS	LDO2_PD_DIS	LDO1_PD_DIS	MEM_PD_DIS	PRO_PD_DIS	CORE_PD_DIS
Charging control registers (CHARGE)									
R62	CHG_BUCK	CHG_TEMP	CHG_USB_ILIM	CHG_BUCK_LP	CHG_BUCK_EN	ISET_BUCK			

R	Function	7	6	5	4	3	2	1	0
R63	WAIT_CONT	WAIT_DIR	RTC_CLOCK	WAIT_MODE	EN_32KOUT	DELAY_TIME			
R64	ISET	ISET_DCIN	ISET_USB						
R65	BAT_CHG	ICHG_PRE	ICHG_BAT						
R66	CHG_CONT	VCHG_BAT	VCH_THR						
R67	INPUT_CONT	TCTR_MODE	VCHG_DROP	DCIN_SUSP	VBUS_SUSP	TCTR			
R68	CHG_TIME	CHG_TIME							
Backup battery charging control registers (BBAT)									
R69	BBAT_CONT	BCHARGER_ISET	BCHARGER_VSET						
Boost and LED driver control registers (LED)									
R70	BOOST	E_B_FAULT	M_B_FAULT	BOOST_FRQ	BOOST_ILIM	LED3_IN_EN	LED2_IN_EN	LED1_IN_EN	BOOST_EN
R71	LED_CONT	Not used	LED3_ICONT	LED3_RAMP	LED3_EN	LED2_RAMP	LED2_EN	LED1_RAMP	LED1_EN
R72	LEDMIN	LEDMIN_CURRENT							
R73	LED1_CONF	LED1_CURRENT							
R74	LED2_CONF	LED2_CURRENT							
R75	LED3_CONF	LED3_CURRENT							
R76	LED1_CONT	LED1_DIM	LED1_PWM						
R77	LED2_CONT	LED2_DIM	LED2_PWM						
R78	LED3_CONT	LED3_DIM	LED3_PWM						
R79	LED4_CONT	LED4_DIM	LED4_PWM						
R80	LED5_CONT	LED5_DIM	LED5_PWM						
GP-ADC control registers (GPADC)									
R81	ADC_MAN	Not used	Not used	Not used	MAN_CONV	MUX_SEL			
R82	ADC_CONT	COMP1V2_EN	ADC_MODE	TBAT_ISRC_EN	AD4_ISRC_EN	AUTO_AD6_EN	AUTO_AD5_EN	AUTO_AD4_EN	AUTO_VDD_EN
R83	ADC_RES_L	Not used	Not used	Not used	Not used	Not used	Not used	ADC_RES_LSB	

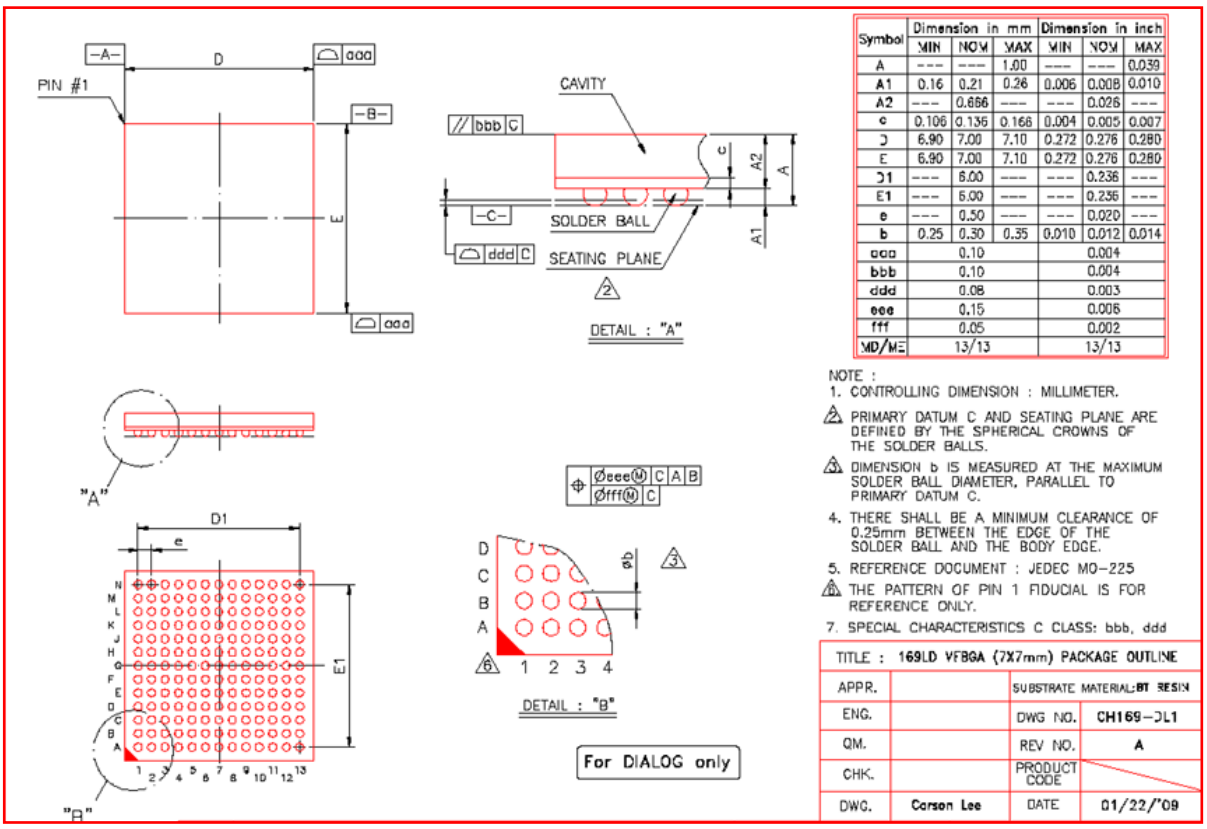
R	Function	7	6	5	4	3	2	1	0
R84	ADC_RES_H	ADC_RES_MSB							
R85	VDD_RES	VDDOUT_RES							
R86	VDD_MON	VDDOUT_MON							
R87	ICHG_AV	ICHG_AV							
R88	ICHG_THD	ICHG_THD							
R89	ICHG_END	ICHG_END							
R90	TBAT_RES	TBAT_RES							
R91	TBAT_HIGHP	TBAT_HIGHP							
R92	TBAT_HIGHN	TBAT_HIGHN							
R93	TBAT_LOW	TBAT_LOW							
R94	T_OFFSET	T_OFFSET							
R95	ADCIN4_RES	ADCIN4_RES							
R96	AUTO4_HIGH	AUTO4_HIGH							
R97	AUTO4_LOW	AUTO4_LOW							
R98	ADCIN5_RES	ADCIN5_RES							
R99	AUTO5_HIGH	AUTO5_HIGH							
R100	AUTO5_LOW	AUTO5_LOW							
R101	ADCIN6_RES	ADCIN6_RES							
R102	AUTO6_HIGH	AUTO6_HIGH							
R103	AUTO6_LOW	AUTO6_LOW							
R104	TJUNC_RES	TJUNC_RES							
TSI control registers (TSI)									
R105	TSI_CONT_A	TSI_DELAY	TSI_SKIP	TSI_MODE	PEN_DET_EN	AUTO_TSI_EN			
R106	TSI_CONT_B	ADCREF	TSI_MAN	TSI_MUX	TSI_SEL_3	TSI_SEL_2	TSI_SEL_1	TSI_SEL_0	

R	Function	7	6	5	4	3	2	1	0
R107	TSI_X_MSB	TSI_XM							
R108	TSI_Y_MSB	TSI_YM							
R109	TSI_LSB	Not used	PEN_DOWN	TSI_ZL	TSI_YL	TSI_XL			
R110	TSI_Z_MSB	TSI_ZM							
RTC calendar and alarm (RTC)									
R111	COUNT_S	Not used	MONITOR	COUNT_SEC					
R112	COUNT_MI	Not used	Not used	COUNT_MIN					
R113	COUNT_H	Not used	Not used	Not used	COUNT_HOUR				
R114	COUNT_D	Not used	Not used	Not used	COUNT_DAY				
R115	COUNT_MO	Not used	Not used	Not used	Not used	COUNT_MONTH			
R116	COUNT_Y	Not used	Not used	COUNT_YEAR					
R117	ALARM_MI	TICK_TYPE	ALARM_TYPE	ALARM_MIN					
R118	ALARM_H	Not used	Not used	Not used	ALARM_HOUR				
R119	ALARM_D	Not used	Not used	Not used	ALARM_DAY				
R120	ALARM_MO	Not used	Not used	Not used	Not used	ALARM_MONTH			
R121	ALARM_Y	TICK_ON	ALARM_ON	ALARM_YEAR					
R122	SECOND_A	SECONDS_A							
R123	SECOND_B	SECONDS_B							
R124	SECOND_C	SECONDS_C							
R125	SECOND_D	SECONDS_D							
PAGE 1									
Customer OTP (MEM)									
R128	PAGE_CON	REG_PAGE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
R129	CHIP_ID	MRC	TRC						

R	Function	7	6	5	4	3	2	1	0
R130	CONFIG_ID	CUSTOMER_ID	CONF_ID						
R131	OTP_CONT	GP_WRITE_DIS	OTP_CONF_LOCK	OTP_GP_LOCK	Not used	OTP_CONF	OTP_GP	OTP_RP	OTP_TRANSFER
R132	OSC_TRIM	TRIM_32K							
R133	GP_ID_0	GP_0							
R134	GP_ID_1	GP_1							
R135	GP_ID_2	GP_2							
R136	GP_ID_3	GP_3							
R137	GP_ID_4	GP_4							
R138	GP_ID_5	GP_5							
R139	GP_ID_6	GP_6							
R140	GP_ID_7	GP_7							
R141	GP_ID_8	GP_8							
R142	GP_ID_9	GP_9							

26 Package information

26.1 Package outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.00	---	---	0.039
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	---	0.656	---	---	0.026	---
c	0.106	0.136	0.166	0.004	0.005	0.007
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D1	---	6.00	---	---	0.236	---
E1	---	6.00	---	---	0.236	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.10			0.004	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		13/13			13/13	

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MO-225
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd

TITLE : 169LD VFBGA (7X7mm) PACKAGE OUTLINE			
APPR.		SUBSTRATE MATERIAL: BT RESIN	
ENG.		DWG NO.	CH169-DL1
QM.		REV NO.	A
CHK.		PRODUCT CODE	
DWG.	Carson Lee	DATE	01/22/'09

Figure 59: 169 BGA (7 x 7 mm), bottom view

27 External component selection

27.1 Capacitor selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails.

When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account. On the VDDOUT main supply rail a minimum distributed capacitance of 30 µF with the following split is recommended:

- 10 µF close to VDDOUT pin
- 10 µF close to VDDMEM_PERI, VDD_CORE_PRO buck supply pins
- 10 µF close to boost converter input (coil)
- 2x 1 µF close to VDD_LDOx pins

Table 191: Recommended capacitor types

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
VLDO1, VLDO2, VLDO5, VLDO9 output bypass	4x 1 µF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A105KE15D
VLDO3, VLDO4, VLDO6, VLDO7, VLDO8, VLDO10 output bypass	6x 2.2 µF	0402	X5R +/-15 %	+/-20 %	6.3 V	Murata GRM155R60J225ME95D
VDDCORE output bypass	1x 100 nF	0402	X7R +/-15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
VBUCKPER, VBUCKMEM output bypass	2x 10 µF	0805	X7R +/-15 %	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
VBUCKPRO, VBUCKCORE output bypass (also in merged mode)	2x 22 µF	0805	X5R +/-15 %	+/-20 %	6.3 V	Murata GRM21BR60J226ME39L
VMEM_SW, VCORE_SW output bypass	2x 100 nF	0402	X7R +/-15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
VBOOST output bypass	1x 2.2 µF	1206	X7R +/-15 %	+/-10 %	25 V	Murata GRM31MR71E225KA93L
VBUS, DCIN bypass	2x 2.2 µF	0603	X5R +/-15 %	+/-10 %	16 V	Murata GRM188R61C225KE15
VBUS_PROT, DCIN_PROT bypass	2x 4.7 µF	0603	X5R +/-15 %	+/-10 %	6.3 V	Murata GRM188R71J475KE19D
VCENTER bypass	1x 10 µF	0805	X7R +/-15 %	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
VDDOUT bypass	3x 10 µF	0805	X7R +/-15 %	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
	2x 1 µF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A105KE15D
VBAT bypass	1x 10 µF	0805	X7R +/-15 %	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
VDDREF bypass	1x 220 nF	0402	X5R +/-15 %	+/-10 %	10 V	Murata GRM155R61A224KE19D
VREF bypass	1x 100 nF	0402	X7R +/-15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
XIN, XOUT bypass to VSS	2x 12 pF	0402	U2J	+/-5 %	50 V	Murata GRM1557U1H120JZ01D

27.2 Inductor selection

Inductors should be selected based upon the following parameters:

- Rated maximum current: Usually a coil provides two current limits, one specifies the maximum current at which the inductance derating due to saturation effects is limited to be within a specified tolerance (typically 20 % or 30 %) of the peak current. The second limit is defined by the maximum power dissipation and is applied to the effective current
- DC resistance: critical to converter efficiency and should therefore be minimized
- Inductance: given by converter electrical characteristics; is 4.7 µH for all DA9052 switched mode converters

Table 192: Recommended inductor types

Application	Value	Size	Max I	Tolerance	DC res. (Ω) typ	Type
BUCKPER, BUCKMEM, BUCKPRO, BUCKCORE	4x 4.7 µH	3 x 3 x 1.2 mm	1.2 A	+/-20 %	0.13	TDK VLS3012T-4R7M1R0
Merged BUCKCORE/ BUCKPRO	1x 2.2 µH	3 x 3 x 1.2 mm	1.7 A	+/-20 %	0.08	TDK VLS3012T-2R2M1R5
BOOST	1x 4.7 µH	3 x 3 x 1.2 mm	1.2 A	+/-20 %	0.13	TDK VLS3012T-4R7M1R0
CHARGER BUCK	1x 4.7 µH	3 x 3 x 1.2 mm	1.2 A	+/-20 %	0.13	TDK VLS3012T-4R7M1R0

27.3 Resistors

Table 193: Recommended resistor types

Application	Value	Size	Tolerance (%)	P max (mW)	Type
BOOST current sense	100 mΩ	0402	+/-2	125	Panasonic ERJ2BSGR10x
IREF bias current reference	200 kΩ	0402	+/-1	100	Panasonic ERJ2RKF2003x

27.4 External pass transistors and Schottky diodes

Table 194: Recommended types

Application	Package	Type
BOOST FET + SCHOTTKY	WDFN6 2x2x0.8 mm	ON Semiconductor NTLJF4156N
VBUS overvoltage protection FET	SOT-23	CSD25301W1015, PMV65XP
DCIN overvoltage protection FET	SOT-23	CSD25301W1015, PMV65XP
System load switch (active diode) FET	SOT-23 3x2.6x1 mm	Vishay Siliconix Si2333CDS

27.5 Backup battery

The backup battery charger supports Lithium coin cells as well as Supercaps/Goldcaps. However if the internal RTC clock is used, the battery's nominal voltage should be above 3 V to allow reasonable backup times though the backup battery charger allows charge voltages from 1.1 V to 3.1 V (for example, for external RTC clock modules).

Table 195: Example backup battery

Type	Size	Manufacturer
Lithium Battery (rechargeable) ML414, 1.0 mAh, 3.1 V	4.8 (dia.) x 1.4 mm	Sanyo, Panasonic
Electric Double Layer Capacitor (Gold Capacitor) EECEN0F204xx, 0.2 F, 3.3 V	6.8 (dia.) x 1.8 mm	Panasonic
Electric Double Layer Capacitor (Gold Capacitor) EECEP0E333A, 0.033 F, 2.6 V	3.8 (dia.) x 1.5 mm	Panasonic

27.6 Battery pack temperature sensor (NTC)

In order to achieve reasonable accuracy over the relevant temperature range (for example, 0 °C to 50 °C for charging) by using the internal 50 µA current source, the recommended NTC should have a nominal resistance of 10 kΩ and its resistance should not exceed 50 kΩ within this range.

Table 196: Example battery pack temperature sensor (NTC)

Type	Size	Manufacturer
NCP15XH103J03RC	0402	Murata

27.7 Crystal

The Real Time Clock module requires an external 32.768 kHz crystal.

For crystal selection the effective load capacitance has to be taken into account. It includes both external capacitors on pins XIN and XOUT in series combination and the PCB and DA9052 stray capacitances.

For example, if two times 12 pF external capacitors are used, which gives a series combination of 6 pF, and the stray capacitance is 3 pF, then the crystal type specified for a load capacitance of 9 pF should be chosen.

Different stray capacitances may require different external capacitors and/or a different crystal type.

Furthermore the series resistance of the crystal must not exceed 100 kΩ.

Table 197: Recommended crystal type

Type	Size	Manufacturer
CC7V-T1A 32.768 kHz 9.0 pF +/-30 ppm	3.2x1.5x0.9 mm	Micro Crystal

28 Layout guidelines

28.1 General recommendations

- Appropriate trace width and amount of vias should be used for all power supply paths.

  Too high trace resistances can prevent the system from proper operation for example efficiency and current ratings of switch mode converters and charger might be degraded. Furthermore the PCB might be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.

  Special care must be taken to the DA9052 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row connection in an inner layer is recommended (depending on the maximum current two or more vias might be required).
- A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references like the VDDREF capacitor and IREF resistor should be referred to a silent ground which is connected at a star point underneath or close to the DA9052 main ground connection.
- Generally all power tracks with discontinuous and / or high currents should be kept as short as possible.
- Noise sensitive analog signals like feedback lines or crystal connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.
- For further information please see Application Note AN-PM-010 PCB Layout Guidelines for Dialog PMICs, available on the Dialog website.

28.2 System supply and charger

- Trace resistance of the VBUSPROT (or DCIN_PROT) bypass capacitor to VCENTER has to be minimized to allow proper operation of the charge and system current control.
- In case an external pMOS transistor is used to bypass the internal active diode, its connection trace resistance has to be kept to a minimum.
- The placement of the distributed capacitors at VDDOUT must ensure that all VDD inputs, especially to the buck converters and LDOs, are connected to a bypass capacitor close to the pads. It is recommended to place at least 2x 1 µF capacitors close to the LDO supply pads and at least 1x 10 µF close to the buck VDD rail.

  Using a local power plane underneath the chip for VDDOUT might be considered.
- Adequate heat sink areas should be used for at least one terminal of the external overvoltage protection and / or active diode FETs.

28.3 LDOs and switched mode supplies

- Transient current loops area of the switched mode converters should be minimized.
- The common references (VDDREF capacitor, IREF resistor) should be placed close to DA9052, cross coupling to any noisy digital or analog trace must be avoided.
- Output capacitors of the LDOs should be placed close to the output pins. Small capacitors (for example 100 nF) are also required close to the input pins of the supplied devices.
- Care must be taken that no current is carried on feedback lines (buck output voltages VBUCKxx and boost current sense inputs (BOOST_SENSE_P/N).

28.4 Crystal oscillator

- The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetric traces.
- The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines are buried between two ground layers, surrounded by additional ground traces.

28.5 DA9052 thermal connection, land pad and stencil design

- The DA9052 provides a center ground plane, which is soldered directly to the PCB's center ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.
- Solder mask openings for the ground pad must be split by following a certain pattern like stripes or round shapes or squares, as a solid square would apply too much solder paste and the signal pads might not be connected properly.

  As DA9052 also provides different sizes of the signal pads, some adaption of the mask openings might be required as well (generally small pads a bit larger, large pads a bit smaller than the pad itself). Vias inside or next to the pads should be filled. An appropriately fine solder paste is required.

29 Definitions

29.1 Power dissipation and thermal design

When designing with the DA9052 consideration must be given to power dissipation as the level of integration of the device can result in high power dissipation when all functions are operating with high battery voltages. Exceeding the package power dissipation will result in the internal thermal sensor shutting down the device until it has cooled sufficiently.

The package includes thermal management paddle to enable improved heat spreading on the PCB.

Linear regulators operating with a high current and high differential voltage between input and output will dissipate the following power.

$$P_{diss} = (V_{in} - V_{out}) * I_{out}$$

Example – a regulator supplying 150 mA @ 2.8 V from a fully charged lithium battery (VDD=4.1 V):

P_{diss} = (4.1 V to 2.8 V) * 0.15 A = 195 mW

For switching regulators:

$$P_{out} = P_{in} * efficiency$$

Therefore:

$$P_{diss} = P_{in} - P_{out}$$

$$P_{diss} = \frac{P_{out}}{efficiency} - P_{out}$$

$$P_{diss} = P_{out} * \left(\frac{1}{efficiency} - 1\right)$$

$$P_{diss} = I_{out} * V_{out} * \left(\frac{1}{efficiency} - 1\right)$$

Example – an 85 % efficient buck converter supplying 1.2 V @ 400 mA

$$P_{diss} = 1.2V * 0.4A * \left(\frac{1}{0.85} - 1\right) = 85mW$$

As the DA9052 is a multiple regulator configuration each supply must be considered and summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

29.2 Regulator parameter - dropout voltage

In the DA9052 a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and when entering the dropout condition the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on the output voltage tracks the input voltage and regulation ceases. As the DA9052 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the ON resistance of the device. In the device the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm process Dialog are able to achieve very small pass transistor sizes for superior performance, Vdropout = Vin – Vout = Rdson * Iout.

When defining dropout voltage it is specified in relation to a minimum acceptable change in output voltage. For example all Dialog regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest ON resistance for internal device) and maximum current load.

29.3 Regulator parameter - power supply rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 A before reaching a steady state of 1.4 A (see below). Due to the battery having a finite internal resistance (typically 0.5 Ω) these current peaks induce ripple on the battery voltage of up to 500 mV. As the supplies to the audio and RF are derived from this supply it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions when the battery is at its minimum operating voltage, when there is minimum headroom available due to dropout.

29.4 Regulator parameter – line regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage ΔVreg (regulator operating with a constant load current) in response to a change in the input voltage ΔVin. Transient line regulation is a measurement of the peak change ΔVreg in regulated voltage seen when the line input voltage changes.

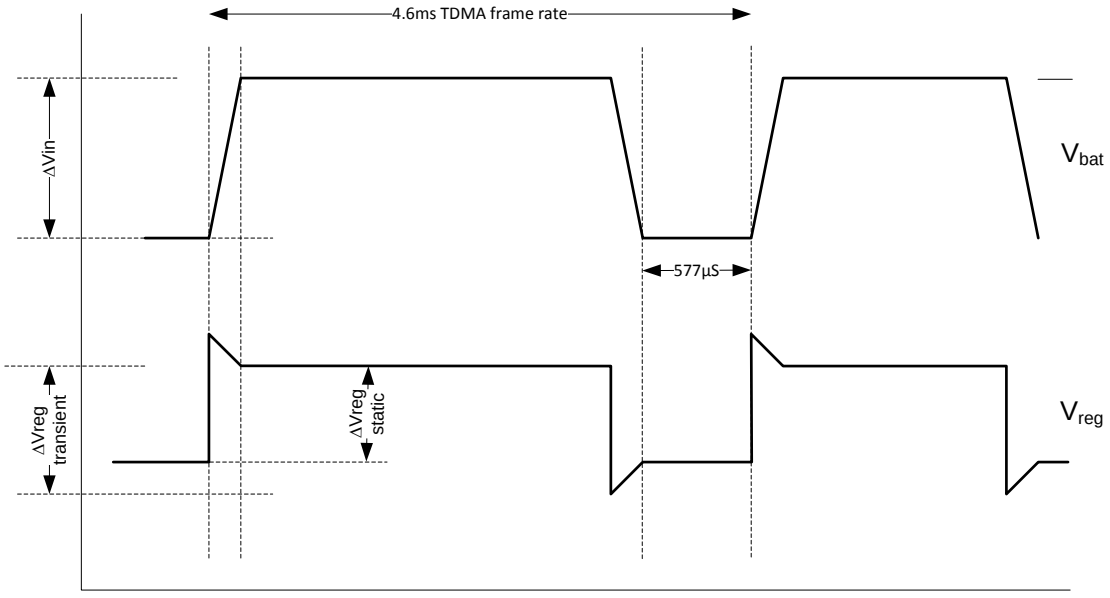


Figure 60: Static line regulation

29.5 Regulator parameter – load regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage ΔVreg in response to a change in the regulator loading Δload whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage ΔVreg seen when the regulator load changes.

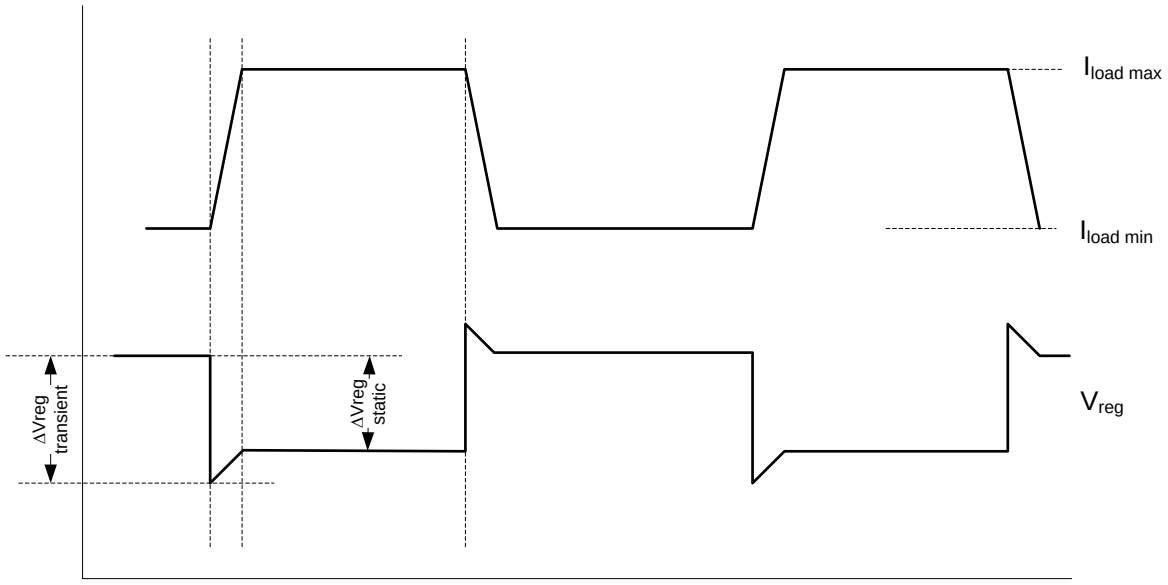


Figure 61: Static load regulation

30 Ordering information

Table 198: Ordering information

Part Number	Package	Shipment	Pack quantity
DA9052-xxC51	7*7 169 bump BGA Pb-free/green	tray	260
DA9052-xxC52	7*7 169 bump BGA Pb-free/green	T&R	3,000

30.1 Variants ordering information

DA9052 supports delivery of customized variants, please contact your local Dialog Semiconductor office or representative to discuss requirements.

30.2 Additional applications information

Please contact Dialog Semiconductor for latest application information on the DA9052 and other power management devices.

Revision history

Revision	Date	Description
DA9052-00-IDS21_091210	December 09	Inclusion of this table LED boost description modified to indicate that a greater number of LEDs can be driven under certain conditions. Corrected LDO1,6,7,9&10 noise figures Removed unnecessary charger buck load regulation from table. Changed R63 DELAY_TIME 111 is now reserved use only. Removed temperature range from each table, covered by operating conditions. Updated contact telephone numbers Corrected Register Overview table
DA9052-00-IDS21_100224	February 10	Inclusion of BGA package detail for Panasonic
DA9052-00-IDS21_100602	June 10	Removed draft status Updated Absolute Maximum Ratings Added a Note to VBUS Over-Voltage Protection and USB Suspend New section Operation without Battery Updated External Pass Transistors and Schottky Diodes
DA9052-00-IDS2B	Jun 11	Added BGA package option to P1. Updated Current limit specs for Bucks Removed comment on OTP registers above supply domain table Updated Digital I/O table. Updated GPIO characteristics table Updated Power on reset table Updated Buckcore Buckpro load regulation value updated Buckmem output voltage range/settings updated Buckmem pull down resistor value updated charger buck PFM current limit values updated Charger mode CV output voltage accuracy updated VCHG_EXCESS min value updated DCCC and active diode activation voltage Changed text for fixed threshold comparator updated WLED output current and accuracy updated Battery charger Iset currents removed VBAT_OVER from Flow chart updated recommended capacitor and transistor tables Corrected LDO VDD max values minor typo corrections
DA9052-00-IDS2C	Nov 12	Updated Boost max supply current Updated Buck Max supply voltage values Corrected ONKEY description to edge triggered Updated LDO5 dropout max voltage Updated WLED current matching value Updated 32 kHz Oscillator description Updated Active mode description Updated Layout recommendation VREF/IREF component description

Revision	Date	Description
		Updated Office Phone numbers.
2.5	13-Feb-2017	Product alignment and formatting amendments

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS compliance

Dialog Semiconductor complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.

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