General Description

DA9068 is a power management IC (PMIC) optimized for supplying systems with multi-core CPUs, I/O, DDR memory, and peripherals.

DA9068 contains an integrated Power Management Controller (PMC) for multiple power supplies (programmable LDO regulators and buck converters). DA9068 features a programmable power sequencer that handles start-up and shut-down sequences. Power mode transitions can be triggered with software control, GPIOs, or with the on-key. Several types of on-key presses can be detected to trigger different power-mode transitions.

All 25 linear regulators use Dialog's SmartMirror™ dynamic biasing technique which maintains high performance over a wide range of operating conditions and a power saving mode to minimize the quiescent current. The regulators have output voltages programmable via the device control interface.

The eight buck converters do not require external Schottky diodes and offer a power saving mode (PFM mode) for optimal light load efficiency. The DC-DC converters use either 2 MHz or 3 MHz switching frequency giving high efficiency and allowing the use of small external inductors (down to 1 µH).

Dynamic voltage control (DVC) allows supply voltages of DA9068 to be controlled dynamically according to the operating point of the system. The control can be realized via direct register writes through the I^2C interface or via GPIOs.

The real-time clock (RTC) with an external crystal oscillator provides time-keeping and alarm functions. In addition, a watchdog timer is included for system monitoring purposes.

Furthermore, DA9068 contains a general purpose 12-bit analog-to-digital converter (GPADC) and general purpose I/O pins (GPIO). These modules are implemented to support functions such as battery voltage supervision and device over-temperature protection.

DA9068 can be completely controlled from the host by software writes to registers, which brings high flexibility to the design of applications.

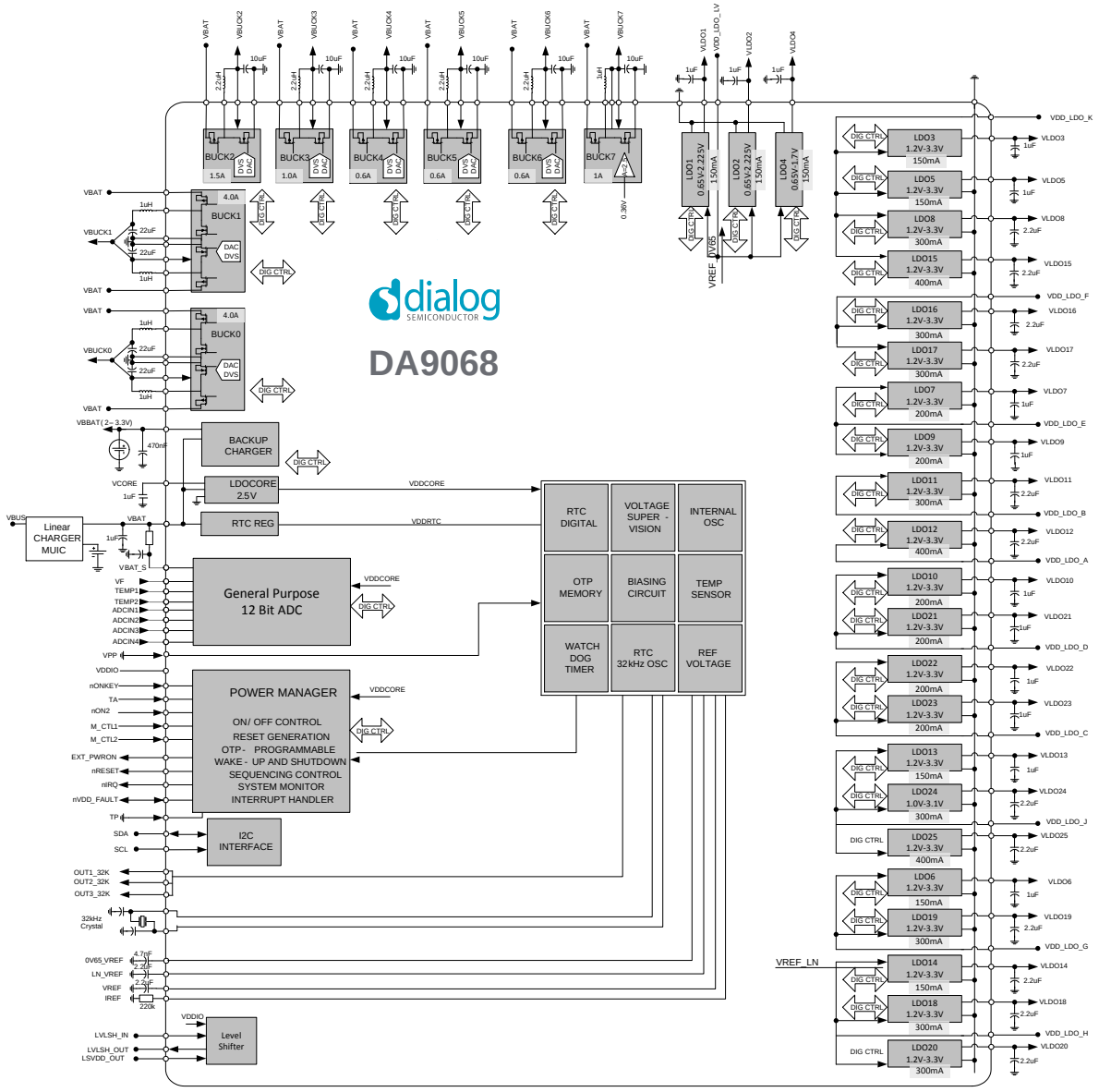
Key Features

- Input voltage 2.8 V to 4.5 V
- Eight buck converters with dynamic voltage control
  - 2 x 4000 mA Dual-Phase
  - 1 x 1500 mA
  - 1 x 1000 mA
  - 3 x 600 mA
  - 1 x 1000 mA
- 25 LDO regulators
  - 8 x 150 mA
  - 6 x 200 mA
  - 8 x 300 mA
  - 3 x 400 mA
- Programmable power-mode sequencer
- System supply and junction temperature monitoring
- 12-bit general purpose ADC
- Coin cell or super-capacitor charger
- Ultra-low-power real-time clock with alarm
- 32 kHz oscillator with an external crystal
- -30 °C to +85 °C temperature range
- WLCSP, 4 mm x 6 mm, 0.4 mm pitch

Applications

- Supply for multi-core application processors
- Smartphones and tablets

Block Diagram



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1 Pinout

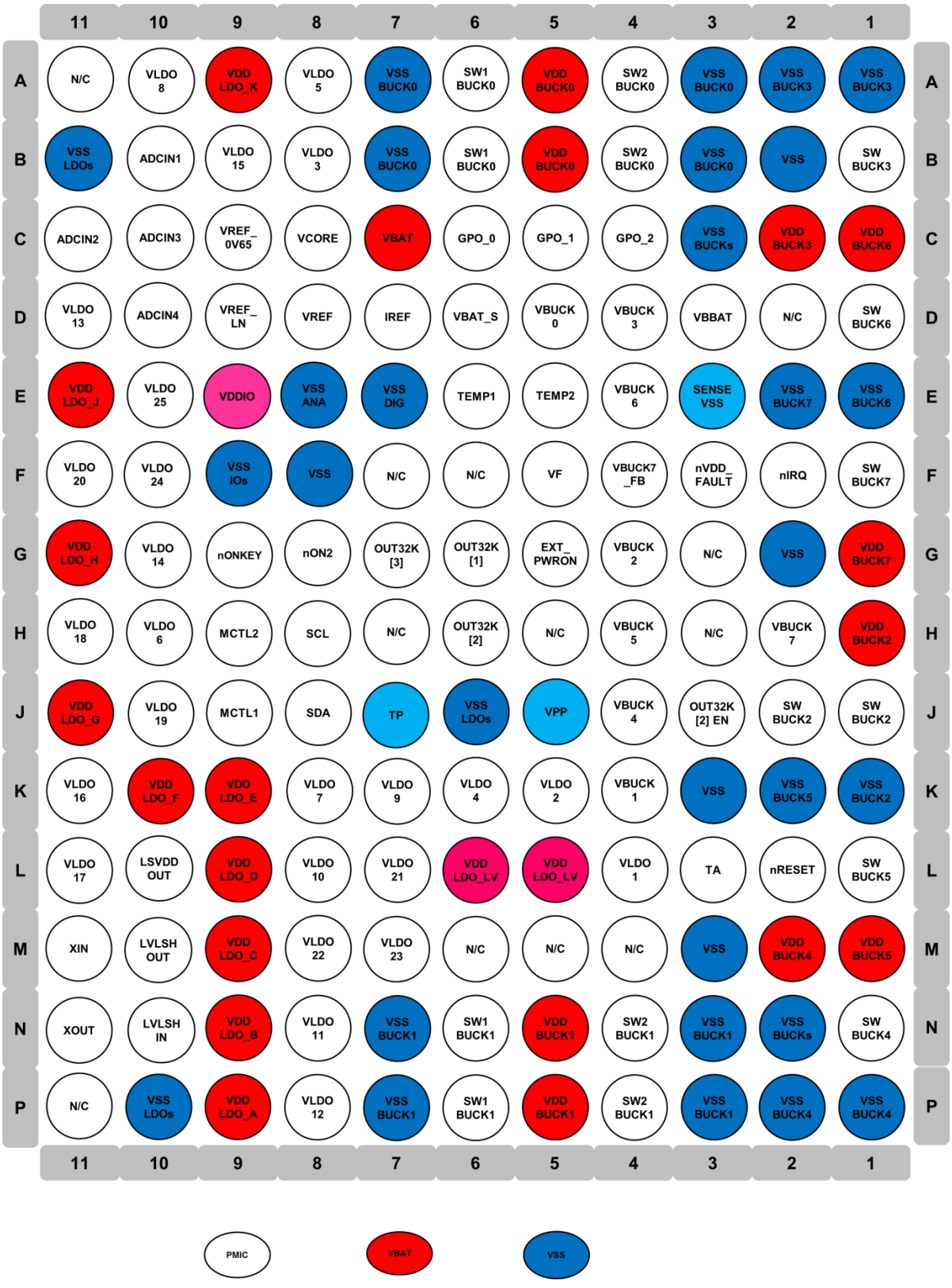

Figure 2: Connection Diagram

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
Power Manager			
G9	nONKEY	DI	ON/OFF key / HW input for watchdog supervision
J9	MCTL1	DI	Active high mode control input 1
H9	MCTL2	DI	Active high mode control input 2
L3	TA	DI	Travel adaptor wakeup control
G8	nON2	DI	Active low wakeup control
L2	nRESET	DO	Active low RESET towards host
G5	EXT_PWRON	DO	External regulator enable output
F2	nIRQ	DO	Active low IRQ line towards host
F3	nVDD_FAULT	DIO	Active low Indication for low supply voltage
J5	VPP	AI	Programming voltage
J7	TP	AI	Test pin / Power Commander mode enable
I^2C Interfaces			
H8	SCL	DI	I^2C clock
J8	SDA	DIO	I^2C data
Voltage Regulators			
L4	VLDO1	AO	LDO1 output voltage
K5	VLDO2	AO	LDO2 output voltage
B8	VLDO3	AO	LDO3 output voltage
K6	VLDO4	AO	LDO4 output voltage
A8	VLDO5	AO	LDO5 output voltage
H10	VLDO6	AO	LDO6 output voltage
K8	VLDO7	AO	LDO7 output voltage
A10	VLDO8	AO	LDO8 output voltage
K7	VLDO9	AO	LDO9 output voltage
L8	VLDO10	AO	LDO10 output voltage
N8	VLDO11	AO	LDO11 output voltage
P8	VLDO12	AO	LDO12 output voltage
D11	VLDO13	AO	LDO13 output voltage
G10	VLDO14	AO	LDO14 output voltage
B9	VLDO15	AO	LDO15 output voltage
K11	VLDO16	AO	LDO16 output voltage
L11	VLDO17	AO	LDO17 output voltage
H11	VLDO18	AO	LDO18 output voltage
J10	VLDO19	AO	LDO19 output voltage
F11	VLDO20	AO	LDO20 output voltage
L7	VLDO21	AO	LDO21 output voltage

Pin No.	Pin Name	Type (Table 2)	Description
M8	VLDO22	AO	LDO22 output voltage
M7	VLDO23	AO	LDO23 output voltage
F10	VLDO24	AO	LDO24 output voltage
E10	VLDO25	AO	LDO25 output voltage
P9	VDD_LDO_A	PWR	LDO12 supply voltage
N9	VDD_LDO_B	PWR	LDO11 supply voltage
M9	VDD_LDO_C	PWR	LDO22/23 supply voltage
L9	VDD_LDO_D	PWR	LDO10/21 supply voltage
K9	VDD_LDO_E	PWR	LDO7/9 supply voltage
K10	VDD_LDO_F	PWR	LDO6/18 supply voltage
J11	VDD_LDO_G	PWR	LDO17/19/20 supply voltage
G11	VDD_LDO_H	PWR	LDO14/16 supply voltage
E11	VDD_LDO_J	PWR	LDO13/24/25 supply voltage
A9	VDD_LDO_K	PWR	LDO3/5/8/15 supply voltage
L5, L6	VDD_LDO_LV	PWR	LDO1/2/4 supply voltage
C8	VCORE	AO	2.5 V internal PMIC supply
DC-DC Buck Converters			
D5	VBUCK0	AI	Buck0 sense input
A6, B6	SW1BUCK0	AO	Buck0 switching output – Phase 1
A4, B4	SW2BUCK0	AO	Buck0 switching output – Phase 2
A5, B5	VDD_BUCK0	PWR	Buck0 supply
A3, A7 B3, B7	VSS_BUCK0	VSS	Buck0 ground
K4	VBUCK1	AI	Buck1 sense input
N6, P6	SW1BUCK1	AO	Buck1 switching output – Phase 1
N4, P4	SW2BUCK1	AO	Buck1 switching output – Phase 2
N5, P5	VDD_BUCK1	PWR	Buck1 supply
N3, N7 P3, P7	VSS_BUCK1	VSS	Buck1 ground
G4	VBUCK2	AI	Buck2 sense input
J1, J2	SWBUCK2	AO	Buck2 switching output
H1	VDD_BUCK2	PWR	Buck2 supply
K1	VSS_BUCK2	VSS	Buck2 ground
D4	VBUCK3	AI	Buck3 sense input
B1	SWBUCK3	AO	Buck3 switching output
C2	VDD_BUCK3	PWR	Buck3 supply
A1, A2	VSS_BUCK3	VSS	Buck3 ground
J4	VBUCK4	AI	Buck4 sense input
N1	SWBUCK4	AO	Buck4 switching output

Pin No.	Pin Name	Type (Table 2)	Description
M2	VDD_BUCK4	PWR	Buck4 supply
P1, P2	VSS_BUCK4	VSS	Buck4 ground
H4	VBUCK5	AI	Buck5 sense input
L1	SWBUCK5	AO	Buck5 switching output
M1	VDD_BUCK5	PWR	Buck5 supply
K2	VSS_BUCK5	VSS	Buck5 ground
E4	VBUCK6	AI	Buck6 sense input
D1	SWBUCK6	AO	Buck6 switching output
C1	VDD_BUCK6	PWR	Buck6 supply
E1	VSS_BUCK6	VSS	Buck6 ground
RF Buck			
F4	VBUCK7_FB	AI	Buck7 sense input
F1	SWBUCK7	AO	Buck7 switching output
H2	VBUCK7	AO	Buck7 output
G1	VDD_BUCK7	PWR	Buck7 supply
E2	VSS_BUCK7	VSS	Buck7 ground
E3	VSS_SENSE	VSS	Buck7 GND sense input
GPADC			
D6	VBAT_S	AI	Sense connection to battery
E6	TEMP1	AI	Connection to primary NTC
E5	TEMP2	AI	Connection to secondary NTC
F5	VF	AI	Connection to battery detect circuit
B10	ADCIN1	AI	Voltage input
C11	ADCIN2	AI	Voltage input
C10	ADCIN3	AI	Voltage input
D10	ADCIN4	AI	Voltage input
Reference and Bias Generation			
D8	VREF	AO	Reference voltage output
D9	VREF_LN	AO	Low noise reference voltage
C9	VREF_0V65	AO	Aux reference voltage
D7	IREF	AO	Connection for R_{REF} resistor
XTAL Oscillator			
M11	XIN	AIO	32 kHz crystal connection
N11	XOUT	AIO	32 kHz crystal connection
G6	OUT1_32K	DO	32 kHz oscillator buffer output
H6	OUT2_32K	DO	32 kHz oscillator buffer output
G7	OUT3_32K	DO	32 kHz oscillator buffer output
J3	OUT2_32K_EN	DI	32 kHz oscillator buffer 2 enable

Pin No.	Pin Name	Type (Table 2)	Description
Back-Up Battery Charger			
D3	VBBAT	AIO	Backup battery connection Coin-Cell or Super-Cap
Level Shifter			
N10	LVLSH_IN	DI	Level-shifter input
M10	LVLSH_OUT	DO	Level-shifter output
L10	LSVDD_OUT	PWR	Level-shifter output supply
General Purpose outputs			
C6	GPO_0	DO	General purpose output 0
C5	GPO_1	DO	General purpose output 1
C4	GPO_2	DO	General purpose output 2
VDD			
C7	VBAT	PWR	PMIC supply rail
E9	VDDIO	PWR	I/O voltage supply
VSS			
B11, J6, P10	VSS_LDOs	VSS	VSS_LDO
B2, F8, G2, K3, M3	VSS	VSS	VSS_SUB
C3, N2	VSS_BUCKs	VSS	VSS_BUCK
F9	VSS_IOs	VSS	VSS_IO
E7	VSS_DIG	VSS	VSS_DIG
E8	VSS_ANA	VSS	VSS_ANA
NC			
A11, D2, F6, F7, G3, H3, H5, H7, M4, M5, M6, P11		NC	No connection

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
PWR	Power	VSS	Ground

2 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_{STG}	Storage temperature		-40	+95	°C
T_A	Operating temperature		-30	+85	°C
V_{BAT}	Power Supply Voltage	VBAT, VDD_LDO<x>, VDD_BUCK<x>	-0.3	5.5	V
V_{LDO_LV}		VDD_LDO_LV	-0.3	2.75	V
V_{DDIO}		VDDIO	1.6	5.5	V
V_{LVLSH}		LSVDD_OUT	1.2	5.5	V
V_{IN_D}	Input Pin Voltage	nONKEY, TA, nON2, MCTL1/2, OUT2_32K_EN, TP, LVLSH_IN, SDA, SCL	-0.3	V_{BAT} + 0.3	V
$V_{IN\_A\_LV}$		VBUCK<x>, TEMP1/2, VF, ADCIN1/2/3/4, XIN/XOUT	-0.3	2.75	V
$V_{IN\_A\_HV}$		VBAT_S, VBUCK7, VBUCK7_FB	-0.3	V_{BAT} + 0.3	V
P_{MAX}	Maximum power dissipation			1.2	W
V_{ESD_HBM}	ESD protection	HBM	2		kV
V_{ESD_CDM}		CDM	500		V

Note 1 Stresses beyond those listed under ‘Absolute Maximum Ratings’ may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating temperature		-30		+85	°C
V_{BAT}	Supply voltage	VBAT, VDD_LDO<x>, VDD_BUCK<x>			4.5	V
V_{LDO_LV}		VDD_LDO_LV	0		2.5	V
V_{DDIO}		VDDIO	1.5		3.3	V
V_{LVLSH}		LSVDD_OUT	1.2		3.3	V
V_{IN_D}	Input Pin Voltage	nONKEY, nON2	0		V_{BAT}	V
V_{IN_D}		TA, TP	0		5.0	V
V_{IN_D}		MCTL1/2, OUT2_32K_EN, LVLSH_IN, SDA, SCL	0		V_{DDIO}	V
$V_{IN\_A\_LV}$		VBUCK<x>, TEMP1/2, VF, ADCIN1/2/3/4, XIN/XOUT	0		2.5	V
$V_{IN\_A\_HV}$		VBAT_S, VBUCK7, VBUCK7_FB	0		V_{BAT}	V

3.1 Current Consumption

Table 5: Current Consumption

Operating Mode	Conditions (T_A = 25 °C) Note 1	Min	Typ	Max	Unit
RTC	No main battery. Supplied by BBAT		1.1	1.5	µA
NO-POWER	Voltage Detection ON V_{BAT} < 2.5 V		15	20	µA
POWERDOWN	RTC unit ON, All other blocks OFF (Note 2) $V_{BAT} < V_{DD\_FAULT\_LOWER}$		45	55	µA
MODE 1 (SLEEP)	Seven buck converters (PFM mode) Buck7 OFF 25 LDOs (Sleep Mode) RTC ON Clock module OFF (I^2C interface OFF)		250	300	µA
MODE 2 (ACTIVE)	Eight buck converters (PFM mode) 25 LDOs (Active Mode) RTC ON Clock module ON (I^2C interface ON)		550	650	µA

Note 1 Temperature dependent leakages may result in increased current consumption at higher T_A

Note 2 ACTIVE to POWERDOWN transition with register PD_DIS = 0xFF

4 Electrical Characteristics

4.1 Standard 150 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 6: LDO3, 5, 6, 13 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.2		3.3	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		1		uF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	150			mA
		$V_{DD} < 1.8$ V	100			
		$V_{DD} < 1.5$ V	50			
I_{MAX_SLEEP}	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	15			mA
I_{SHORT}	Short circuit current			300		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		5.5 + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in	I_{OUT} = 0 mA		2		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
	SLEEP mode	I_{OUT} = I_{MAX}/10		2 + 1 % I_{OUT}		
I_{Q_OFF}	Quiescent current when off				1	µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull-down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.2 Standard 200 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 7: LDO7, 9, 10, 21, 22, 23 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.2		3.3	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		1.0		uF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		+35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	200			mA
		$V_{DD} < 1.8$ V	133.3			
		$V_{DD} < 1.5$ V	66.7			
I_{MAX_SLEEP}	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	20			mA
I_{SHORT}	Short circuit current			400		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		5.5 µA + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in SLEEP mode	I_{OUT} = 0 mA		2		µA
		$I_{OUT} = I_{MAX}/10$		2 + 1 % I_{OUT}		

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current when off				1	µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.3 Standard 300 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 8: LDO8, 11, 16, 17, 18, 19, 20 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.2		3.3	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage(AC/DC) and temperature coefficients		2.2		µF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage(AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	300			mA
		$V_{DD} < 1.8$ V	200			
		$V_{DD} < 1.5$ V	100			
$I_{MAXSLEEP}$	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	30			mA
I_{SHORT}	Short circuit current			600		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		5.5.µA + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in SLEEP mode	I_{OUT} = 0 mA		2		µA
		$I_{OUT} = I_{MAX}/10$		2 + 1 % I_{OUT}		
I_{Q_OFF}	Quiescent current when off				1	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull-down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.4 Standard 400 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 9: LDO12, 15, 25 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.2		3.3	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		2.2		uF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	400			mA
		$V_{DD} < 1.8$ V	266.7			
		$V_{DD} < 1.5$ V	133.3			
$I_{MAXSLEEP}$	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	40			mA
I_{SHORT}	Short circuit current			800		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		7 µA + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in SLEEP mode	I_{OUT} = 0 mA		2.5		µA
		I_{OUT} = 0.1 I_{MAX}		2.5 + 1 % I_{OUT}		
I_{Q_OFF}	Quiescent current when off				1	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.5 Low Noise 150 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 10: LDO14 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.2		3.3	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		2.2		µF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	150			mA
		$V_{DD} < 1.8$ V	100			
		$V_{DD} < 1.5$ V	50			
$I_{MAXSLEEP}$	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	15			mA
I_{SHORT}	Short circuit current			300		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	60	70		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		40		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		10 µA + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in SLEEP mode	I_{OUT} = 0 mA		2		µA
		I_{OUT} = 0.1 I_{MAX}		2 + 1 % I_{OUT}		

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current when off				1	µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.6 Low Voltage 150 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{DD_LDO} = 1.5 V to 2.5 V.

Table 11: LDO1, 2, 4 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		1.2		2.5	V
V_{LDO1}, V_{LDO2}	Output voltage	Programmable in 25 mV steps $I_{OUT} = I_{MAX}$	0.65		2.225	V
V_{LDO4}	Output voltage	Programmable in 25 mV steps $I_{OUT} = I_{MAX}$	0.65		1.7	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		1.0		µF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current		150			mA
I_{SHORT}	Short circuit current			300		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = 1.5 V to 2.5 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 2.0 V to 2.5 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 2.5 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 2.5 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 2.5 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		2.5 µA + 0.5 % I_{OUT}		µA
I_{Q_OFF}	Quiescent current when off	Excluding High Temp. Leakage			1	µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull down resistance when off	V_{OUT} = 0.1 V		25		Ω

4.7 Low Voltage 300 mA LDO

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 12: LDO24 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage		2.0		5.0	V
		Supplied from buck	1.5		5.0	
V_{LDO}	Output voltage	Programmable in 50 mV steps $I_{OUT} = I_{MAX}$	1.0		3.1	V
V_{LDO_ACC}	Output accuracy	$I_{OUT} = I_{MAX}$	-3		3	%
C_{OUT}	Stabilization capacitor	Including voltage (AC/DC) and temperature coefficients		2.2		µF
C_{OUT_ACC}	Stabilization capacitor accuracy	Including voltage (AC/DC) and temperature coefficients	-55		35	%
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{MAX}	Maximum output current	$V_{DD} \geq 2.1$ V	300			mA
		$V_{DD} < 1.8$ V	200			
		$V_{DD} < 1.5$ V	100			
$I_{MAXSLEEP}$	Maximum output current	$V_{DD} \geq 1.8$ V Sleep mode	30			mA
I_{SHORT}	Short circuit current			600		mA
$V_{DROPOUT}$	Dropout voltage	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		200	300	mV
V_{S_LINE}	Static line regulation	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		25	50	mV
PSRR	Power supply rejection ratio	f = 10 Hz to 10 kHz V_{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$	50	60		dB
N	Output noise	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
I_{Q_ON}	Quiescent current when on	$I_{OUT} = I_{MAX}$		5.5.µA + 0.5 % I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current in SLEEP mode	I_{OUT} = 0 mA		2		µA
		I_{OUT} = 0.1 I_{MAX}		2 + 1 % I_{OUT}		
I_{Q_OFF}	Quiescent current when off				1	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	10 % to 90 %			300	µs
t_{OFF}	Turn-off time	90 % to 10 %			10	ms
R_{OFF}	Pull down resistance when off	V_{OUT} = 0.1 V V_{BAT} = 3.6 V		45		Ω

4.8 Buck0

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 13: Buck0 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
V_{DD}	Input voltage		2.8		4.5	V
$C_{1/2\_OUT}$	Output capacitance per phase	Including voltage and temperature coefficient	10	22		µF
$C_{1/2\_OUT\_ACC}$	Output capacitance accuracy per phase	Including voltage and temperature coefficient			30	%
ESR_{COUT}	Output capacitor ESR per phase	f > 100 kHz All capacitor and track impedances		10	25	mΩ
ESL_{COUT}	Output capacitor ESL per phase	f > 100 kHz All capacitor and track impedances			1.5	nH
$L_{1/2\_BUCK}$	Inductor value per phase			1.0		µH
$L_{1/2\_BUCK\_ACC}$	Inductor value accuracy per phase		-30		30	%
$R_{L1/2BUCK}$	Inductor resistance			75	120	mΩ
V_{BUCK0}	Output voltage	$I_{OUT} = I_{MAX}$	600	Note 1	1393.75	mV
V_{BUCK0_ACC}	Output voltage accuracy	Incl. static line / load regulation	-3	Note 2	+3	%
V_{OUT_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$		5	10	mV
V_{TR_LOAD}	Load regulation transient	I_{OUT} = 1 mA to 2000 mA V_{OUT} > 0.9 V L = 1 µH dI/dt = 250 mA/µs		25	35	mV
		I_{OUT} = 1 mA / 2000 mA V_{OUT} > 0.9 V L = 1 µH dI/dt = 1000 mA/µs		30	40	
V_{TR_LINE}	Line regulation transient	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 2000 mA $t_r = t_f$ =10 µs		5	10	mV
I_{MAX}	Output current		4000			mA
I_{LIM_P}	Peak inductor current limit per phase	BUCK0_SYNC_ILIM Programmable in steps of 80 mA	80		2560	mA
I_{Q_OFF}	Quiescent current when off				1	µA
I_{Q_ON}	Quiescent current in synchronous rectification mode	Open Loop Note 3		15		mA
f	Switching frequency			3		MHz
D	Switching duty cycle		10		95	%
t_{ON}	Turn-on time				1	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PD}	Output pull-down resistor	V_{OUT} = 0.5 V Can be switched off			100	Ω
η	Efficiency	I_{OUT} = 300 mA to I_{MAX} V_{DD} < 4.2 V	75	85		%
R_{PMOS}	PMOS on resistance	Including pin and routing			150	mΩ
R_{NMOS}	NMOS on resistance	Including pin and routing			50	mΩ
PFM Mode						
I_{MODE_SW}	PWM to PFM mode switching current	BUCK0_IAUTSLP Programmable in steps of 64 mA	64		1024	mA
I_{LIM}	Peak Inductor Current Limit per phase	BUCK0_SLEEP_ILIM Programmable in steps of 80 mA	80		2560	mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0 mA		35	45	µA
f_{OP}	Frequency of operation		0		5	MHz
η	Efficiency	I_{OUT} = 10 mA to 750 mA		85		%
t_{TRANS}	Mode transition time			16	18	µs

Note 1 Programmable in 6.25 mV steps. Programmable DVC ramp rate can be (25, 12.5, 6.25, 3.125) mV/µs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

4.9 Buck1

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 14: Buck1 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
V_{DD}	Input voltage		2.8		4.5	V
$C_{1/2\_OUT}$	Output capacitance per phase	Including voltage and temperature coefficient	10	22		µF
$C_{1/2\_OUT\_ACC}$	Output capacitance accuracy per phase	Including voltage and temperature coefficient			30	%
ESR_{COUT}	Output capacitor ESR per phase	f > 100 kHz All capacitor and track impedances		10	25	mΩ
ESL_{COUT}	Output capacitor ESL per phase	f > 100 kHz All capacitor and track impedances			1.5	nH
$L_{1/2\_BUCK}$	Inductor value per phase			1.0		µH
$L_{1/2\_BUCK\_ACC}$	Inductor value accuracy per phase		-30		30	%
$R_{L1/2BUCK}$	Inductor resistance			75	120	mΩ
V_{BUCK1}	Output voltage	$I_{OUT} = I_{MAX}$	600	Note 1	1393.75	mV
V_{BUCK1_ACC}	Output voltage accuracy	Incl. static line / load regulation	-3	Note 2	3	%
V_{OUT_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$		5	10	mV
V_{TR_LOAD}	Load regulation transient	I_{OUT} = 1 mA to 2000 mA V_{OUT} > 0.9 V L = 1 µH dI/dt = 250 mA/µs		25	35	mV
		I_{OUT} = 1 mA to 2000 mA V_{OUT} > 0.9 V L = 1 µH dI/dt = 1000 mA/µs		30	40	
V_{TR_LINE}	Line regulation transient	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 2000 mA $t_r = t_f$ = 10 µs		5	10	mV
I_{MAX}	Output current		4000			mA
I_{LIM_P}	Peak inductor current limit per phase	BUCK1_SYNC_ILIM Programmable in steps of 80 mA	80		2560	mA
I_{Q_OFF}	Quiescent current when off				1	µA
I_{Q_ON}	Quiescent current in synchronous rectification mode	Open Loop Note 3		15		mA
f	Switching frequency			3		MHz
D	Switching duty cycle		10		95	%
t_{ON}	Turn-on time				1	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PD}	Output pull down resistor	V_{OUT} = 0.5 V Can be switched off			100	Ω
η	Efficiency	I_{OUT} = 300 mA to I_{MAX} V_{DD} < 4.2 V	75	85		%
R_{PMOS}	On resistance PMOS	Incl. pin and routing			200	mΩ
R_{NMOS}	On resistance NMOS	Incl. pin and routing			70	mΩ
PFM Mode						
I_{MODE_SW}	PWM to PFM mode switching current	BUCK1_IAUTSLP Programmable in steps of 64 mA	64		1024	mA
I_{LIM}	Peak Inductor Current Limit per phase	BUCK1_SLEEP_ILIM Programmable in steps of 80 mA	80		2560	mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0		35	45	µA
f_{OP}	Frequency of operation		0		5	MHz
η	Efficiency	I_{OUT} = 10 mA to 750 mA		85		%
t_{TRANS}	Mode transition time			16	18	µs

Note 1 Programmable in 6.25 mV steps. Programmable DVC ramp rate can be (25, 12.5, 6.25, 3.125) mV/µs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

4.10 Buck2

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 15: Buck2 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
V_{DD}	Input voltage		2.8		4.5	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient	4.7	10		µF
C_{OUT_ACC}	Output capacitance accuracy	Including voltage and temperature coefficient			30	%
ESR_{COUT}	Output capacitor ESR	f > 100 kHz All capacitor and track impedances		10	25	mΩ
ESL_{COUT}	Output capacitor ESL	f > 100 kHz All capacitor and track impedances			1.5	nH
L_{BUCK}	Inductor value			2.2		µH
L_{BUCK_ACC}	Inductor value accuracy		-30		30	%
R_{LBUCK}	Inductor resistance			75	120	mΩ
V_{BUCK2}	Output voltage	I_{OUT} = I_{MAX}	600	Note 1	1393.75	mV
V_{BUCK2_ACC}	Output voltage accuracy	Incl. static line / load regulation	-3	Note 2	3	%
V_{OUT_RPL}	Output voltage ripple	I_{OUT} = I_{MAX}		10		mV
V_{TR_LOAD}	Load regulation transient	I_{OUT} = 1 mA to 750 mA V_{OUT} > 0.9 V L = 2.2 µH dI/dt = 50 mA/µs		20	30	mV
		I_{OUT} = 1 mA to 750 mA V_{OUT} > 0.9 V L = 2.2 µH dI/dt = 250 mA/µs		30	40	
V_{TR_LINE}	Line regulation transient	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 750 mA t_r = t_f = 10 µs		5	10	mV
I_{MAX}	Output current		1500			mA
I_{LIM_P}	Peak inductor current limit	BUCK2_SYNC_ILIM = 00		1100		mA
		BUCK2_SYNC_ILIM = 01		1650		
		BUCK2_SYNC_ILIM = 10		2200		
		BUCK2_SYNC_ILIM = 11		2750		
$I_{LIM\_P\_ACC}$	Peak inductor current limit accuracy		-20		20	%
I_{Q_OFF}	Quiescent current when off				1	µA
I_{Q_ON}	Quiescent current in synchronous rectification mode	Open Loop Note 3		5		mA
f	Switching frequency			2		MHz

Parameter	Description	Conditions	Min	Typ	Max	Unit
D	Switching duty cycle		10		95	%
t_{ON}	Turn-on time				1	ms
R_{PD}	Output pull down resistor	V_{OUT} = 0.5 V Can be switched off			200	Ω
η	Efficiency	I_{OUT} = 150 mA to I_{MAX} V_{DD} < 4.2 V	75	85		%
RP_{MOS}	On resistance PMOS	Incl. pin and routing			200	mΩ
R_{NMOS}	On resistance NMOS	Incl. pin and routing			70	mΩ
PFM Mode						
I_{MODE_SW}	PWM to PFM mode switching current			100		mA
I_{LIM}	Peak inductor current limit			200		mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0		25	35	µA
f	Frequency of operation		0		5	MHz
η	Efficiency	I_{OUT} = 10 mA to I_{MODE_SW}		85		%
t_{TRANS}	Mode transition time			16	18	µs

Note 1 Programmable in 6.25 mV steps. DVC ramp rate can be (25, 12.5, 6.25, 3.125) mV/µs.

Note 2 Limited to +-35mV at low voltage settings

Note 3 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

4.11 Buck3

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 16: Buck3 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
VDD	Input voltage		2.8		4.5	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient	4.7	10		µF
C_{OUT_ACC}	Output capacitance accuracy	Including voltage and temperature coefficient			30	%
ESR_{COUT}	Output capacitor ESR	f > 100 kHz All capacitor and track impedances		10	25	mΩ
ESL_{COUT}	Output capacitor ESL	f > 100 kHz All capacitor and track impedances			1.5	nH
L_{BUCK}	Inductor value			2.2		µH
L_{BUCK_ACC}	Inductor value		-30		30	%
R_{LBUCK}	Inductor resistance			75	120	mΩ
V_{BUCK3}	Output voltage	$I_{OUT} = I_{MAX}$	600	Note 1	1393.75	mV
V_{BUCK3_ACC}	Output voltage accuracy	Incl. static line / load regulation	-3	Note 2	+3	%
V_{OUT_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$		10		mV
V_{TR_LOAD}	Load regulation transient	I_{OUT} = 1 mA to 500 mA dI/dt = 50 mA/µs		20	30	mV
		I_{OUT} = 1 mA to 500 mA dI/dt = 250 mA/µs		30	40	
V_{TR_LINE}	Line regulation transient	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA $t_r = t_f$ = 10 µs		5	10	mV
I_{OUT}	Output current		1000			mA
I_{LIM_P}	Peak inductor current limit	BUCK3_SYNC_ILIM=00		750		mA
		BUCK3_SYNC_ILIM=01		1100		
		BUCK3_SYNC_ILIM=10		1450		
		BUCK3_SYNC_ILIM=11		1800		
$I_{LIM\_P\_ACC}$	Peak inductor current limit accuracy		-20		20	%
I_{Q_OFF}	Quiescent current when off				1	µA
I_{Q_ON}	Quiescent current in synchronous rectification mode	Open Loop Note 3		3.5		mA
f	Switching frequency			2		MHz
D	Switching duty cycle		10		95	%
t_{ON}	Turn-on time				1	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PD}	Output pull down resistor	V_{OUT} = 0.5 V Can be switched off			100	Ω
η	Efficiency	I_{OUT} = 150 mA to I_{MAX} V_{DD} < 4.2 V	75	85		%
R_{PMOS}	On resistance PMOS	Incl. pin and routing			300	mΩ
R_{NMOS}	On resistance NMOS	Incl. pin and routing			100	mΩ
PFM Mode						
I_{MODE_SW}	PWM to PFM mode switching current			100		mA
I_{LIM}	Peak inductor current limit			200		mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0		25	35	µA
f	Frequency of operation		0		5	MHz
η	Efficiency	I_{OUT} = 10 mA to I_{MODE_SW}		85		%
t_{TRANS}	Mode transition time			16	18	µs

Note 1 Programmable in 6.25 mV steps. DVC ramp rate can be (25, 12.5, 6.25, or 3.125) mV/µs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

4.12 Buck4, Buck5, Buck6

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 17: Buck4, Buck5, Buck6 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
V_{DD}	Input voltage		2.8		4.5	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient	4.7	10		µF
C_{OUT_ACC}	Output capacitance accuracy	Including voltage and temperature coefficient			30	%
ESR_{COUT}	Output capacitor ESR	f > 100 kHz All capacitor and track impedances		10	25	mΩ
ESL_{COUT}	Output capacitor ESL	f > 100 kHz All capacitor and track impedances			1.5	nH
L_{BUCK}	Inductor value			2.2		µH
L_{BUCK_ACC}	Inductor value		-30		30	%
R_{LBUCK}	Inductor resistance			75	120	mΩ
V_{BUCK}	Output voltage	$I_{OUT} = I_{MAX}$	1400	Note 1	2193.75	mV
V_{BUCK_ACC}	Output voltage accuracy	Incl. static line / load regulation	-3	Note 2	+3	%
V_{OUT_RPL}	Output voltage ripple	$I_{OUT} = I_{MAX}$		10		mV
V_{TR_LOAD}	Load regulation transient	I_{OUT} = 1 mA to 300 mA dI/dt = 50 mA/µs		20	30	mV
		I_{OUT} = 1 mA to 300 mA dI/dt = 250 mA/µs		30	40	
V_{TR_LINE}	Line regulation transient	VDD = 3.0 V to 3.6 V I_{OUT} = 300 mA $t_r = t_f$ = 10 µs		5	10	mV
I_{MAX}	Output current		600			mA
I_{LIM_P}	Peak inductor current limit	BUCK4/5/6_SYNC_ILIM=0 0		350		mA
		BUCK4/5/6_SYNC_ILIM=0 1		550		
		BUCK4/5/6_SYNC_ILIM=1 0		750		
		BUCK4/5/6_SYNC_ILIM=1 1		950		
$I_{LIM\_P\_ACC}$	Peak inductor current limit accuracy		-20		20	%
I_{Q_OFF}	Quiescent current when off				1	µA
I_{Q_ON}	Quiescent current in synchronous rectification mode	Open Loop Note 3		2.5		mA
f	Switching frequency			2		MHz

Parameter	Description	Conditions	Min	Typ	Max	Unit
D	Switching duty cycle		10		95	%
t_{ON}	Turn-on time				1	ms
R_{PD}	Output pull down resistor	V_{OUT} = 0.5 V Can be switched off			200	Ω
η	Efficiency	I_{OUT} = 150 mA to I_{MAX} V_{DD} < 4.2 V	75	85		%
R_{PMOS}	On resistance PMOS	Incl. pin and routing			600	mΩ
R_{NMOS}	On resistance NMOS	Incl. pin and routing			300	mΩ
PFM Mode						
I_{MODE_SW}	PWM to PFM mode switching current			100		mA
I_{LIM}	Peak inductor current limit			200		mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0		25	35	µA
f	Frequency of operation		0		5	MHz
η	Efficiency	I_{OUT} = 10 mA to I_{MODE_SW}		85		%
t_{TRANS}	Mode transition time			16	18	µs

Note 1 Programmable in 6.25 mV steps. DVC ramp rate can be (25, 12.5, 6.25, or 3.125) mV/µs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

4.13 Buck7

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.8 V to 4.5 V.

Table 18: Buck7 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
ACTIVE Mode						
V_{DD}	Input voltage		2.8		4.5	V
C_{OUT}	Output capacitance	Including voltage and temperature coefficient		10		µF
C_{OUT_ACC}	Output capacitance accuracy	Including voltage and temperature coefficient	-55		30	%
ESR_{COUT}	Output capacitor ESR	f > 100 kHz All capacitor and track impedances		5	10	mΩ
L_{BUCK}	Inductor value	f = 6 MHz		0.5		µH
		f = 3 MHz		1.0		
L_{BUCK_ACC}	Inductor value accuracy		-30		30	%
R_{LBUCK}	Inductor resistance			50	125	mΩ
V_{BUCK7}	Output voltage			0.9		V
V_{BUCK7_ACC}	Output voltage accuracy	Incl. static line / load regulation	-50		50	mV
I_{MAX}	Output current		1000			mA
I_{LIM_P}	Peak inductor current limit	BUCK7_ILIM_P=00		1.0		A
		BUCK7_ILIM_P=01		1.5		
		BUCK7_ILIM_P=10		2.0		
		BUCK7_ILIM_P=11		2.5		
$I_{LIM\_P\_ACC}$	Peak inductor current limit		-30		30	%
I_{LIM_N}	NMOS negative current limit	BUCK7_ILIM_N=00		-0.6		A
		BUCK7_ILIM_N=01		-1.1		
		BUCK7_ILIM_N=10		-1.6		
		BUCK7_ILIM_N=11		-2.1		
$I_{LIM\_N\_ACC}$	NMOS negative current limit		-30		30	%
R_{PMOS}	PMOS On resistance	Including pin and routing		0.2	0.4	Ω
R_{NMOS}	NMOS On resistance	Including pin and routing		0.12	0.25	Ω
I_{Q_OFF}	Quiescent current when off	RFBUCK_EN = 0			1	µA
I_{Q_ON}	Quiescent current in Sync (PWM) mode	Open Loop Note 1		1.1		mA
f	Switching frequency	L = 0.5 µH		6		MHz
		L = 1.0 µH		3		
t_{ON}	Turn-on time	C_{OUT} = 4.7 µF V_{IN} = 3.7 V, from RFBUCK_EN = 1 to 95 %V_{OUT}		15	20	µs

Parameter	Description	Conditions	Min	Typ	Max	Unit
η	Efficiency	V_{IN} = 3.8 V V_{OUT} = 0.9 V I_{OUT} = 500 mA		85		%
V_{SYNC}	PFM to PWM voltage threshold Note 2	Forced PWM Mode V_{SYNC} < 360 mV	160		460	mV
PFM Mode						
V_{SLEEP}	PWM to PFM voltage threshold Note 2	Forced PFM Mode V_{SLEEP} > 360 mV	160		460	mV
I_{SLEEP}	Mode switching current threshold	Auto Mode V_{SLEEP} < 360 mV < V_{SYNC}	75		125	mA
I_{Q_PFM}	Quiescent current in PFM mode	I_{OUT} = 0		90		µA
η	Efficiency	V_{IN} = 3.8 V V_{OUT} = 0.9 V I_{OUT} = 22.5 mA		80 (TBC)		%

Note 1 Open loop PWM. In closed loop configuration, switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

Note 2 Programmable in 20 mV steps using register BUCKRF_THR.

4.14 GPADC

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{CORE} = 2.5 V.

Table 19: GPADC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
	ADC resolution	Manual Conversion		12		bit
V_{ACC}	Absolute accuracy		12		15	mV
INL	Integral non-linearity			±2	±4	LSB
DNL	Differential non-linearity			±1	±2	LSB
V_{IN}	ADC supply voltage			2.5		V
V_{ADC_REF}	ADC reference voltage			2.5		V
I_{OUT}	ADC operating current	During conversion		135		µA
I_{PWR_DWN}	Power down current				1	µA
f_{CLK}	ADC clock			0.5		MHz
t_{AUTO_ZERO}	Auto-zero time			10		µs
t_{SAMP}	Total sampling time	Including the Auto-Zero time		26		µs
t_{CONV}	Conversion time			24		µs
t_{TOT}	Total ADC conversion time			50		µs
R_S	Maximum source impedance	Note 1			200	kΩ
R_{INT}	Internal Mux resistance			5		kΩ
C_S	Internal sampling capacitor			10		pF
C_{INT}	Total input capacitance	Parasitic and pad capacitance included		11		pF
t_{ACQ}	Acquisition time	~9τ = 9 x (R_S + R_{INT}) x C_{INT}			20	µs
V_{VBAT}	VBAT voltage range	ADC=[(VBAT-2.5) x 0.5] x 4095 gain = 1.25	2.5		4.5	V
V_{TEMP}	TEMP1/2 voltage range	ADC=[V_{IN} / 2.5] x 4095 gain = 1.0	0		2.5	V
V_{VF}	VF voltage range	ADC=[V_{IN} / 2.5] x 4095 gain = 1.0	0		2.5	V
V_{ADCIN}	ADCIN1/2/3/4 voltage range	ADC=[V_{IN} / 2.5] x 4095 gain = 1.0	0		2.5	V
	Inter channel isolation			60		dB
I_{SRC_ADC}	TEMP / VF current source			50		µA
$I_{SRC\_ADC\_ACC}$	TEMP / VF current source accuracy		-2.5		2.5	%

Note 1 R_S – impedance of the external source sampled by the ADC.

4.15 Voltage and Temperature Monitoring

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5 V.

Table 20: Temperature Monitoring Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
$V_{DD\_FAULT\_LOWER}$	VDD_FAULT lower level Note 1		2.4 Note 2	2.9	3.15	V
$V_{DD\_FAULT\_UPPER}$	VDD_FAULT upper level Note 1		$V_{DD\_FAULT\_LOWER}$ + 150 mV		$V_{DD\_FAULT\_LOWER}$ + 300 mV	V
$V_{DD\_FAULT\_CRIT}$	VDD_FAULT critical level Note 1		2.2	$V_{DD\_FAULT\_LOWER}$ - 200 mV	2.95	V
V_{DD_MON}	VDD_MON level			$V_{DD\_FAULT\_UPPER}$ - 3 %		V
T_{CRIT}	Critical temperature level		125	140	155	°C

Note 1 The VDD_FAULT threshold levels are configured via the VDD_FAULT_ADJ and VDD_HYST_ADJ register controls.

Note 2 Settings lower than 2.85 V are intended for test purposes only.

4.16 RTC

Unless otherwise noted, T_A = +25 °C, and V_{DDRTC} = 1.5 V to 2.75 V.

NOTE
V_{DDRTC} is derived from either V_{BAT} or V_{BBAT}.

Table 21: RTC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{DDRTC}	RTC domain current consumption	from V_{BBAT}		1.3		µA
		from V_{BAT}		7		
t_{BBAT}	Backup time	Supercap connected (22 µAh capacity, V_{BBAT} = 3.3 V to 2.0 V)	12			h

4.17 Crystal Oscillator

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{DDRTC} = 1.5 V to 2.75 V.

NOTE
V_{DDRTC} is derived from either V_{BAT} or V_{BBAT}.

Table 22: Crystal Oscillator Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DDRTC}	Supply voltage		1.5		2.75	V
f_{OSC}	Oscillator frequency			32.768		kHz
J_{PER}	Clock jitter (Peak-to-peak period jitter, 1000 samples)	High performance mode			25	ns
		Low power mode			100	
C_{XTAL}	Crystal capacitance			7	9	pF
R_{XTAL}	Crystal ESR				100	kΩ
P_{MAX}	Crystal drive level		1			µW
t_{START}	Start-up time			1	2	s
I_{DD}	Current consumption	High performance mode		1		µA
		Low power mode		0.65		

4.18 Backup Battery Charger

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.0 V.

Table 23: Backup Battery Charger Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SET_BCHG}	Backup battery charging current set by BBCHG_ISET	V_{BAT} = 3.6 V V_{BBAT} = 2.5 V	100		6000	µA
V_{SET_BCHG}	Charger termination voltage set by BBCHG_VSET	V_{BAT} = 3.6 V	1.8		3.3	V
I_{SHORT}	Backup battery short circuit current	V_{BBAT} = 0 V		9		mA
C_{OUT}	Stabilization capacitor		-55%	470	+35%	nF
ESR_{COUT}	ESR of capacitor	f > 1 MHz			0.1	Ω
I_{THR_LPM}	Low power mode activation current threshold			65		µA
V_{DEACT_LPM}	Low power mode de-activation voltage	V_{SET} - V_{BBAT}		200		mV
I_Q	Quiescent current from VBAT	I_{OUT} > 100 µA		5.25 + 1.75 % I_{OUT}		µA
		I_{OUT} < 50 µA		5.25 + 1.50 % I_{OUT}		
dV_{BS_HYST}	Bulk-switch hysteresis	V_{BAT} - V_{BBAT}		65		mV
I_{Q_BS}	Bulk-switch quiescent current	V_{BAT} = 0 V		0.35		µA
		V_{BBAT} = 0 V		1.5		

4.19 GPIO

Unless otherwise noted, T_A = -30 °C to +85 °C, V_{BAT} = 2.5 V to 5.5 V, and V_{DDIO} = 1.6 V to 3.6 V.

Table 24: GPIO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	M_CTL1, M_CTL2, OUT2_32K_EN, nVDDFAULT Input high voltage	VDDINT mode	1.0		VDDIO	V
		VDDIO mode	0.7 * VDDIO		VDDIO	
V_{IH}	nONKEY, nON2 Input high voltage	VDDINT mode	1.0		VBAT	V
		VDDIO mode	0.7 * VDDIO		VBAT	
V_{IH}	TA Input high voltage	VDDINT mode	1.0		5.0	V
		VDDIO mode	0.7 * VDDIO		5.0	
V_{IL}	M_CTL1, M_CTL2, nONKEY, nON2, TA, OUT2_32K_EN, nVDDFAULT Input low voltage	VDDINT mode	-0.3		0.4	V
		VDDIO mode	-0.3		0.3 * VDDIO	
V_{OH}	nIRQ, nRESET, nVDD_FAULT, OUT1_32K, OUT2_32K, OUT3_32K, GPO_0/1/2 Output high voltage	I_{LOAD} = 1 mA	0.8 * VDDIO		VDDIO	V
V_{OL}	nIRQ, nRESET, nVDD_FAULT OUT1_32K, OUT2_32K, OUT3_32K, GPO_0/1/2 Output low voltage	I_{LOAD} = -1 mA	0		0.3	V
I_{OUT}	Source current capability GPOs, PM I/Os	$V_{OUT} = V_{DDIO}$ - 0.5 V		-1 Note 1		mA
I_{IN}	Sink current capability GPOs, PM I/Os	V_{OUT} = 0.5 V		1		mA
R_{UP}	I/O pull-up resistor	V_{DDIO} = 1.5 V	100	180	300	kΩ
		V_{DDIO} = 1.8 V	70	120	170	
		V_{DDIO} = 3.3 V	25	40	60	
R_{PU}	Pull-up resistor nONKEY, nON2		140	200	260	kΩ
f	Maximum I/O frequency	Input and output Signals	10			MHz

Note 1 For V_{DDIO} < 1.5 V, the source current is limited to 0.5 mA.

4.20 Level Shifter

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.5 V.

Table 25: Level Shifter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{LSVDD_OUT}	Level shifter supply voltage		1.2		2.5	V
V_{IH}	LVLSH_IN Input high voltage	VDDINT mode	1.0		VDDIO	V
		VDDIO mode	0.7 * VDDIO		VDDIO	
V_{IL}	LVLSH_IN Input low voltage	VDDINT mode	-0.3		0.4	V
		VDDIO mode	-0.3		0.3 * VDDIO	
V_{OH}	LVLSH_OUT Output high voltage	I_{LOAD} = 1 mA	0.8 * V_{LSVDD_OUT}		V_{LSVDD_OUT}	V
V_{OL}	LVLSH_OUT Output low voltage	I_{LOAD} = -1 mA	0		0.3	V
I_{OUT}	Source current capability	V_{LVLSH_OUT} = V_{LSVDD_OUT} - 0.5 V		-1		mA
	Sink current capability	V_{LVLSH_OUT} = 0.5 V		1		mA
f	Maximum I/O frequency		10			MHz

4.21 2-Wire (I^2C) Interface

Unless otherwise noted, T_A = -30 °C to +85 °C, and V_{BAT} = 2.5 V to 5.5 V.

Table 26: 2-Wire (I^2C) Interface Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	SCL, SDA Input high voltage	VDDINT mode	1.0		V_{DDIO}	V
		VDDIO mode	0.7 * V_{DDIO}		V_{DDIO}	
V_{IL}	SCL, SDA Input low voltage	VDDINT mode	-0.3		0.4	V
		VDDIO mode	-0.3		0.3 * V_{DDIO}	
V_{OL}	SDA Output low voltage	Standard 1 kΩ pull-up to V_{DD_EXT}	0		0.2 * V_{DD_EXT}	V
t_{STOP_START}	Bus free time STOP to START		1.3			µs
C_{LOAD}	Bus line capacitive load				100	pF
Standard Mode						
f_{CLK}	CLK clock frequency		1		400	kHz
t_{STOP_START}	Bus free time STOP to START		1.3			µs
t_{START_SETUP}	Start condition set-up time		0.6			µs
t_{START_HOLD}	Start condition hold time		0.6			µs
t_{CLK_LO}	CLK low time		1.3			µs
t_{CLK_HI}	CLK high time		0.6			µs
t_{RISE_FALL}	2-wire CLK and DATA rise/fall time				300	ns
t_{DATA_SETUP}	Data set-up time		100			ns
t_{DATA_HOLD}	Data hold-time		0			ns
t_{STOP_SETUP}	Stop condition set-up time		0.6			µs
High Speed Mode						
f_{CLK}	CLK clock frequency		1		1700	kHz
t_{START_SETUP}	Start condition set-up time		160			ns
t_{START_HOLD}	Start condition hold time		160			ns
t_{CLK_LO}	CLK low time		160			ns
t_{CLK_HI}	CLK high time		60			ns
$t_{RISE\_FALL\_CLK}$	HS-2-WIRE CLK rise/fall time				40	ns
$t_{RISE\_FALL\_DATA}$	HS-2-WIRE DATA rise/fall time				80	ns
t_{DATA_SETUP}	Data set-up time		10			ns
t_{DATA_HOLD}	Data hold-time		0			ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{STOP_SETUP}	Stop condition set-up time		16			ns

5 Functional Description

5.1 Switching Regulators (DC/DC Buck Converters)

Table 27: Switching Regulators

Block	V_{OUT} (V)	I_{OUT} (mA)	External Components	Control Note 1
Buck0 Dual-Phase	0.6 to 1.4	PWM: 4000 PFM: 2000	L1/L2 = 1.0 µH / C1/C2$_{OUT}$ = 22 µF	SC/I^{2}C
Buck1 Dual-Phase	0.6 to 1.4	PWM: 4000 PFM: 2000	L1/L2 = 1.0 µH / C1/C2$_{OUT}$ = 22 µF	SC/I^{2}C
Buck2	0.6 to 1.4	1500	L = 2.2 µH / C_{OUT} = 10 µF	SC/I^{2}C
Buck3	0.6 to 1.4	1000	L = 2.2 µH / C_{OUT} = 10 µF	SC/I^{2}C
Buck4	1.4 to 2.2	600	L = 2.2 µH / C_{OUT} = 10 µF	SC/I^{2}C
Buck5	1.4 to 2.2	600	L = 2.2 µH / C_{OUT} = 10 µF	SC/I^{2}C
Buck6	1.4 to 2.2	600	L = 2.2 µH / C_{OUT} = 10 µF	SC/I^{2}C
Buck7 RF Buck	0.9	PWM: 1000 PFM: 100	L = 1.0 µH / C_{OUT} = 10 µF	I^{2}C

Note 1 In this column, SC = PMIC Sequencer Control

5.1.1 Single-Phase Switching Regulators

DC-DC converters Buck2 to Buck6 (see Figure 3) are high efficiency synchronous step-down regulators operating at 2 MHz frequency and providing individual output voltages with ±3 % accuracy. The default output voltages of these regulators are loaded from OTP and can be programmed in 6.25 mV steps. The switching frequency is chosen to be high enough to allow the use of a small 2.2 µH inductor.

The operating mode of the buck converter is selected via the buck control register bits. The buck converter can be forced to operate in either Synchronous mode (PWM) or Sleep mode (PFM). Additionally, the buck converter has an Automatic mode where it will switch between Synchronous and Sleep modes depending on the load current. In Sleep mode, these buck converters always work in PFM. An internal zero-crossing comparator is used to time the turn-off of the NMOS output transistor, thereby removing the need for an external Schottky diode. The quiescent current for all these buck converters in PFM is 25 µA.

All DA9068 single-phase buck converters have programmable pull-down resistors. These are enabled when the buck is turned off and have a nominal value of 100 Ω. These pull-down resistors can be disabled via the PD_DIS control in the BUCK<x>_CONF1 registers.

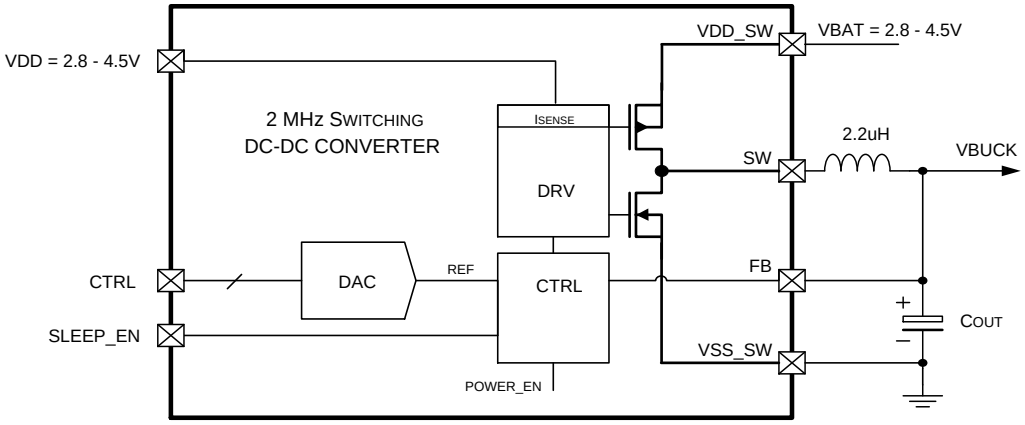

Figure 3: Single-Phase Buck Block Diagram

5.1.2 Multi-Phase Switching Regulators

DC-DC converters Buck0 and Buck1 (see Figure 4) are dual-phase high efficiency synchronous step-down regulators operating at 3 MHz frequency and providing output voltages with ±3 % accuracy. The default output voltage is loaded from OTP and can be programmed in 6.25 mV steps. The dual-phase architecture and the chosen operating frequency allow the use of small 1 µH inductors, and provide reduced output voltage ripple even at high current loads (up to 4 A [2 A per phase]).

These bucks feature programmable mode of operation which can be set to either Synchronous mode (PWM) or Sleep mode (PFM). Additionally, these bucks can be configured in Automatic mode where they switch between Synchronous and Sleep mode depending on the load current. The mode transition current threshold is also programmable.

The typical quiescent current of the converters in PFM mode is 35 µA.

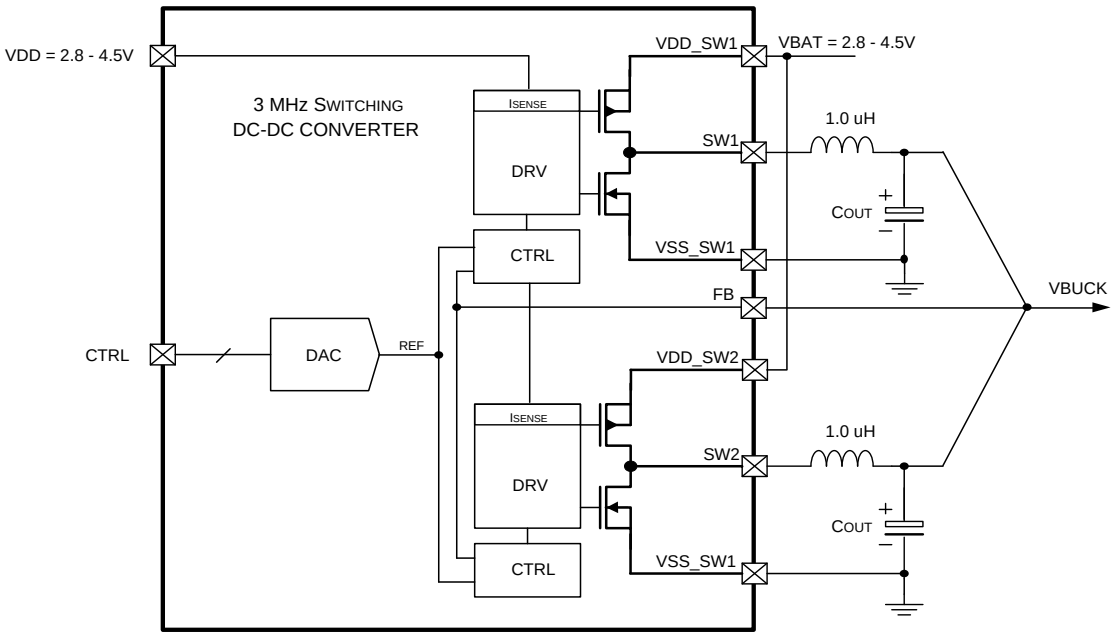

Figure 4: Dual-Phase Buck Block Diagram

The DA9068 dual-phase buck converters have programmable pull-down resistors. These are enabled when the buck is turned off and have a nominal value of 100 Ω. These pull-down resistors can be disabled via the PD_DIS control in the BUCK<x>_CONF1 registers.

5.1.3 RF Switching Regulator

DC-DC converter Buck7 (see Figure 5) is a high efficiency synchronous step-down regulator operating at 6 MHz or 3 MHz frequency. Its target application is to provide power for the 3G/3.5G(LTE) RF power amplifiers in mobile phone platforms. The regulator has a fixed output voltage of 0.9 V.

The buck architecture and the chosen operating frequency allow the use of small 0.5 µH/1 µH inductors, and provide fast output voltage transient response (typically 5 µs for a full scale output transition). The operating mode of the buck converter is controlled by the programmable V_{SYNC} and V_{SLEEP} voltage threshold registers. Depending on their setting, the buck can be forced to operate in either Synchronous mode or Sleep mode. Additionally, the buck can be configured in Automatic mode where it switches between Synchronous and Sleep mode depending on the load current. This high configurability allows further optimization of the RF system efficiency.

The turn-on/-off of this regulator is controlled by software (I^2C register writes).

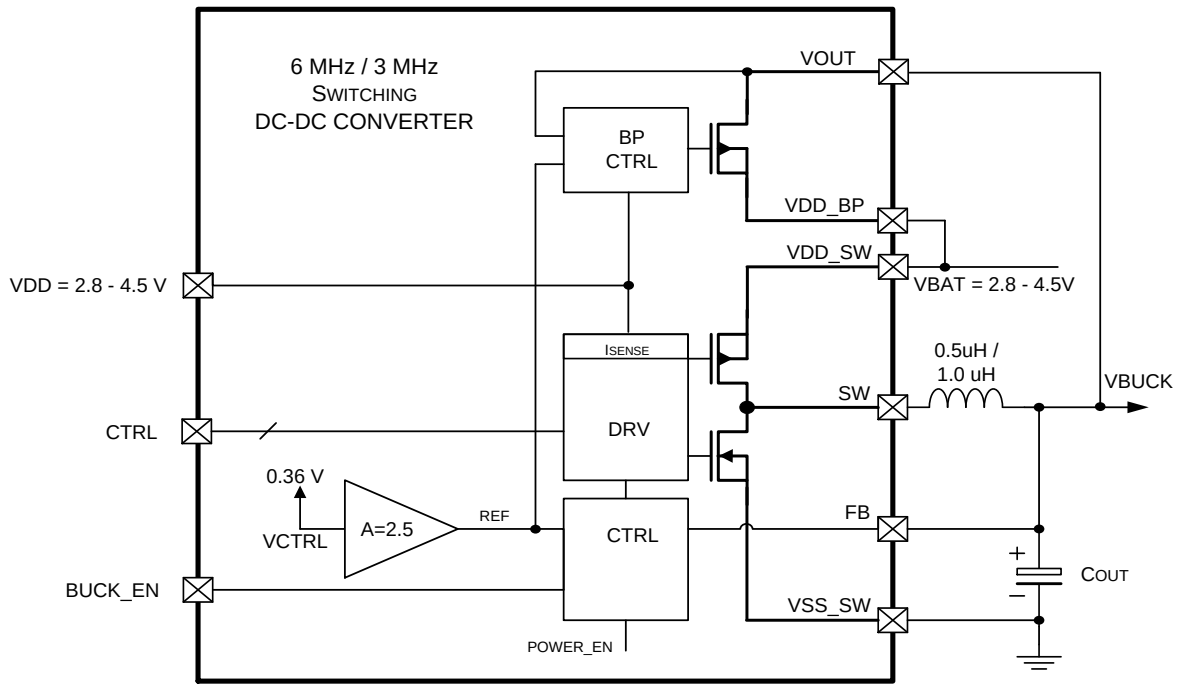

Figure 5: RF Buck Block Diagram

5.2 Linear Regulators (LDOs)

Several types of low dropout regulators are integrated in DA9068, each optimized for performance depending on the most critical parameter of the circuitry supplied. For high performance analog supplies (such as audio and RF), the regulators have been designed to offer high PSRR and low noise. For the digital supplies, PSRR is relaxed, saving quiescent current and, for the PMIC core/RTC supplies, quiescent current has been optimized as the most important performance parameters.

Table 28: Linear Regulator Summary

Block	V_{OUT} (V)	I_{OUT} (mA)	Comment	Control Note 1
LDO1	0.65 to 2.225	150	C_{OUT} = 1.0 µF, Step size 25 mV, Low voltage	SC/I^2C
LDO2	0.65 to 2.225	150	C_{OUT} = 1.0 µF, Step size 25 mV, Low voltage	SC/I^2C
LDO3	1.2 to 3.3	150	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO4	0.65 to 1.7	150	C_{OUT} = 1.0 µF, Step size 25 mV, Low voltage	SC/I^2C
LDO5	1.2 to 3.3	150	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO6	1.2 to 3.3	150	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO7	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO8	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	SC/I^2C
LDO9	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO10	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	SC/I^2C
LDO11	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	SC/I^2C
LDO12	1.2 to 3.3	400	C_{OUT} = 2.2 µF, Step size 50 mV	SC/I^2C
LDO13	1.2 to 3.3	150	C_{OUT} = 1.0 µF, Step size 50 mV	I^2C
LDO14	1.2 to 3.3	150	C_{OUT} = 2.2 µF, Step size 50 mV, Low noise	I^2C
LDO15	1.2 to 3.3	400	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO16	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO17	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO18	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO19	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO20	1.2 to 3.3	300	C_{OUT} = 2.2 µF, Step size 50 mV	I^2C
LDO21	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	I^2C
LDO22	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	I^2C
LDO23	1.2 to 3.3	200	C_{OUT} = 1.0 µF, Step size 50 mV	I^2C
LDO24	1.0 to 3.1	300	C_{OUT} = 2.2 µF, Step Size 50 mV	I^2C
LDO25	1.2 to 3.3	400	C_{OUT} = 2.2 µF, Step Size 50 mV	I^2C
LDO_CORE	2.5	5	C_{OUT} = 1.0 µF, Internal PMIC LDO	-
BBAT_CHG	1.8 to 3.3	0.1 to 6 (programmable)	Programmable output voltage CC/CV regulation loop	I^2C

Note 1 SC - PMIC Sequencer Control

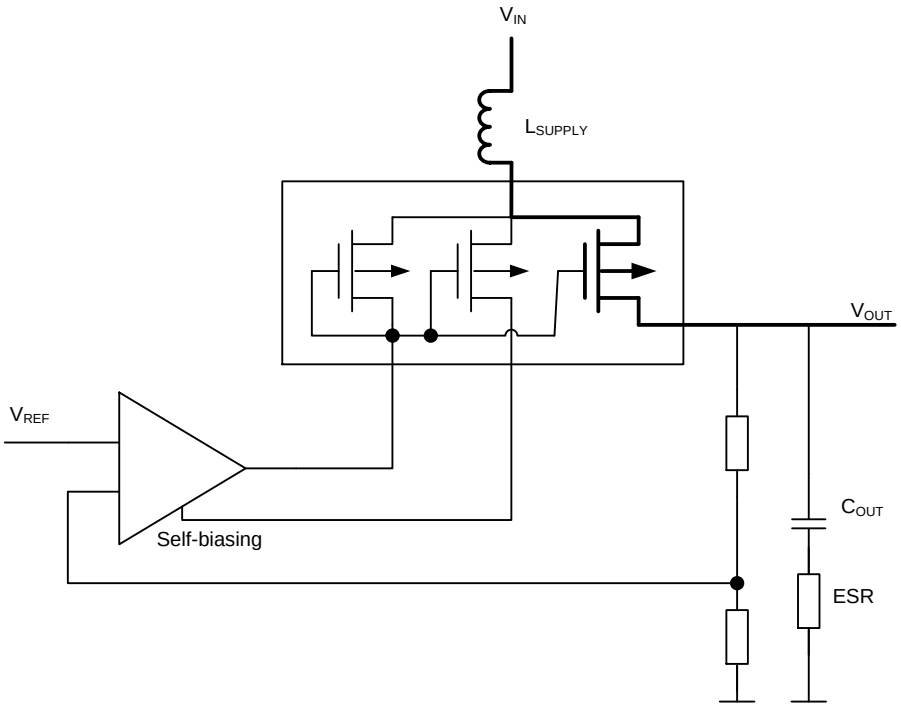

Figure 6: SmartMirror LDO

All regulators employ Dialog Semiconductor's SmartMirror dynamic biasing technology which guarantees a high phase margin within the regulator control loop and offers stable performance with small output capacitances over a wide range of output currents. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is also maintained across the full operating current range. However, quiescent current consumption is scaled to demand, giving improved efficiency when demand is low.

All regulator output voltages are fully programmable via the control interface allowing optimization of the complete system for maximum performance and power efficiency.

The default voltage for all LDOs is OTP-programmable. The voltages can be changed via the I^2C interface.

All DA9068 LDO regulators feature programmable (via LDO<x>_PD_DIS registers) pull-down resistors, which can be enabled or disabled when the regulator is powered down.

The input supplies for the DA9068 LDOs are organized in the following groups:

- VDD_LDO_A – LDO12
- VDD_LDO_B – LDO11
- VDD_LDO_C – LDO22 and LDO23
- VDD_LDO_D – LDO10 and LDO21
- VDD_LDO_E – LDO7 and LDO9
- VDD_LDO_F – LDO16 and LDO17
- VDD_LDO_G – LDO6 and LDO19
- VDD_LDO_H – LDO14, LDO18, and LDO20
- VDD_LDO_J – LDO13, LDO24, and LDO25
- VDD_LDO_K – LDO3, LDO5, LDO8, and LDO15
- VDD_LDO_LV – LDO1, LDO2, and LDO4

5.3 General Purpose ADC

DA9068 features a 12-bit multi-channel ADC that can be configured (via the ADC_MODE register control) in high speed mode (measurement sequences repeated every 2 ms) or in economy mode (measurements performed every 20 ms). The ADC provides a manual conversion mode as well as an automatic mode, in which the ADC is able to operate in the background without software intervention by using the built-in controller.

The GPADC can be configured as ON, OFF, or SLEEP in each of the MCTL modes via the GPADC_MCTL register.

The ADC utilizes a sample-and-hold successive approximation switched-capacitor architecture that is powered and referenced from the internal VCORE (2.5 V) supply rail. The GPADC also features an input analog multiplexer with a switched capacitor input prescaler, followed by a track-and-hold circuit that ensures stable input voltages during the conversion.

The integrated DA9068 GPADC can be used to monitor various internal and external voltage, current and temperature levels. Table 29 describes the allocation, the gain, and the measurement range of the ADC input channels.

Table 29: ADC Input Channels

Channel No.	Channel Name	Nominal Gain (V/V)	Measurement Range (V)	Description
0	VBAT	1.25	2.5 to V_{BAT}	Battery voltage
1	TEMP1	1	0 to 2.5	Battery NTC voltage (optional current source)
2	TEMP2	1	0 to 2.5	Battery NTC voltage (optional current source)
3	VF	1	0 to 2.5	Battery detection voltage (optional current source)
4	TJUNC	3	0 to 0.833	Internal temp. sensor voltage
5	ADCIN1	1	0 to 2.5	Voltage measurement
6	ADCIN2	1	0 to 2.5	Voltage measurement
7	ADCIN3	1	0 to 2.5	Voltage measurement
8	ADCIN4	1	0 to 2.5	Voltage measurement

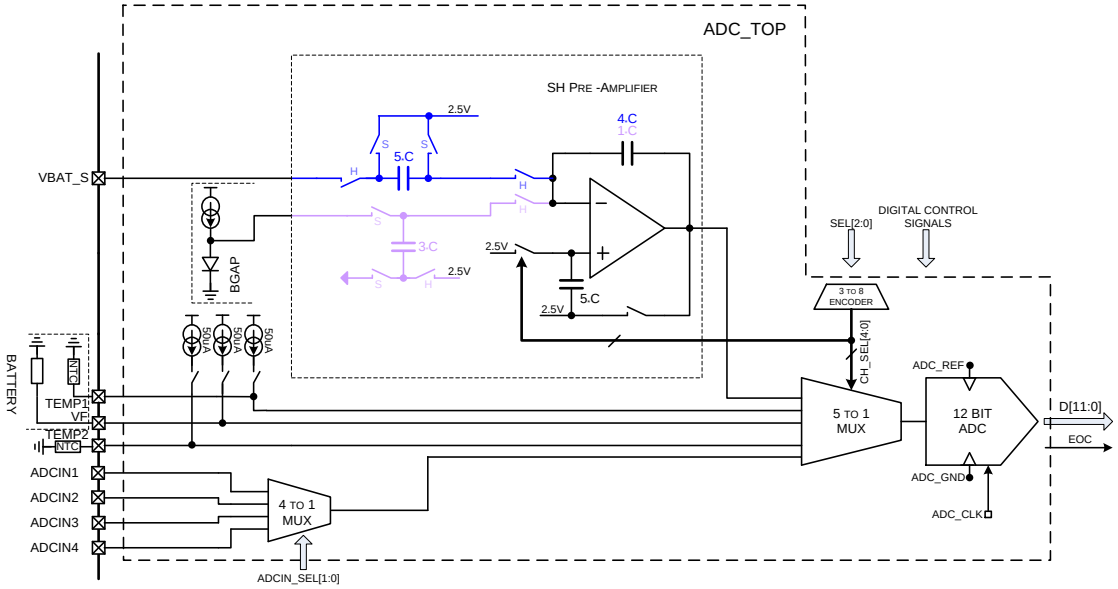

Figure 7: GPADC Block Diagram

On DA9068, the A-to-D conversion is performed by a switched capacitor (SC) successive approximation register (SAR) ADC. The actual ADC is preceded by a 5:1 input multiplexer that controls the channel selection, routes the appropriate input signal to the SC circuit, and ensures the inter-channel isolation. The input voltage range of the SC ADC core is from 0 V to 2.5 V, hence any input signal outside this range has to be pre-scaled before being routed to the input of the converter. The ADC core is supplied from the internal 2.5 V VCORE rail, which is also used to provide the positive reference voltage for the ADC. A dedicated quiet V_{SS} signal is used for the negative reference voltage of SC circuit.

The implemented track-and-hold circuit ensures a stable voltage on the input of the SC ADC during the conversion. Figure 8 shows the polarity and the timing of the external and internal signals controlling the track and hold sequence of the converter. The clock (f_{CLK} = 0.5 MHz) and the enable signal (EN) are provided by the main PM control logic, while all the other signals are internally generated. The timing diagram illustrates a tracking period of 13 clock cycles, that is 26 µs (inclusive of 10 µs auto-zero time) and a conversion period of 24 µs, hence a total ADC conversion cycle of 50 µs.

The end of the conversion is flagged by the EOC signal which indicates the availability of the data bits D[11:0]. Once the PM controller has read the result, it de-asserts the EN signal which terminates the current conversion cycle. A new cycle can be started on the following rising edge of the clock.

The channel selection control signals SEL[2:0] must be present prior to, or at least coincident with, the assertion of the ADC enable signal. This is to ensure that the tracking period is not affected by late assertion of the external digital controls. For the same reason, in case of dynamic control of the TEMP and VF current sources they have to be enabled (turned on) at least 100 µs before the next NTC or respectively VF measurement.

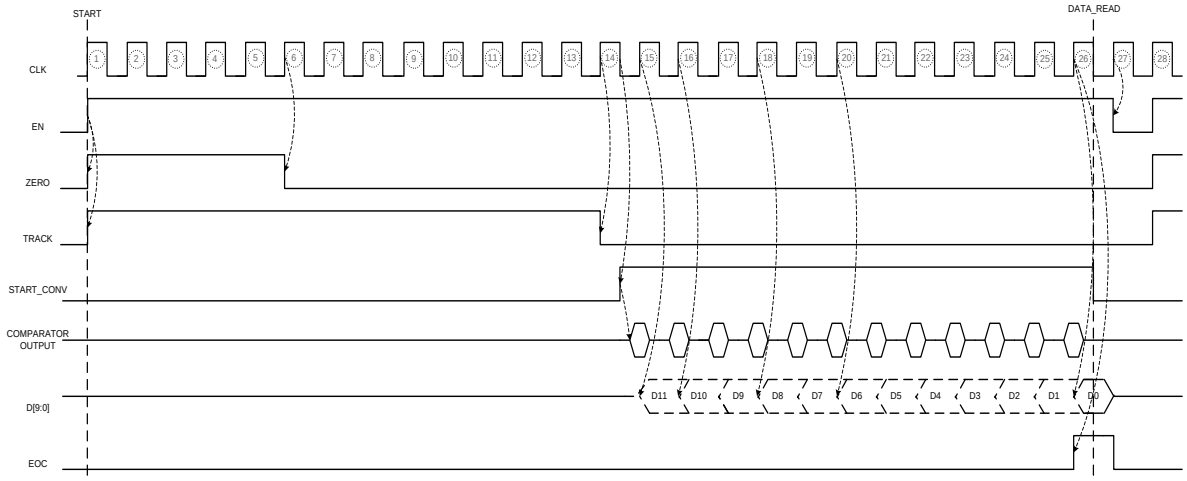

Figure 8: Track and Hold Sequence Timing Diagram

5.3.1 ADC Measurement Modes

5.3.1.1 Manual Conversion Mode

The manual ADC measurements are initiated by host writes to the MAN_CONV register control. The ADC powers up and performs a single conversion of the selected (via MUX_SEL and ADCIN_SEL) input signal. After storing the 12-bit result, the main PM controller powers down the ADC and clears the MAN_CONV register.

5.3.1.2 Automatic Conversion Mode

The automatic conversion mode is controlled by a dedicated automatic measurement scheduler that is part of the main PM controller. The automatic mode allows monitoring of the system voltage V_{BAT} (A0), the battery temperature TEMP1 (A1), an additional temperature TEMP2 (A2), the VF detection (A3) input, and one of the four ADCIN inputs (A4).

The automatic sequence consists of 10 slots, each with fixed 200 µs duration, see Figure 9.

Slot No.	0	1	2	3	4	5	6	7	8	9
	A0	R	M	A3	A1	M	A4	A2	M	A5

A0 Automatic Measurement of VBAT_S Input
A1 Automatic Measurement of TEMP1 Input
A2 Automatic Measurement of TEMP2 Input
A3 Automatic Measurements of VF Input
A4 Automatic Measurements of ADCIN Channel
A5 Automatic Measurement of TJUNC (Internal Junction Temperature)
M Slot Available for Manual Measurement
R Reserved Slot

Figure 9: Sequence of Automatic ADC Measurements

5.3.2 ADC Measurement Channels

5.3.2.1 A0 V_{BAT} Voltage Measurement

This ADC channel is used to monitor the voltage of the main battery. As the voltage level on this input can be higher than 2.5 V, the signal is processed by the pre-amplifier prior to the actual conversion. The input VBAT_S is star (Kelvin) connected to the battery. An external RC filter with a cut-off frequency of 45 Hz to 100 Hz (that is, 100 kΩ and 220 nF) is recommended.

V_{BAT} is measured and compared with the VBAT_MON threshold. If the reading is below this level for a number of three consecutive readings an E_VDD_LOW event is generated. After nIRQ assertion, the automatic measurement of channel A0 is paused for reading. The host has to clear the associated event flag (the event-causing value is kept inside the result register) to re-enable the supervision of V_{BAT}.

5.3.2.2 A1 TEMP1, A2 TEMP2, A3 VF Voltage Measurements

These channels are included in the automatic measurement sequence and, when enabled, can provide general purpose voltage monitoring of the corresponding inputs.

Battery temperature is measured on channel A1 and compared with two temperature thresholds, TEMP1_HIGHP and TEMP1_LOW. If three consecutive TEMP1 readings are greater than TEMP1_HIGHP or less than TEMP1_LOW, the event flag is set and E_TEMP1 interrupt is generated. The generation of this interrupt can be masked by M_TEMP1.

NOTE
On DA9068, the medium temperature threshold TEMP1_HIGHN associated with the TEMP1 channel should be configured with the same value as the one programmed in the TEMP1_HIGHP register.

The TEMP2 input can be used for monitoring a different temperature point in the system. The measured value on channel A2 is compared with two temperature thresholds, TEMP2_HIGHP and TEMP2_LOW. If three consecutive TEMP2 readings are greater than TEMP2_HIGHP or less than TEMP2_LOW, the event flag is set and E_TEMP2 interrupt is generated. The generation of this interrupt can be masked by M_TEMP2.

NOTE
On DA9068, the medium temperature threshold TEMP2_HIGHN associated with the TEMP2 channel should be configured with the same value as the one programmed in the TEMP2_HIGHP register.

The VF channel is used for battery detection and needs to detect whether a 1.5 kΩ, 4.7 kΩ, 10 kΩ, or 27 kΩ resistor is connected to GND. The VF measured value is compared against two threshold levels, VF_HIGH and VF_LOW. If three consecutive VF readings are greater than VF_HIGH or less than VF_LOW, the corresponding event flag is set and E_VF interrupt is generated. The generation of this interrupt can be masked by M_VF. The VF_HIGH threshold comparison can be used for battery removal detection.

In addition, the TEMP1/2 and VF channels can also be used for resistance measurements. The external resistor to be measured should be connected to the input pin and the internal 50 µA current source in the ADC should be enabled. The operation of the 50 µA current source is controlled by the TEMP1_ISRC_EN, TEMP2_ISRC_EN, and VF_ISR_EN register controls.

When the temperature channels measurements are enabled in the Auto Mode sequence and TEMP1/2_ISRC_EN = 0, the current source is dynamically switched off at the end of the conversion and switched back on one slot prior to the next TEMP1/2 measurement. This operation reduces the current consumption but requires extra time to charge the external capacitance on the input node. When TEMP1/2_ISRC_EN = 1 in Auto Mode, the current source is permanently turned on.

When the VF measurement is enabled in the Auto Mode sequence, and the corresponding ISRC_EN = 0, the current source is turned off. When ISRC_EN = 1, the respective internal current source is dynamically switched on and off with the same timing as for the TEMP1/2 channels.

During manual measurements (the automatic measurement of the respective channel has been disabled), all channels have the same current source control. Therefore, when <xxx>_ISRC_EN = 0, the internal 50 µA source is off and, when <xxx>_ISRC_EN = 1 it is permanently on.

5.3.2.3 A4 ADCIN1/2/3/4 Voltage Measurements

The ADCIN channel is a general purpose voltage measurement channel. The ADCIN_SEL configuration bits determine which of the four ADCIN input signals is to be processed in the current measurement slot.

5.4 Voltage and Temperature Monitoring

5.4.1 System Voltage Monitoring

The supervision of the system supply, V_{BAT}, is done by four comparators. One comparator monitors the $V_{DD\_FAULT\_UPPER}$ threshold (indicating a valid battery/external supply) and the other three monitor the under-voltage levels – V_{DD_MON}, $V_{DD\_FAULT\_LOWER}$ (fault condition indicator), and $V_{DD\_FAULT\_CRIT}$. During normal operation (not in RTC mode), the V_{BAT} monitoring circuit is always on and, as such, is designed to have low current consumption.

When the V_{BAT} voltage drops below the V_{DD_MON} level (typically 3.1 V), an event and associated interrupt is generated. This is an indication that the battery is discharging and approaching a fault condition level. When the V_{BAT} voltage drops below the $V_{DD\_FAULT\_LOWER}$ level (typically 2.9 V), the nRESET output signal is asserted after a 150 ms debounce time. This is normally the case when the main battery is being slowly discharged (typical operation).

After the nRESET assertion, the PMIC starts a controlled shutdown sequence that turns off all system supplies. At the end of the sequence, the internal PM controller is reset and the PMIC will not auto-boot next time the system supply is above the $V_{DD\_FAULT\_UPPER}$ threshold, unless the AUTO_BOOT bit is set or a case of momentary power loss was detected (see Section 7.7 for details of Sudden Momentary Power Loss [SMPL]).

When the battery is removed and the V_{BAT} discharge is significantly faster, nRESET is asserted 64 µs after the system supply falls below the $V_{DD\_FAULT\_CRIT}$ level (typically 2.7 V). In this case, the PM controller performs an emergency shutdown by turning off all supplies simultaneously.

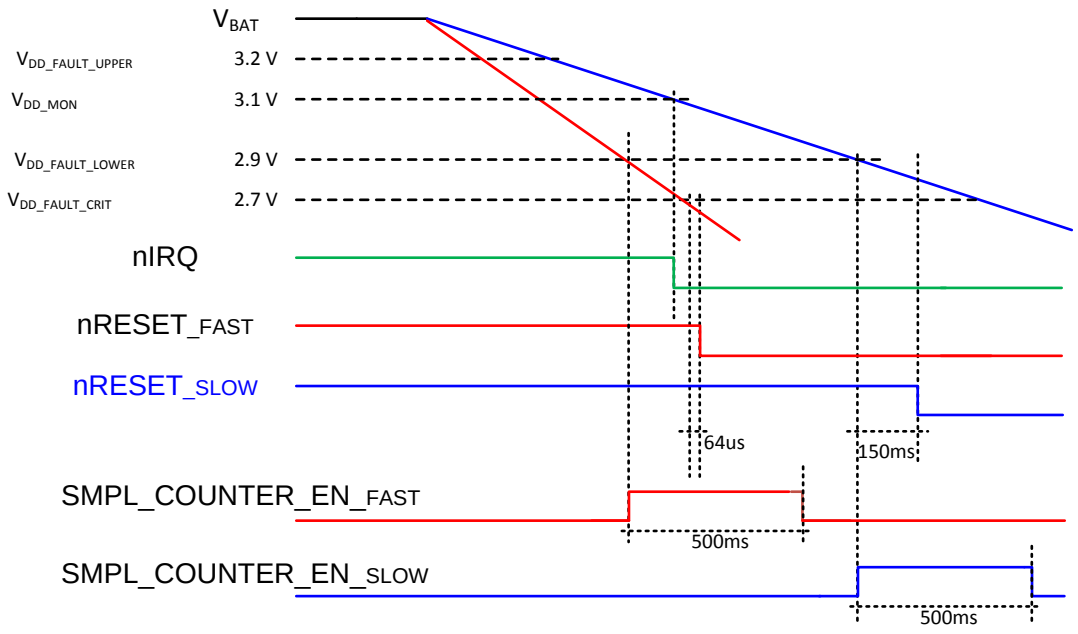

Figure 10: System Voltage Monitoring

5.4.2 Temperature Monitoring

In order to protect DA9068 from damage caused by excessive power dissipation, the internal Temperature Monitor circuit performs continuous monitoring (except for the RTC mode of operation) of the internal junction temperature.

DA9068 has a critical over-temperature threshold (T_{CRIT}) of about 140 °C.

The output of the internal temperature comparator is monitored by the digital control logic. The control logic shuts down DA9068 (transition to RESET state) and asserts TEMP_OVER in the FAULT_LOG register when three consecutive measurements indicate that the internal junction temperature exceeds the over-temperature threshold (T_{JUNC} > 140°C). The fault condition remains asserted until the temperature drops below the safe temperature threshold:

$$T_{JUNC} < T_{CRIT} - 10\ °C$$

By using the junction temperature channel (A4) of the GPADC the host can measure the exact die temperature.

6 RTC Domain

The RTC Mode of operation is an ultra-low power mode in which all blocks, except for the RTC block, are powered down. The active RTC block maintains the RTC clock counter and alarm functions. The RTC block is powered from a dedicated supply rail VDDRTC. The RTC circuit includes the following functional blocks:

- 32 kHz oscillator providing the clock for the RTC counter and the RTC control logic
- RTC counter keeping track of the real time
- Control Logic managing the Alarm, Wake Up and Enable/Disable functions and the proper transfer of control and data from/to the main PMC logic
- POR circuit
- Auxiliary logic and Level Shifters

DA9068 can enter RTC mode of operation as described below:

- When the VBBAT (the backup battery supply) is the only available voltage source in the system (no main battery), DA9068 enters RTC mode as all the other supply domains are down. The transfer of control from the main PM control logic to the RTC control logic and the isolation of the interface signals is triggered by the assertion of the main POR signal (VCORE < 2 V).
- If the RTC_AUTO_EN register bit is set, PM controller transition to POWERDOWN mode (sequencer slot ID0) automatically forces DA9068 to RTC mode even in the presence of a valid VBAT supply

NOTE
Forced RTC mode is intended for test purposes only. It is not recommended for real applications as the BBAT Charger is disabled and the charging of the backup power source is not maintained.

The following conditions can wake up DA9068 from RTC mode:

- Re-insertion of the system supply VBAT followed by the assertion of nONKEY, TA or nON2.
- Alarm or Tick event in the presence of a valid VBAT supply (VBAT > VBBAT + 65 mV). If VBAT does not fulfill this condition, DA9068 does not wakeup but the Alarm event is memorized.
- SMPL event, that is, re-insertion of the system supply VBAT before the expiration of the SMPL timer.

6.1 Crystal Oscillator

The 32 kHz clock on DA9068 is generated by an ultra-low power oscillator that works with an external piezoelectric crystal at 32.768 kHz. The start-up time of the oscillator is typically 0.5 s to 1 s over the VDDRTC supply voltage range. When XTAL_EN = 0, the 32 kHz oscillator is disabled and the clock multiplexer CLK MUX is configured to route in the external clock signal provided at the XOUT port. To achieve the desired crystal frequency, DA9068 requires external capacitors to ground on each of the crystal pins. Depending on the parasitic capacitance of the board, the value of these capacitors varies between 5 pF and 10 pF. When a crystal is not mounted, the XTAL pins that are not driven (by external clock signal in bypass mode) should be grounded. The oscillator inputs are designed to withstand a leakage current equivalent at least to the leakage of a 100 MΩ resistor connected between the XTAL pin and any signal level between VCORE and GND.

The 32 kHz clock signal is made available at the OUT1_32K, OUT2_32K, and OUT3_32K pins. The output clock buffers can be initially enabled/disabled in the OTP configuration. Additionally, the OUT2_32K can be completely disabled via the control bit settings or via a GPIO.

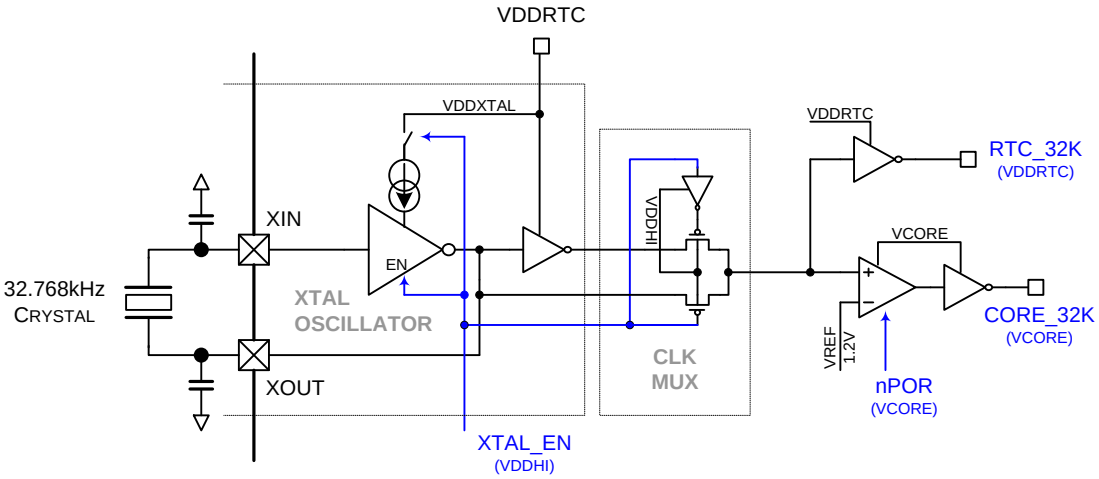

Figure 11: 32 kHz Crystal Oscillator

6.2 RTC Counters and Alarms

DA9068 features a calendar counter with an associated alarm register. When set, the calendar alarm generates an IRQ and a wake-up event on the expiry of the calendar counter.

The RTC calendar counter counts the number of 32 kHz clock periods and provides a sec, min, hrs, day, month, and year outputs. Year 0 corresponds to 2000. The counter can count up to 63 years. The value of the RTC calendar can be read or written to via the power manager interface. A read of the seconds register (COUNT_S) latches the current RTC calendar count into the COUNT_S to COUNT_Y registers (coherent for approximately 0.5 s), that is, receiving an updated calendar value requires a read of COUNT_S register.

NOTE
Reading the calendar registers in page mode must begin at COUNT_S.

DA9068 has an alarm register containing sec, min, hrs, day, month, and year. When the RTC calendar counter register value equals the value set in the calendar alarm register, an IRQ event is generated and DA9068 wakes up from POWERDOWN mode and given that $V_{BAT} > V_{BBAT}$ also from RTC mode. The trigger also sets a bit in the event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_TYPE, is either asserted every second or minute. The power manager registers ALARM_ON and TICK_ON, enable/disable the alarm and tick respectively.

NOTE
Values written into the RTC calendar and alarm registers have to be within the allowed value range (see register description). For example, a maximum of 60 is allowed for seconds or minutes.

The RTC calendar counter is reset to zero when the VDDRTC nPOR is asserted. The power manager register bit MONITOR is set to 0 each time the VRTC domain goes through a power down cycle. When setting the time and date, the software has to set the MONITOR bit to 1, in order to enable/re-enable the RTC supply generator and the RTC domain digital block (counters and control logic). Setting MONITOR = 1 also allows the detection of a subsequent loss of the clock.

6.3 Backup Battery Charger

DA9068 provides a backup battery charger for charging of Lithium-Manganese coin cell batteries and super capacitors. This charger features both constant current (CC) and constant voltage (CV) charging modes. The transition between the modes is automatic as the battery voltage approaches the target voltage level. The termination voltage is programmable in 100 mV steps from 1.8 V to 3.3 V via the BBCHG_VSET control register. The charging current is set by the BBCHG_ISET register from 0.1 mA to 6 mA in 100 µA steps up to 1 mA, and 1 mA steps in the higher range. The PMIC logic controls the enable/disable of the charger via the BBCHG_EN register bit.

The backup battery charger automatically switches itself off when it reaches the programmed termination voltage. To conserve the charge in the supercap/backup battery, the whole RTC domain is then supplied from VBAT. To maintain the charge of the backup source, the BBAT charger has to be restarted periodically by SW. The automatic termination can be permanently disabled by setting the BBAT_ILIMIT_IGNORE register bit to 1.

The BBAT_MCTL[3:0] control registers determine whether the backup battery charger stays ON or is turned OFF in the four different power states defined by the MCTL[2:1] inputs.

The charger also switches off automatically during NO-POWER and RTC mode.

The backup battery charger is powered from the main supply V_{BAT}. To prevent this rail being back-powered from the backup battery (when no main supply is present), the bulk connection of the output P-FET power device is dynamically controlled by a dedicated bulk-switch comparator. When the comparator detects that the backup battery voltage V_{BBAT} is greater than the main supply it turns off the output pass transistor and connects its bulk to V_{BBAT}. The output PMOS transistor is re-enabled and its bulk switched to V_{BAT} when the comparator detects $V_{BAT} > V_{BBAT}$ + 65 mV. The bulk-switch comparator is an always-on circuit, with an extremely low quiescent current (especially from the backup battery side).

7 PM Digital Control

7.1 DA9068 Operating Modes

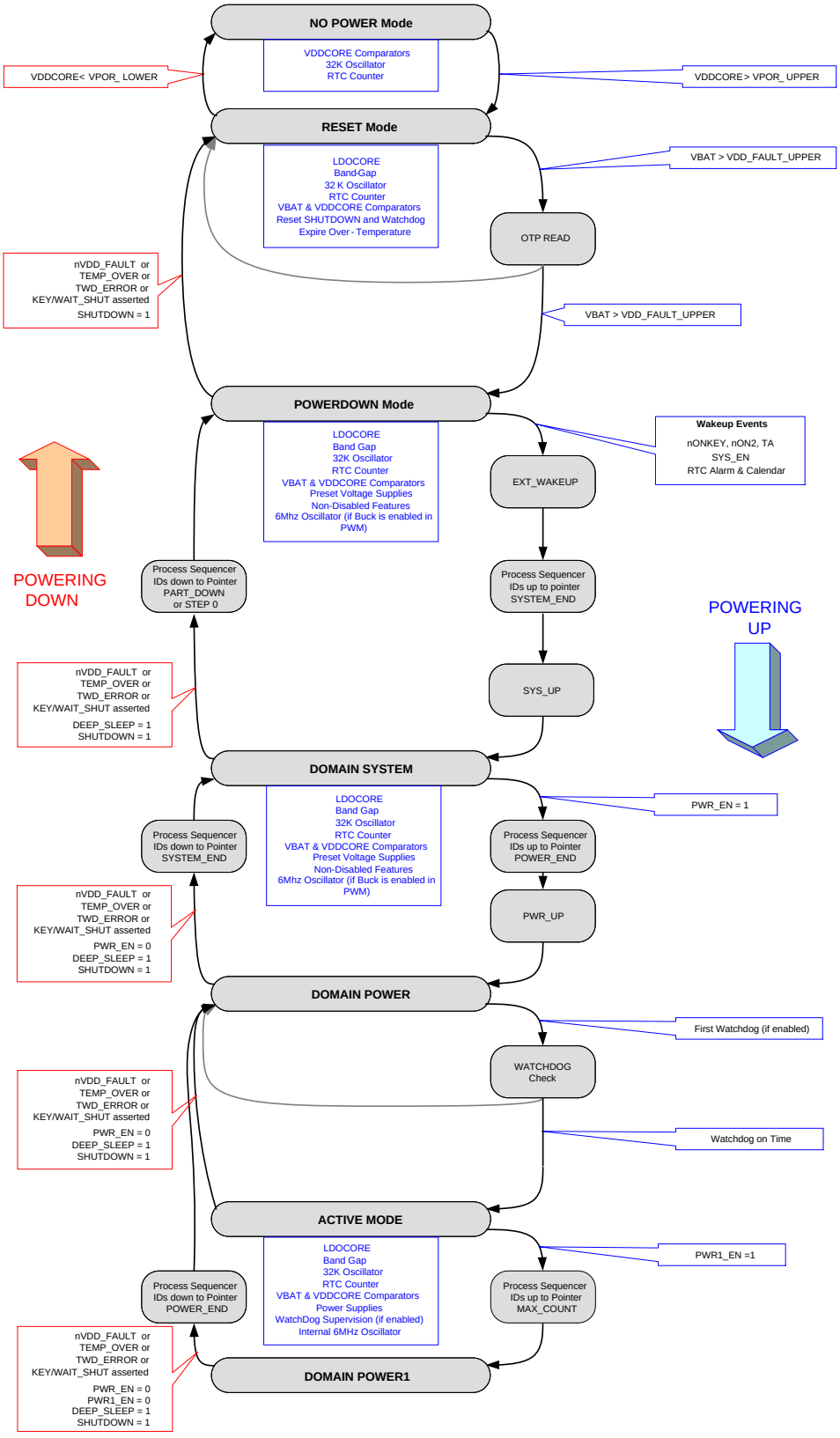

Figure 12: Operating Modes

7.1.1 NO-POWER Mode

NO-POWER mode is the initial state DA9068 enters when being powered up for the first time (cold start). Once active, DA9068 enters NO-POWER mode when low V_{BAT} supply voltage causes the internally regulated PMIC supply (V_{CORE}) to drop below the V_{POR_LOWER} threshold (for example, during continued discharge of main battery). Under these conditions, an internal power-on-reset (nPOR) is asserted and the main DA9068 digital controller is reset.

When DA9068 detects a good main battery supply (V_{BAT} > 2.5 V), which rises V_{CORE} > V_{POR_UPPER}, it loads the OTP (if the part is programmed) and progresses to RESET mode.

7.1.2 RESET Mode

DA9068 is in RESET mode whenever a complete application reset is required. RESET mode is entered after a cold start when progressing from NO-POWER mode or can be forced by the user via a long press of nONKEY (control bit AUTO_BOOT = 0), or from the host processor by assertion of the SHUTDOWN register bit. DA9068 also enters RESET mode after error detection. The following error conditions force DA9068 to enter RESET mode:

- a WATCHDOG write from the host outside of the watchdog time window (if WD was enabled)
- an under-voltage detection at V_{BAT} (V_{BAT} < $V_{DD\_FAULT\_LOWER}$ [debounced] or V_{BAT} < $V_{DD\_FAULT\_CRIT}$)
- an internal die over-temperature detection

In order to allow the host to determine the reason for the reset, a FAULT_LOG register records the cause. The processor resets this register by writing 0xFF via the power manager bus. Reset conditions such as SHUTDOWN via register bit, WATCHDOG, and over-temperature errors expire automatically, and DA9068 progresses from RESET to POWERDOWN mode when there is a valid V_{BAT} supply. If the RESET was initiated by a HW reset (nONKEY long press), a 500 ms time out will be inserted before the PMIC attempts to power up again.

When returning from POWERDOWN mode, RESET mode is entered after the complete power down of the SYSTEM domain (sequencer position 0). RESET is a low power mode with LDOCORE, RTC counter, over-temperature, and V_{BAT} monitors being the only active blocks. All other DA9068 supplies are automatically disabled to avoid battery discharge. The nRESET port is always asserted low when DA9068 is in RESET mode.

Apart from E_ALARM and E_TICK, all asserted events are automatically cleared on entry to RESET mode. The DA9068 register configuration is re-loaded from OTP when leaving RESET mode.

7.1.3 POWERDOWN Mode

DA9068 is in POWERDOWN mode whenever the power domain SYSTEM is disabled (even partially). This mode is entered when progressing from RESET mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low power mode instructions from the host (assertion of DEEP_SLEEP or SHUTDOWN register bit) or happens as an interim state during application shutdown to RESET mode.

During POWERDOWN mode, LDOCORE, the nONKEY, nON2, and TA inputs, and the RTC counter are active. In addition, GPIO ports, GPADC, backup battery charger, and the control interface continue running if not disabled via register PD_DIS. Disabling blocks during POWERDOWN mode saves quiescent current, especially if all the blocks that require the main clock are disabled. If the host no longer communicates during POWERDOWN mode, the control interface may be temporarily disabled too (controls PM-IF_PD). The internal oscillator (6 MHz) only runs on demand (to support the GPADC or enabled bucks that are not forced to PFM mode). The application supervision by WATCHDOG timer is discontinued in POWERDOWN mode.

When the return to POWERDOWN Mode was initiated by a DEEP_SLEEP command, the sequencer pointer is stopped at position PART_DOWN inside the domain SYSTEM, which will result in a partial POWERDOWN mode.

7.1.4 ACTIVE Mode

DA9068 is in ACTIVE mode after the host processor has performed at least one initial 'Alive' watchdog write (or alternatively an initial assertion of the KEEP_ACT pin) inside the target time window. This watchdog condition can be disabled via setting TWDSCALE to zero.

In ACTIVE mode, as well as the core PMIC blocks (LDOCORE, RTC counter, internal oscillator), a set of supplies and peripheral features such as the GPADC and backup battery charger are also usually enabled. Status information can be read from the host processor via the power manager interface and DA9068 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ). Temperature and voltages (internal to DA9068) can be monitored and any fault conditions flagged to the host processor.

7.2 Power Supply Sequencer

The start-up of DA9068 supplies is performed with a sequencer that contains a programmable step timer, a variable ID array of time slot pointers, and four predefined pointers (SYSTEM_END, POWER_END, MAX_COUNT, and PART_DOWN). The sequencer is able to control up to 22 IDs (six buck converters, 12 LDOs, Wait ID, and a POWERDOWN register), which can be grouped in three power domains. The power domains have a configurable size and their borders are defined by the location pointers SYSTEM_END, POWER_END, and MAX_COUNT.

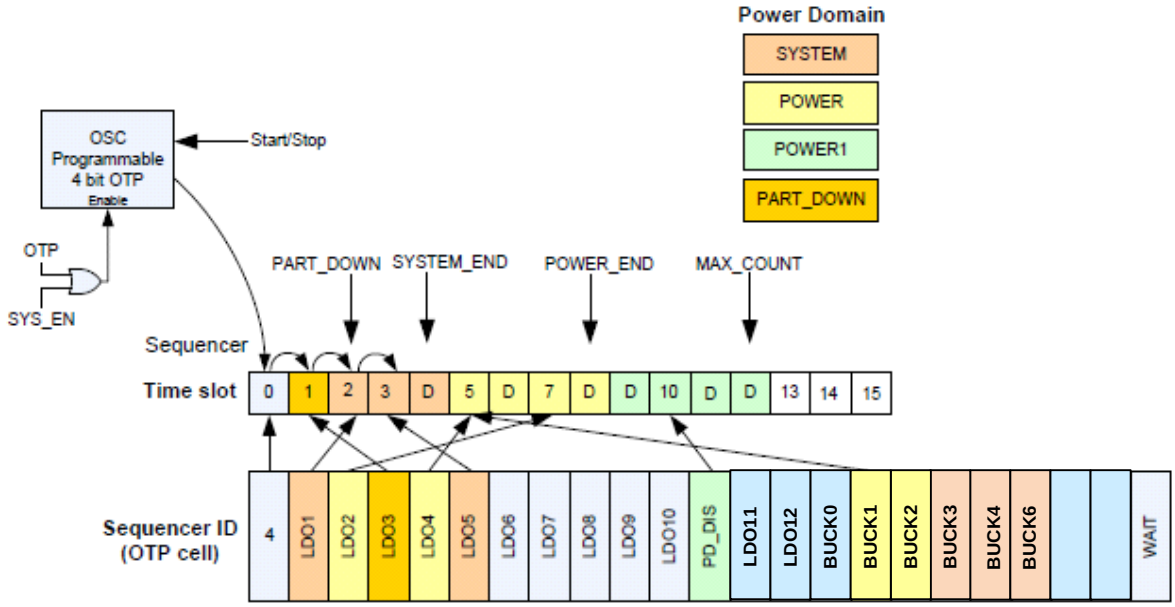

Figure 13: Allocation of Supplies into the Sequencer Time Slots

The lowest level power domain, SYSTEM, starts at step 1 and ends at the step that is defined by the location pointer SYSTEM_END. The second-level domain, POWER, starts at the successive step and ends at POWER_END. The third level-domain POWER1 starts at the consecutive step and ends at MAX_COUNT. The values of pointer SYSTEM_END, POWER_END, and MAX_COUNT are predefined in OTP registers and should be configured to be SYSTEM_END < POWER_END < MAX_COUNT.

The SYSTEM domain can be viewed as a basic set of supplies that are mandatory to power up the application. The POWER domain includes supplies that are required in addition to get the application 'Alive' and set DA9068 to ACTIVE mode.

The POWER1 domain can be viewed as a sub-domain of POWER that can be used for additional hardware/software initiated control of supply blocks during ACTIVE mode (for a sub-application such as WLAN or GSM baseband, for example).

Up to six buck converters and 12 LDOs can be assigned unique sequencer IDs. The power-up sequence is then defined by an OTP register bank that contains a series of supplies (and other

features), which are pointing towards a sequencer time slot. Several supplies can point to the same time slot and by that will be enabled by the sequencer in parallel. Time slots that have no IDs pointing towards them are dummy steps that only insert a configurable time delay (marked as 'D' in Figure 13). Supplies that are not pointing towards a sequencer time slot (with a step number greater than zero and less than MAX_COUNT) will not be enabled by the power sequencer and have to be controlled individually by the host (via the power manager interface).

When powering up the sequencer, behavior is configured at step 0. If DEF_SUPPLY is asserted, supplies that are default enabled in the OTP settings are switched on. If SYS_EN is asserted (via OTP) the sequencer continues with step 1 which enables all supplies (features) from the OTP register bank that are pointing towards step 1, then moves to step 2, 3, and so on. The sequencer progresses until it reaches the position of pointer SYSTEM_END. Now all supplies of the first power domain SYSTEM are enabled and DA9068 asserts the E_SEQ_RDY interrupt.

Before continuing, the sequencer checks for an asserted PWR_EN (via register write or OTP). When PWR_EN = 1 the supplies in the POWER domain are enabled sequentially. The sequencer stops at step POWER_END, asserts the E_SEQ_RDY interrupt, enables the initial WATCHDOG timer, and waits for an 'Alive' feedback from the host processor. This starts the ACTIVE mode of DA9068.

The POWER1 domain can be enabled by PWR1_EN = 1 (asserted via register write or OTP). It enables all consecutive supplies until step MAX_COUNT has been reached and then asserts the E_SEQ_RDY interrupt. The POWER1 domain offers no dedicated status indicator, but the end of its power-up sequence can be selected to start the RESET timer.

The delay between the sequencer steps is controlled via a 4-bit OTP programmable timer unit, SEQ_TIME, with a default delay of 128 µs per step (minimum 32 µs and maximum 8 ms). The delay time between individual supplies can be extended by leaving consecutive steps having no IDs pointing to it (Dummy supply), which provides an independent delay configured via control SEQ_DUMMY.

When DA9068 is powering down, the sequencer disables the supplies in reverse order and timing. If the power down was initiated by releasing PWR1_EN, the sequencer stops to modify supplies when the domain pointer POWER_END is reached. If PWR_EN was disabled, the POWER1 domain is powered down, followed by POWER, until the sequencer reaches the pointer SYSTEM_END.

DA9068 does not accept any power mode transition commands until the sequencer has stopped processing IDs. All regulators and buck converters in power domains POWER1, POWER, and SYSTEM, will be sequentially disabled in reverse order. No IRQ or wake-up is generated when SYS_EN changes from active to passive state.

If the low-power mode was initiated by asserting the control register DEEP_SLEEP, the sequencer first powers down the POWER1 and POWER domains, continues with the SYSTEM domain, and stops when pointer PART_DOWN has been reached (PART_DOWN has to point into domain SYSTEM). Wake-up events are enabled when powering down to sequencer step 0 or pointer PART_DOWN (ignored outside of POWERDOWN mode). The sequencer asserts the E_SEQ_RDY interrupt whenever reaching the target pointer position. When processing step 0, all supplies (beside LDOCORE) can be set to their OTP default state (if bit DEF_SUPPLY of step 0 is asserted), but the voltage levels remain unchanged. To minimize the inrush currents on the battery, it is recommended not to default enable more than one supply at step 0.

Asserting control register bit SHUTDOWN causes DA9068 to power down to step 0 and then forces the PMIC into RESET mode.

DA9068 features, such as the OUT1_32K output buffer or the auto ADC measurements, can be disabled temporarily in POWERDOWN mode via register PD_DIS. The timing for processing PD_DIS can be defined by the placement of PD_DIS inside the sequence. Features asserted in PD_DIS are enabled when PD_DIS is processed during a power-up sequence.

The nRES_MODE configuration at sequencer step 0 enables the assertion of nRESET at the beginning of a power down sequence and starts the reset timer during the subsequent powering up. The reset timer starts to run from the selected event RESET_EVENT and releases the nRESET port after the reset timer has expired.

7.3 System Monitor (Watchdog)

After powering up the POWER domain, DA9068 can initiate an initial Watchdog monitor function (if this feature is enabled via control TWDSCALE). If the WATCHDOG is enabled, the host processor has to write logic 1 within a configured TWDMAX time to bit WATCHDOG (in register CONTROL_C) to indicate that it is 'Alive' after SYS_UP was asserted. If the host does not write 1 to the WATCHDOG bit within the TWDMAX time, DA9068 asserts TWD_ERROR in the FAULT_LOG register and powers down to RESET mode.

After this first write to the WATCHDOG, the host must write to the watchdog bit within a configured time window or DA9068 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode. The WATCHDOG error condition is cleared when entering the RESET mode. The time window has a minimum time TWDMIN fixed at 256 ms and a maximum time TWDMAX of nominally 2.048 s. The TWDMAX value can be extended by multiplying the nominal TWDMAX by the register bits TWDSCALE. TWDSCALE is used to extend the TWDMAX time by x1, x2, x4, x8, x16, x32, or x64.

Changing the maximum value of the time window or the state of KEEPACT_EN bit requires TWDSCALE to be zero (WATCHDOG is disabled) for a minimum of 100 µs. This requires the host to first switch off the WATCHDOG for at least 150 µs before configuring it with a new timing window scale value (TWDSCALE).

The WATCHDOG bit can also be asserted from the host via hardware by asserting KEEP_ACT. This is mode selected via control KEEPACT_EN, which disables the control of the WATCHDOG bit via the host control interface. The in-time assertion of nONKEY then also enables DA9068 to transfer into ACTIVE mode. Once in the ACTIVE mode, DA9068 continues to monitor the system unless it is disabled by setting TWDSCALE to zero. If the WATCHDOG register bit is set to a 1 within the time window, the Watchdog monitor resets the timer, sets the WATCHDOG bit back to zero (bit is always read as zero), and waits for the next Watchdog signal.

7.4 Power Manager/System I/Os

DA9068 features several unidirectional, dedicated Power Management I/Os, which are configured in hardware as either inputs or outputs.

7.4.1 Input Ports

Table 30: Input Ports

PAD Name	Type	PAD Description	Configuration
nONKEY	DI	ON/OFF key / HW watchdog input Active low input	Internal 200 kΩ pull-up to VBAT VDDIO/VDDINT supply rail
TA	DI	TA wakeup input Active high input	5.5 V tolerant input VDDIO/VDDINT supply rail
nON2	DI	nON2 wakeup input Active low input	Internal 200 kΩ pull-up to VBAT VDDIO/VDDINT supply rail
M_CTL1	DI	Mode control input 1 Active high input	VDDIO/VDDINT supply rail
M_CTL2	DI	Mode control input 2 Active high input	VDDIO/VDDINT supply rail
OUT2_32K_EN	DI	ON/OFF control for the OUT2_32K output	VDDIO/VDDINT supply rail
TP	AI	Test input Power Commander enable	Internal pull-down to GND
LVLSH_IN	DI	Level-shifter input	VDDIO/VDDINT supply rail

7.4.1.1 ON/OFF and Hardware Watchdog (nONKEY/KEEP_ACT)

The nONKEY signal is a level, active-low, wake-up interrupt/event intended to switch-on the DA9068 supplied application. nONKEY is always enabled during POWERDOWN mode, so that the application can also be switched-on with a disabled GPIO extender. The nONKEY related events can be disabled via the respective interrupt mask M_nONKEY bits. The DA9068 nONKEY port has an internal 200 kΩ resistor to VBAT.

Each nONKEY press generates an event after a programmable (10 ms to 480 ms) debounce time (register nONKEY_DEB). It can generate nONKEY_LO interrupt if enabled via the interrupt mask bit M_nONKEY_LO. The release of the nONKEY also generates an event after the debounce time programmed in the nONKEY_DEB register. The corresponding nONKEY_HI interrupt can be disabled via the M_ONKEY_HI mask bit.

nONKEY_HOLD is an additional event/interrupt generated by a longer press of the nONKEY (hold time 0.5 s to 4 s, programmable via the NONKEY_HOLD_<x>_DEB registers). When the PMIC is in the POWERDOWN state, the nONKEY_HOLD event is generated after a debounce time nONKEY_HOLDON_DEB. Such an event acts as a wakeup causing a transition towards the SYSTEM domain state. When the PMIC is in the ACTIVE state, the nONKEY_HOLD event is generated after a debounce time nONKEY_HOLDOFF_DEB. The nONKEY_HOLD interrupt generation can be masked via the M_nONKEY_HOLD control bit.

DA9068 also features hardware reboot/reset triggered by nONKEY being asserted for a period of 7.5 s (default setting). The long (reboot/reset) press time is programmable (register PRESS_TIME) from 3 s to 10 s in 0.5 s increments. This functionality can be disabled by clearing power manager control register bit nONKEY_SD. The hardware reboot is enabled by default (ONKEY_AUTOBOOT_EN = 1) and the hardware reset can be enabled via the power manager control register bit nONKEY_SD.

nONKEY also causes a wakeup event in RTC mode (no debouncing).

To ensure the correct functionality, the configuration of the nONKEY debounce times should satisfy the following requirement: NONKEY_DEB < NONKEY_HOLDx_DEB < PRESS_TIME.

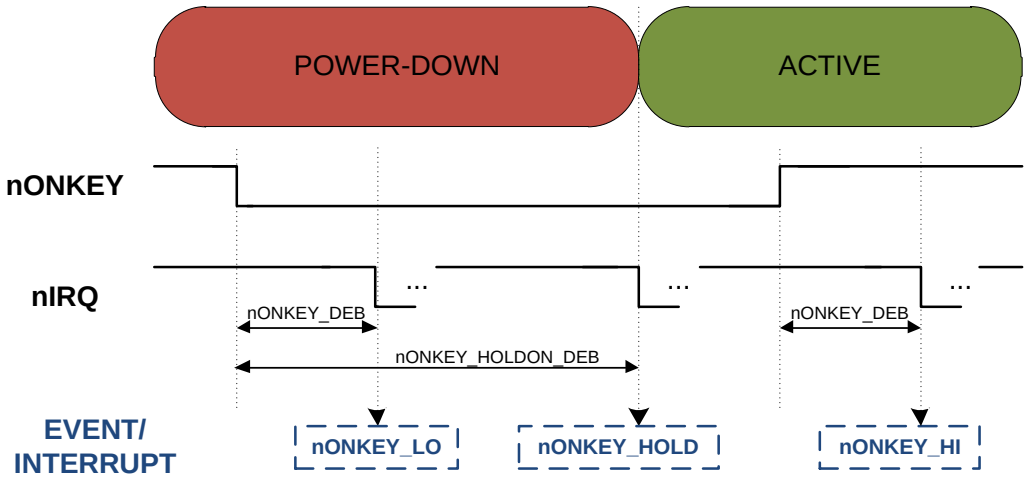

Figure 14: nONKEY ON

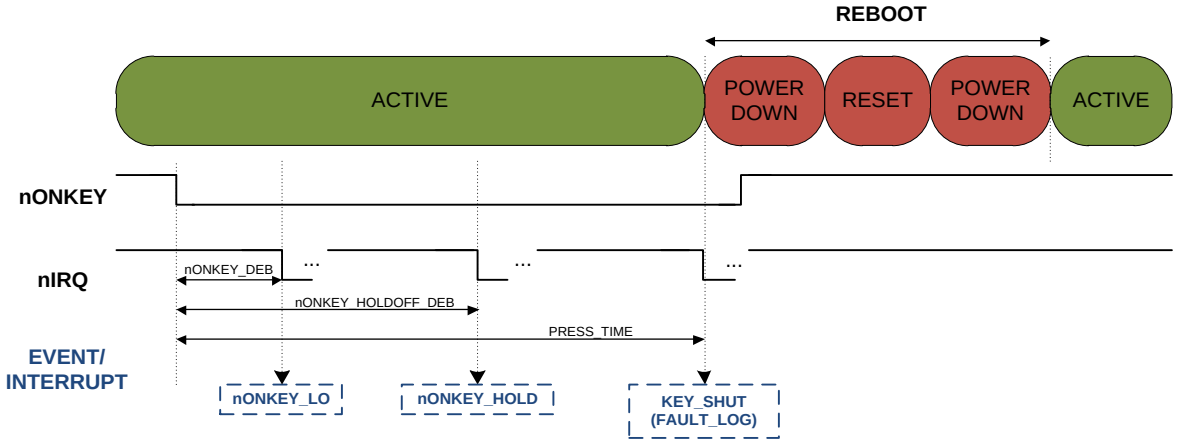

Figure 15: nONKEY OFF (Reboot) (ONKEY_AUTOBOOT_EN = 1)

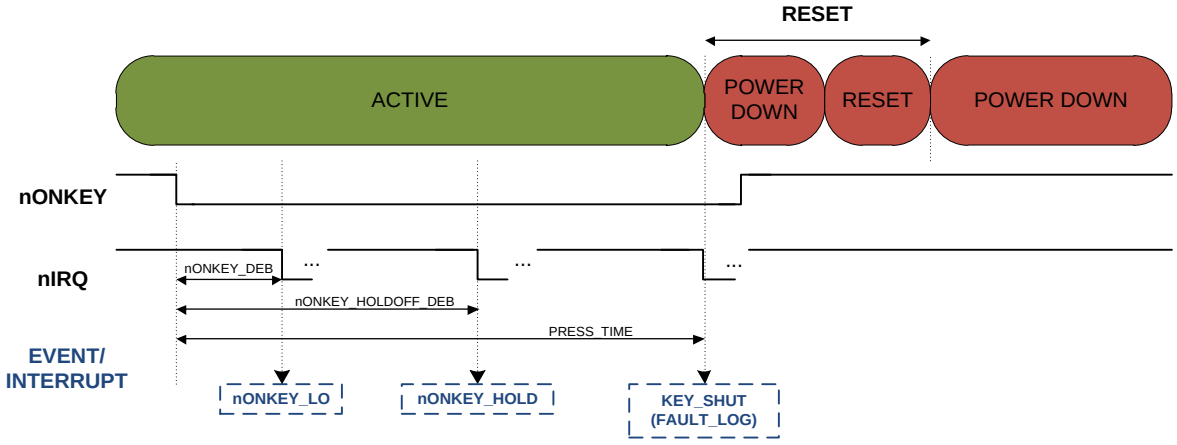

Figure 16: nONKEY OFF (RESET) (ONKEY_AUTOBOOT_EN = 0)

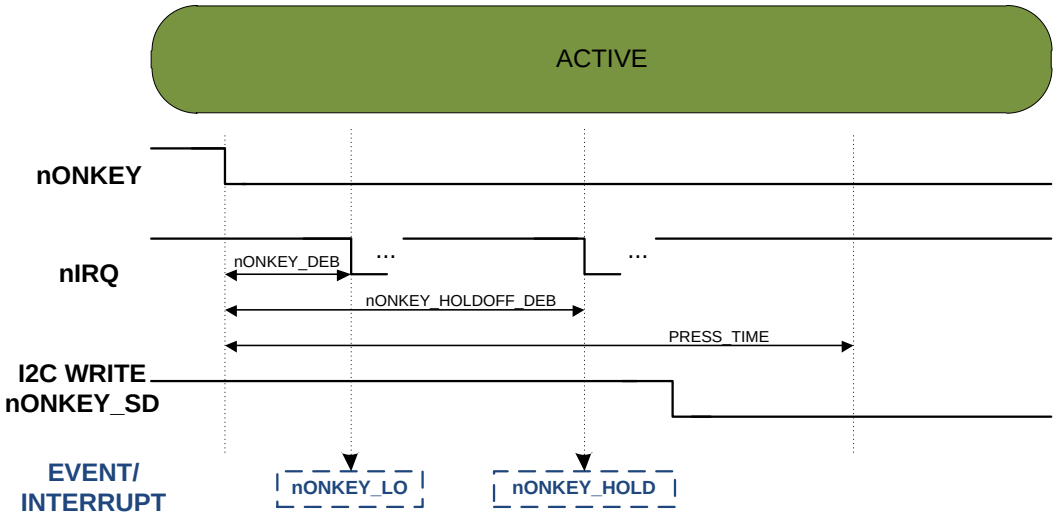

Figure 17: nONKEY Shutdown (with Lock Enabled) (nONKEY_SD = 0)

As illustrated in Figure 18, the nONKEY long press can also generate a Software Reset, when this feature is enabled via the ONKEY_SD_RESET_PULSE_EN control register bit. If this function is enabled, the PM controller generates a 500 ms system reset pulse on the nRESET output without resetting the PMIC itself, that is, all the PMIC controlled supplies remain in the state they were in prior to the nONKEY long press.

When both this feature and the nONKEY shutdown (nONKEY_SD = 1) are enabled, the latter takes precedence and a long nONKEY press will result in a shutdown.

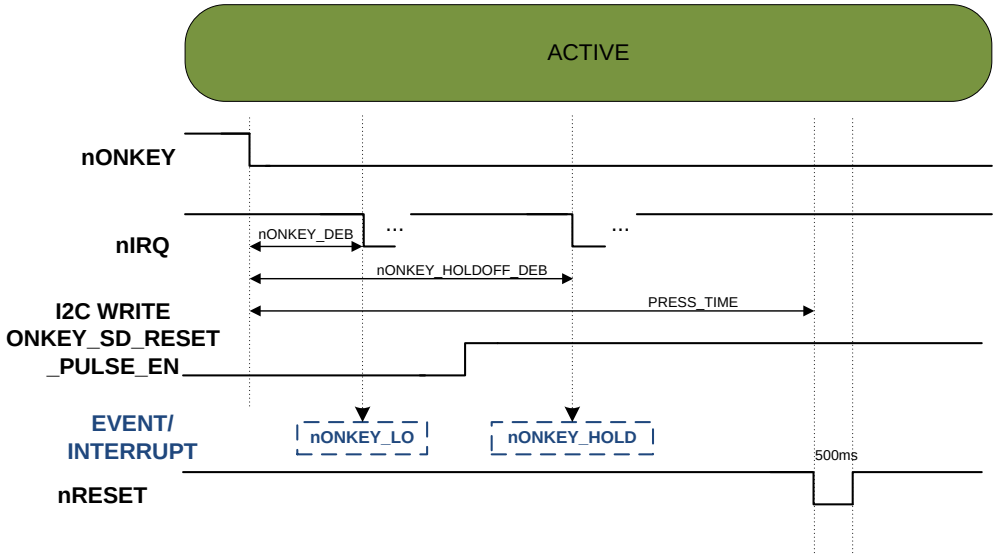

Figure 18: nONKEY Software nRESET (ONKEY_SD_RESET_PULSE_EN = 1)

With control bit KEEPACT_EN set, nONKEY can alternatively be assigned to the watchdog unit so that every assertion of the pin (rising edge sensitive) sets the WATCHDOG bit, similar to a write via the power manager bus. The host has to release KEEP_ACT in advance to the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 µs.

7.4.1.2 Active Low Wakeup Input (nON2)

The nON2 signal is an active-low, wakeup event intended to switch-on DA9068. This DA9068 port has an internal 200 kΩ resistor to VBAT. A change of the nON2 input to active state (configured by nON2_TYPE register) generates an event (stored in the EVENT_C register) and an interrupt, if not masked by the M_nON2 bit. If configured (control register bit nON2_MODE = 1), the nON2 event also generates a wakeup event. nON2 is always enabled while in POWERDOWN mode, so that the application can also be switched-on with a disabled GPIO extender. nON2 is also a wakeup event in RTC mode (no debouncing).

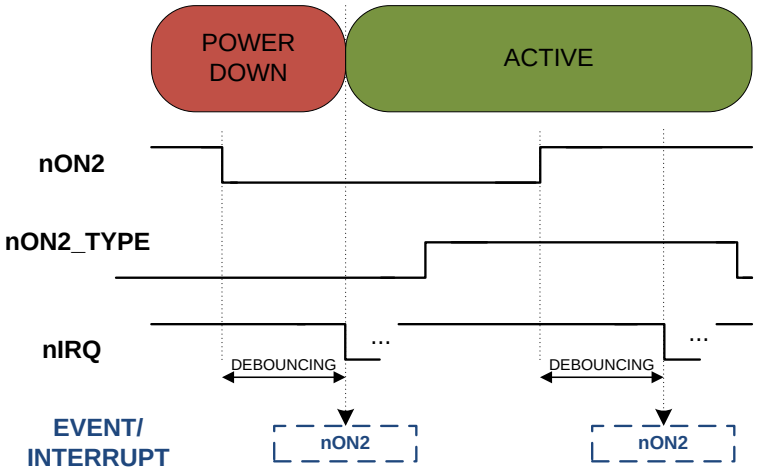

Figure 19: nON2 ON

7.4.1.3 Travel Adapter Input (TA)

The TA signal is an active-high, wake-up interrupt/event intended to switch-on the DA9068 supplied application. A change of the TA input to active state (configured by TA_TYPE register) generates an event (stored in the EVENT_C register) and an interrupt if not masked by the M_TA bit. If configured (control register bit TA_MODE = 1), the TA event also generates a wake-up event. TA is always enabled during POWERDOWN mode so that the application can also be switched on with a disabled GPIO extender.

TA is also a wakeup event in RTC mode (no debouncing).

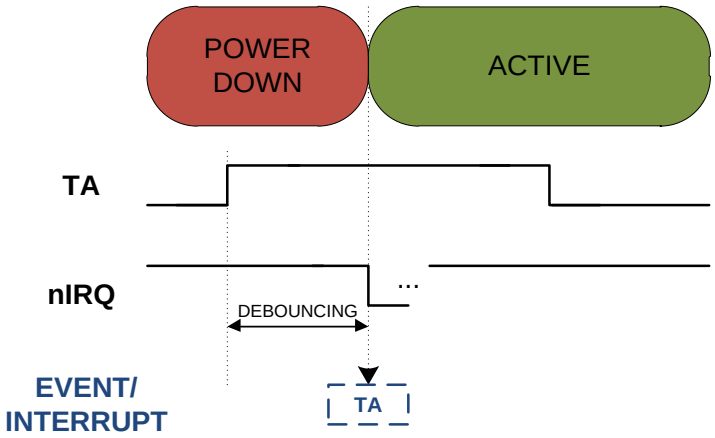

Figure 20: TA ON

The nONKEY, nON2, and TA inputs also act as wake up events that bring DA9068 out of the low power SLEEP mode and resume the normal ACTIVE mode operation. Additionally they cause the PMIC to wake up from RTC mode and transition to POWERDOWN mode. These signals are debounced before the PMIC wakes up from POWERDOWN mode (normal ACTIVE mode wake up). There is no debouncing when waking up from RTC or SLEEP mode.

All DA9068 power manager input buffers can operate from either the VDDIO or the VDDINT supply rail (configuration defined by the PM_I_V register bit).

7.4.1.4 Wakeup from SLEEP

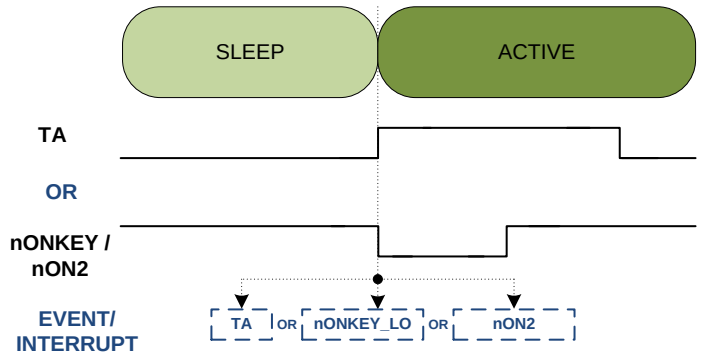

Figure 21: Wakeup from SLEEP

7.4.1.5 Wakeup from RTC

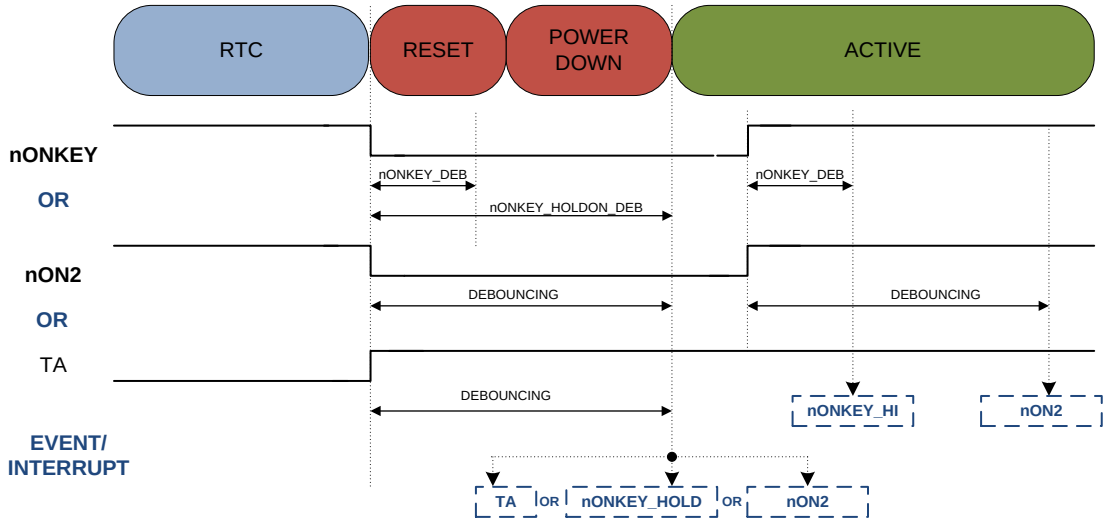

Figure 22: Wakeup from RTC

7.4.1.6 Mode Control Inputs (MCTL1 and MCTL2)

M_CTL1 and M_CTL2 are input signals from the host processor to DA9068 controlling the PMIC and supplies modes of operation. Both inputs are active high and define the functional modes shown in Table 31.

Table 31: M_CTL Input Modes

MCTL2	MCTL1	Mode No.	Operating Mode
0	0	0	SLEEP
0	1	1	NORMAL
1	0	2	LP (Low Power)
1	1	3	TURBO

Changes in the state of these control inputs do not generate events/interrupts and do not force PM logic transitions through the main states, that is, they do not trigger Power Up, Power Down, or Shutdown sequences.

Mode_0/Mode_2 configures DA9068 in SLEEP/LP mode, forcing the DA9068-controlled supplies into a low current consumption mode. This configuration does not change the state of DA9068, it changes the operational mode of the GPADC, LDO and buck supplies as per the settings of the corresponding GPADC_MCTL[3:0], LDO<x>_MCTL[3:0] and BUCK<x>_MCTL[3:0] registers. Normally, in SLEEP and LP modes, the LDO output current is reduced to 10 % of the active state I_{MAX} and the buck converters are configured in Forced PFM mode. Optionally, every LDO and buck supply can be disabled (powered down) or forced to stay ON (active mode with full current capability) during SLEEP/LP mode via the LDO<x>_MCTL and BUCK<x>_MCTL register settings.

In SLEEP/LP mode, the output voltages of Buck0, Buck1, and Buck4 can be automatically set to a different level as defined in the VBUCK0_RET, VBUCK1_RET, and VBUCK4_RET retention voltage registers. Similarly, in TURBO mode, the Buck0 output voltage can be set automatically to a different level as defined in the VBUCK0_TUR voltage register.

When the SLEEP/LP mode is disabled, DA9068 returns to its normal operating mode (Mode_1), with supply outputs defined by the configuration of LDO<x>_MCTL and BUCK<x>_MCTL registers.

The host must ensure the reduced load conditions (10 % of the nominal output current) before forcing DA9068 into SLEEP/LP mode. Similarly, it should first de-assert SLEEP (via MCTL1/2 inputs) before reapplying the full load on the supplies.

The MCTL pins are only active while the MCTL_EN register is set. When active, they have complete control of the supplies, the GPADC, and the digital clock, allowing each supply to be independently configured as ON, OFF, or in SLEEP/LP. The host must set MCTL_EN when it is powered, sequencing has completed and M_CTL<x> pins are correctly driven. The host can clear MCTL_EN at any time, but it is automatically cleared when the state machine leaves ACTIVE state. When transitioning between MCTL control and LDO<x>_EN control and when changing MCTL settings, any supplies that are changing will do so simultaneously.

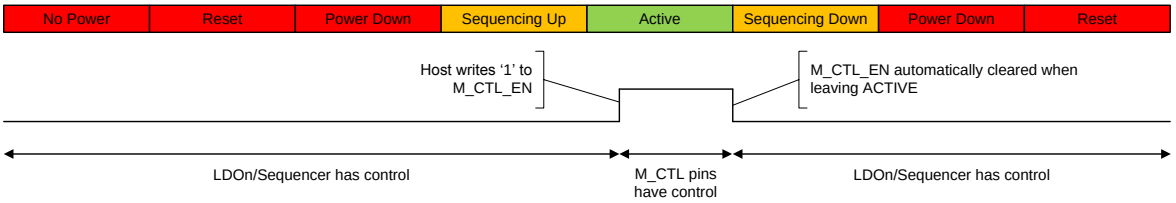

Figure 23: Control from MCTL pins

The LDOs can be in ON, OFF, or SLEEP in each of the four MCTL modes. This is controlled by the LDO<x>_MCTL<n> register and applies to all user LDOs.

Buck0 to Buck6 can also be set to ON, OFF, or SLEEP in each of the M_CTL modes. Buck0, 1, and 4 DVC ramp to a different voltage (VBUCK0/1/4_RET) when configured to be in SLEEP. Buck0 has an additional fourth mode of TURBO, where it DVC ramps to the voltage defined in the VBUCK0_TUR register. The bucks are controlled with BUCK<x>_MCTL[3:0] registers.

The GPADC can be configured as ON, OFF, or SLEEP/LP in each of the MCTL modes via the GPADC_MCTL<x> registers. When configured to SLEEP/LP mode, the ADC operates in the economy mode, that is, performing measurements every 20 ms. If the TEMP1/2 or VF current sources are enabled, they are dynamically switched off at the end of the conversion when the ADC is configured in SLEEP/LP mode.

The digital clock is also configurable to ON or OFF in each of the four MCTL modes. When the clock is off, only certain events can re-awaken the clock and hence the PMIC, see Table 32. When not under MCTL control, the digital clock is normally ON. There is a relationship between being able to turn the clock off and the bucks needing the clock to operate, see Table 32. The clock is controlled with DIG_CLK_MCTL<n>.

Table 32: Digital Clock State

DIG_CLK_MCTL<n>	BUCK<x>_MCTL<n>	Digital Clock State:
0		ON
1	All OFF	OFF
1	All OFF or SLEEP	OFF (after bucks have DVCed to VBUCK<x>_RET and all bucks transitioned to forced PFM)
1	Any ON (or Turbo)	ON (until all bucks have transitioned into PFM due to low load demand), then OFF. If the load does not reduce or the bucks are not in AUTO, PFM may never be achieved and the clock will remain ON. Also, if the clock does get stopped, it will NOT start again in response to an increased load.

7.4.1.7 OUT2_32K Enable Input (OUT2_32K_EN)

The OUT2_32K_EN pin is an active-high input dedicated to the ON/OFF control of the OUT2_32K output.

7.4.1.8 Level-Shifter Input (LVLSH_IN)

The LVLSH_IN pin is a digital input that is level-shifted into LVLSH_OUT output pin.

7.4.1.9 Test Control Input (TP)

TP is a dedicated DA9068 input pin (active-high level) used to enable the operation in Power Commander mode. It is recommended to connect this input to the ground (VSS) node on the application board.

7.4.1.10 Programming Voltage Input (VPP)

VPP is a dedicated DA9068 input used to provide the high voltage (7.5 V) needed for programming the OTP memory. It is recommended to connect this input to the ground (VSS) node on the application board.

7.4.2 Output Ports

Table 33: Output Ports

PAD Name	Type	PAD Description	Configuration
nIRQ	DO	Active Low IRQ Line towards Host	Push/Pull Output
nRESET	DO	Active Low RESET towards Host	Push/Pull Output
EXT_PWRON	DO	Active High Enable signal for external regulator(s)	Push/Pull Output
nVDD_FAULT	DIO	Active Low Indicator for Low V_{BAT}	Push/Pull Output
OUT1_32K	DO	32 kHz Clock Buffer	Push/Pull Output
OUT2_32K	DO	32 kHz Clock Buffer	Push/Pull Output
OUT3_32K	DO	32 kHz Clock Buffer	Push/Pull Output
LVLSH_OUT	DO	Level-Shifter Output	Push/Pull Output
GPO_0	DO	General Purpose Output	Push/Pull Output
GPO_1	DO	General Purpose Output	Push/Pull Output
GPO_2	DO	General Purpose Output	Push/Pull Output

7.4.2.1 Interrupt Request (nIRQ)

nIRQ is an active-low output signal which indicates that an interrupt causing event has occurred and that event and status information is available in the related registers. Such information can be temperature and voltage of the PMIC, fault conditions, status changes at input ports, and so on. The event registers hold information about the events that have occurred. Events are triggered by a status change of the monitored signals.

When an event bit is set, the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ is not released until the related event registers are cleared by writing 1 to the event bit (bits written containing a zero will leave the related event register bits unchanged). The event registers should be written in page/repeated mode because the nIRQ will not be released until all registers with an asserted event have been reset.

New events that occur during writing the event registers will be held until all the event registers have been written. Then they are passed to the event register. This ensures that the host processor does not miss them. The same will happen to all events occurring whilst the sequencer processes time slots (delayed generation of interrupts).

7.4.2.2 Reset Output (nRESET)

The nRESET signal is an active-low output signal from DA9068 to the host processor, which tells the host to enter the hardware reset state. nRESET is always asserted at the beginning of a DA9068 cold start from NO-POWER mode and when the DA9068 initiates the power-down sequence to RESET mode via the user assertion of nONKEY long press, reset from host via control bit SHUTDOWN, or from a DA9068 detected error condition.

After being asserted, nRESET remains low until the reset timer expires. The expiry time can be configured via RESET_TIMER from 1 ms to 1 s. The reset timer trigger signal can be configured via RESET_EVENT to be EXT_WAKEUP, SYS_UP, or PWR_UP.

7.4.2.3 External Regulator Enable Output (EXT_PWRON)

The EXT_PWRON signal is an active-high output signal from DA9068 to the external supply regulator(s) that controls the turn ON and turn OFF of the respective system supply rail(s). The timing of the EXT_PWRON signal assertion/deassertion is controlled by the EXT_PWRON_STEP configuration bits which define the sequencer slot the EXT_PWRON function is allocated to.

7.4.2.4 VBAT Supply Fault (nVDD_FAULT)

nVDD_FAULT is an active-low output signal to the host processor to indicate a VBAT low status. The assertion of nVDD_FAULT indicates that the main battery voltage is low ($V_{BAT} < V_{DD\_FAULT\_LOWER}$) and therefore informs the host processor that if this power condition persists for the next 150 ms the PM controller will initiate the power down sequence. When used as a dedicated nVDDFAULT output (GPIO_PIN = 00), this port is configured as push-pull (PP) output. During the initial DA9068 start-up sequence, this output is in tri-state mode until the device leaves RESET mode and the port is configured from the OTP.

If nVDDFAULT is not used as a dedicated System/PM output, this port can be configured (via the corresponding GPIO_PIN register settings) as a GPIO port (GPIO0).

NOTE
This pin is also used in the Power Commander mode (TP connected to VCORE) to indicate that DA9068 is waiting for the I^2C interface to load the registers with values (replacing the standard values from OTP). nVDD_FAULT is released after the last register has been loaded.

7.4.2.5 Real Time Clock Outputs (OUT1/2/3_32K)

The OUT1/2/3_32K outputs provide the system with the buffered DA9068 32 kHz oscillator clock. Once DA9068 is powered from a valid VBAT supply, the 32 kHz oscillator will always run after the initial start-up from NO-POWER mode and until the device reaches NO-POWER mode again. The OUT1/3_32K buffer can be disabled during POWERDOWN mode with the OUT_32K_PD control bit. DA9068 also provides a dedicated OUT2_32K_EN OTP control bit and a dedicated OUT2_32K_EN input, both of which can be used to enable/disable the second clock output.

OUT1/2/3_32K ports are hardware configured as push-pull output drivers.

7.4.2.6 General Purpose Outputs (GPO_0/1/2)

DA9068 features three general purpose outputs, GPO_0/1/2. They are controlled by a dedicated I^2C register. Their outputs are powered from the V_{DDIO} supply voltage.

7.5 GPIO

DA9068 features one general purpose I/O pin, nVDDFAULT (if not used as low battery voltage indicator output, see Section 7.4.2.4). It is controlled by a dedicated I^2C register and is powered from the VDDIO supply voltage.

The nVDDFAULT GPIO can be configured (GPIO_nON2 register settings) as:

- an active-high or active-low input
- a push-pull output
- an open-drain output with an internal pull up to VDDIO
- an open-drain output with an external pull up resistor to the target voltage level

To guarantee the safe and predictable GPIO operation in all applications, as well to avoid potential leakage and/or shorts between the I/O supply rails, and to prevent DA9068 being back-powered by the VDDIO supply, it is imperative that the following condition is met under all circumstances:

$$(V_{SS} - 0.3\ V) \leq V_{PAD} \leq (V_{DDIO} + 0.3\ V)$$

The input signals can be debounced (configurable debounce time via control DEBOUNCING, 10 ms default) or the state of the assigned status register GPI<x> can be directly changed to high or low. Whenever the status has changed to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked inside the nIRQMASK register).

In RESET mode (prior to the initial OTP read), the GPIO port is configured as a tri-stated open-drain (OD) output with no internal pull-up resistors. When the GPIO module is temporarily disabled by the power sequencer (via GPIO_PD register), level transitions on the input will no longer be detected, but the I/O drivers will not change their configuration and programmed levels.

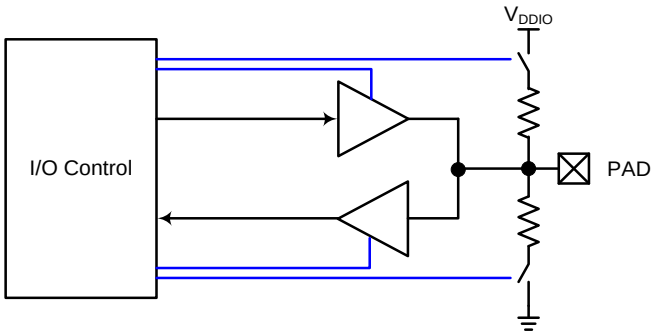

Figure 24: GPIO Block Diagram

7.6 Level-Shifter

DA9068 features one general purpose Level-Shifter.

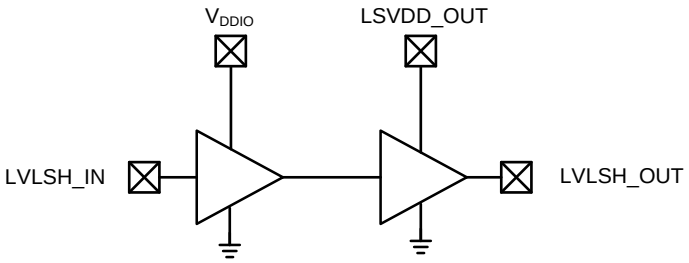

Figure 25: Level-Shifter Block Diagram

7.7 Power-Up Timing

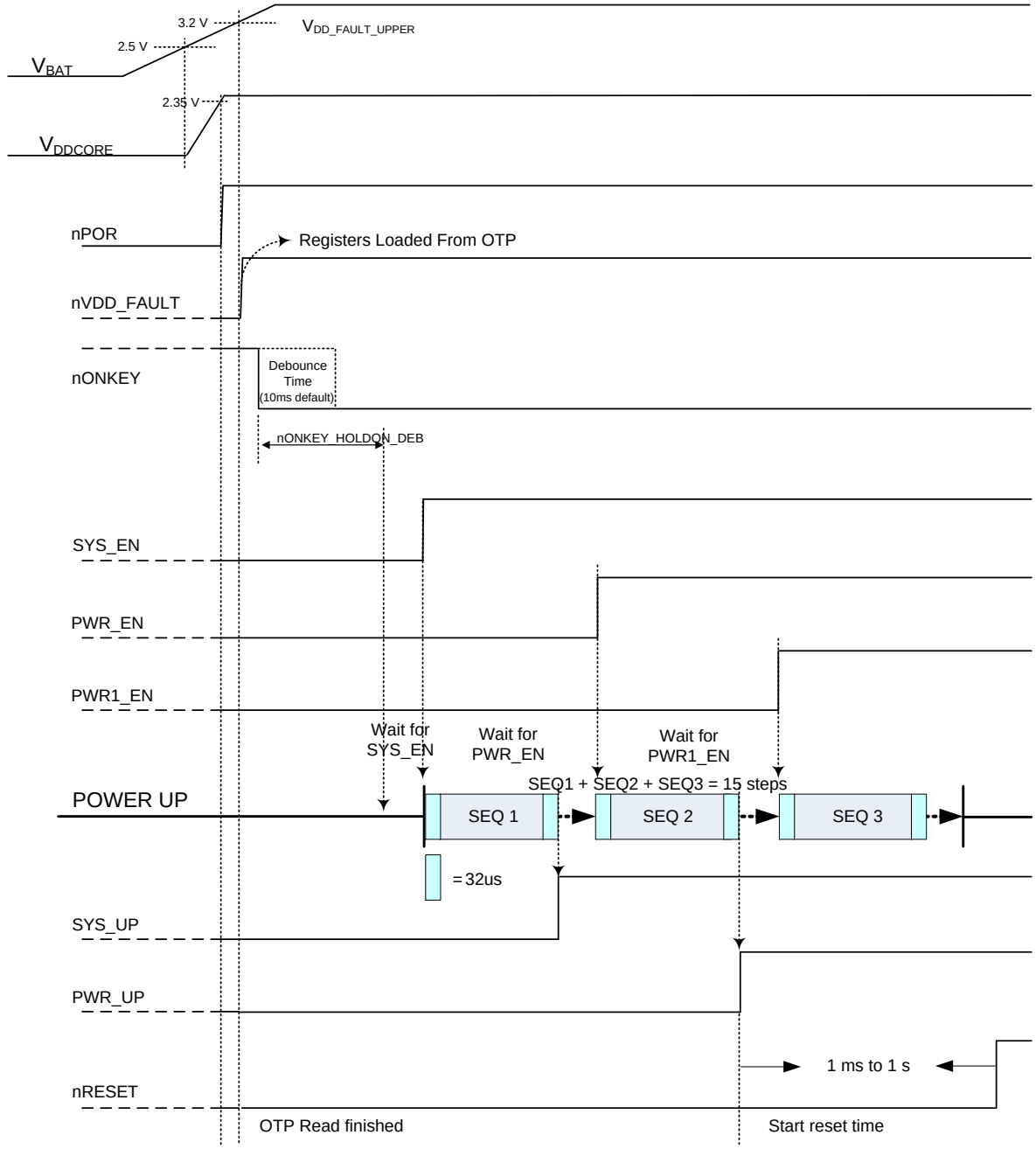

Figure 26: Typical Start-Up Diagram

7.7.1 Power-On Reset (nPOR)

The correct start-up of DA9068 is guaranteed by an internal power-on reset nPOR (active low), generated by the initial connection of the VBAT supply. If a backup power source (battery or super capacitor) was connected to the application before the main power, DA9068 remains off and draws no current.

While VCORE < VPOR_UPPER, the internal nPOR is asserted and DA9068 does not turn on (NO-POWER mode). When VCORE rises above VPOR_UPPER, the nPOR is negated, the RTC counter and FAULT_LOG register are reset, and DA9068 progresses to RESET mode.

From POWERDOWN mode, DA9068 continues with powering up supplies if the power domain SYSTEM was asserted via input port (or set via OTP settings) and AUTO_BOOT was enabled (or a valid wake-event has happened during POWERDOWN mode). Figure 26 shows the start-up events and an example of a typical initial sequence.

If DA9068 causes a RESET from under-voltage detected during start-up or within 10 seconds after releasing nRESET (the start-up initiating supply is not strong enough to supply the application), the PMIC asserts VDD_START in the fault log register and temporarily disables the AUTO_BOOT and the SMPL features for the consecutive start-up. Only events from the user inputs nONKEY, nON2, or TA trigger a wake-up from this specific state. AUTO_BOOT and SMPL are set back to their default values (AUTO_BOOT and SMPL inhibit are cleared) the next time DA9068 is in the domain SYSTEM state.

7.7.2 Application Wake-Up

A valid wake-up event (nONKEY, nON2, TA, RTC Alarm, or SYS_EN register write) initiates an application power up from POWERDOWN mode. If the POWERDOWN mode was reached by progressing from RESET mode, the power sequencer can also be started without waiting for a wake-up event if AUTO_BOOT was asserted or SMPL condition was detected.

If the power domains are not pre-enabled by OTP, the host processor has to control the further application start-up (for example, via the power domain enable registers). Alternatively, DA9068 continues stand-alone, powering up the OTP enabled domains via the power domain sequencer. Start-up from RESET mode powers up the application automatically only if SYS_EN is asserted from the host processor or is set by default from OTP.

Continuing into ACTIVE mode requires an assertion of PWR_EN (from host register write or enabled from OTP). After starting the WATCHDOG timer, the host processor must assert the WATCHDOG timer within the configured time window, via the power manager bus (if Watchdog is enabled). If this does not happen, the state machine will terminate the ACTIVE mode at the end of the time window and return to RESET mode.

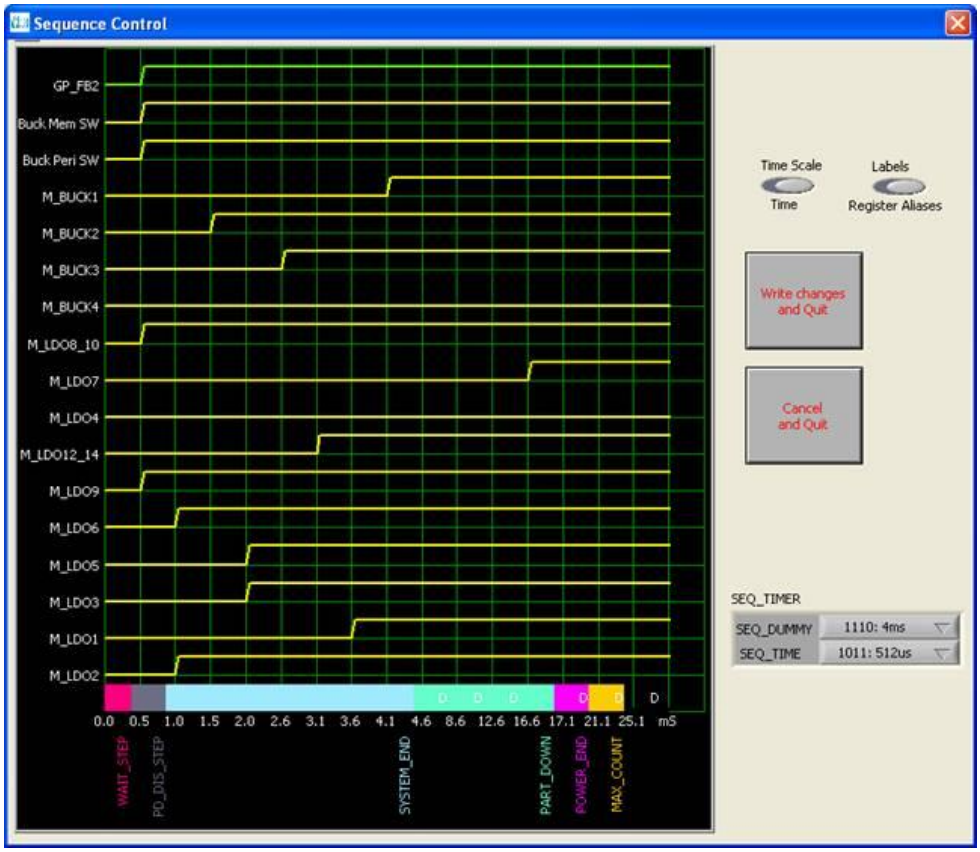

Figure 27: Example Start-Up of DA9068 Powering Up System Supplies

7.8 Control Interface

DA9068 is completely SW-controlled from the host by registers and offers one serial control interface (I^2C) to access these registers. Data is shifted into or out from DA9068 under the control of the host processor, which also provides the serial clock.

The DA9068 interface is a general purpose I^2C interface that can operate in Fast Mode (up to 400 kHz) and High Speed Mode (up to 1.7 MHz) with external (system) pull-up resistors.

7.8.1 DA9068 2-Wire (I^2C) Interface

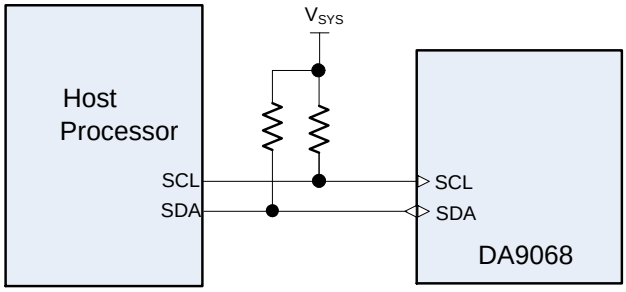

Figure 28: I^2C Interface

Table 34: Serial Interface Pads

PAD Name	Interface	Type	PAD Description
SCL	I^2C	DI	General Purpose I^2C CLOCK (external pull-up)
SDA		DIO	General Purpose I^2C DATA (external pull-up)

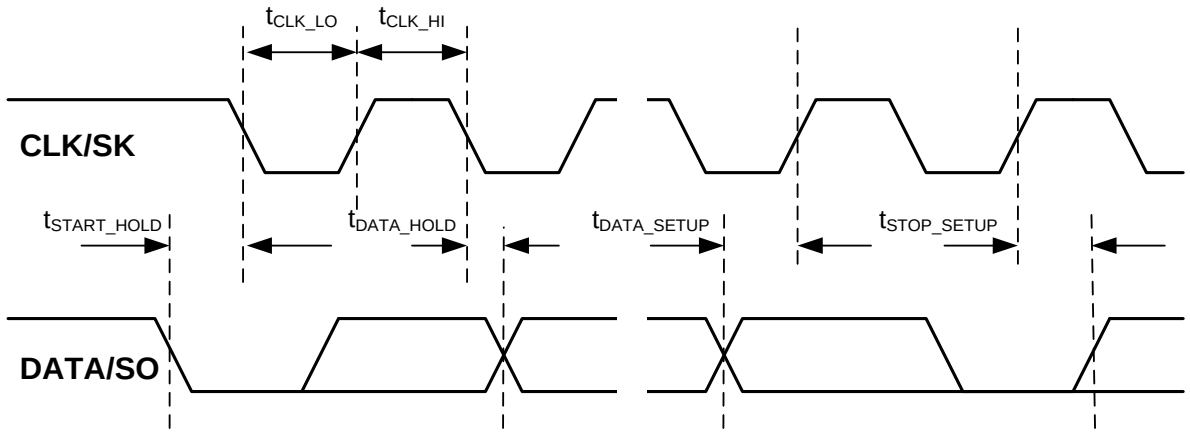

Figure 29: I^2C Bus Timing

8 Register Map

Table 35 provides a summary of the registers. A description of each register is provided in Appendix A.

Table 35: Register Summary

Register	Addr	7	6	5	4	3	2	1	0
Status / Config									
STATUS_A	0x0001	Reserved	M_CTL		VDD_MON_S	Reserved	Reserved	Reserved	Reserved
STATUS_B	0x0002	Reserved	SEQUENCING	Reserved 0	Reserved	Reserved	Reserved 0	Reserved 0	nONKEY
STATUS_C	0x0003	Reserved 0	Reserved 0	GPIO_0	nON2	TA	GPIO_1	Reserved 0	RTC_SMPL
EVENT_A	0x0004	E_TICK	E_SEQ_RDY	E_ALARM	E_VDD_MON	E_VDD_LOW	E_TBAT2	Reserved 0	E_VF
EVENT_B	0x0005	Reserved 0	Reserved 0	E_ADC_EOM	E_TBAT1	E_nONKEY_HOLD_OFF	E_nONKEY_HOLD_ON	E_nONKEY_HI	E_nONKEY_LO
EVENT_C	0x0006	Reserved 0	Reserved 0	GPIO_0	nON2	TA	GPIO_1	Reserved 0	RTC_SMPL
FAULT_LOG	0x0007	WAIT_SHUT	Reserved 0	KEY_SHUT	Reserved	TEMP_OVER	VDD_START	VDD_FAULT	TWD_ERROR
IRQ_MASK_A	0x0008	M_TICK	M_SEQ_RDY	M_ALARM	M_VDD_MON	M_VDD_LOW	M_TBAT2	Reserved 1	M_VF
IRQ_MASK_B	0x0009	Reserved	Reserved	M_ADC_EOM	M_TBAT1	M_nONKEY_HOLD_OFF	M_nONKEY_HOLD_ON	M_nONKEY_HI	M_nONKEY_LO
IRQ_MASK_C	0x000A	Reserved 0	Reserved 0	M_GPIO_0	M_nON2	M_TA	M_GPIO_1	Reserved 1	M_RTC_SMPL
CONTROL_A	0x000B	GPI_V	Reserved 1	Reserved 1	PM_I_V	PM_IF_V	PWR1_EN	PWR_EN	SYS_EN
CONTROL_B	0x000C	SHUTDOWN	DEEP_SLEEP	WRITE_MODE	I2C_SPEED	Reserved	AUTO_BOOT	Reserved	Reserved
CONTROL_C	0x000D	WATCHDOG	TWDSCALE			DEBOUNCING			Reserved 0
CONTROL_D	0x000E	Reserved	ONKEY_SD_RESET_PULSE_EN	ONKEY_AUTOBOOT_EN	nONKEY_SD	KEEPACT_EN	Reserved	EXT_PWRON_DEBUG_EN	EXT_PWRON_PULSE_EN
PD_DIS	0x000F	PM_CONT_PD	OUT_32K_PD	CHG_BBAT_PD	Reserved 0	HS_2_WIRE_PD	PM_IF_PD	GP_ADC_PD	GPIO_PD
INTERFACE	0x0010	IF_BASE_ADDR			Reserved	Reserved	Reserved	Reserved	Reserved
RESET	0x0011	RESET_EVENT		RESET_TIMER					
GPIO									
SMPL_GPIO_0	0x0012	Reserved 1	Reserved 1	Reserved 1	Reserved 0	Reserved 1	Reserved 1	Reserved 1	Reserved 0
TA_GPIO_1	0x0013	TA_MODE	TA_TYPE	TA_PIN		GPIO1_MODE	GPIO1_TYPE	GPIO1_PIN	
GPIO_0_nON2	0x0014	GPIO0_MODE	GPIO0_TYPE	GPIO0_PIN		nON2_MODE	nON2_TYPE	nON2_PIN	
Sequencer									
ID_0_1	0x0015	LDO1_STEP				WAIT_ID_ALWAYS	SYS_PRE	DEF_SUPPLY	nRES_MODE
ID_2_3	0x0016	LDO3_STEP				LDO2_STEP			
ID_4_5	0x0017	LDO5_STEP				LDO4_STEP			
ID_6_7	0x0018	LDO7_STEP				LDO6_STEP			
ID_8_9	0x0019	LDO9_STEP				LDO8_STEP			
ID_10_11	0x001A	LDO11_STEP				LDO10_STEP			
ID_12_13	0x001B	PD_DIS_STEP				LDO12_STEP			
ID_14_15	0x001C	BUCK1_STEP				BUCK0_STEP			
ID_16_17	0x001D	BUCK3_STEP				BUCK2_STEP			
ID_18_19	0x001E	BUCK6_STEP				BUCK4_STEP			
ID_20_21	0x001F	Reserved	Reserved	Reserved	Reserved	EXT_PWRON_STEP			
SEQ_STATUS	0x0020	SEQ_POINTER				WAIT_STEP			
SEQ_A	0x0021	POWER_END				SYSTEM_END			
SEQ_B	0x0022	PART_DOWN				MAX_COUNT			
SEQ_TIMER	0x0023	SEQ_DUMMY				SEQ_TIME			
Supplies									
BUCK0_CONF0	0x0024	BUCK0_EN	VBUCK0						
BUCK0_CONF1	0x0025	BUCK0_PD_DIS	BUCK0_SYNC_ILIM					BUCK0_MODE	
BUCK0_CONF2	0x0026	Reserved 0	Reserved 1	Reserved 0	BUCK0_SLEEP_ILIM				
BUCK1_CONF0	0x0027	BUCK1_EN	VBUCK1						
BUCK1_CONF1	0x0028	BUCK1_PD_DIS	BUCK1_SYNC_ILIM					BUCK1_MODE	
BUCK1_CONF2	0x0029	Reserved 0	Reserved 1	Reserved 0	BUCK1_SLEEP_ILIM				
BUCK2_CONF0	0x002A	BUCK2_EN	VBUCK2						
BUCK2_CONF1	0x002B	BUCK2_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK2_SYNC_ILIM		BUCK2_MODE	
BUCK3_CONF0	0x002C	BUCK3_EN	VBUCK3						
BUCK3_CONF1	0x002D	BUCK3_PD_DIS	BUCK3_START_MODE		Reserved	BUCK3_SYNC_ILIM		BUCK3_MODE	
BUCK4_CONF0	0x002E	BUCK4_EN	VBUCK4						

Register	Addr	7	6	5	4	3	2	1	0
BUCK4_CONF1	0x002F	BUCK4_PD_DIS	BUCK4_START_MODE		Reserved	BUCK4_SYNC_ILIM		BUCK4_MODE	
BUCK5_CONF0	0x0030	Reserved 0	VBUCK5						
BUCK5_CONF1	0x0031	BUCK5_PD_DIS	BUCK5_START_MODE		Reserved	BUCK5_SYNC_ILIM		BUCK5_MODE	
BUCK6_CONF0	0x0032	BUCK5and6_EN	VBUCK6						
BUCK6_CONF1	0x0033	BUCK6_PD_DIS	BUCK6_START_MODE		Reserved	BUCK6_SYNC_ILIM		BUCK6_MODE	
BUCKRF_THR	0x0034	RFBUCK_SNC_THR				RFBUCK_SLP_THR			
BUCKRF_CONF	0x0035	RFBUCK_EN	Reserved	RFBUCK_6M_SEL	RFBUCK_I_BYP_LMT	RFBUCK_I_N_LMT_SEL		RFBUCK_I_P_LMT_SEL	
LDO1	0x0036	LDO1_PD_DIS	LDO1_EN	VLDO1					
LDO2	0x0037	LDO2_PD_DIS	LDO2_EN	VLDO2					
LDO3	0x0038	LDO3_PD_DIS	LDO3_EN	VLDO3					
LDO4	0x0039	LDO4_PD_DIS	LDO4_EN	VLDO4					
LDO5	0x003A	LDO5_PD_DIS	LDO5_EN	VLDO5					
LDO6	0x003B	LDO6_PD_DIS	LDO6_EN	VLDO6					
LDO7	0x003C	LDO7_PD_DIS	LDO7_EN	VLDO7					
LDO8	0x003D	LDO8_PD_DIS	LDO8_EN	VLDO8					
LDO9	0x003E	LDO9_PD_DIS	LDO9_EN	VLDO9					
LDO10	0x003F	LDO10_PD_DIS	LDO10_EN	VLDO10					
LDO11	0x0040	LDO11_PD_DIS	LDO11_EN	VLDO11					
LDO12	0x0041	LDO12_PD_DIS	LDO12_EN	VLDO12					
LDO13	0x0042	LDO13_PD_DIS	LDO13_EN	VLDO13					
LDO14	0x0043	LDO14_PD_DIS	LDO14_EN	VLDO14					
LDO15	0x0044	LDO15_PD_DIS	LDO15_EN	VLDO15					
LDO16	0x0045	LDO16_PD_DIS	LDO16_EN	VLDO16					
LDO17	0x0046	LDO17_PD_DIS	LDO17_EN	VLDO17					
LDO18	0x0047	LDO18_PD_DIS	LDO18_EN	VLDO18					
LDO19	0x0048	LDO19_PD_DIS	LDO19_EN	VLDO19					
LDO20	0x0049	LDO20_PD_DIS	LDO20_EN	VLDO20					
LDO21	0x004A	LDO21_PD_DIS	LDO21_EN	VLDO21					
LDO22	0x004B	LDO22_PD_DIS	LDO22_EN	VLDO22					
LDO23	0x004C	LDO23_PD_DIS	LDO23_EN	VLDO23					
LDO24	0x004D	LDO24_PD_DIS	LDO24_EN	VLDO24					
LDO25	0x004E	LDO25_PD_DIS	LDO25_EN	VLDO25					
SUPPLY	0x004F	OUT2_32K_EN	CLK_32K_INV	Reserved	BBCHG_EN	Reserved	Reserved	Reserved	Reserved 0
Mode Control									
LDO1_MCTL	0x0050	LDO1_MCTL3		LDO1_MCTL2		LDO1_MCTL1		LDO1_MCTL0	
LDO2_MCTL	0x0051	LDO2_MCTL3		LDO2_MCTL2		LDO2_MCTL1		LDO2_MCTL0	
LDO3_MCTL	0x0052	LDO3_MCTL3		LDO3_MCTL2		LDO3_MCTL1		LDO3_MCTL0	
LDO4_MCTL	0x0053	LDO4_MCTL3		LDO4_MCTL2		LDO4_MCTL1		LDO4_MCTL0	
LDO5_MCTL	0x0054	LDO5_MCTL3		LDO5_MCTL2		LDO5_MCTL1		LDO5_MCTL0	
LDO6_MCTL	0x0055	LDO6_MCTL3		LDO6_MCTL2		LDO6_MCTL1		LDO6_MCTL0	
LDO7_MCTL	0x0056	LDO7_MCTL3		LDO7_MCTL2		LDO7_MCTL1		LDO7_MCTL0	
LDO8_MCTL	0x0057	LDO8_MCTL3		LDO8_MCTL2		LDO8_MCTL1		LDO8_MCTL0	
LDO9_MCTL	0x0058	LDO9_MCTL3		LDO9_MCTL2		LDO9_MCTL1		LDO9_MCTL0	
LDO10_MCTL	0x0059	LDO10_MCTL3		LDO10_MCTL2		LDO10_MCTL1		LDO10_MCTL0	
LDO11_MCTL	0x005A	LDO11_MCTL3		LDO11_MCTL2		LDO11_MCTL1		LDO11_MCTL0	
LDO12_MCTL	0x005B	LDO12_MCTL3		LDO12_MCTL2		LDO12_MCTL1		LDO12_MCTL0	
LDO13_MCTL	0x005C	LDO13_MCTL3		LDO13_MCTL2		LDO13_MCTL1		LDO13_MCTL0	
LDO14_MCTL	0x005D	LDO14_MCTL3		LDO14_MCTL2		LDO14_MCTL1		LDO14_MCTL0	
LDO15_MCTL	0x005E	LDO15_MCTL3		LDO15_MCTL2		LDO15_MCTL1		LDO15_MCTL0	
LDO16_MCTL	0x005F	LDO16_MCTL3		LDO16_MCTL2		LDO16_MCTL1		LDO16_MCTL0	

Register	Addr	7	6	5	4	3	2	1	0
LDO17_MCTL	0x0060	LDO17_MCTL3		LDO17_MCTL2		LDO17_MCTL1		LDO17_MCTL0	
LDO18_MCTL	0x0061	LDO18_MCTL3		LDO18_MCTL2		LDO18_MCTL1		LDO18_MCTL0	
LDO19_MCTL	0x0062	LDO19_MCTL3		LDO19_MCTL2		LDO19_MCTL1		LDO19_MCTL0	
LDO20_MCTL	0x0063	LDO20_MCTL3		LDO20_MCTL2		LDO20_MCTL1		LDO20_MCTL0	
LDO21_MCTL	0x0064	LDO21_MCTL3		LDO21_MCTL2		LDO21_MCTL1		LDO21_MCTL0	
LDO22_MCTL	0x0065	LDO22_MCTL3		LDO22_MCTL2		LDO22_MCTL1		LDO22_MCTL0	
LDO23_MCTL	0x0066	LDO23_MCTL3		LDO23_MCTL2		LDO23_MCTL1		LDO23_MCTL0	
LDO24_MCTL	0x0067	LDO24_MCTL3		LDO24_MCTL2		LDO24_MCTL1		LDO24_MCTL0	
LDO25_MCTL	0x0068	LDO25_MCTL3		LDO25_MCTL2		LDO25_MCTL1		LDO25_MCTL0	
BUCK0_MCTL	0x0069	BUCK0_MCTL3		BUCK0_MCTL2		BUCK0_MCTL1		BUCK0_MCTL0	
BUCK1_MCTL	0x006A	BUCK1_MCTL3		BUCK1_MCTL2		BUCK1_MCTL1		BUCK1_MCTL0	
BUCK2_MCTL	0x006B	BUCK2_MCTL3		BUCK2_MCTL2		BUCK2_MCTL1		BUCK2_MCTL0	
BUCK3_MCTL	0x006C	BUCK3_MCTL3		BUCK3_MCTL2		BUCK3_MCTL1		BUCK3_MCTL0	
BUCK4_MCTL	0x006D	BUCK4_MCTL3		BUCK4_MCTL2		BUCK4_MCTL1		BUCK4_MCTL0	
BUCK5_MCTL	0x006E	BUCK5_MCTL3		BUCK5_MCTL2		BUCK5_MCTL1		BUCK5_MCTL0	
BUCK6_MCTL	0x006F	BUCK6_MCTL3		BUCK6_MCTL2		BUCK6_MCTL1		BUCK6_MCTL0	
BUCK_RF_MCTL	0x0070	BUCK_RF_MCTL3		BUCK_RF_MCTL2		BUCK_RF_MCTL1		BUCK_RF_MCTL0	
GPADC_MCTL	0x0071	GPADC_MCTL3		GPADC_MCTL2		GPADC_MCTL1		GPADC_MCTL0	
MISC_MCTL	0x0072	DIG_CLK_MCTL3	DIG_CLK_MCTL2	DIG_CLK_MCTL1	DIG_CLK_MCTL0	BBAT_MCTL3	BBAT_MCTL2	BBAT_MCTL1	BBAT_MCTL0
VBUCK0_MCTL_RET	0x0073	Reserved	VBUCK0_RET						
VBUCK0_MCTL_TUR	0x0074	Reserved	VBUCK0_TUR						
VBUCK1_MCTL_RET	0x0075	Reserved	VBUCK1_RET						
VBUCK4_MCTL_RET	0x0076	Reserved	VBUCK4_RET						
Control									
WAIT_CONT	0x0077	WAIT_DIR	RTC_CLOCK	WAIT_MODE	EN_32K	DELAY_TIME			
ONKEY_CONT1	0x0078	NONKEY_DEB				PRESS_TIME			
ONKEY_CONT2	0x0079	Reserved	NONKEY_HOLD_OFF_DEB			Reserved	NONKEY_HOLD_ON_DEB		
POWER_CONT	0x007A	NON2_MCTRL_WAKE_DIS	RTC_AUTO_EN	Reserved 0	Reserved 0	BBAT_ILIM_IGNORE	Reserved 0	Reserved 0	MCTRL_EN
VDDFAULT	0x007B	Reserved	Reserved	vdd_fault_adj				vdd_hyst_adj	
BBAT_CONT	0x007C	BCHARGER_ISET				BCHARGER_VSET			
ADC									
ADC_MAN	0x007D	ISRC_50U	Reserved	Reserved	MAN_CONV	MUX_SEL			
ADC_CONT	0x007E	ADC_AUTO_EN	ADC_MODE	TEMP1_ISRC_EN	VF_ISRC_EN	TEMP2_ISRC_EN	AUTO_ADCIN_EN	AUTO_VF_EN	AUTO_VBAT_EN
ADC_RES_L	0x0080	Reserved	Reserved	Reserved	Reserved	ADC_RES_LSB			
ADC_RES_H	0x0081	ADC_RES_MSB							
VBAT_RES	0x0082	VBAT_RES_MSB							
VDDOUT_MON	0x0083	VDDOUT_MON							
TEMP1_RES	0x0084	TBAT1_RES							
TEMP1_HIGHP	0x0085	TEMP1_HIGHP							
TEMP1_HIGHN	0x0086	TEMP1_HIGHN							
TEMP1_LOW	0x0087	TEMP1_LOW							
T_OFFSET	0x0088	T_OFFSET							
VF_RES	0x0089	VF_RES_MSB							
VF_HIGH	0x008A	VF_HIGH							
VF_LOW	0x008B	VF_LOW							
ADCIN5_RES	0x008C	ADCIN_RES							
TEMP2_RES	0x008F	TBAT2_RES							
TEMP2_HIGHP	0x0090	TEMP2_HIGHP							
TEMP2_HIGHN	0x0091	TEMP2_HIGHN							
TEMP2_LOW	0x0092	TEMP2_LOW							
TJUNC_RES	0x0093	TJUNC_RES							
ADC_RES_AUTO1	0x0094	TEMP1_RES_LSB				VBAT_RES_LSB			
ADC_RES_AUTO2	0x0095	ADCIN_RES_LSB				VF_RES_LSB			
ADC_RES_AUTO3	0x0096	TJUNC_RES_LSB				TEMP2_RES_LSB			
RTC									
COUNT_S	0x0097	Reserved	Reserved	COUNT_SEC					
COUNT_MI	0x0098	Reserved	Reserved	COUNT_MIN					
COUNT_H	0x0099	Reserved	Reserved	Reserved	COUNT_HOUR				
COUNT_D	0x009A	Reserved	Reserved	Reserved	COUNT_DAY				
COUNT_MO	0x009B	Reserved	Reserved	Reserved	Reserved	COUNT_MONTH			
COUNT_Y	0x009C	Reserved	MONITOR	COUNT_YEAR					
ALARM_S	0x009D	Reserved	Reserved	ALARM_SEC					
ALARM_MI	0x009E	TICK_TYPE	Reserved	ALARM_MIN					
ALARM_H	0x009F	Reserved	Reserved	Reserved	ALARM_HOUR				
ALARM_D	0x00A0	Reserved	Reserved	Reserved	ALARM_DAY				
ALARM_MO	0x00A1	Reserved	Reserved	Reserved	Reserved	ALARM_MONTH			

Register	Addr	7	6	5	4	3	2	1	0
ALARM_Y	0x00A2	TICK_ON	ALARM_ON	ALARM_YEAR					
RTC_REG_3	0x00A3	RTC_REGS_3							
RTC_REG_2	0x00A4	RTC_REGS_2							
RTC_REG_1	0x00A5	RTC_REGS_1							
RTC_REG_0	0x00A6	RTC_REGS_0							
OTP Config									
CHIP_ID	0x00A7	MRC				TRC			
CONFIG_ID	0x00A8	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	CONF_ID		
OTP_CONT	0x00A9	GP_WRITE_DIS	OTP_CONF_LOCK	Reserved	Reserved	OTP_CONF	Reserved	OTP_RP	OTP_TRANSFER
OSC_TRIM	0x00AA	TRIM_32K							
GP_ID_0	0x00AB	GP_0							
GP_ID_1	0x00AC	GP_1							
GP_ID_2	0x00AD	GP_2							
GP_ID_3	0x00AE	GP_3							
GP_ID_4	0x00AF	GP_4							
GP_ID_5	0x00B0	GP_5							
Configuration									
GEN_CONF_0	0x00B1	ADCIN_SEL							
GEN_CONF_1	0x00B2	GPO_CTRL							
BUCK0_CONF5	0x0129	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK0_IAUTSLP			
BUCK1_CONF5	0x0134	Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK1_IAUTSLP			
BUCK7_PDDIS_EXT_CTRL_32K	0x015B	buck7_pddis_ext_ctrl_32k							

9 Package Information

9.1 Package Outlines

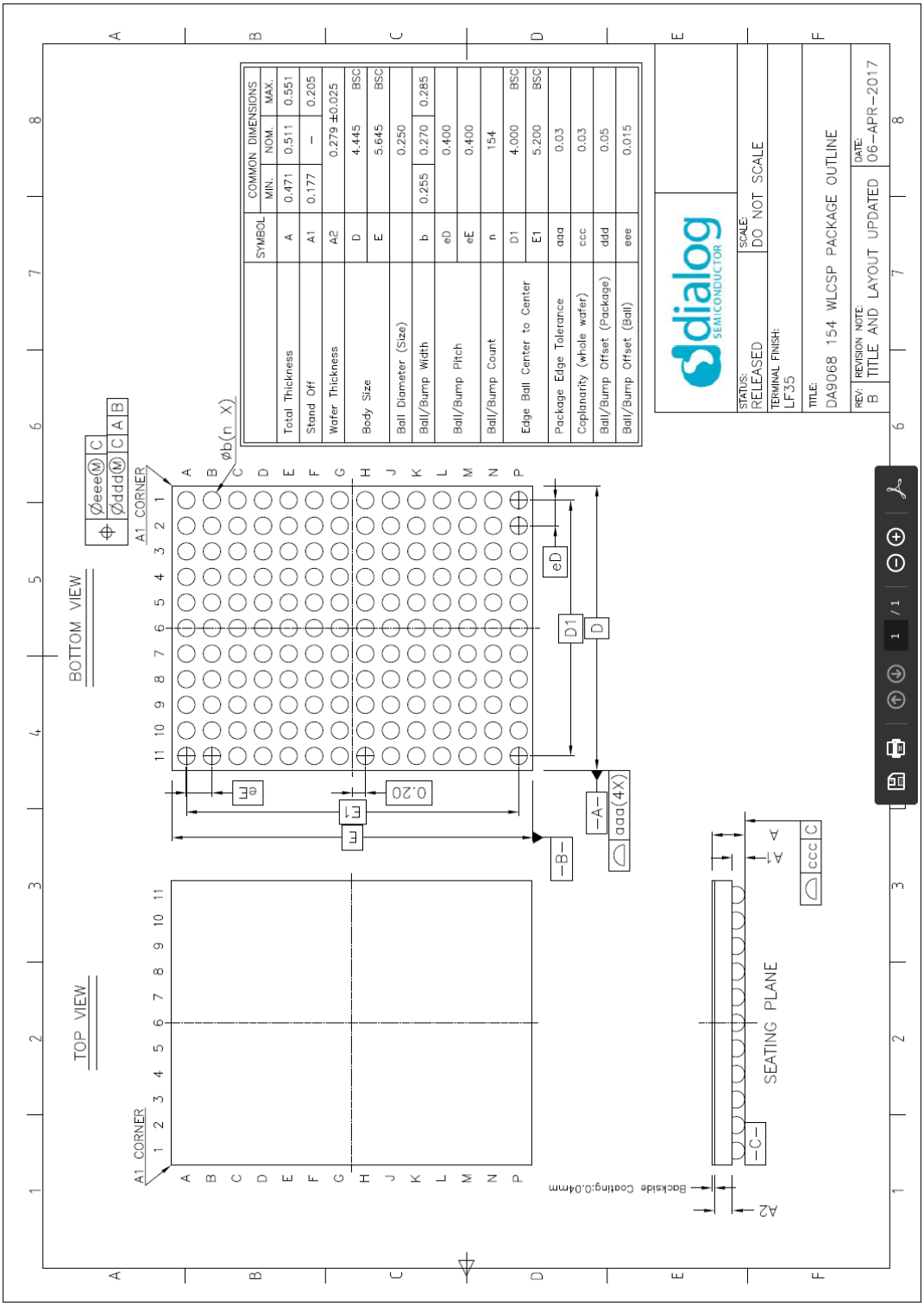

Figure 30: Package Outline Drawing

10 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Dialog Semiconductor sales representative.

Table 36: Ordering Information

Part Number (Note 1)	Package	Size (mm)	Shipment Form	Pack Quantity
DA9068-xxyy2	WLCSP	4 x 6, 0.4 pitch	T&R	

Note 1 xx represents a placeholder for the specific OTP variant.

Appendix A Register Descriptions

This appendix describes the registers summarized in Section 8.

A.1 Status / Config

Table 37: Register STATUS_A

Address	Name	POR value	Status
0x0001	STATUS_A	0x00	

7	6	5	4	3	2	1	0
Reserved	M_CTL		VDD_MON_S	Reserved	Reserved	Reserved	Reserved

Field name	Bits	Type	POR	Description
M_CTL	[6:5]	RO	0x0	M_CTL pin level
VDD_MON_S	[4]	RO	0x0	VDD monitor level

Table 38: Register STATUS_B

Address	Name	POR value	Status
0x0002	STATUS_B	0x00	

7	6	5	4	3	2	1	0
Reserved	SEQUENCING	Reserved 0	Reserved	Reserved	Reserved 0	Reserved 0	nONKEY

Field name	Bits	Type	POR	Description
SEQUENCING	[6]	RO	0x0	Sequencer is processing IDs
nONKEY	[0]	RO	0x0	nONKEY status

Table 39: Register STATUS_C

Address	Name	POR value	Status
0x0003	STATUS_C	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	GPIO_0	nON2	TA	GPIO_1	Reserved 0	RTC_SMPL

Field name	Bits	Type	POR	Description
GPIO_0	[5]	RO	0x0	unused
nON2	[4]	RO	0x0	nON2 monitor level
TA	[3]	RO	0x0	TA monitor level
GPIO_1	[2]	RO	0x0	unused
RTC_SMPL	[0]	RO	0x0	RTC_SMPL

Table 40: Register EVENT_A

Address	Name	POR value	IRQ event
0x0004	EVENT_A	0x00	

7	6	5	4	3	2	1	0
E_TICK	E_SEQ_RDY	E_ALARM	E_VDD_MON	E_VDD_LOW	E_TBAT2	Reserved 0	E_VF

Field name	Bits	Type	POR	Description
E_TICK	[7]	RW W1CL	0x0	Event - RTC Tick Alarm
E_SEQ_RDY	[6]	RW W1CL	0x0	Event - Sequencer Reached Stop Position
E_ALARM	[5]	RW W1CL	0x0	Event - RTC Calendar Alarm
E_VDD_MON	[4]	RW W1CL	0x0	Event - VDD below vdd_mon comparator threshold (3.1 V)
E_VDD_LOW	[3]	RW W1CL	0x0	Event - VDD below vddout_mon ADC threshold
E_TBAT2	[2]	RW W1CL	0x0	Event - TBAT2 temperature threshold out of range
E_VF	[0]	RW W1CL	0x0	Event - VF is out of range

Table 41: Register EVENT_B

Address	Name	POR value	IRQ event
0x0005	EVENT_B	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	E_ADC_EOM	E_TBAT1	E_nONKEY_HOLD_OFF	E_nONKEY_HOLD_ON	E_nONKEY_HI	E_nONKEY_LO

Field name	Bits	Type	POR	Description
E_ADC_EOM	[5]	RW W1CL	0x0	Event - ADC Manual Conversion Result Ready
E_TBAT1	[4]	RW W1CL	0x0	Event TBAT1 temperature threshold out of range
E_nONKEY_HOLD_OFF	[3]	RW W1CL	0x0	Event - nONKEY low for longer than Unknown Register: HOLD_OFF_DEB in Active state Assertion
E_nONKEY_HOLD_ON	[2]	RW W1CL	0x0	Event - nONKEY low for longer than Unknown Register: HOLD_ON_DEB in inactive state Assertion
E_nONKEY_HI	[1]	RW W1CL	0x0	Event - nONKEY High for Field: NONKEY_DEB (Reg: ONKEY_CONT1 [0x0078]) Assertion
E_nONKEY_LO	[0]	RW W1CL	0x0	Event - nONKEY low for Field: NONKEY_DEB (Reg: ONKEY_CONT1 [0x0078]) Assertion

Table 42: Register EVENT_C

Address	Name	POR value	IRQ event
0x0006	EVENT_C	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	GPIO_0	nON2	TA	GPIO_1	Reserved 0	RTC_SMPL

Field name	Bits	Type	POR	Description
GPIO_0	[5]	RW W1CL	0x0	Event- GPIO_0
nON2	[4]	RW W1CL	0x0	Event – nON2
TA	[3]	RW W1CL	0x0	Event - TA
GPIO_1	[2]	RW W1CL	0x0	Event- GPIO_1
RTC_SMPL	[0]	RW W1CL	0x0	Event - RTC_SMPL

Table 43: Register FAULT_LOG

Address	Name	POR value	
0x0007	FAULT_LOG	0x02	

7	6	5	4	3	2	1	0
WAIT_SHUT	Reserved 0	KEY_SHUT	Reserved	TEMP_OVER	VDD_START	VDD_FAULT	TWD_ERROR

Field name	Bits	Type	POR	Description
WAIT_SHUT	[7]	RW W1CL	0x0	Power Down by Time Out of ID WAIT_STEP
KEY_SHUT	[5]	RW W1CL	0x0	Power Down by a Long Press of nONKEY
TEMP_OVER	[3]	RW W1CL	0x0	Junction Over Temperature Detection
VDD_START	[2]	RW W1CL	0x0	Power Down by VBAT Under Voltage Detection (within 10 seconds from releasing nRESET)
VDD_FAULT	[1]	RW W1CL	0x1	Power Down by VBAT Under Voltage Detection
TWD_ERROR	[0]	RW W1CL	0x0	Watchdog Time Violation

Table 44: Register IRQ_MASK_A

Address	Name	POR value	IRQ event mask
0x0008	IRQ_MASK_A	0x02	

7	6	5	4	3	2	1	0
M_TICK	M_SEQ_RDY	M_ALARM	M_VDD_MON	M_VDD_LOW	M_TBAT2	Reserved 1	M_VF

Field name	Bits	Type	POR	Description
M_TICK	[7]	RW OTP	0x0	nIRQ Mask - RTC Tick Alarm Event
M_SEQ_RDY	[6]	RW OTP	0x0	nIRQ Mask - Sequencer Reached Stop Position Event
M_ALARM	[5]	RW OTP	0x0	nIRQ Mask - RTC Calendar Alarm Event
M_VDD_MON	[4]	RW OTP	0x0	nIRQ_Mask - VDD_MON voltage level warning
M_VDD_LOW	[3]	RW OTP	0x0	nIRQ_Mask - VDD below ADC vdd_mon threshold
M_TBAT2	[2]	RW OTP	0x0	nIRQ Mask - TBAT1 temperature threshold out of range
M_VF	[0]	RW OTP	0x0	nIRQ_Mask - VF out of range

Table 45: Register IRQ_MASK_B

Address	Name	POR value	IRQ event mask
0x0009	IRQ_MASK_B	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	M_ADC_EOM	M_TBAT1	M_nONKEY_HOLD_OFF	M_nONKEY_HOLD_ON	M_nONKEY_HI	M_nONKEY_LO

Field name	Bits	Type	POR	Description
M_ADC_EOM	[5]	RW OTP	0x0	nIRQ Mask - ADC Manual Conversion Result Ready Event
M_TBAT1	[4]	RW OTP	0x0	nIRQ Mask - TBAT1 temperature threshold out of range
M_nONKEY_HOLD_OFF	[3]	RW OTP	0x0	nIRQ Mask - nONKEY_HOLD_OFF Assertion Event
M_nONKEY_HOLD_ON	[2]	RW OTP	0x0	nIRQ Mask - nONKEY_HOLD_ON Assertion Event
M_nONKEY_HI	[1]	RW OTP	0x0	nIRQ Mask - nONKEY_HI Assertion Event
M_nONKEY_LO	[0]	RW OTP	0x0	nIRQ Mask - nONKEY_LO Assertion Event

Table 46: Register IRQ_MASK_C

Address	Name	POR value	IRQ event mask
0x000A	IRQ_MASK_C	0x27	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	M_GPIO_0	M_nON2	M_TA	M_GPIO_1	Reserved 1	M_RTC_SMPL

Field name	Bits	Type	POR	Description
M_GPIO_0	[5]	RW OTP	0x1	nIRQ Mask - GPIO_0
M_nON2	[4]	RW OTP	0x0	nIRQ Mask - nON2 montior
M_TA	[3]	RW OTP	0x0	nIRQ Mask - TA montior
M_GPIO_1	[2]	RW OTP	0x1	nIRQ Mask - GPIO_1
M_RTC_SMPL	[0]	RW OTP	0x1	nIRQ Mask - RTC_SMPL

Table 47: Register CONTROL_A

Address	Name	POR value	System control
0x000B	CONTROL_A	0x63	

7	6	5	4	3	2	1	0
GPI_V	Reserved 1	Reserved 1	PM_I_V	PM_IF_V	PWR1_EN	PWR_EN	SYS_EN

Field name	Bits	Type	POR	Description
GPI_V	[7]	RW OTP	0x0	GPIO Input Buffers and M_CTL Powered from: Value: 0x0 (POR) – VDDINT Value: 0x1 – VDDIO
PM_I_V	[4]	RW OTP	0x0	nONKEY, TA and nON2 Inputs Powered from: Value: 0x0 (POR) – VDDINT Value: 0x1 – VDDIO
PM_IF_V	[3]	RW OTP	0x0	SCL and SDA Inputs Powered from: Value: 0x0 (POR) – VDDINT Value: 0x1 – VDDIO
PWR1_EN	[2]	RW OTP	0x0	Target Status of Power Domain POWER1: - OTP/SW Configured

Field name	Bits	Type	POR	Description
PWR_EN	[1]	RW OTP	0x1	Target Status of Powr Domain POWER: - OTP/SW Configured
SYS_EN	[0]	RW OTP	0x1	Target Status of Power Domain SYSTEM: - State of GPI (OTP default ignored) or - OTP/SW Configured (configured by GPIO_2_PIN register setting)

Table 48: Register CONTROL_B

Address	Name	POR value	System control
0x000C	CONTROL_B	0x24	

7	6	5	4	3	2	1	0
SHUTDOWN	DEEP_SLEEP	WRITE_MODE	I2C_SPEED	Reserved	AUTO_BOOT	Reserved	Reserved

Field name	Bits	Type	POR	Description
SHUTDOWN	[7]	RW RT0	0x0	If set to '1' the Sequencer powers down to RESET Mode. Automatically cleared (back to 0) before leaving RESET mode
DEEP_SLEEP	[6]	RW RT0	0x0	If set to '1' PMIC goes to Deep Sleep Mode (sequencer stops at pointer PART_DOWN). Automatically cleared (back to 0) before powering up from POWER_DOWN mode
WRITE_MODE	[5]	RW OTP	0x1	I^2C Write Mode **Value** / **Description** 0x0 / 0: Page Write Mode 0x1 (POR) / 1: Repeated Write Mode
I2C_SPEED	[4]	RW OTP	0x0	I2C DATA READ Speed **Value** / **Description** 0x0 (POR) / 0: 400 kHz 0x1 / 1: 1.7 MHz
AUTO_BOOT	[2]	RW OTP	0x1	Sequencer Start Up Requires: **Value** / **Description** 0x0 / 0: Valid Wake Up Event 0x1 (POR) / 1: No Wake Up (PMIC Automatically Starts)

Table 49: Register CONTROL_C

Address	Name	POR value	System control
0x000D	CONTROL_C	0x02	

7	6	5	4	3	2	1	0
WATCHDOG	TWDSCALE			DEBOUNCING			Reserved 0

Field name	Bits	Type	POR	Description
WATCHDOG	[7]	RO	0x0	If set to '1', watchdog timer is reset. Automatically cleared back to '0'
TWDSCALE	[6:4]	RW OTP	0x0	Watchdog timer control Value: 0x0 (POR) – 000: Watchdog Disabled 0x1 – 001: 1x scaling applied to TWDMAX period 0x2 – 010: 2x 0x3 – 011: 4x 0x4 – 100: 8x 0x5 – 101: 16x 0x6 – 110: 32x 0x7 – 111: 64x
DEBOUNCING	[3:1]	RW OTP	0x1	GPI, TA and nON2 Debounce Time Value: 0x0 – 000: No Debounce 0x1 (POR) – 001: 10.24 ms 0x2 – 010: 20.48 ms 0x3 – 011: 40.96 ms 0x4 – 100: 80 ms 0x5 – 101: 160 ms 0x6 – 110: 320 ms 0x7 – 111: 640 ms

Table 50: Register CONTROL_D

Address	Name	POR value	System control
0x000E	CONTROL_D	0x00	

7	6	5	4	3	2	1	0
Reserved	ONKEY_SD_RESET_PULSE_EN	ONKEY_AUTOBOOT_EN	nONKEY_SD	KEEPACT_EN	Reserved	EXT_PWRON_DEBUG_EN	EXT_PWRON_PULSE_EN

Field name	Bits	Type	POR	Description
ONKEY_SD_RESET_PULSE_EN	[6]	RW OTP	0x0	Allow LONG_PRESS to generate a 500 ms active pulse on nRESET and NOT shut down.
ONKEY_AUTOBOOT_EN	[5]	RW OTP	0x0	Allow an autoboot after a long nONKEY press, regardless of the AUTOBOOT register
nONKEY_SD	[4]	RW OTP	0x0	Allow a long press Field: PRESS_TIME (Reg: ONKEY_CONT1 [0x0078]) of nONKEY to cause a shutdown
KEEPACT_EN	[3]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: nONKEY Enabled 0x1: 1: nONKEY Disabled, KEEPACT Enabled (HW Assertion of bit WATCHDOG)
EXT_PWRON_DEBUG_EN	[1]	RW OTP	0x0	Enables an nONKEY Long Press or EXT_PWRON_PULSE_EN to generate a 100 µs pulse (low) on the EXT_PWRON pin (GPIO1)
EXT_PWRON_PULSE_EN	[0]	RW W1CL	0x0	Generate a pulse on EXT_PWRON

Table 51: Register PD_DIS

Address	Name	POR value	Power down disable
0x000F	PD_DIS	0x00	

7	6	5	4	3	2	1	0
PM_CONT_PD	OUT_32K_PD	CHG_BBAT_PD	Reserved 0	HS_2_WIRE_PD	PM_IF_PD	GP_ADC_PD	GPIO_PD

Field name	Bits	Type	POR	Description
PM_CONT_PD	[7]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: SYS_EN Enabled during POWERDOWN 0x1: 1: Auto-Disable SYS_EN during POWERDOWN (force the detection of a pending Active state by re-enabling the pin through a passive state of the related GPI status register)

Field name	Bits	Type	POR	Description
OUT_32K_PD	[6]	RW OTP	0x0	Value: 0x0 (POR) — 0: OUT_32K Enabled during POWERDOWN Value: 0x1 — 1: Auto-Disable OUT_32K Output Buffer during POWERDOWN mode (auto re-enable when executing PD_DIS ID during power-up from NO-POWER mode)
CHG_BBAT_PD	[5]	RW OTP	0x0	Value: 0x0 (POR) — 0: Backup Battery Charger Enabled during POWERDOWN mode Value: 0x1 — 1: Auto-Disable Backup Battery Charger during POWERDOWN
HS_2_WIRE_PD	[3]	RW OTP	0x0	Value: 0x0 (POR) — 0: High Speed Interface (I2C_1) Not Disabled during POWERDOWN Value: 0x1 — 1: Auto-Disable High Speed Interface during POWERDOWN
PM_IF_PD	[2]	RW OTP	0x0	Value: 0x0 (POR) — 0: Power Manager Interface (I2C_2) Not Disabled during POWERDOWN Value: 0x1 — 1: Auto-Disable Power Manager Interface during POWERDOWN
GP_ADC_PD	[1]	RW OTP	0x0	Value: 0x0 (POR) — 0: Allow Configured ADC Measurements during POWERDOWN Value: 0x1 — 1: Auto-Disable Auto and Manual Measurements
GPIO_PD	[0]	RW OTP	0x0	Value: 0x0 (POR) — 0: GPIO extender enabled during POWERDOWN Value: 0x1 — 1: Auto-Disable of features configured as GPIO pins during POWERDOWN mode (force the detection of a pending Active state on GPIs by re-enabling the pin through a passive state of the related GPI status register)

Table 52: Register INTERFACE

Address	Name	POR value	
0x0010	INTERFACE	0x80	

7	6	5	4	3	2	1	0
IF_BASE_ADDR			Reserved	Reserved	Reserved	Reserved	Reserved

Field name	Bits	Type	POR	Description
IF_BASE_ADDR	[7:5]	RW OTP	0x4	3 MSB of the I^2C Interfaces Base Address XXX10000 10010010 = 0x92 write address of HS (I^2C) IF 10010011 = 0x93 read address of HS (I^2C) IF

Table 53: Register RESET

Address	Name	POR value	
0x0011	RESET	0x45	

7	6	5	4	3	2	1	0
RESET_EVENT		RESET_TIMER					

Field name	Bits	Type	POR	Description
RESET_EVENT	[7:6]	RW OTP	0x1	RESET Timer Started by: Value: 0x0 — 00: EXT_WAKEUP Value: 0x1 (POR) — 01: SYS_UP Value: 0x2 — 10: PWR_UP (internal signal) Value: 0x3 — 11: PWR1_UP (internal signal)
RESET_TIMER	[5:0]	RW OTP	0x5	RESET timer duration Value: 0x0 — 000000: RESET disabled Value: 0x1 — 000001: 1.024 ms Value: 0x2 — 000010: 2.048 ms Value: 0x3 — 000011: 3.072 ms Value: 0x4 — 000100: 4.096 ms Value: 0x5 (POR) — 000101: 5.120 ms Value: ... — .... Value: 0x1E — 011110: 30.720 ms Value: 0x1F — 011111: 31.744 ms Value: 0x20 — 100000: 32.768 ms Value: 0x21 — 100001: 65.536 ms Value: 0x22 — 100010: 98.304 ms Value: ... — ..... Value: 0x3D — 111101: 983.040 ms Value: 0x3E — 111110: 1015.808 ms Value: 0x3F — 111111: 1048.576 ms

A.2 GPIO

Table 54: Register SMPL_GPIO_0

Address	Name	POR value	
0x0012	SMPL_GPIO_0	0xEE	

7	6	5	4	3	2	1	0
Reserved 1	Reserved 1	Reserved 1	Reserved 0	Reserved 0	Reserved 1	Reserved 0	Reserved 0

Table 55: Register TA_GPIO_1

Address	Name	POR value	
0x0013	TA_GPIO_1	0xDE	

7	6	5	4	3	2	1	0
TA_MODE	TA_TYPE	TA_PIN		GPIO1_MODE	GPIO1_TYPE	GPIO1_PIN	

Field name	Bits	Type	POR	Description
TA_MODE	[7]	RW OTP	0x1	TA monitor: Input/Output Configured as: **Value** / **Description** 0x0 / 0: TA monitor: Debounce OFF 0x1 (POR) / 1: TA monitor: Debounce ON
TA_TYPE	[6]	RW OTP	0x1	TA monitor: Input/Output Configured as: **Value** / **Description** 0x0 / 0: TA monitor: Active Low 0x1 (POR) / 1: TA monitor: Active High
TA_PIN	[5:4]	RW OTP	0x1	TA monitor: PIN Configured as: **Value** / **Description** 0x0 / 00: N/A 0x1 (POR) / 01: TA monitor 0x2 / 10: N/A 0x3 / 11: N/A
GPIO1_MODE	[3]	RW OTP	0x1	Unused **Value** / **Description** 0x0 / 0: GPI: Debounce OFF; GPO: Output driven Low 0x1 (POR) / 1: GPI: Debounce ON; GPO: Output driven High
GPIO1_TYPE	[2]	RW OTP	0x1	Unused **Value** / **Description** 0x0 / 0: GPI:Active Low ; GPO_OD: internal PUP to VDDIO 0x1 (POR) / 1: GPI:Active HIGH ; GPO_OD: external PUP

Field name	Bits	Type	POR	Description
GPIO1_PIN	[1:0]	RW OTP	0x2	GPIO and EXT_PWRON output Value: 0x0 (0x2 (POR)) / Description: 00: EXT_PWRON (0x1: 01: GPI; 0x2 (POR): 10: GPO_OD (Open Drain); 0x3: 11: GPO_PP (Push-Pull))

Table 56: Register GPIO_nON2

Address	Name	POR value	
0x0014	GPIO_0_nON2	0xE9	

7	6	5	4	3	2	1	0
GPIO0_MODE	GPIO0_TYPE	GPIO0_PIN		nON_MODE	nON_TYPE	nON_PIN	

Field name	Bits	Type	POR	Description
GPIO0_MODE	[7]	RW OTP	0x1	GPIO MODE configured as: Value: 0x0 / Description: 0: GPI: Debounce OFF; GPO: Output driven Low Value: 0x1 (POR) / Description: 1: GPI: Debounce ON; GPO: Output driven High
GPIO0_TYPE	[6]	RW OTP	0x1	GPIO TYPE configured as: Value: 0x0 / Description: 0: GPI:Active Low ; GPO_OD: internal PUP to VDDIO Value: 0x1 (POR) / Description: 1: GPI:Active HIGH ; GPO_OD: external PUP
GPIO0_PIN	[5:4]	RW OTP	0x2	GPIO PIN configured as: Value: 0x0 / Description: 00: nVDDFAULT Value: 0x1 / Description: 01: GPI Value: 0x2 (POR) / Description: 10: GPO_OD (Open Drain) Value: 0x3 / Description: 11: GPO_PP (Push-Pull)
nON2_MODE	[3]	RW OTP	0x1	nON2 monitor: Input/Output Configured as: Value: 0x0 / Description: 0: nON2 monitor: Debounce OFF Value: 0x1 (POR) / Description: 1: nON2 monitor: Debounce ON

<table>
<tr><th>Field name</th><th>Bits</th><th>Type</th><th>POR</th><th>Description</th></tr>
<tr><td>nON2_TYPE</td><td>[2]</td><td>RW
OTP</td><td>0x0</td><td>nON2 monitor: Input/Output Configured as:
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0
(POR)</td><td>0: nON2 monitor: Active Low</td></tr>
<tr><td>0x1</td><td>1: nON2 monitor: Active High</td></tr>
</table></td></tr>
<tr><td>nON2_PIN</td><td>[1:0]</td><td>RW
OTP</td><td>0x1</td><td>nON2 monitor: PIN Configured as:
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>00: N/A</td></tr>
<tr><td>0x1
(POR)</td><td>01: nON2 monitor</td></tr>
<tr><td>0x2</td><td>10: N/A</td></tr>
<tr><td>0x3</td><td>11: N/A</td></tr>
</table></td></tr>
</table>

A.3 Sequencer

Table 57: Register ID_0_1

Address	Name	POR value	
0x0015	ID_0_1	0x11	

7	6	5	4	3	2	1	0
LDO1_STEP				WAIT_ID_ALWAYS	SYS_PRE	DEF_SUPPLY	nRES_MODE

Field name	Bits	Type	POR	Description
LDO1_STEP	[7:4]	RW OTP	0x1	Power Sequencer Time for LDO1
WAIT_ID_ALWAYS	[3]	RW OTP	0x0	WAIT_ID Configuration: **Value** / **Description** 0x0 (POR): 0: Only Perform the WAIT_ID Step on First Use of Sequencer 0x1: 1: Perform the WAIT_ID Step on Subsequent Uses of Sequencer.
SYS_PRE	[2]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: Set SYS_UP as Configured from Supplies Pre-Settings 0x1: 1: Always De-Assert SYS_UP before Powering Down Domain SYSTEM
DEF_SUPPLY	[1]	RW OTP	0x0	All Supplies (except LDOCORE) are Enabled/Disabled from OTP Default Mode **Value** / **Description** 0x0 (POR): Disabled 0x1: Enabled
nRES_MODE	[0]	RW OTP	0x1	**Value** / **Description** 0x0: 0: No assertion of nRESET during POWERDOWN Mode 0x1 (POR): 1: Assert nRESET when Entering POWERDOWN Mode (release after leaving POWERDOWN)

Table 58: Register ID_2_3

Address	Name	POR value	
0x0016	ID_2_3	0x03	

7	6	5	4	3	2	1	0
LDO3_STEP				LDO2_STEP			

Field name	Bits	Type	POR	Description
LDO3_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for LDO3
LDO2_STEP	[3:0]	RW OTP	0x3	Power Sequencer Time for LDO2

Table 59: Register ID_4_5

Address	Name	POR value	
0x0017	ID_4_5	0x00	

7	6	5	4	3	2	1	0
LDO5_STEP				LDO4_STEP			

Field name	Bits	Type	POR	Description
LDO5_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for LDO5
LDO4_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for LDO4

Table 60: Register ID_6_7

Address	Name	POR value	
0x0018	ID_6_7	0x50	

7	6	5	4	3	2	1	0
LDO7_STEP				LDO6_STEP			

Field name	Bits	Type	POR	Description
LDO7_STEP	[7:4]	RW OTP	0x5	Power Sequencer Time for LDO7
LDO6_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for LDO6

Table 61: Register ID_8_9

Address	Name	POR value	
0x0019	ID_8_9	0x00	

7	6	5	4	3	2	1	0
LDO9_STEP				LDO8_STEP			

Field name	Bits	Type	POR	Description
LDO9_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for LDO9
LDO8_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for LDO8

Table 62: Register ID_10_11

Address	Name	POR value	
0x001A	ID_10_11	0x00	

7	6	5	4	3	2	1	0
LDO11_STEP				LDO10_STEP			

Field name	Bits	Type	POR	Description
LDO11_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for LDO11
LDO10_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for LDO10

Table 63: Register ID_12_13

Address	Name	POR value	
0x001B	ID_12_13	0x00	

7	6	5	4	3	2	1	0
PD_DIS_STEP				LDO12_STEP			

Field name	Bits	Type	POR	Description
PD_DIS_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for Power Down Disable (PD_DIS)
LDO12_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for LDO12

Table 64: Register ID_14_15

Address	Name	POR value	
0x001C	ID_14_15	0x35	

7	6	5	4	3	2	1	0
BUCK1_STEP				BUCK0_STEP			

Field name	Bits	Type	POR	Description
BUCK1_STEP	[7:4]	RW OTP	0x3	Power Sequencer Time for BUCK1 (Dual Phase)
BUCK0_STEP	[3:0]	RW OTP	0x5	Power Sequencer Time for BUCK0 (Dual Phase)

Table 65: Register ID_16_17

Address	Name	POR value	
0x001D	ID_16_17	0x00	

7	6	5	4	3	2	1	0
BUCK3_STEP				BUCK2_STEP			

Field name	Bits	Type	POR	Description
BUCK3_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for BUCK3
BUCK2_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for BUCK2

Table 66: Register ID_18_19

Address	Name	POR value	
0x001E	ID_18_19	0x00	

7	6	5	4	3	2	1	0
BUCK6_STEP				BUCK4_STEP			

Field name	Bits	Type	POR	Description
BUCK6_STEP	[7:4]	RW OTP	0x0	Power Sequencer Time for BUCK6
BUCK4_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for BUCK4

Table 67: Register ID_20_21

Address	Name	POR value	
0x001F	ID_20_21	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	EXT_PWRON_STEP			

Field name	Bits	Type	POR	Description
EXT_PWRON_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for EXT_PWRON output

Table 68: Register SEQ_STATUS

Address	Name	POR value	
0x0020	SEQ_STATUS	0x00	

7	6	5	4	3	2	1	0
SEQ_POINTER				WAIT_STEP			

Field name	Bits	Type	POR	Description
SEQ_POINTER	[7:4]	RW	0x0	Actual Pointer Position (Time Slot) of Power Sequencer
WAIT_STEP	[3:0]	RW OTP	0x0	Power Sequencer Time for Wait Step

Table 69: Register SEQ_A

Address	Name	POR value	
0x0021	SEQ_A	0x96	

7	6	5	4	3	2	1	0
POWER_END				SYSTEM_END			

Field name	Bits	Type	POR	Description
POWER_END	[7:4]	RW OTP	0x9	OTP Pointer - Last Supply of Domain POWER
SYSTEM_END	[3:0]	RW OTP	0x6	OTP Pointer - Last Supply of Domain SYSTEM

Table 70: Register SEQ_B

Address	Name	POR value	
0x0022	SEQ_B	0x49	

7	6	5	4	3	2	1	0
PART_DOWN				MAX_COUNT			

Field name	Bits	Type	POR	Description
PART_DOWN	[7:4]	RW OTP	0x4	OTP Pointer - Partial POWERDOWN Mode
MAX_COUNT	[3:0]	RW OTP	0x9	OTP Pointer - Last Supply of Domain POWER1

Table 71: Register SEQ_TIMER

Address	Name	POR value	
0x0023	SEQ_TIMER	0x3D	

7	6	5	4	3	2	1	0
SEQ_DUMMY				SEQ_TIME			

Field name	Bits	Type	POR	Description
SEQ_DUMMY	[7:4]	RW OTP	0x3	Time for empty Sequence slots

Value	Description
0x0	0000: 32 µs
0x1	0001: 64 µs
0x2	0010: 96 µs
0x3 (POR)	0011: 128 µs
0x4	0100: 160 µs
0x5	0101: 192 µs
0x6	0110: 224 µs
0x7	0111: 256 µs
0x8	1000: 288 µs
0x9	1001: 384 µs
0xA	1010: 448 µs
0xB	1011: 512 µs
0xC	1100: 1.024 ms
0xD	1101: 2.048 ms
0xE	1110: 4.096 ms
0xF	1111: 8.192 ms

<table>
<tr><th>Field name</th><th>Bits</th><th>Type</th><th>POR</th><th>Description</th></tr>
<tr><td>SEQ_TIME</td><td>[3:0]</td><td>RW
OTP</td><td>0xd</td><td>Time for each non-empty Sequence slot
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>0000: 32 µs</td></tr>
<tr><td>0x1</td><td>0001: 64 µs</td></tr>
<tr><td>0x2</td><td>0010: 96 µs</td></tr>
<tr><td>0x3</td><td>0011: 128 µs</td></tr>
<tr><td>0x4</td><td>0100: 160 µs</td></tr>
<tr><td>0x5</td><td>0101: 192 µs</td></tr>
<tr><td>0x6</td><td>0110: 224 µs</td></tr>
<tr><td>0x7</td><td>0111: 256 µs</td></tr>
<tr><td>0x8</td><td>1000: 288 µs</td></tr>
<tr><td>0x9</td><td>1001: 384 µs</td></tr>
<tr><td>0xA</td><td>1010: 448 µs</td></tr>
<tr><td>0xB</td><td>1011: 512 µs</td></tr>
<tr><td>0xC</td><td>1100: 1.024 ms</td></tr>
<tr><td>0xD</td><td>1101: 2.048 ms</td></tr>
<tr><td>0xE</td><td>1110: 4.096 ms</td></tr>
<tr><td>0xF</td><td>1111: 8.192 ms</td></tr>
</table></td></tr>
</table>

A.4 Supplies

Table 72: Register BUCK0_CONF0

Address	Name	POR value	
0x0024	BUCK0_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK0_EN	VBUCK0						

Field name	Bits	Type	POR	Description
BUCK0_EN	[7]	RW OTP	0x0	Value / Description: 0x0 (POR): 0: BUCK0 Disabled 0x1: 1: BUCK0 Enabled
VBUCK0	[6:0]	RW OTP	0x50	Buck Dual Phase Voltage. Value / Description: 0x0: 0000000: 600 mV 0x1: 0000001: 606.25 mV 0x2: 0000001: 612.5 mV ...: ... 0x3D: 1111101: 1.38125 V 0x3E: 1111110: 1.3875 V 0x3F: 1111111:1.39375 V

Table 73: Register BUCK0_CONF1

Address	Name	POR value	
0x0025	BUCK0_CONF1	0x09	

7	6	5	4	3	2	1	0
BUCK0_PD_DIS	BUCK0_SYNC_ILIM					BUCK0_MODE	

Field name	Bits	Type	POR	Description
BUCK0_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value / Description: 0x0 (POR): 0: Enable Pull Down Resistor 0x1: 1: No Pull Down Resistor When Off

Field name	Bits	Type	POR	Description
BUCK0_SYNC_ILIM	[6:2]	RW OTP	0x2	BUCK0 Current Limit: Value: Description 0x0: 00000: 80 mA 0x1: 00001: 160 mA ...: ... 0x1E: 11110: 2480 mA 0x1F: 11111: 2560 mA
BUCK0_MODE	[1:0]	RW OTP	0x1	BUCK0 Operating Mode: Value: Description 0x0: 00: Sleep Mode (PFM) 0x1 (POR): 01: Automatic Mode 0x2: 10: Synchronous Mode (PWM) 0x3: 11: Reserved

Table 74: Register BUCK0_CONF2

Address	Name	POR value	
0x0026	BUCK0_CONF2	0x42	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 1	Reserved 0	BUCK0_SLEEP_ILIM				

Field name	Bits	Type	POR	Description
BUCK0_SLEEP_ILIM	[4:0]	RW OTP	0x2	BUCK0 Sleep Current Limit: Value: Description 0x0: 00000: 80 mA 0x1: 00001: 160 mA ...: ... 0x1E: 11110: 2480 mA 0x1F: 11111: 2560 mA

Table 75: Register BUCK1_CONF0

Address	Name	POR value	
0x0027	BUCK1_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK1_EN	VBUCK1						

Field name	Bits	Type	POR	Description
BUCK1_EN	[7]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: BUCK1 Disabled 0x1: 1: BUCK1 Enabled
VBUCK1	[6:0]	RW OTP	0x50	Buck Dual Phase Voltage. **Value** / **Description** 0x0: 0000000: 600 mV 0x1: 0000001: 606.25 mV 0x2: 0000001: 612.5 mV ...: ... 0x3D: 1111101: 1.38125 V 0x3E: 1111110: 1.3875 V 0x3F: 1111111:1.39375 V

Table 76: Register BUCK1_CONF1

Address	Name	POR value	
0x0028	BUCK1_CONF1	0x09	

7	6	5	4	3	2	1	0
BUCK1_PD_DIS	BUCK1_SYNC_ILIM					BUCK1_MODE	

Field name	Bits	Type	POR	Description
BUCK1_PD_DIS	[7]	RW OTP	0x0	Pull down disable **Value** / **Description** 0x0 (POR): 0: Enable Pull Down Resistor 0x1: 1: No Pull Down Resistor When Off
BUCK1_SYNC_ILIM	[6:2]	RW OTP	0x2	BUCK1 Current Limit: **Value** / **Description** 0x0: 00000: 80 mA 0x1: 00001: 160 mA ...: ... 0x1E: 11110: 2480 mA 0x1F: 11111: 2560 mA

Field name	Bits	Type	POR	Description
BUCK1_MODE	[1:0]	RW OTP	0x1	BUCK1 Operating Mode: Value / Description 0x0 / 00: Sleep Mode (PFM) 0x1 (POR) / 01: Automatic Mode 0x2 / 10: Synchronous Mode (PWM) 0x3 / Reserved

Table 77: Register BUCK1_CONF2

Address	Name	POR value	
0x0029	BUCK1_CONF2	0x42	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 1	Reserved 0	BUCK1_SLEEP_ILIM				

Field name	Bits	Type	POR	Description
BUCK1_SLEEP_ILIM	[4:0]	RW OTP	0x2	BUCK1 Sleep Current Limit: Value / Description 0x0 / 00000: 80 mA 0x1 / 00001: 160 mA ... / ... 0x1E / 11110: 2480 mA 0x1F / 11111: 2560 mA

Table 78: Register BUCK2_CONF0

Address	Name	POR value	
0x002A	BUCK2_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK2_EN	VBUCK2						

Field name	Bits	Type	POR	Description
BUCK2_EN	[7]	RW OTP	0x0	Value / Description 0x0 (POR) / 0: BUCK2 Disabled 0x1 / 1: BUCK2 Enabled

Field name	Bits	Type	POR	Description
VBUCK2	[6:0]	RW OTP	0x50	Buck Target Voltage. Value / Description 0x0: 0000000: 600 mV 0x1: 0000001: 606.25 mV 0x2: 0000001: 612.5 mV ...: ... 0x3D: 1111101: 1.38125 V 0x3E: 1111110: 1.3875 V 0x3F: 1111111:1.39375 V

Table 79: Register BUCK2_CONF1

Address	Name	POR value	
0x002B	BUCK2_CONF1	0x29	

7	6	5	4	3	2	1	0
BUCK2_PD_DIS	Reserved 0	Reserved 1	Reserved	BUCK2_SYNC_ILIM		BUCK2_MODE	

Field name	Bits	Type	POR	Description
BUCK2_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value / Description 0x0 (POR): 0: Enable Pull Down Resistor 0x1: 1: No Pull Down Resistor When Off
BUCK2_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK2 Current Limit: Value / Description 0x0: 00: 900 mA 0x1: 01: 1500 mA 0x2 (POR): 10: 2100 mA 0x3: 11: 2700 mA
BUCK2_MODE	[1:0]	RW OTP	0x1	BUCK2 Operating Mode: Value / Description 0x0: 00: Sleep Mode (PFM) 0x1 (POR): 01: Automatic Mode 0x2: 10: Synchronous Mode (PWM) 0x3: 11: Reserved

Table 80: Register BUCK3_CONF0

Address	Name	POR value	
0x002C	BUCK3_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK3_EN	VBUCK3						

Field name	Bits	Type	POR	Description
BUCK3_EN	[7]	RW OTP	0x0	Value: 0x0 (POR) – 0: BUCK3 Disabled Value: 0x1 – 1: BUCK3 Enabled
VBUCK3	[6:0]	RW OTP	0x50	Buck Target Voltage. Value: 0x0 – 0000000: 600 mV Value: 0x1 – 0000001: 606.25 mV Value: 0x2 – 0000001: 612.5 mV Value: ... – ... Value: 0x3D – 1111101: 1.38125 V Value: 0x3E – 1111110: 1.3875 V Value: 0x3F – 1111111:1.39375 V

Table 81: Register BUCK3_CONF1

Address	Name	POR value	
0x002D	BUCK3_CONF1	0x29	

7	6	5	4	3	2	1	0
BUCK3_PD_DIS	BUCK3_START_MODE		Reserved	BUCK3_SYNC_ILIM		BUCK3_MODE	

Field name	Bits	Type	POR	Description
BUCK3_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value: 0x0 (POR) – 0: Enable Pull Down Resistor Value: 0x1 – 1: No Pull Down Resistor When Off
BUCK3_START_MODE	[6:5]	RW OTP	0x1	BUCK Start Mode: Value: 0x0 – 00: Soft Startup Value: 0x1 (POR) – 01: Standard Startup Value: 0x2 – 10: Fast Startup Value: 0x3 – 11: Reserved

Field name	Bits	Type	POR	Description
BUCK3_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK3 Current Limit: Value / Description 0x0 / 00: 600 mA 0x1 / 01: 1000 mA 0x2 (POR) / 10: 1400 mA 0x3 / 11: 1800 mA
BUCK3_MODE	[1:0]	RW OTP	0x1	BUCK3 Operating Mode: Value / Description 0x0 / 00: Sleep Mode (PFM) 0x1 (POR) / 01: Automatic Mode 0x2 / 10: Synchronous Mode (PWM) 0x3 / 11: Reserved

Table 82: Register BUCK4_CONF0

Address	Name	POR value	
0x002E	BUCK4_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK4_EN	VBUCK4						

Field name	Bits	Type	POR	Description
BUCK4_EN	[7]	RW OTP	0x0	Value / Description 0x0 (POR) / 0: BUCK Disabled 0x1 / 1: BUCK Enabled
VBUCK4	[6:0]	RW OTP	0x50	Buck Target Voltage. Value / Description 0x0 / 0000000: 1.40 V 0x1 / 0000001: 1.40625 V 0x2 / 0000001: 1.4125 V ... / ... 0x3D / 1111101: 2.18125 V 0x3E / 1111110: 2.1875 V 0x3F / 1111111: 2.19375 V

Table 83: Register BUCK4_CONF1

Address	Name	POR value	
0x002F	BUCK4_CONF1	0x29	

7	6	5	4	3	2	1	0
BUCK4_PD_DIS	BUCK4_START_MODE		Reserved	BUCK4_SYNC_ILIM		BUCK4_MODE	

Field name	Bits	Type	POR	Description
BUCK4_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value: 0x0 (POR) — 0: Enable Pull Down Resistor Value: 0x1 — 1: No Pull Down Resistor When Off
BUCK4_START_MODE	[6:5]	RW OTP	0x1	BUCK Start Mode: Value: 0x0 — 00: Soft Startup Value: 0x1 (POR) — 01: Standard Startup Value: 0x2 — 10: Fast Startup Value: 0x3 — 11: Reserved
BUCK4_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: Value: 0x0 — 00: 300 mA Value: 0x1 — 01: 500 mA Value: 0x2 (POR) — 10: 700 mA Value: 0x3 — 11: 900 mA
BUCK4_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: Value: 0x0 — 00: Sleep Mode (PFM) Value: 0x1 (POR) — 01: Automatic Mode Value: 0x2 — 10: Synchronous Mode (PWM) Value: 0x3 — 11: Reserved

Table 84: Register BUCK5_CONF0

Address	Name	POR value	
0x0030	BUCK5_CONF0	0x50	

7	6	5	4	3	2	1	0
Reserved 0	VBUCK5						

Field name	Bits	Type	POR	Description
VBUCK5	[6:0]	RW OTP	0x50	Buck Target Voltage.

Value	Description
0x0	0000000: 1.40 V
0x1	0000001: 1.40625 V
0x2	0000001: 1.4125 V
...	...
0x3D	1111101: 2.18125 V
0x3E	1111110: 2.1875 V
0x3F	1111111: 2.19375 V

Table 85: Register BUCK5_CONF1

Address	Name	POR value	
0x0031	BUCK5_CONF1	0x29	

7	6	5	4	3	2	1	0
BUCK5_PD_DIS	BUCK5_START_MODE		Reserved	BUCK5_SYNC_ILIM		BUCK5_MODE	

Field name	Bits	Type	POR	Description
BUCK5_PD_DIS	[7]	RW OTP	0x0	Pull down disable

Value	Description
0x0 (POR)	0: Enable Pull Down Resistor
0x1	1: No Pull Down Resistor When Off

Field name	Bits	Type	POR	Description
BUCK5_START_MODE	[6:5]	RW OTP	0x1	BUCK Start Mode:

Value	Description
0x0	00: Soft Startup
0x1 (POR)	01: Standard Startup
0x2	10: Fast Startup
0x3	11: Reserved

Field name	Bits	Type	POR	Description
BUCK5_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: Value / Description 0x0 / 00: 300 mA 0x1 / 01: 500 mA 0x2 (POR) / 10: 700 mA 0x3 / 11: 900 mA
BUCK5_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: Value / Description 0x0 / 00: Sleep Mode (PFM) 0x1 (POR) / 01: Automatic Mode 0x2 / 10: Synchronous Mode (PWM) 0x3 / 11: Reserved

Table 86: Register BUCK6_CONF0

Address	Name	POR value	
0x0032	BUCK6_CONF0	0x50	

7	6	5	4	3	2	1	0
BUCK5and6_EN	VBUCK6						

Field name	Bits	Type	POR	Description
BUCK5and6_EN	[7]	RW OTP	0x0	Value / Description 0x0 (POR) / 0: BUCK Disabled 0x1 / 1: BUCK Enabled
VBUCK6	[6:0]	RW OTP	0x50	Buck Target Voltage. Value / Description 0x0 / 0000000: 1.40 V 0x1 / 0000001: 1.40625 V 0x2 / 0000001: 1.4125 V ... / ... 0x3D / 1111101: 2.18125 V 0x3E / 1111110: 2.1875 V 0x3F / 1111111: 2.19375 V

Table 87: Register BUCK6_CONF1

Address	Name	POR value	
0x0033	BUCK6_CONF1	0x29	

7	6	5	4	3	2	1	0
BUCK6_PD_DIS	BUCK6_START_MODE		Reserved	BUCK6_SYNC_ILIM		BUCK6_MODE	

Field name	Bits	Type	POR	Description
BUCK6_PD_DIS	[7]	RW OTP	0x0	Pull down disable Value: 0x0 (POR) — 0: Enable Pull Down Resistor Value: 0x1 — 1: No Pull Down Resistor When Off
BUCK6_START_MODE	[6:5]	RW OTP	0x1	BUCK Start Mode: Value: 0x0 — 00: Soft Startup Value: 0x1 (POR) — 01: Standard Startup Value: 0x2 — 10: Fast Startup Value: 0x3 — 11: Reserved
BUCK6_SYNC_ILIM	[3:2]	RW OTP	0x2	BUCK Current Limit: Value: 0x0 — 00: 300 mA Value: 0x1 — 01: 500 mA Value: 0x2 (POR) — 10: 700 mA Value: 0x3 — 11: 900 mA
BUCK6_MODE	[1:0]	RW OTP	0x1	BUCK Operating Mode: Value: 0x0 — 00: Sleep Mode (PFM) Value: 0x1 (POR) — 01: Automatic Mode Value: 0x2 — 10: Synchronous Mode (PWM) Value: 0x3 — 11: Reserved

Table 88: Register BUCKRF_THR

Address	Name	POR value	
0x0034	BUCKRF_THR	0xC0	

7	6	5	4	3	2	1	0
RFBUCK_SNC_THR				RFBUCK_SLP_THR			

Field name	Bits	Type	POR	Description
RFBUCK_SNC_THR	[7:4]	RW OTP	0xc	Force sync (PWM) mode threshold. The device is forced into sync mode if 360 mV is higher than this. Value: 0x0 – 0000: 160 mV; 0x1 – 0001: 180 mV; ... – ...; 0xE – 1110: 440 mV; 0xF – 1111: 460 mV
RFBUCK_SLP_THR	[3:0]	RW OTP	0x0	Force sleep (PFM) mode threshold. The device is forced into sleep mode if 360 mV is lower than this. Value: 0x0 (POR) – 0000: 160 mV; 0x1 – 0001: 180 mV; ... – ...; 0xE – 1110: 440 mV; 0xF – 1111: 460 mV

Table 89: Register BUCKRF_CONF

Address	Name	POR value	
0x0035	BUCKRF_CONF	0x25	

7	6	5	4	3	2	1	0
RFBUCK_EN	Reserved	RFBUCK_6M_SEL	RFBUCK_I_BYP_LMT	RFBUCK_I_N_LMT_SEL		RFBUCK_I_P_LMT_SEL	

Field name	Bits	Type	POR	Description
RFBUCK_EN	[7]	RW OTP	0x0	Host Control of RF Buck
RFBUCK_6M_SEL	[5]	RW OTP	0x1	1:6 MHz, 0:3 MHz
RFBUCK_I_BYP_LMT	[4]	RW OTP	0x0	0:1.0 A, 1:1.6 A
RFBUCK_I_N_LMT_SEL	[3:2]	RW OTP	0x1	Negative Current Limit Selection (00:0.6 A, 01:1.1 A, 10:1.6 A, 11:2.1 A)
RFBUCK_I_P_LMT_SEL	[1:0]	RW OTP	0x1	Current Limit Selection (00:1 A, 01:1.5 A, 10:2 A, 11:2.5 A)

Table 90: Register LDO1

Address	Name	POR value	
0x0036	LDO1	0x00	

7	6	5	4	3	2	1	0
LDO1_PD_DIS	LDO1_EN	VLDO1					

Field name	Bits	Type	POR	Description
LDO1_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO1_EN	[6]	RW OTP	0x0	LDO Enable Value: 0x0 (POR) — 0: LDO1 Disabled Value: 0x1 — 1: LDO1 Enabled
VLDO1	[5:0]	RW OTP	0x0	LDO voltage select Value: 0x0 (POR) — 000000: 0.650 V Value: 0x1 — 000001: 0.675 V Value: 0x2 — 000010: 1.10 V Value: ... — ... Value: 0x3E — 111111: 2.200 V Value: 0x3F — 111111: 2.225 V

Table 91: Register LDO2

Address	Name	POR value	
0x0037	LDO2	0x20	

7	6	5	4	3	2	1	0
LDO2_PD_DIS	LDO2_EN	VLDO2					

Field name	Bits	Type	POR	Description
LDO2_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO2_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO1 [0x0036] for details
VLDO2	[5:0]	RW OTP	0x20	LDO voltage select. See Register: LDO1 [0x0036] for details

Table 92: Register LDO3

Address	Name	POR value	
0x0038	LDO3	0x00	

7	6	5	4	3	2	1	0
LDO3_PD_DIS	LDO3_EN	VLDO3					

Field name	Bits	Type	POR	Description
LDO3_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO3_EN	[6]	RW OTP	0x0	LDO Enable Value: 0x0 (POR) — 0: LDO3 Disabled Value: 0x1 — 1: LDO3 Enabled
VLDO3	[5:0]	RW OTP	0x0	LDO3 voltage select Value: 0x0 (POR) — 000000: 1.20 V Value: 0x1 — 000001: 1.25 V Value: 0x2 — 000010: 1.30 V Value: ... — ... Value: 0xB — 001011: 1.75 V Value: 0xC — 001100: 1.80 V Value: 0xD — 001101: 1.85 V Value: ... — ... Value: 0x20 — 100000: 2.80 V Value: 0x21 — 100001: 2.85 V Value: 0x22 — 100010: 2.90 V Value: ... — ... Value: 0x28 — 101000: 3.20 V Value: 0x29 — 101001: 3.25 V Value: 0x2A — 101010: 3.30 V Value: ... — 101010: 3.30 V

Table 93: Register LDO4

Address	Name	POR value	
0x0039	LDO4	0x00	

7	6	5	4	3	2	1	0
LDO4_PD_DIS	LDO4_EN	VLDO4					

Field name	Bits	Type	POR	Description
LDO4_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO1 [0x0036] for details
LDO4_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO1 [0x0036] for details
VLDO4	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO1 [0x0036] for details Clamped at 0x2A = 1.7 V

Table 94: Register LDO5

Address	Name	POR value	
0x003A	LDO5	0x00	

7	6	5	4	3	2	1	0
LDO5_PD_DIS	LDO5_EN	VLDO5					

Field name	Bits	Type	POR	Description
LDO5_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO5_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO5	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 95: Register LDO6

Address	Name	POR value	
0x003B	LDO6	0x00	

7	6	5	4	3	2	1	0
LDO6_PD_DIS	LDO6_EN	VLDO6					

Field name	Bits	Type	POR	Description
LDO6_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO6_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO6	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 96: Register LDO7

Address	Name	POR value	
0x003C	LDO7	0x00	

7	6	5	4	3	2	1	0
LDO7_PD_DIS	LDO7_EN	VLDO7					

Field name	Bits	Type	POR	Description
LDO7_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO7_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO7	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 97: Register LDO8

Address	Name	POR value	
0x003D	LDO8	0x00	

7	6	5	4	3	2	1	0
LDO8_PD_DIS	LDO8_EN	VLDO8					

Field name	Bits	Type	POR	Description
LDO8_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO8_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO8	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 98: Register LDO9

Address	Name	POR value	
0x003E	LDO9	0x00	

7	6	5	4	3	2	1	0
LDO9_PD_DIS	LDO9_EN	VLDO9					

Field name	Bits	Type	POR	Description
LDO9_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO9_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO9	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 99: Register LDO10

Address	Name	POR value	
0x003F	LDO10	0x00	

7	6	5	4	3	2	1	0
LDO10_PD_DIS	LDO10_EN	VLDO10					

Field name	Bits	Type	POR	Description
LDO10_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO10_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO10	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 100: Register LDO11

Address	Name	POR value	
0x0040	LDO11	0x00	

7	6	5	4	3	2	1	0
LDO11_PD_DIS	LDO11_EN	VLDO11					

Field name	Bits	Type	POR	Description
LDO11_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO11_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO11	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 101: Register LDO12

Address	Name	POR value	
0x0041	LDO12	0x00	

7	6	5	4	3	2	1	0
LDO12_PD_DIS	LDO12_EN	VLDO12					

Field name	Bits	Type	POR	Description
LDO12_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO12_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO12	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 102: Register LDO13

Address	Name	POR value	
0x0042	LDO13	0x00	

7	6	5	4	3	2	1	0
LDO13_PD_DIS	LDO13_EN	VLDO13					

Field name	Bits	Type	POR	Description
LDO13_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO13_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO13	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 103: Register LDO14

Address	Name	POR value	
0x0043	LDO14	0x00	

7	6	5	4	3	2	1	0
LDO14_PD_DIS	LDO14_EN	VLDO14					

Field name	Bits	Type	POR	Description
LDO14_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO14_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO14	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 104: Register LDO15

Address	Name	POR value	
0x0044	LDO15	0x00	

7	6	5	4	3	2	1	0
LDO15_PD_DIS	LDO15_EN	VLDO15					

Field name	Bits	Type	POR	Description
LDO15_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO15_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO15	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 105: Register LDO16

Address	Name	POR value	
0x0045	LDO16	0x00	

7	6	5	4	3	2	1	0
LDO16_PD_DIS	LDO16_EN	VLDO16					

Field name	Bits	Type	POR	Description
LDO16_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO16_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO16	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 106: Register LDO17

Address	Name	POR value	
0x0046	LDO17	0x00	

7	6	5	4	3	2	1	0
LDO17_PD_DIS	LDO17_EN	VLDO17					

Field name	Bits	Type	POR	Description
LDO17_PD_DIS	[7]	RW OTP	0x0	LDO configure bit. See Register: LDO3 [0x0038] for details
LDO17_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO17	[5:0]	RW OTP	0x0	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 107: Register LDO18

Address	Name	POR value	
0x0047	LDO18	0x14	

7	6	5	4	3	2	1	0
LDO18_PD_DIS	LDO18_EN	VLDO18					

Field name	Bits	Type	POR	Description
LDO18_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO18_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO18	[5:0]	RW OTP	0x14	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 108: Register LDO19

Address	Name	POR value	
0x0048	LDO19	0x14	

7	6	5	4	3	2	1	0
LDO19_PD_DIS	LDO19_EN	VLDO19					

Field name	Bits	Type	POR	Description
LDO19_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO19_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO19	[5:0]	RW OTP	0x14	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 109: Register LDO20

Address	Name	POR value	
0x0049	LDO20	0x14	

7	6	5	4	3	2	1	0
LDO20_PD_DIS	LDO20_EN	VLDO20					

Field name	Bits	Type	POR	Description
LDO20_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO20_EN	[6]	RW OTP	0x0	LDO Enable. See Register: LDO3 [0x0038] for details
VLDO20	[5:0]	RW OTP	0x14	LDO voltage select. See Register: LDO3 [0x0038] for details

Table 110: Register LDO21

Address	Name	POR value	
0x004A	LDO21	0x14	

7	6	5	4	3	2	1	0
LDO21_PD_DIS	LDO21_EN	VLDO21					

Field name	Bits	Type	POR	Description
LDO21_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO21_EN	[6]	RW OTP	0x0	LDO 21 Enable. See Register: LDO3 [0x0038] for details
VLDO21	[5:0]	RW OTP	0x14	LDO 21 voltage select. See Register: LDO3 [0x0038] for details

Table 111: Register LDO22

Address	Name	POR value	
0x004B	LDO22	0x14	

7	6	5	4	3	2	1	0
LDO22_PD_DIS	LDO22_EN	VLDO22					

Field name	Bits	Type	POR	Description
LDO22_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO22_EN	[6]	RW OTP	0x0	LDO 22 Enable. See Register: LDO3 [0x0038] for details
VLDO22	[5:0]	RW OTP	0x14	LDO 22 voltage select. See Register: LDO3 [0x0038] for details

Table 112: Register LDO23

Address	Name	POR value	
0x004C	LDO23	0x14	

7	6	5	4	3	2	1	0
LDO23_PD_DIS	LDO23_EN	VLDO23					

Field name	Bits	Type	POR	Description
LDO23_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO23_EN	[6]	RW OTP	0x0	LDO 23 voltage select. See Register: LDO3 [0x0038] for details
VLDO23	[5:0]	RW OTP	0x14	LDO 23 voltage select. See Register: LDO3 [0x0038] for details

Table 113: Register LDO24

Address	Name	POR value	
0x004D	LDO24	0x14	

7	6	5	4	3	2	1	0
LDO24_PD_DIS	LDO24_EN	VLDO24					

Field name	Bits	Type	POR	Description
LDO24_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO24_EN	[6]	RW OTP	0x0	LDO 24 voltage select
VLDO24	[5:0]	RW OTP	0x14	LDO 24 voltage select. **Value** / **Description** 0x0 / 000000: 1.00 V 0x1 / 000001: 1.05 V 0x2 / 000010: 1.10 V ... / ... 0xB / 001011: 1.55 V 0xC / 001100: 1.60 V 0xD / 001101: 1.65 V ... / ... 0x20 / 100000: 2.60 V 0x21 / 100001: 2.65 V 0x22 / 100010: 2.70 V ... / ... 0x28 / 101000: 3.00 V 0x29 / 101001: 3.05 V 0x2A / 101010: 3.10 V ... / 101010: 3.10 V

Table 114: Register LDO25

Address	Name	POR value	
0x004E	LDO25	0x14	

7	6	5	4	3	2	1	0
LDO25_PD_DIS	LDO25_EN	VLDO25					

Field name	Bits	Type	POR	Description
LDO25_PD_DIS	[7]	RW OTP	0x0	Pull down disable. See above for details
LDO25_EN	[6]	RW OTP	0x0	LDO 25 voltage select. See Register: LDO3 [0x0038] for details
VLDO25	[5:0]	RW OTP	0x14	LDO 25 voltage select. See Register: LDO3 [0x0038] for details

Table 115: Register SUPPLY

Address	Name	POR value	
0x004F	SUPPLY	0x10	

7	6	5	4	3	2	1	0
OUT2_32K_EN	CLK_32K_INV	Reserved	BBCHG_EN	Reserved	Reserved	Reserved	Reserved 0

Field name	Bits	Type	POR	Description
OUT2_32K_EN	[7]	RW OTP	0x0	Enable for second 32 kHz Output
CLK_32K_INV	[6]	RW OTP	0x0	Inverts RTC clock input to Digital
BBCHG_EN	[4]	RW VOL OTP	0x1	Backup Battery Charger Enable Value / Description 0x0: 0: BBAT Charger Disabled 0x1 (POR): 1: BBAT Charger Enabled

A.5 Mode Control

Table 116: Register LDO1_MCTL

Address	Name	POR value	
0x0050	LDO1_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO1_MCTL3		LDO1_MCTL2		LDO1_MCTL1		LDO1_MCTL0	

Field name	Bits	Type	POR	Description
LDO1_MCTL3	[7:6]	RW OTP	0x1	LDO1 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO1_MCTL2	[5:4]	RW OTP	0x1	LDO1 mode when in M_CTL mode == 10. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x0050]) for details
LDO1_MCTL1	[3:2]	RW OTP	0x1	LDO1 mode when in M_CTL mode == 01. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x0050]) for details
LDO1_MCTL0	[1:0]	RW OTP	0x1	LDO1 mode when in M_CTL mode == 00. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x0050]) for details

Table 117: Register LDO2_MCTL

Address	Name	POR value	
0x0051	LDO2_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO2_MCTL3		LDO2_MCTL2		LDO2_MCTL1		LDO2_MCTL0	

Field name	Bits	Type	POR	Description
LDO2_MCTL3	[7:6]	RW OTP	0x1	LDO2 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO2_MCTL2	[5:4]	RW OTP	0x1	LDO2 mode when in M_CTL mode == 10. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x0051]) for details
LDO2_MCTL1	[3:2]	RW OTP	0x1	LDO2 mode when in M_CTL mode == 01. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x0051]) for details
LDO2_MCTL0	[1:0]	RW OTP	0x1	LDO2 mode when in M_CTL mode == 00. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x0051]) for details

Table 118: Register LDO3_MCTL

Address	Name	POR value	
0x0052	LDO3_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO3_MCTL3		LDO3_MCTL2		LDO3_MCTL1		LDO3_MCTL0	

Field name	Bits	Type	POR	Description
LDO3_MCTL3	[7:6]	RW OTP	0x1	LDO3 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO3_MCTL2	[5:4]	RW OTP	0x1	LDO3 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO3_MCTL1	[3:2]	RW OTP	0x1	LDO3 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO3_MCTL0	[1:0]	RW OTP	0x1	LDO3 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details

Table 119: Register LDO4_MCTL

Address	Name	POR value	
0x0053	LDO4_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO4_MCTL3		LDO4_MCTL2		LDO4_MCTL1		LDO4_MCTL0	

Field name	Bits	Type	POR	Description
LDO4_MCTL3	[7:6]	RW OTP	0x1	LDO4 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO4_MCTL2	[5:4]	RW OTP	0x1	LDO4 mode when in M_CTL mode == 10. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x0053]) for details
LDO4_MCTL1	[3:2]	RW OTP	0x1	LDO4 mode when in M_CTL mode == 01. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x0053]) for details
LDO4_MCTL0	[1:0]	RW OTP	0x1	LDO4 mode when in M_CTL mode == 00. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x0053]) for details

Table 120: Register LDO5_MCTL

Address	Name	POR value	
0x0054	LDO5_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO5_MCTL3		LDO5_MCTL2		LDO5_MCTL1		LDO5_MCTL0	

Field name	Bits	Type	POR	Description
LDO5_MCTL3	[7:6]	RW OTP	0x1	LDO5 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO5_MCTL2	[5:4]	RW OTP	0x1	LDO5 mode when in M_CTL mode == 10. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x0054]) for details
LDO5_MCTL1	[3:2]	RW OTP	0x1	LDO5 mode when in M_CTL mode == 01. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x0054]) for details
LDO5_MCTL0	[1:0]	RW OTP	0x1	LDO5 mode when in M_CTL mode == 00. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x0054]) for details

Table 121: Register LDO6_MCTL

Address	Name	POR value	
0x0055	LDO6_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO6_MCTL3		LDO6_MCTL2		LDO6_MCTL1		LDO6_MCTL0	

Field name	Bits	Type	POR	Description
LDO6_MCTL3	[7:6]	RW OTP	0x1	LDO6 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO6_MCTL2	[5:4]	RW OTP	0x1	LDO6 mode when in M_CTL mode == 10. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x0055]) for details
LDO6_MCTL1	[3:2]	RW OTP	0x1	LDO6 mode when in M_CTL mode == 01. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x0055]) for details
LDO6_MCTL0	[1:0]	RW OTP	0x1	LDO6 mode when in M_CTL mode == 00. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x0055]) for details

Table 122: Register LDO7_MCTL

Address	Name	POR value	
0x0056	LDO7_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO7_MCTL3		LDO7_MCTL2		LDO7_MCTL1		LDO7_MCTL0	

Field name	Bits	Type	POR	Description
LDO7_MCTL3	[7:6]	RW OTP	0x1	LDO7 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO7_MCTL2	[5:4]	RW OTP	0x1	LDO7 mode when in M_CTL mode == 10. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0056]) for details
LDO7_MCTL1	[3:2]	RW OTP	0x1	LDO7 mode when in M_CTL mode == 01. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0056]) for details
LDO7_MCTL0	[1:0]	RW OTP	0x1	LDO7 mode when in M_CTL mode == 00. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0056]) for details

Table 123: Register LDO8_MCTL

Address	Name	POR value	
0x0057	LDO8_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO8_MCTL3		LDO8_MCTL2		LDO8_MCTL1		LDO8_MCTL0	

Field name	Bits	Type	POR	Description
LDO8_MCTL3	[7:6]	RW OTP	0x1	LDO8 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO8_MCTL2	[5:4]	RW OTP	0x1	LDO8 mode when in M_CTL mode == 10. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0057]) for details
LDO8_MCTL1	[3:2]	RW OTP	0x1	LDO8 mode when in M_CTL mode == 01. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0057]) for details
LDO8_MCTL0	[1:0]	RW OTP	0x1	LDO8 mode when in M_CTL mode == 00. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0057]) for details

Table 124: Register LDO9_MCTL

Address	Name	POR value	
0x0058	LDO9_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO9_MCTL3		LDO9_MCTL2		LDO9_MCTL1		LDO9_MCTL0	

Field name	Bits	Type	POR	Description
LDO9_MCTL3	[7:6]	RW OTP	0x1	LDO9 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO9_MCTL2	[5:4]	RW OTP	0x1	LDO9 mode when in M_CTL mode == 10. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0058]) for details
LDO9_MCTL1	[3:2]	RW OTP	0x1	LDO9 mode when in M_CTL mode == 01. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0058]) for details
LDO9_MCTL0	[1:0]	RW OTP	0x1	LDO9 mode when in M_CTL mode == 00. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0058]) for details

Table 125: Register LDO10_MCTL

Address	Name	POR value	
0x0059	LDO10_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO10_MCTL3		LDO10_MCTL2		LDO10_MCTL1		LDO10_MCTL0	

Field name	Bits	Type	POR	Description
LDO10_MCTL3	[7:6]	RW OTP	0x1	LDO10 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO10_MCTL2	[5:4]	RW OTP	0x1	LDO10 mode when in M_CTL mode == 10. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0059]) for details
LDO10_MCTL1	[3:2]	RW OTP	0x1	LDO10 mode when in M_CTL mode == 01. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0059]) for details
LDO10_MCTL0	[1:0]	RW OTP	0x1	LDO10 mode when in M_CTL mode == 00. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0059]) for details

Table 126: Register LDO11_MCTL

Address	Name	POR value	
0x005A	LDO11_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO11_MCTL3		LDO11_MCTL2		LDO11_MCTL1		LDO11_MCTL0	

Field name	Bits	Type	POR	Description
LDO11_MCTL3	[7:6]	RW OTP	0x1	LDO11 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO11_MCTL2	[5:4]	RW OTP	0x1	LDO11 mode when in M_CTL mode == 10. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x005A]) for details
LDO11_MCTL1	[3:2]	RW OTP	0x1	LDO11 mode when in M_CTL mode == 01. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x005A]) for details
LDO11_MCTL0	[1:0]	RW OTP	0x1	LDO11 mode when in M_CTL mode == 00. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x005A]) for details

Table 127: Register LDO12_MCTL

Address	Name	POR value	
0x005B	LDO12_MCTL	0x55	

7	6	5	4	3	2	1	0
LDO12_MCTL3		LDO12_MCTL2		LDO12_MCTL1		LDO12_MCTL0	

Field name	Bits	Type	POR	Description
LDO12_MCTL3	[7:6]	RW OTP	0x1	LDO12 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep; 0x3 – Off
LDO12_MCTL2	[5:4]	RW OTP	0x1	LDO12 mode when in M_CTL mode == 10. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x005B]) for details
LDO12_MCTL1	[3:2]	RW OTP	0x1	LDO12 mode when in M_CTL mode == 01. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x005B]) for details
LDO12_MCTL0	[1:0]	RW OTP	0x1	LDO12 mode when in M_CTL mode == 00. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x005B]) for details

Table 128: Register LDO13_MCTL

Address	Name	POR value	
0x005C	LDO13_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO13_MCTL3		LDO13_MCTL2		LDO13_MCTL1		LDO13_MCTL0	

Field name	Bits	Type	POR	Description
LDO13_MCTL3	[7:6]	RW OTP	0x0	LDO13 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO13_MCTL2	[5:4]	RW OTP	0x0	LDO13 mode when in M_CTL mode == 10. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x005C]) for details
LDO13_MCTL1	[3:2]	RW OTP	0x0	LDO13 mode when in M_CTL mode == 01. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x005C]) for details
LDO13_MCTL0	[1:0]	RW OTP	0x0	LDO13 mode when in M_CTL mode == 00. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x005C]) for details

Table 129: Register LDO14_MCTL

Address	Name	POR value	
0x005D	LDO14_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO14_MCTL3		LDO14_MCTL2		LDO14_MCTL1		LDO14_MCTL0	

Field name	Bits	Type	POR	Description
LDO14_MCTL3	[7:6]	RW OTP	0x0	LDO14 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO14_MCTL2	[5:4]	RW OTP	0x0	LDO14 mode when in M_CTL mode == 10. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x005D]) for details
LDO14_MCTL1	[3:2]	RW OTP	0x0	LDO14 mode when in M_CTL mode == 01. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x005D]) for details
LDO14_MCTL0	[1:0]	RW OTP	0x0	LDO14 mode when in M_CTL mode == 00. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x005D]) for details

Table 130: Register LDO15_MCTL

Address	Name	POR value	
0x005E	LDO15_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO15_MCTL3		LDO15_MCTL2		LDO15_MCTL1		LDO15_MCTL0	

Field name	Bits	Type	POR	Description
LDO15_MCTL3	[7:6]	RW OTP	0x0	LDO15 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO15_MCTL2	[5:4]	RW OTP	0x0	LDO15 mode when in M_CTL mode == 10. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x005E]) for details
LDO15_MCTL1	[3:2]	RW OTP	0x0	LDO15 mode when in M_CTL mode == 01. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x005E]) for details
LDO15_MCTL0	[1:0]	RW OTP	0x0	LDO15 mode when in M_CTL mode == 00. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x005E]) for details

Table 131: Register LDO16_MCTL

Address	Name	POR value	
0x005F	LDO16_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO16_MCTL3		LDO16_MCTL2		LDO16_MCTL1		LDO16_MCTL0	

Field name	Bits	Type	POR	Description
LDO16_MCTL3	[7:6]	RW OTP	0x0	LDO16 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO16_MCTL2	[5:4]	RW OTP	0x0	LDO16 mode when in M_CTL mode == 10. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x005F]) for details
LDO16_MCTL1	[3:2]	RW OTP	0x0	LDO16 mode when in M_CTL mode == 01. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x005F]) for details
LDO16_MCTL0	[1:0]	RW OTP	0x0	LDO16 mode when in M_CTL mode == 00. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x005F]) for details

Table 132: Register LDO17_MCTL

Address	Name	POR value	
0x0060	LDO17_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO17_MCTL3		LDO17_MCTL2		LDO17_MCTL1		LDO17_MCTL0	

Field name	Bits	Type	POR	Description
LDO17_MCTL3	[7:6]	RW OTP	0x0	LDO17 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO17_MCTL2	[5:4]	RW OTP	0x0	LDO17 mode when in M_CTL mode == 10. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x0060]) for details
LDO17_MCTL1	[3:2]	RW OTP	0x0	LDO17 mode when in M_CTL mode == 01. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x0060]) for details
LDO17_MCTL0	[1:0]	RW OTP	0x0	LDO17 mode when in M_CTL mode == 00. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x0060]) for details

Table 133: Register LDO18_MCTL

Address	Name	POR value	
0x0061	LDO18_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO18_MCTL3		LDO18_MCTL2		LDO18_MCTL1		LDO18_MCTL0	

Field name	Bits	Type	POR	Description
LDO18_MCTL3	[7:6]	RW OTP	0x0	LDO18 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO18_MCTL2	[5:4]	RW OTP	0x0	LDO18 mode when in M_CTL mode == 10. See Field: LDO18_MCTL3 (Reg: LDO18_MCTL [0x0061]) for details
LDO18_MCTL1	[3:2]	RW OTP	0x0	LDO18 mode when in M_CTL mode == 01. See Field: LDO18_MCTL3 (Reg: LDO18_MCTL [0x0061]) for details
LDO18_MCTL0	[1:0]	RW OTP	0x0	LDO18 mode when in M_CTL mode == 00. See Field: LDO18_MCTL3 (Reg: LDO18_MCTL [0x0061]) for details

Table 134: Register LDO19_MCTL

Address	Name	POR value	
0x0062	LDO19_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO19_MCTL3		LDO19_MCTL2		LDO19_MCTL1		LDO19_MCTL0	

Field name	Bits	Type	POR	Description
LDO19_MCTL3	[7:6]	RW OTP	0x0	LDO19 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO19_MCTL2	[5:4]	RW OTP	0x0	LDO19 mode when in M_CTL mode == 10. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x0062]) for details
LDO19_MCTL1	[3:2]	RW OTP	0x0	LDO19 mode when in M_CTL mode == 01. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x0062]) for details
LDO19_MCTL0	[1:0]	RW OTP	0x0	LDO19 mode when in M_CTL mode == 00. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x0062]) for details

Table 135: Register LDO20_MCTL

Address	Name	POR value	
0x0063	LDO20_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO20_MCTL3		LDO20_MCTL2		LDO20_MCTL1		LDO20_MCTL0	

Field name	Bits	Type	POR	Description
LDO20_MCTL3	[7:6]	RW OTP	0x0	LDO20 mode when in M_CTL mode == 11. Value: 0x0 (POR) = Off; 0x1 = On; 0x2 = Sleep; 0x3 = Off
LDO20_MCTL2	[5:4]	RW OTP	0x0	LDO20 mode when in M_CTL mode == 10. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x0063]) for details
LDO20_MCTL1	[3:2]	RW OTP	0x0	LDO20 mode when in M_CTL mode == 01. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x0063]) for details
LDO20_MCTL0	[1:0]	RW OTP	0x0	LDO20 mode when in M_CTL mode == 00. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x0063]) for details

Table 136: Register LDO21_MCTL

Address	Name	POR value	
0x0064	LDO21_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO21_MCTL3		LDO21_MCTL2		LDO21_MCTL1		LDO21_MCTL0	

Field name	Bits	Type	POR	Description
LDO21_MCTL3	[7:6]	RW OTP	0x0	LDO21 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO21_MCTL2	[5:4]	RW OTP	0x0	LDO21 mode when in M_CTL mode == 10. See Field: LDO21_MCTL3 (Reg: LDO21_MCTL [0x0064]) for details
LDO21_MCTL1	[3:2]	RW OTP	0x0	LDO21 mode when in M_CTL mode == 01. See Field: LDO21_MCTL3 (Reg: LDO21_MCTL [0x0064]) for details
LDO21_MCTL0	[1:0]	RW OTP	0x0	LDO21 mode when in M_CTL mode == 00. See Field: LDO21_MCTL3 (Reg: LDO21_MCTL [0x0064]) for details

Table 137: Register LDO22_MCTL

Address	Name	POR value	
0x0065	LDO22_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO22_MCTL3		LDO22_MCTL2		LDO22_MCTL1		LDO22_MCTL0	

Field name	Bits	Type	POR	Description
LDO22_MCTL3	[7:6]	RW OTP	0x0	LDO22 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO22_MCTL2	[5:4]	RW OTP	0x0	LDO22 mode when in M_CTL mode == 10. See Field: LDO22_MCTL3 (Reg: LDO22_MCTL [0x0065]) for details
LDO22_MCTL1	[3:2]	RW OTP	0x0	LDO22 mode when in M_CTL mode == 01. See Field: LDO22_MCTL3 (Reg: LDO22_MCTL [0x0065]) for details
LDO22_MCTL0	[1:0]	RW OTP	0x0	LDO22 mode when in M_CTL mode == 00. See Field: LDO22_MCTL3 (Reg: LDO22_MCTL [0x0065]) for details

Table 138: Register LDO23_MCTL

Address	Name	POR value	
0x0066	LDO23_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO23_MCTL3		LDO23_MCTL2		LDO23_MCTL1		LDO23_MCTL0	

Field name	Bits	Type	POR	Description
LDO23_MCTL3	[7:6]	RW OTP	0x0	LDO23 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO23_MCTL2	[5:4]	RW OTP	0x0	LDO23 mode when in M_CTL mode == 10. See Field: LDO23_MCTL3 (Reg: LDO23_MCTL [0x0066]) for details
LDO23_MCTL1	[3:2]	RW OTP	0x0	LDO23 mode when in M_CTL mode == 01. See Field: LDO23_MCTL3 (Reg: LDO23_MCTL [0x0066]) for details
LDO23_MCTL0	[1:0]	RW OTP	0x0	LDO23 mode when in M_CTL mode == 00. See Field: LDO23_MCTL3 (Reg: LDO23_MCTL [0x0066]) for details

Table 139: Register LDO24_MCTL

Address	Name	POR value	
0x0067	LDO24_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO24_MCTL3		LDO24_MCTL2		LDO24_MCTL1		LDO24_MCTL0	

Field name	Bits	Type	POR	Description
LDO24_MCTL3	[7:6]	RW OTP	0x0	LDO_24 mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On; 0x2 – Sleep; 0x3 – Off
LDO24_MCTL2	[5:4]	RW OTP	0x0	LDO_24 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO24_MCTL1	[3:2]	RW OTP	0x0	LDO_24 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO24_MCTL0	[1:0]	RW OTP	0x0	LDO_24 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details

Table 140: Register LDO25_MCTL

Address	Name	POR value	
0x0068	LDO25_MCTL	0x00	

7	6	5	4	3	2	1	0
LDO25_MCTL3		LDO25_MCTL2		LDO25_MCTL1		LDO25_MCTL0	

Field name	Bits	Type	POR	Description
LDO25_MCTL3	[7:6]	RW OTP	0x0	LDO_25 mode when in M_CTL mode == 11. Value / Description: 0x0 (POR) – Off 0x1 – On 0x2 – Sleep 0x3 – Off
LDO25_MCTL2	[5:4]	RW OTP	0x0	LDO_25 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO25_MCTL1	[3:2]	RW OTP	0x0	LDO_25 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details
LDO25_MCTL0	[1:0]	RW OTP	0x0	LDO_25 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x0052]) for details

Table 141: Register BUCK0_MCTL

Address	Name	POR value	
0x0069	BUCK0_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK0_MCTL3		BUCK0_MCTL2		BUCK0_MCTL1		BUCK0_MCTL0	

Field name	Bits	Type	POR	Description
BUCK0_MCTL3	[7:6]	RW OTP	0x1	BUCK0 mode when in M_CTL mode == 11. Value / Description: 0x0 – Off 0x1 (POR) – On 0x2 – Sleep (Force PFM mode) 0x3 – Turbo (Buck0, Others On)
BUCK0_MCTL2	[5:4]	RW OTP	0x1	BUCK0 mode when in M_CTL mode == 10. See Unknown Register: BUCK0MCTL3 for details
BUCK0_MCTL1	[3:2]	RW OTP	0x1	BUCK0 mode when in M_CTL mode == 01. See Field: BUCK0_MCTL3 (Reg: BUCK0_MCTL [0x0069]) for details
BUCK0_MCTL0	[1:0]	RW OTP	0x1	BUCK0 mode when in M_CTL mode == 00. See Field: BUCK0_MCTL3 (Reg: BUCK0_MCTL [0x0069]) for details

Table 142: Register BUCK1_MCTL

Address	Name	POR value	
0x006A	BUCK1_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK1_MCTL3		BUCK1_MCTL2		BUCK1_MCTL1		BUCK1_MCTL0	

Field name	Bits	Type	POR	Description
BUCK1_MCTL3	[7:6]	RW OTP	0x1	BUCK1 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK1_MCTL2	[5:4]	RW OTP	0x1	BUCK1 mode when in M_CTL mode == 10. See Unknown Register: BUCK1MCTL3 for details
BUCK1_MCTL1	[3:2]	RW OTP	0x1	BUCK1 mode when in M_CTL mode == 01. See Field: BUCK1_MCTL3 (Reg: BUCK1_MCTL [0x006A]) for details
BUCK1_MCTL0	[1:0]	RW OTP	0x1	BUCK1 mode when in M_CTL mode == 00. See Field: BUCK1_MCTL3 (Reg: BUCK1_MCTL [0x006A]) for details

Table 143: Register BUCK2_MCTL

Address	Name	POR value	
0x006B	BUCK2_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK2_MCTL3		BUCK2_MCTL2		BUCK2_MCTL1		BUCK2_MCTL0	

Field name	Bits	Type	POR	Description
BUCK2_MCTL3	[7:6]	RW OTP	0x1	BUCK2 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK2_MCTL2	[5:4]	RW OTP	0x1	BUCK2 mode when in M_CTL mode == 10. See Unknown Register: BUCK2MCTL3 for details
BUCK2_MCTL1	[3:2]	RW OTP	0x1	BUCK2 mode when in M_CTL mode == 01. See Field: BUCK2_MCTL3 (Reg: BUCK2_MCTL [0x006B]) for details
BUCK2_MCTL0	[1:0]	RW OTP	0x1	BUCK2 mode when in M_CTL mode == 00. See Field: BUCK2_MCTL3 (Reg: BUCK2_MCTL [0x006B]) for details

Table 144: Register BUCK3_MCTL

Address	Name	POR value	
0x006C	BUCK3_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK3_MCTL3		BUCK3_MCTL2		BUCK3_MCTL1		BUCK3_MCTL0	

Field name	Bits	Type	POR	Description
BUCK3_MCTL3	[7:6]	RW OTP	0x1	BUCK3 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK3_MCTL2	[5:4]	RW OTP	0x1	BUCK3 mode when in M_CTL mode == 10. See Unknown Register: BUCK3MCTL3 for details
BUCK3_MCTL1	[3:2]	RW OTP	0x1	BUCK3 mode when in M_CTL mode == 01. See Field: BUCK3_MCTL3 (Reg: BUCK3_MCTL [0x006C]) for details
BUCK3_MCTL0	[1:0]	RW OTP	0x1	BUCK3 mode when in M_CTL mode == 00. See Field: BUCK3_MCTL3 (Reg: BUCK3_MCTL [0x006C]) for details

Table 145: Register BUCK4_MCTL

Address	Name	POR value	
0x006D	BUCK4_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK4_MCTL3		BUCK4_MCTL2		BUCK4_MCTL1		BUCK4_MCTL0	

Field name	Bits	Type	POR	Description
BUCK4_MCTL3	[7:6]	RW OTP	0x1	BUCK4 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK4_MCTL2	[5:4]	RW OTP	0x1	BUCK4 mode when in M_CTL mode == 10. See Unknown Register: BUCK4MCTL3 for details
BUCK4_MCTL1	[3:2]	RW OTP	0x1	BUCK4 mode when in M_CTL mode == 01. See Field: BUCK4_MCTL3 (Reg: BUCK4_MCTL [0x006D]) for details
BUCK4_MCTL0	[1:0]	RW OTP	0x1	BUCK4 mode when in M_CTL mode == 00. See Field: BUCK4_MCTL3 (Reg: BUCK4_MCTL [0x006D]) for details

Table 146: Register BUCK5_MCTL

Address	Name	POR value	
0x006E	BUCK5_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK5_MCTL3		BUCK5_MCTL2		BUCK5_MCTL1		BUCK5_MCTL0	

Field name	Bits	Type	POR	Description
BUCK5_MCTL3	[7:6]	RW OTP	0x1	BUCK5 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK5_MCTL2	[5:4]	RW OTP	0x1	BUCK5 mode when in M_CTL mode == 10. See Unknown Register: BUCK5MCTL3 for details
BUCK5_MCTL1	[3:2]	RW OTP	0x1	BUCK5 mode when in M_CTL mode == 01. See Field: BUCK5_MCTL3 (Reg: BUCK5_MCTL [0x006E]) for details
BUCK5_MCTL0	[1:0]	RW OTP	0x1	BUCK5 mode when in M_CTL mode == 00. See Field: BUCK5_MCTL3 (Reg: BUCK5_MCTL [0x006E]) for details

Table 147: Register BUCK6_MCTL

Address	Name	POR value	
0x006F	BUCK6_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK6_MCTL3		BUCK6_MCTL2		BUCK6_MCTL1		BUCK6_MCTL0	

Field name	Bits	Type	POR	Description
BUCK6_MCTL3	[7:6]	RW OTP	0x1	BUCK6 mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Sleep (Force PFM mode); 0x3 – Turbo (Buck0, Others On)
BUCK6_MCTL2	[5:4]	RW OTP	0x1	BUCK6 mode when in M_CTL mode == 10. See Unknown Register: BUCK6MCTL3 for details
BUCK6_MCTL1	[3:2]	RW OTP	0x1	BUCK6 mode when in M_CTL mode == 01. See Field: BUCK6_MCTL3 (Reg: BUCK6_MCTL [0x006F]) for details
BUCK6_MCTL0	[1:0]	RW OTP	0x1	BUCK6 mode when in M_CTL mode == 00. See Field: BUCK6_MCTL3 (Reg: BUCK6_MCTL [0x006F]) for details

Table 148: Register BUCK_RF_MCTL

Address	Name	POR value	
0x0070	BUCK_RF_MCTL	0x55	

7	6	5	4	3	2	1	0
BUCK_RF_MCTL3		BUCK_RF_MCTL2		BUCK_RF_MCTL1		BUCK_RF_MCTL0	

Field name	Bits	Type	POR	Description
BUCK_RF_MCTL3	[7:6]	RW OTP	0x1	BUCK_RF mode when in M_CTL mode == 11. Value: 0x0 – Off; 0x1 (POR) – On; 0x2 – Off; 0x3 – Off
BUCK_RF_MCTL2	[5:4]	RW OTP	0x1	BUCK_RF mode when in M_CTL mode == 10. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0070]) for details
BUCK_RF_MCTL1	[3:2]	RW OTP	0x1	BUCK_RF mode when in M_CTL mode == 01. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0070]) for details
BUCK_RF_MCTL0	[1:0]	RW OTP	0x1	BUCK_RF mode when in M_CTL mode == 00. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0070]) for details

Table 149: Register GPADC_MCTL

Address	Name	POR value	
0x0071	GPADC_MCTL	0x00	

7	6	5	4	3	2	1	0
GPADC_MCTL3		GPADC_MCTL2		GPADC_MCTL1		GPADC_MCTL0	

Field name	Bits	Type	POR	Description
GPADC_MCTL3	[7:6]	RW OTP	0x0	GPADC mode when in M_CTL mode == 11. Value: 0x0 (POR) – Off; 0x1 – On if already enabled; 0x2 – Sleep - 20ms mode if already enabled; 0x3 – n/a
GPADC_MCTL2	[5:4]	RW OTP	0x0	GPADC mode when in M_CTL mode == 10. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0071]) for details
GPADC_MCTL1	[3:2]	RW OTP	0x0	GPADC mode when in M_CTL mode == 01. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0071]) for details
GPADC_MCTL0	[1:0]	RW OTP	0x0	GPADC mode when in M_CTL mode == 00. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0071]) for details

Table 150: Register MISC_MCTL

Address	Name	POR value	
0x0072	MISC_MCTL	0xFF	

7	6	5	4	3	2	1	0
DIG_CLK_MCTL3	DIG_CLK_MCTL2	DIG_CLK_MCTL1	DIG_CLK_MCTL0	BBAT_MCTL3	BBAT_MCTL2	BBAT_MCTL1	BBAT_MCTL0

Field name	Bits	Type	POR	Description
DIG_CLK_MCTL3	[7]	RW OTP	0x1	Disable Digital clock when in M_CTL mode == 11
DIG_CLK_MCTL2	[6]	RW OTP	0x1	Disable Digital clock when in M_CTL mode == 10
DIG_CLK_MCTL1	[5]	RW OTP	0x1	Disable Digital clock when in M_CTL mode == 01
DIG_CLK_MCTL0	[4]	RW OTP	0x1	Disable Digital clock when in M_CTL mode == 00
BBAT_MCTL3	[3]	RW OTP	0x1	BBAT enable when in M_CTL mode == 11 Value: 0x0 – Off; 0x1 (POR) – On if already enabled
BBAT_MCTL2	[2]	RW OTP	0x1	BBAT enable when in M_CTL mode == 10 (See BBAT_MCTL3 for details)
BBAT_MCTL1	[1]	RW OTP	0x1	BBAT enable when in M_CTL mode == 01 (See BBAT_MCTL3 for details)
BBAT_MCTL0	[0]	RW OTP	0x1	BBAT enable when in M_CTL mode == 00 (See BBAT_MCTL3 for details)

Table 151: Register VBUCK0_MCTL_RET

Address	Name	POR value	
0x0073	VBUCK0_MCTL_RET	0x0C	

7	6	5	4	3	2	1	0
Reserved	VBUCK0_RET						

Field name	Bits	Type	POR	Description
VBUCK0_RET	[6:0]	RW OTP	0xc	Buck 0 retention (sleep) voltage. See Field: VBUCK0 (Reg: BUCK0_CONF0 [0x0024]) for voltage mapping

Table 152: Register VBUCK0_MCTL_TUR

Address	Name	POR value	
0x0074	VBUCK0_MCTL_TUR	0x0C	

7	6	5	4	3	2	1	0
Reserved	VBUCK0_TUR						

Field name	Bits	Type	POR	Description
VBUCK0_TUR	[6:0]	RW OTP	0xc	Buck 0 turbo voltage. See Field: VBUCK0 (Reg: BUCK0_CONF0 [0x0024]) for voltage mapping

Table 153: Register VBUCK1_MCTL_RET

Address	Name	POR value	
0x0075	VBUCK1_MCTL_RET	0x0C	

7	6	5	4	3	2	1	0
Reserved	VBUCK1_RET						

Field name	Bits	Type	POR	Description
VBUCK1_RET	[6:0]	RW OTP	0xc	Buck 1 retention (sleep) voltage. See Field: VBUCK1 (Reg: BUCK1_CONF0 [0x0027]) for voltage mapping

Table 154: Register VBUCK4_MCTL_RET

Address	Name	POR value	
0x0076	VBUCK4_MCTL_RET	0x0C	

7	6	5	4	3	2	1	0
Reserved	VBUCK4_RET						

Field name	Bits	Type	POR	Description
VBUCK4_RET	[6:0]	RW OTP	0xc	Buck4 retention voltage. See Field: VBUCK4 (Reg: BUCK4_CONF0 [0x002E]) for voltage mapping

A.6 Control

Table 155: Register WAIT_CONT

Address	Name	POR value	
0x0077	WAIT_CONT	0x3B	

7	6	5	4	3	2	1	0
WAIT_DIR	RTC_CLOCK	WAIT_MODE	EN_32K	DELAY_TIME			

Field name	Bits	Type	POR	Description
WAIT_DIR	[7]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: Wait during Power-Up Sequence 0x1: 1: Wait during Power-Up and Power-Down Sequence
RTC_CLOCK	[6]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: No Gating of RTC Calendar Clock 0x1: 1: Clock to RTC Counter is Gated until WAIT is Asserted (depends on WAIT_MODE)
WAIT_MODE	[5]	RW OTP	0x1	OUT32K and RTC internal clock enable mode **Value** / **Description** 0x0: 0: Wait for GPIO1 to be Active 0x1 (POR): 1: Delay Timer Mode Start DELAY_TIME timer and wait until it expires
EN_32K	[4]	RW OTP	0x1	Enable OUT_32K from power-up **Value** / **Description** 0x0: 0: Wait for out_32k_pd 0x1 (POR): 1: output 32K from OTP_load

Field name	Bits	Type	POR	Description
DELAY_TIME	[3:0]	RW OTP	0xb	OUT32K and RTC internal clock delay when in timer mode

Value	Description
0x0	0000: 0 µs
0x1	0001: 540 µs
0x2	0010: 1.0 ms
0x3	0011: 2.0 ms
0x4	0100: 4.1 ms
0x5	0101: 8.2 ms
0x6	0110: 16.4 ms
0x7	0111: 32.8 ms
0x8	1000: 65.5 ms
0x9	1001: 131 ms
0xA	1010: 262 ms
0xB	1011: 524 ms
0xC	1100: 1.0 s
0xD	1101: 2.1 s
0xE	1110: 4.2 s
0xF	1111: 8.4 s

Table 156: Register ONKEY_CONT1

Address	Name	POR value	
0x0078	ONKEY_CONT1	0x19	

7	6	5	4	3	2	1	0
NONKEY_DEB				PRESS_TIME			

Field name	Bits	Type	POR	Description
NONKEY_DEB	[7:4]	RW OTP	0x1	nONKEY short debounce time

Value	Description
0x0	None
0x1 (POR)	10 ms
0x2	20 ms
...	...
0xB	110 ms
0xC	120 ms
0xD	240 ms
0xE	360 ms
0xF	480 ms

Field name	Bits	Type	POR	Description
PRESS_TIME	[3:0]	RW OTP	0x9	Long (shutdown) nONKEY time Value / Description: 0x0: 3.0 s 0x1: 3.5 s ...: ... 0x8: 7.0 s 0x9 (POR): 7.5 s 0xA: 8.0 s ...: ... 0xF: 10.5 s

Table 157: Register ONKEY_CONT2

Address	Name	POR value	
0x0079	ONKEY_CONT2	0x11	

7	6	5	4	3	2	1	0
Reserved	NONKEY_HOLD_OFF_DEB			Reserved	NONKEY_HOLD_ON_DEB		

Field name	Bits	Type	POR	Description
NONKEY_HOLD_OFF_DEB	[6:4]	RW OTP	0x1	nONKEY hold to request shutdown debounce time Value / Description: 0x0: 0.5 s 0x1 (POR): 1.0 s ...: ... 0x5: 3.0 s 0x6: 3.5 s 0x7: 4.0 s
NONKEY_HOLD_ON_DEB	[2:0]	RW OTP	0x1	nONKEY hold on time (cauese POC wakeup). Same enumeration as Field: NONKEY_HOLD_OFF_DEB (Reg: OUT2_32K_ONKEY_CONT [0x0079])

Table 158: Register POWER_CONT

Address	Name	POR value	
0x007A	POWER_CONT	0x08	

7	6	5	4	3	2	1	0
NON2_MCTRL_WAKE_DIS	Reserved 0	Reserved 0	Reserved 0	BBAT_ILIM_IGNORE	Reserved 0	Reserved 0	MCTRL_EN

Field name	Bits	Type	POR	Description
NON2_MCTRL_WAKE_DIS	[7]	RW	0x0	Disable MCTL_wakeup by nON2 when set to 1
BBAT_ILIM_IGNORE	[3]	RW OTP	0x1	When this bit is set active (1) it allows the backup battery charger to be ON even when the current limit is reached.
MCTRL_EN	[0]	RW OTP	0x0	Enable the use of M_CTL pins (only in Active) **Value** / **Description** 0x0 (POR): 0: Mode Control pins MCTRL[1:0] Disabled 0x1: 1: Mode Control pins MCTRL[1:0] Enabled in ACTIVE state

Table 159: Register VDDFAULT

Address	Name	POR value	
0x007B	VDDFAULT	0x2B	

7	6	5	4	3	2	1	0
Reserved	Reserved	VDD_FAULT_ADJ				VDD_HYST_ADJ	

Field name	Bits	Type	POR	Description
VDD_FAULT_ADJ	[5:2]	RW OTP	0xA	Modifies the threshold voltage for VDD, default setting of 0b1010 gives value if 2.90 V.
VDD_HYST_ADJ	[1:0]	RW OTP	0x3	Modifies the hysteresis in the comparator. The default value of 0b11 sets an upper voltage limit of 3.222 V

Table 160: Register BBAT_CONT

Address	Name	POR value	
0x007C	BBAT_CONT	0xFF	

7	6	5	4	3	2	1	0
BCHARGER_ISET				BCHARGER_VSET			

Field name	Bits	Type	POR	Description
BCHARGER_ISET	[7:4]	RW OTP	0xf	Backup battery charger current

Value	Description
0x0	0000: 0 µA
0x1	0001: 100 µA
0x2	0010: 200 µA
0x3	0011: 300 µA
0x4	0100: 400 µA
0x5	0101: 500 µA
0x6	0110: 600 µA
0x7	0111: 700 µA
0x8	1000: 800 µA
0x9	1001: 900 µA
0xA	1010: 1 mA
0xB	1011: 2 mA
0xC	1100: 3 mA
0xD	1101: 4 mA
0xE	1110: 5 mA
0xF	1111: 6 mA

Field name	Bits	Type	POR	Description
BCHARGER_VSET	[3:0]	RW OTP	0xf	Backup battery charger voltage

Value	Description
0x0	0000: 1.8 V
0x1	0001: 1.9 V
0x2	0010: 2.0 V
0x3	0011: 2.1 V
0x4	0100: 2.2 V
0x5	0101: 2.3 V
0x6	0110: 2.4 V
0x7	0111: 2.5 V
0x8	1000: 2.6 V
0x9	1001: 2.7 V
0xA	1010: 2.8 V
0xB	1011: 2.9 V
0xC	1100: 3.0 V
0xD	1101: 3.1 V
0xE	1110: 3.2 V
0xF	1111: 3.3 V

A.7 ADC

Table 161: Register ADC_MAN

Address	Name	POR value	
0x007D	ADC_MAN	0x80	

7	6	5	4	3	2	1	0
ISRC_50U	Reserved	Reserved	MAN_CONV	MUX_SEL			

Field name	Bits	Type	POR	Description
ISRC_50U	[7]	RW OTP	0x1	Use a 50 µA current source for TEMP1 and TEMP2 rather than 10 µA.
MAN_CONV	[4]	RW VOL	0x0	Perform Manual Conversion. (reset to 0 when conversion is complete)
MUX_SEL	[3:0]	RW OTP	0x0	ADC multiplexer channel select for manual conversions **Value** / **Description** 0x0 (POR): 0000: VBAT_S pin (Channel A0) Selected 0x2: 0010: TEMP1 pin (Channel A1) Selected 0x4: 0100: VF pin (Channel A3) Selected 0x5: 0101: ADCIN (Channel A4) Selected 0x6: 0110: TEMP2 pin (Channel A2) Selected 0x8: 1000: internal TJUNC (Channel A4) Selected

Table 162: Register ADC_CONT

Address	Name	POR value	
0x007E	ADC_CONT	0x00	

7	6	5	4	3	2	1	0
ADC_AUTO_EN	ADC_MODE	TEMP1_ISRC_EN	VF_ISRC_EN	TEMP2_ISRC_EN	AUTO_ADCIN_EN	AUTO_VF_EN	AUTO_VBAT_EN

Field name	Bits	Type	POR	Description
ADC_AUTO_EN	[7]	RW OTP	0x0	ADC Auto Measurements Enabled
ADC_MODE	[6]	RW OTP	0x0	**Value** / **Description** 0x0 (POR): 0: Measurement Sequence Interval 20 ms (economy mode) 0x1: 1: Measurement Sequence Interval 2 ms
TEMP1_ISRC_EN	[5]	RW OTP	0x0	TEMP1 50 µA Current Source Enabled: **Value** / **Description** 0x0 (POR): 0: Enabled One Slot Before Measurement (disabled after measurement) 0x1: 1: Permanently Enabled

Field name	Bits	Type	POR	Description
VF_ISRC_EN	[4]	RW OTP	0x0	VF 50 µA Current Source Enabled: Value: 0x0 (POR) — 0:Disabled Value: 0x1 — 1: Permanently Enabled in Manual mode. Dynamic in Auto mode
TEMP2_ISRC_EN	[3]	RW OTP	0x0	TEMP2 50 µA Current Source Enabled: Value: 0x0 (POR) — 0: Enabled One Slot Before Measurement (disabled after measurement) Value: 0x1 — 1: Permanently Enabled
AUTO_ADCIN_EN	[2]	RW OTP	0x0	ADCIN Auto Measurements Enabled
AUTO_VF_EN	[1]	RW OTP	0x0	VF Auto Measurements Enabled
AUTO_VBAT_EN	[0]	RW OTP	0x0	VDDOUT Auto Measurements Enabled

Table 163: Register ADC_RES_L

Address	Name	POR value	
0x0080	ADC_RES_L	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ADC_RES_LSB			

Field name	Bits	Type	POR	Description
ADC_RES_LSB	[3:0]	RO	0x0	12 Bit Manual Conversion Result (4 LSBs)

Table 164: Register ADC_RES_H

Address	Name	POR value	
0x0081	ADC_RES_H	0x00	

7	6	5	4	3	2	1	0
ADC_RES_MSB							

Field name	Bits	Type	POR	Description
ADC_RES_MSB	[7:0]	RO	0x0	12 Bit Manual Conversion Result (8 MSBs)

Table 165: Register VBAT_RES

Address	Name	POR value	
0x0082	VBAT_RES	0x00	

7	6	5	4	3	2	1	0
VBAT_RES_MSB							

Field name	Bits	Type	POR	Description
VBAT_RES_MSB	[7:0]	RO	0x0	Auto VBAT_S Conversion Result (8 MSBs) 00000000 corresponds to 2.5 V 11111111 corresponds to 4.5 V

Table 166: Register VDDOUT_MON

Address	Name	POR value	
0x0083	VDDOUT_MON	0x00	

7	6	5	4	3	2	1	0
VDDOUT_MON							

Field name	Bits	Type	POR	Description
VDDOUT_MON	[7:0]	RW OTP	0x0	Battery Monitor threshold

Table 167: Register TEMP1_RES

Address	Name	POR value	
0x0084	TEMP1_RES	0x00	

7	6	5	4	3	2	1	0
TBAT1_RES							

Field name	Bits	Type	POR	Description
TBAT1_RES	[7:0]	RO	0x0	Auto TEMP1 Conversion Result (8 MSBs) 00000000 - 11111111

Table 168: Register TEMP1_HIGHP

Address	Name	POR value	
0x0085	TEMP1_HIGHP	0x00	

7	6	5	4	3	2	1	0
TEMP1_HIGHP							

Field name	Bits	Type	POR	Description
TEMP1_HIGHP	[7:0]	RW OTP	0x0	TEMP1 High threshold

Table 169: Register TEMP1_HIGHN

Address	Name	POR value	
0x0086	TEMP1_HIGHN	0x00	

7	6	5	4	3	2	1	0
TEMP1_HIGHN							

Field name	Bits	Type	POR	Description
TEMP1_HIGHN	[7:0]	RW OTP	0x0	TEMP1 Medium threshold

Table 170: Register TEMP1_LOW

Address	Name	POR value	
0x0087	TEMP1_LOW	0xFF	

7	6	5	4	3	2	1	0
TEMP1_LOW							

Field name	Bits	Type	POR	Description
TEMP1_LOW	[7:0]	RW OTP	0xFF	TEMP1 Low threshold

Table 171: Register T_OFFSET

Address	Name	POR value	
0x0088	T_OFFSET	0x00	

7	6	5	4	3	2	1	0
T_OFFSET							

Field name	Bits	Type	POR	Description
T_OFFSET	[7:0]	RW OTP	0x0	Offset Calibration TJUNC measurement 10000000 - 01111111 (signed 2's compliment)

Table 172: Register VF_RES

Address	Name	POR value	
0x0089	VF_RES	0x00	

7	6	5	4	3	2	1	0
VF_RES_MSB							

Field name	Bits	Type	POR	Description
VF_RES_MSB	[7:0]	RO	0x0	Auto VF Conversion Result (8 MSBs) 00000000 - 11111111

Table 173: Register VF_HIGH

Address	Name	POR value	
0x008A	VF_HIGH	0xFF	

7	6	5	4	3	2	1	0
VF_HIGH							

Field name	Bits	Type	POR	Description
VF_HIGH	[7:0]	RW OTP	0xFF	VF High threshold

Table 174: Register VF_LOW

Address	Name	POR value	
0x008B	VF_LOW	0x00	

7	6	5	4	3	2	1	0
VF_LOW							

Field name	Bits	Type	POR	Description
VF_LOW	[7:0]	RW OTP	0x0	VF Low threshold

Table 175: Register ADCIN_RES

Address	Name	POR value	
0x008C	ADCIN_RES	0x00	

7	6	5	4	3	2	1	0
ADCIN_RES							

Field name	Bits	Type	POR	Description
ADCIN_RES	[7:0]	RO	0x0	Auto ADCIN Conversion Result (8 MSBs) 00000000 - 11111111

Table 176: Register TEMP2_RES

Address	Name	POR value	
0x008F	TEMP2_RES	0x00	

7	6	5	4	3	2	1	0
TBAT2_RES							

Field name	Bits	Type	POR	Description
TEMP2_RES	[7:0]	RO	0x0	Auto TEMP2 Conversion Result (8 MSBs) 00000000 - 11111111

Table 177: Register TEMP2_HIGHP

Address	Name	POR value	
0x0090	TEMP2_HIGHP	0x00	

7	6	5	4	3	2	1	0
TEMP2_HIGHP							

Field name	Bits	Type	POR	Description
TEMP2_HIGHP	[7:0]	RW OTP	0x0	TEMP2 High threshold

Table 178: Register TEMP2_HIGHN

Address	Name	POR value	
0x0091	TEMP2_HIGHN	0x00	

7	6	5	4	3	2	1	0
TEMP2_HIGHN							

Field name	Bits	Type	POR	Description
TEMP2_HIGHN	[7:0]	RW OTP	0x0	TEMP2 Medium threshold

Table 179: Register TEMP2_LOW

Address	Name	POR value	
0x0092	TEMP2_LOW	0xFF	

7	6	5	4	3	2	1	0
TEMP2_LOW							

Field name	Bits	Type	POR	Description
TEMP2_LOW	[7:0]	RW OTP	0xFF	TEMP2 Low threshold

Table 180: Register TJUNC_RES

Address	Name	POR value	
0x0093	TJUNC_RES	0x00	

7	6	5	4	3	2	1	0
TJUNC_RES							

Field name	Bits	Type	POR	Description
TJUNC_RES	[7:0]	RO	0x0	Auto TJUNC Conversion Result (8 MSBs) 00000000 - 11111111

Table 181: Register ADC_RES_AUTO1

Address	Name	POR value	
0x0094	ADC_RES_AUTO1	0x00	

7	6	5	4	3	2	1	0
TEMP1_RES_LSB				VBAT_RES_LSB			

Field name	Bits	Type	POR	Description
TEMP1_RES_LSB	[7:4]	RO	0x0	Auto TEMP1 Conversion Result
VBAT_RES_LSB	[3:0]	RO	0x0	Auto VBAT_S Conversion Result

Table 182: Register ADC_RES_AUTO2

Address	Name	POR value	
0x0095	ADC_RES_AUTO2	0x00	

7	6	5	4	3	2	1	0
ADCIN_RES_LSB				VF_RES_LSB			

Field name	Bits	Type	POR	Description
ADCIN_RES_LSB	[7:4]	RO	0x0	Auto ADCIN Conversion Result
VF_RES_LSB	[3:0]	RO	0x0	Auto VF Conversion Result

Table 183: Register ADC_RES_AUTO3

Address	Name	POR value	
0x0096	ADC_RES_AUTO3	0x00	

7	6	5	4	3	2	1	0
TJUNC_RES_LSB				TEMP2_RES_LSB			

Field name	Bits	Type	POR	Description
TJUNC_RES_LSB	[7:4]	RO	0x0	Auto TJUNC Conversion Result
TEMP2_RES_LSB	[3:0]	RO	0x0	Auto TEMP2 Conversion Result

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Table 184: Register COUNT_S

Address	Name	POR value	
0x0097	COUNT_S	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	COUNT_SEC					

Field name	Bits	Type	POR	Description
COUNT_SEC	[5:0]	RW	0x0	0x00 - 0x3B: RTC SECONDS. When read, latches data in COUNT_MIN - COUNT_YEAR

Table 185: Register COUNT_MI

Address	Name	POR value	
0x0098	COUNT_MI	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	COUNT_MIN					

Field name	Bits	Type	POR	Description
COUNT_MIN	[5:0]	RW	0x0	0x00 - 0x3B: RTC MINUTES

Table 186: Register COUNT_H

Address	Name	POR value	
0x0099	COUNT_H	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	COUNT_HOUR				

Field name	Bits	Type	POR	Description
COUNT_HOUR	[4:0]	RW	0x0	0x00 - 0x17: RTC HOURS

Table 187: Register COUNT_D

Address	Name	POR value	
0x009A	COUNT_D	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	COUNT_DAY				

Field name	Bits	Type	POR	Description
COUNT_DAY	[4:0]	RW	0x1	0x01 - 0x1F: RTC DAYS

Table 188: Register COUNT_MO

Address	Name	POR value	
0x009B	COUNT_MO	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	COUNT_MONTH			

Field name	Bits	Type	POR	Description
COUNT_MONTH	[3:0]	RW	0x1	0x01 - 0x0C: RTC MONTHS

Table 189: Register COUNT_Y

Address	Name	POR value	
0x009C	COUNT_Y	0x00	

7	6	5	4	3	2	1	0
Reserved	MONITOR	COUNT_YEAR					

Field name	Bits	Type	POR	Description
MONITOR	[6]	RW	0x0	RTC Status: Value: 0x0 (POR) — 0: Read-out - RTC Clock/Counters OFF (RTC not started or reset after power loss) Value: 0x1 — 1: Read-out - Clock ON / Time OK (set to 1 when Setting Time to start the RTC and arm the monitor function)
COUNT_YEAR	[5:0]	RW	0x0	0x00 - 0x3F: RTC YEARS (0 corresponds to year 2000) A write to this register latches the registers COUNT_SEC to COUNT_MONTH into the current RTC calendar counter

Table 190: Register ALARM_S

Address	Name	POR value	
0x009D	ALARM_S	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	ALARM_SEC					

Field name	Bits	Type	POR	Description
ALARM_SEC	[5:0]	RW	0x0	0x00 - 0x3B: Alarm SECONDS Setting

Table 191: Register ALARM_MI

Address	Name	POR value	
0x009E	ALARM_MI	0x80	

7	6	5	4	3	2	1	0
TICK_TYPE	Reserved	ALARM_MIN					

Field name	Bits	Type	POR	Description
TICK_TYPE	[7]	RW	0x1	Tick Alarm Interval: Value: 0x0 – 0: One Second; 0x1 (POR) – 1: One Minute
ALARM_MIN	[5:0]	RW	0x0	0x00 - 0x3B: Alarm MINUTES Setting

Table 192: Register ALARM_H

Address	Name	POR value	
0x009F	ALARM_H	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ALARM_HOUR				

Field name	Bits	Type	POR	Description
ALARM_HOUR	[4:0]	RW	0x0	0x00 - 0x17: Alarm HOURS Setting

Table 193: Register ALARM_D

Address	Name	POR value	
0x00A0	ALARM_D	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	ALARM_DAY				

Field name	Bits	Type	POR	Description
ALARM_DAY	[4:0]	RW	0x1	0x01 - 0x1F: Alarm DAYS Setting

Table 194: Register ALARM_MO

Address	Name	POR value	
0x00A1	ALARM_MO	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ALARM_MONTH			

Field name	Bits	Type	POR	Description
ALARM_MONTH	[3:0]	RW	0x1	0x01 - 0x0C: Alarm MONTHS Setting

Table 195: Register ALARM_Y

Address	Name	POR value	
0x00A2	ALARM_Y	0x00	

7	6	5	4	3	2	1	0
TICK_ON	ALARM_ON	ALARM_YEAR					

Field name	Bits	Type	POR	Description
TICK_ON	[7]	RW	0x0	Enable tick function. Interval set by TICK_TYPE
ALARM_ON	[6]	RW	0x0	Enable alarm function
ALARM_YEAR	[5:0]	RW	0x0	0x00 - 0x3F: Alarm YEAR Setting (0 corresponds to year 2000). A write to this register latches the registers ALARM_SEC to ALARM_MONTH

Table 196: Register RTC_REG_3

Address	Name	POR value	
0x00A3	RTC_REG_3	0x00	

7	6	5	4	3	2	1	0
RTC_REGS_3							

Field name	Bits	Type	POR	Description
RTC_REGS_3	[7:0]	RW W1CL	0x0	8 bit register located in RTC VDD Domain

Table 197: Register RTC_REG_2

Address	Name	POR value	
0x00A4	RTC_REG_2	0x00	

7	6	5	4	3	2	1	0
RTC_REGS_2							

Field name	Bits	Type	POR	Description
RTC_REGS_2	[7:0]	RW W1CL	0x0	8 bit register located in RTC VDD Domain

Table 198: Register RTC_REG_1

Address	Name	POR value	
0x00A5	RTC_REG_1	0x00	

7	6	5	4	3	2	1	0
RTC_REGS_1							

Field name	Bits	Type	POR	Description
RTC_REGS_1	[7:0]	RW W1CL	0x0	8 bit register located in RTC VDD Domain

Table 199: Register RTC_REG_0

Address	Name	POR value	
0x00A6	RTC_REG_0	0x00	

7	6	5	4	3	2	1	0
RTC_REGS_0							

Field name	Bits	Type	POR	Description
RTC_REGS_0	[7:0]	RW W1CL	0x0	8 bit register located in RTC VDD Domain This is the trigger register which starts the transfer of all four registers.

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Table 200: Register CHIP_ID

Address	Name	POR value	
0x00A7	CHIP_ID	0x00	

7	6	5	4	3	2	1	0
MRC				TRC			

Field name	Bits	Type	POR	Description
MRC	[7:4]	RO	0x0	Read back of Mask Revision Code (MRC) Value: 0x0 (POR) = AA; 0x1 = AB
TRC	[3:0]	RO OTP	0x0	Read back of OTP Trimming Release Code (TRC) - starts with code 0

Table 201: Register CONFIG_ID

Address	Name	POR value	
0x00A8	CONFIG_ID	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	CONF_ID		

Field name	Bits	Type	POR	Description
CONF_ID	[2:0]	RO OTP	0x0	ID for Customer Variant of Start-up Voltages and Sequencer Configuration

Table 202: Register OTP_CONT

Address	Name	POR value	
0x00A9	OTP_CONT	0x00	

7	6	5	4	3	2	1	0
GP_WRITE_DIS	OTP_CONF_LOCK	Reserved	Reserved	OTP_CONF	Reserved	OTP_RP	OTP_TRANSFER

Field name	Bits	Type	POR	Description
GP_WRITE_DIS	[7]	RW OTP	0x0	GP_ID Registers Write Access Value: 0x0 (POR) — 0: Enables Write Access to GP_ID Registers Value: 0x1 — 1: Read Only GP_ID Registers Note: Write access for fusing only, control state is loaded from OTP defaults after POR
OTP_CONF_LOCK	[6]	RW OTP	0x0	OTP Lock Control: Value: 0x0 (POR) — 0: OTP Registers R10 to R106 Not Locked after Programming (only for unmarked evaluation samples) Value: 0x1 — 1: OTP registers R10 to R106 Locked during Programming (set for all marked parts, no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR
OTP_CONF	[3]	RW	0x0	Value: 0x0 (POR) — 0: No Action Value: 0x1 — 1: Transfer Includes Configuration R10 to R106 (plus OTP_CONF_LOCK)
OTP_RP	[1]	RW	0x0	OTP Transfer Type: Value: 0x0 (POR) — 0: Read Value: 0x1 — 1: Programming (Write)
OTP_TRANSFER	[0]	RW	0x0	OTP Status Indicator: Value: 0x0 (POR) — 0: Read-out - No Transfer in Progress (writing 1 to this bit initiates the fusing of selected OTP cells with the content from corresponding Value: 0x1 — 1: Read-out - Transfer in Progress

Table 203: Register OSC_TRIM

Address	Name	POR value	
0x00AA	OSC_TRIM	0x00	

7	6	5	4	3	2	1	0
TRIM_32K							

Field name	Bits	Type	POR	Description
TRIM_32K	[7:0]	RW OTP	0x0	32K Oscillator Frequency Control:

Value	Description
0x80	10000000: -244.1 ppm
...	...
0xFF	11111111: -1.9 ppm
0x0 (POR)	00000000: OFF
0x1	00000001: 1.9 ppm (1/(32768*16))
...	...
0x7F	01111111: 242.2 ppm

Table 204: Register GP_ID_0

Address	Name	POR value	
0x00AB	GP_ID_0	0x00	

7	6	5	4	3	2	1	0
GP_0							

Field name	Bits	Type	POR	Description
GP_0	[7:0]	RW	0x0	General Purpose Data

Table 205: Register GP_ID_1

Address	Name	POR value	
0x00AC	GP_ID_1	0x00	

7	6	5	4	3	2	1	0
GP_1							

Field name	Bits	Type	POR	Description
GP_1	[7:0]	RW	0x0	General Purpose Data

Table 206: Register GP_ID_2

Address	Name	POR value	
0x00AD	GP_ID_2	0x00	

7	6	5	4	3	2	1	0
GP_2							

Field name	Bits	Type	POR	Description
GP_2	[7:0]	RW	0x0	General Purpose Data

Table 207: Register GP_ID_3

Address	Name	POR value	
0x00AE	GP_ID_3	0x00	

7	6	5	4	3	2	1	0
GP_3							

Field name	Bits	Type	POR	Description
GP_3	[7:0]	RW OTP	0x0	General Purpose Data from Fuse Array (OTP)

Table 208: Register GP_ID_4

Address	Name	POR value	
0x00AF	GP_ID_4	0x00	

7	6	5	4	3	2	1	0
GP_4							

Field name	Bits	Type	POR	Description
GP_4	[7:0]	RW OTP	0x0	General Purpose Data from Fuse Array (OTP)

Table 209: Register GP_ID_5

Address	Name	POR value	
0x00B0	GP_ID_5	0x00	

7	6	5	4	3	2	1	0
GP_5							

Field name	Bits	Type	POR	Description
GP_5	[7:0]	RW OTP	0x0	General Purpose Data from Fuse Array (OTP)

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Table 210: Register GEN_CONF_0

Address	Name	POR value	
0x00B1	GEN_CONF_0	0x00	

7	6	5	4	3	2	1	0
ADCIN_SEL							

Field name	Bits	Type	POR	Description	
ADCIN_SEL	[7:0]	RW OTP	0x0	**Value**	**Description**
				1:0	00:adcin_1, 01:adcin_2, 10:adcin_3, 11:adcin_4
				7:2	reserved

Table 211: Register GEN_CONF_1

Address	Name	POR value	
0x00B2	GEN_CONF_1	0x00	

7	6	5	4	3	2	1	0
GPO_CTRL							

Field name	Bits	Type	POR	Description	
GPO_CTRL	[7:0]	RW OTP	0x0	GPO Output Level Control	
				Value	**Description**
				0:0	gpo0_out
				1:1	gpo1_out
				2:2	gpo2_out
				7:3	reserved

Table 212: Register BUCK0_CONF5

Address	Name	POR value	
0x0129	BUCK0_CONF5	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK0_IAUTSLP			

Field name	Bits	Type	POR	Description
BUCK0_IAUTSLP	[3:0]	RW OTP	0x0	BUCK Auto Sleep Sync to Sleep Threshold: Value: 0x0 (POR) — 0000: 64 mA 0x1 — 0001: 128 mA ... — ... 0xE — 1110: 960 mA 0xF — 1111: 1024 mA

Table 213: Register BUCK1_CONF5

Address	Name	POR value	
0x0134	BUCK1_CONF5	0x00	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	BUCK1_IAUTSLP			

Field name	Bits	Type	POR	Description
BUCK1_IAUTSLP	[3:0]	RW OTP	0x0	BUCK1 Auto Sleep Threshold: Value: 0x0 (POR) — 0000: 64 mA 0x1 — 0001: 128 mA ... — ... 0xE — 1110: 960 mA 0xF — 1111: 1024 mA

Table 214: Register BUCK7_PDDIS_EXT_CTRL_32K

Address	Name	POR value	
0x015B	BUCK7_PDDIS_EXT_CTRL_32K	0x00	

7	6	5	4	3	2	1	0
buck7_pddis_ext_ctrl_32k							

Field name	Bits	Type	POR	Description
buck7_pddis_ext_ctrl_32k	[7:0]	RW OTP	0x0	Spares

Value	Description
1:0	reserved
2:2	OUT32K_EXTCTR_EN
4:3	reserved
5:5	BUCK7_PD_DIS
7:6	reserved

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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