High-Performance Multi-Phase DC-DC Buck Converter

General Description

DA9092 is a high-performance Power Management IC suitable for supplying high-current rails in CPUs, GPUs, SOCs in multiple end-applications. The device is capable of supporting up to 52 A of peak current in a compact offering, with fully integrated power devices.

DA9092 can be configured as either a 20 A quad-phase buck converter or two 10 A dual-phase buck converters. The input voltage range of 2.2 V to 5.5 V makes it suited for a wide range of low voltage systems, including all single cell battery powered systems. The DA9092 is optimized for a very small footprint – each phase will only need a 0.10 µH inductor. The output voltage is programmable from 0.3 V to 1.275 V in 5 mV steps. If higher output voltage is desired, the output voltage can be programmed from 0.6 V to 1.9 V in 10 mV steps.

To guarantee the highest accuracy and support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented in DA9092.

The pass devices are fully integrated, so no external FETs or Schottky diodes are needed.

A soft start-up is implemented, which limits the inrush current from the input node and secures a slope-controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, either via direct register write through the communication interface (I^2C compatible) or via an external input pin (VSEL).

DA9092 implements integrated over-temperature and over-current protections for increased system reliability, without the need for external sensing components.

The configurable I^2C slave ID selection via CONF allows multiple instances of DA9092 to be placed in the application sharing the same communication interface with different addresses.

Key Features

- 2.2 V to 5.5 V input voltage
- Selectable output voltage range:
  - 0.3 V to 1.275 V, 5 mV step
  - 0.6 V to 1.9 V, 10 mV step
- 1x 20 A quad-phase converter (52 A peak output current)
- 2x 10 A dual-phase converters (26 A peak output current)
- 3 MHz nominal switching frequency
- ±1 % accuracy (static)
- Fast transient response
- Dynamic voltage control (DVC)
- Automatic phase shedding
- Integrated power switches
- Remote sensing at point of load
- I^2C compatible interface
- Support 1.8 V level GPI input
- Adjustable soft-start
- -40 °C to +85 ºC Temperature range
- Package 6x9 WLCSP 2.48 mm x 3.68 mm (0.4 mm pitch)

Applications

- Game console
- Smartphones
- Tablet PCs
- Mobile computing

System Diagram

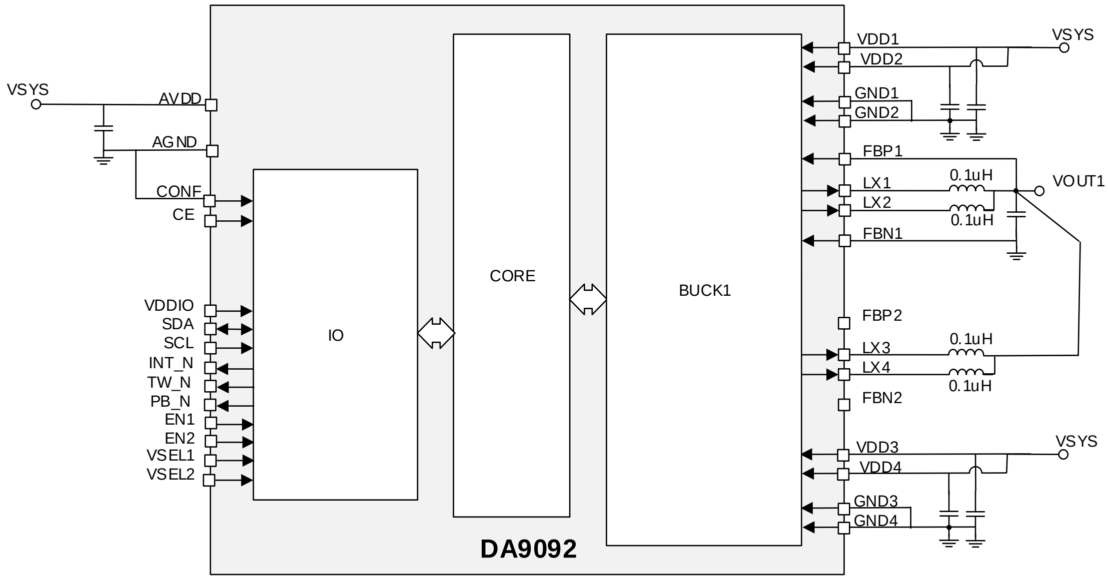

Figure 1: 1-Channel Quad-Phase Configuration Simplified Schematic Diagram

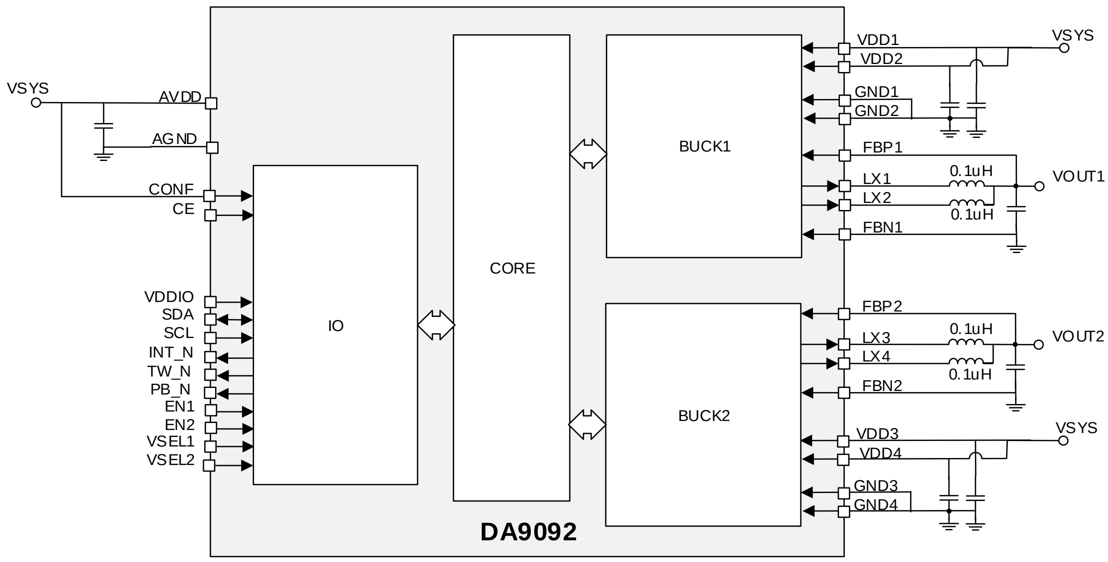

Figure 2: 2-Channel Dual-Phase Configuration Simplified Schematic Diagram

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1 Terms and Definitions

ATE	Automated test equipment
CPU	Central processing unit
DDR	Dual data rate
DVC	Dynamic voltage control
FET	Field effect transistor
FM+	Fast mode plus
GBD	Guaranteed by design
GBQ	Guaranteed by qualification
GBSPC	Guaranteed by statistical process characterization
GPI	General purpose input
GPIO	General purpose input/output
GPU	Graphics processing unit
IC	Integrated circuit
HW	Hardware
Li-Ion	Lithium-ion
OTP	One time programmable
OV	Over-voltage
PCB	Printed circuit board
PRS	Product requirements specification
SCL	Serial clock
SDA	Serial data
SIPP	Single in-line pin package
SoC	System on chip
SW	Software
UV	Under-voltage
UVLO	Under-voltage lockout

2 Pinout

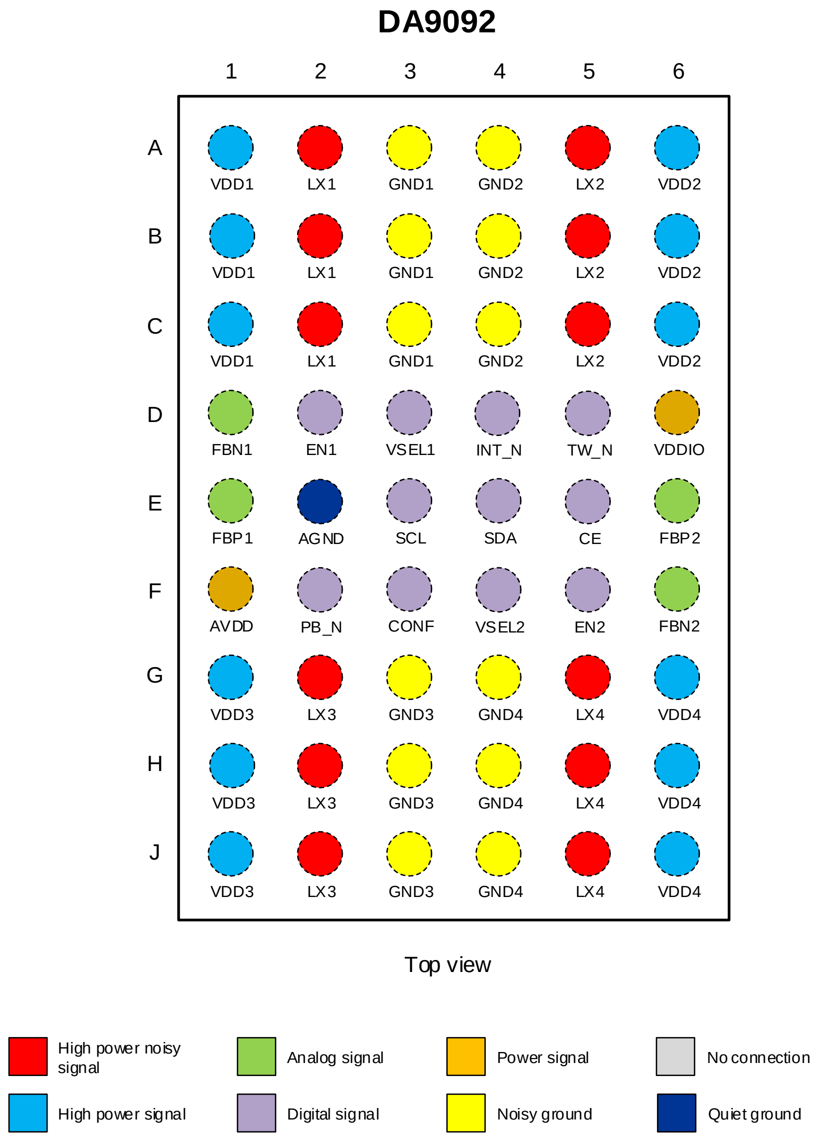


Figure 3: DA9092 Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Drive (mA)	Description
A1, B1, C1	VDD1	PWR	5000	Power supply for phase1
A2, B2, C2	LX1	AIO	5000	LX node of phase1
A3, B3, C3	GND1	GND	5000	Power ground of phase1
A4, B4, C4	GND2	GND	5000	Power ground of phase2
A5, B5, C5	LX2	AIO	5000	LX node of phase2
A6, B6, C6	VDD2	PWR	5000	Power supply for phase2
D1	FBN1	AI	10	Negative remote sense input for CH1
D2	EN1	DI	10	Enable/disable input of CH1
D3	VSEL1	DI	10	External voltage control pin of CH1

Pin #	Pin Name	Type (Table 2)	Drive (mA)	Description
D4	INT_N	DOD	10	Interrupt output, active low
D5	TW_N	DOD	10	Thermal warning output, active low
D6	VDDIO	PWR	15	Power supply for IO
E1	FBP1	AI	10	Positive remote sense input of CH1
E2	AGND	GND	15	Ground of internal analog circuitry
E3	SCL	DI	15	I^2C clock
E4	SDA	DIOD	15	I^2C data
E5	CE	DI	10	Chip enable
E6	FBP2	AI	10	Positive remote sense input of CH2
F1	AVDD	PWR	10	Power supply for internal analog circuitry
F2	PB_N	DOD	10	Power-bad output, active low
F3	CONF	DI	10	Configuration mode select (1Ch-4Ph or 2Ch-2Ph+2Ph)
F4	VSEL2	DI	10	External voltage control pin of CH2
F5	EN2	DI	10	Enable/disable input of CH2
F6	FBN2	AI	10	Negative remote sense input of CH2
G1, H1, J1	VDD3	PWR	5000	Power supply for phase3
G2, H2, J2	LX3	AIO	5000	LX node of phase3
G3, H3, J3	GND3	GND	5000	Power ground of phase3
G4, H4, J4	GND4	GND	5000	Power ground of phase4
G5, H5, J5	LX4	AIO	5000	LX node of phase4
G6, H6, J6	VDD4	PWR	5000	Power supply for phase4

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DOD	Digital output open drain	AO	Analog output
DIOD	Digital input/output open drain	AIO	Analog input/output
PWR	Power	GND	Ground

3 Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{STG}	Storage temperature		-65		150	°C
T_J	Junction temperature		-40		150	°C
V_{PIN}	Voltage on pins		-0.3		6	V

3.2 Electrostatic Discharge Ratings

Table 4: Electrostatic Discharge Ratings

Parameter	Description	Conditions	Value	Unit
ESD_{HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	2	kV
ESD_{CDM}	Maximum ESD protection	Charged device model (CDM)	0.5	kV

3.3 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Description	Conditions Note 1	Min	Typ	Max	Unit
V_{IN}	System supply voltage VDD, AVDD		2.2	3.7	5.5	V
V_{VDDIO}	I/O supply voltage Note 2		1.62	1.8	1.98	V
V_{SEL_I2C}	Voltage on VSEL1, VSEL2, SDA, SCL		-0.3		5.5	V
V_{OD}	Voltage on open drain pins INT_N, TW_N, PB_N		-0.3		VVDDIO+0.3	V
V_{PIN}	Voltage on other pins		-0.3		VIN+0.3	V
T_J	Junction temperature		-40		125	°C
T_A	Ambient temperature		-40		85	°C

Note 1 Within the specified limits, a lifetime of 10 years is guaranteed. If operating outside of these recommended conditions, please consult with Renesas Electronics.

Note 2 V_{VDDIO} is 3.3 V compatible as long as V_{IN} is ≥ 3.3 V.

3.4 Thermal Characteristics

Table 6: Thermal Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{θ_JA}	Package thermal resistance Note 1			25.1		°C/W
P_D	Power dissipation	Derating factor above T_A = 70 °C: 39.8 mW/°C		2786		mW

Note 1 Obtained from package thermal simulation, 2S2P 4L board (JEDEC), influenced by PCB technology and layout.

3.5 Buck Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.2 V ≤ V_{IN} ≤ 5.5 V, f_{sw} = 3 MHz.

Table 7: Quad-Phase Buck Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External electrical conditions						
C_{OUT}	Output capacitance, including voltage and temperature coefficient	Per phase	-40%	3~5 *10	+30%	µF
ESR_{COUT}	Output capacitor series resistance, per capacitor	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence	Per phase	-50%	100	+20%	nH
DCR_L	Inductor DC resistance	Per phase		4		mΩ
Electrical performance						
V_{OUT}	Output voltage	Satisfy $V_{DROPOUT}$ spec Programmable in 5 mV steps (CH<x>_VSTEP = 0)	0.3		1.275	V
$V_{DROPOUT}$	Dropout voltage (Voltage difference between input and output)	At I_{OUT_MAX} For V_{OUT}			1.2	V
$V_{OUT\_ACC\_DC\_25C}$	Static voltage accuracy of output voltage (in PWM mode)	V_{OUT} < 1.0 V, T_A = 25 °C, No load	-5		5	mV
$V_{OUT\_ACC\_DC2\_25C}$	Static voltage accuracy of output voltage (in PWM mode)	V_{OUT} ≥ 1.0 V, T_A = 25 °C, No load	-0.5		0.5	%
$V_{OUT\_ACC\_DC}$	Static voltage accuracy of output voltage (in PWM mode)	V_{OUT} < 1.0 V Including load and line regulation	-10		10	mV
$V_{OUT\_ACC\_DC2}$	Static voltage accuracy of output voltage (in PWM mode)	V_{OUT} ≥ 1.0 V Including load and line regulation	-1		1	%
V_{THR_OV}	Over-voltage threshold (no hysteresis)	Delta from target V_{OUT}	100	150	200	mV
$V_{THR\_UV\_RISE}$	Under-voltage threshold (rise)	Delta from target V_{OUT}	-80	-50	-20	mV
$V_{THR\_UV\_FALL}$	Under-voltage threshold (fall)	Delta from target V_{OUT}	-200	-150	-100	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OUT2}	Output voltage	Satisfy $V_{DROPOUT2}$ spec 1 phase operation (CH<x>_MAXPH_VSEL_HI/ LO =0x0) Programmable in 10 mV steps (CH<x>_VSTEP = 1) V_{IN} ≥ 2.5 V Note 1	0.6		1.9	V
V_{OUT2_LV}	Output voltage	Satisfy $V_{DROPOUT2\_LV}$ spec 1 phase operation (CH<x>_MAXPH_VSEL_HI/ LO =0x0) Programmable in 10 mV steps (CH<x>_VSTEP = 1) Note 1	0.6		1.5	V
$V_{DROPOUT2}$	Dropout voltage (voltage difference between input and output)	At I_{OUT_MAX} For V_{OUT2} V_{IN} ≥ 2.5 V			0.6	V
$V_{DROPOUT2\_LV}$	Dropout voltage (voltage difference between input and output)	At I_{OUT_MAX} For V_{OUT2_LV}			0.7	V
$V_{OUT2\_ACC\_DC}$	Static voltage accuracy of output voltage (in PWM mode)	For V_{OUT2} Including load and line regulation	-20		20	mV
V_{THR_OV2}	Over-voltage threshold (no hysteresis)	Delta from target V_{OUT2}	200	300	400	mV
$V_{THR\_UV\_RISE2}$	Under-voltage threshold (rise)	Delta from target V_{OUT2}	-160	-100	-40	mV
$V_{THR\_UV\_FALL2}$	Under-voltage threshold (fall)	Delta from target V_{OUT2}	-400	-300	-200	mV
I_{OUT_MAX}	Maximum output current	Per phase	5			A
$I_{OUT\_MAX\_PK}$	Maximum output current during transient	Per phase	13			A
I_{LIM}	Current limit, programmable per phase Note 2	Adjustable with 2.5 A step	7.5	17.5	22.5	A
I_{LIM_ACC}	Current limit accuracy Note 2	V_{IN} ≥ 2.7 V	-15		20	%
I_{LIM_ACC2}	Current limit accuracy Note 2	V_{IN} < 2.7 V and CH<x>_ILIM = 0x0~0x4	-15		20	%
I_{LIM_ACC3}	Current limit accuracy Note 2	V_{IN} < 2.7 V and CH<x>_ILIM = 0x5	17.5 * 85%		20 * 120%	A

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{LIM_ACC4}	Current limit accuracy Note 2	V_{IN} < 2.7 V and CH<x>_ILIM = 0x6	17.5 * 85%		22.5 * 120%	A
f_{SW}	Switching frequency	V_{IN} ≥ 2.5 V	2.85	3	3.15	MHz
f_{SW2}	Switching frequency	V_{IN} < 2.5 V	2.7	3	3.3	MHz
t_{ON_MIN}	Minimum turn-on pulse 0 % duty is also supported			20		ns
t_{BUCK_EN}	Turn-on time	From EN<x> = 1 to switching start			50	µs
R_{PD_LX}	Output pull-down resistance for each phase at LX node	V_{IN} = 3.7 V V_{LX} = 0.5 V Per phase	70	100	130	Ω
R_{ON_PMOS}	On resistance of switching PMOS	V_{IN} = 3.7 V Per phase		19		mΩ
R_{ON_NMOS}	On resistance of switching NMOS	V_{IN} = 3.7 V Per phase		6		mΩ
PFM Mode						
$I_{Q\_PFM\_1PH}$	Quiescent current in PFM	V_{IN} = 3.7 V No load AVDD current		500		µA
$I_{Q\_PFM\_1PH\_25k}$	Quiescent current in PFM with audible noise reduction	V_{IN} = 3.7 V No load AVDD current		500		µA

Note 1 Multi-phase operation (CH<x>_MAXPH_VSEL_HI/LO =0x0) is not guaranteed.

Note 2 t_{ON} > 40 ns

3.6 Performance and Supervision Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.2 V ≤ V_{IN} ≤ 5.5 V

Table 8: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{UVLO_RL}	UVLO release voltage		2.2	2.25	2.3	V
V_{UVLO}	UVLO lock-out voltage		2.1	2.15	2.2	V
T_{WARN}	Temperature warning threshold	TEMP_WARN_SEL = 0x0	115	125	135	°C
T_{CRIT}	Temperature shutdown threshold		130	140	150	°C
I_{IN_OFF}	Supply current chip disable	Off state T_A = 27 °C CE = 0		0.2	2	µA
I_{IN_STB}	Supply current stand-by mode	On state T_A = 27 °C CE = 1 Buck off	5	10	20	µA

3.7 Digital I/O Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.2 V ≤ V_{IN} ≤ 5.5 V

Table 9: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IH_CONF}	Input high voltage, CONF		0.75*AVDD		AVDD	V
V_{IL_CONF}	Input low voltage, CONF				0.25*AVDD	V
t_{IC_EN}	IC enable time				1000	µs
V_{IH}	Input high voltage, except CONF		0.75*VVDDIO		VVDDIO	V
V_{IL}	Input low voltage, except CONF				0.25*VVDDIO	V
V_{OL}	Output low voltage SDA, INT_N, TW_N,PB_N	Open drain I_{OUT} = 1 mA			0.2*VVDDIO	V
I_{OD_LKG}	Output leak current SDA, INT_N, TW_N,PB_N	Open drain Output is Hi-Z V_{OUT} = V_{VDDIO}			100	nA
R_{PD}	Pull-down resistor, VSEL<x>, EN<x>		50	100	150	kΩ

3.8 Timing Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 2.2 V ≤ V_{IN} ≤ 5.5 V

Table 10: I2C Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{BUS}	Bus free time between a STOP and START condition		0.5			µs
C_{BUS}	Bus line capacitive load				550	pF
f_{SCL}	SCL clock frequency		0		1000	kHz
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE_STD}	SCL and SDA rise time	Requirement for input Standard mode			1000	ns
t_{RISE_FAST}	SCL and SDA rise time	Requirement for input Fast mode			300	ns
t_{RISE_FPLUS}	SCL and SDA rise time	Requirement for input Fast mode plus			120	ns
t_{FALL_STD}	SCL and SDA fall time	Requirement for input Standard mode			1000	ns
t_{FALL_FAST}	SCL and SDA fall time	Requirement for input Fast mode	20*VVDDIO/5.5		300	ns
t_{FALL_FPLUS}	SCL and SDA fall time	Requirement for input Fast mode plus	20*VVDDIO/5.5		120	ns
t_{SETUP_START}	Start condition setup time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{SETUP_STOP}	Stop condition setup time		0.26			µs
t_{DATA}	Data valid time				0.45	µs
t_{SETUP_DATA}	Data setup time		50			ns
t_{DATA_ACK}	Data valid acknowledge time				0.45	µs
t_{HOLD_DATA}	Data hold time		0			ns

3.9 Typical Buck Performance

Unless otherwise noted, the operating conditions are: T_A = 25 °C, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, f_{sw} = 3 MHz, L = 100 nH, C_{OUT} = 10 x 10 µF (per phase), and Mode = AUTO.

NOTE
AUTO = Automatic transitions between single and full phase, and between synchronous PWM mode and PFM. PWM = PWM with phase-shedding.

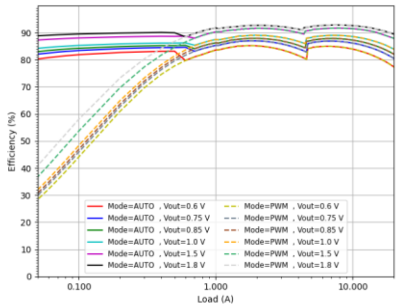


Figure 4: 4-Phase Efficiency (V_{IN} = 3.3 V)

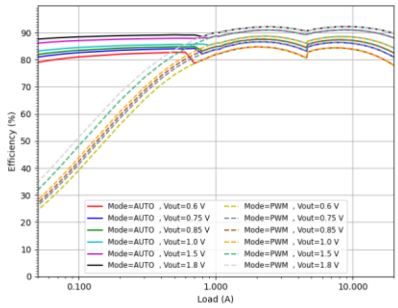


Figure 5: 4-Phase Efficiency (V_{IN} = 3.8 V)

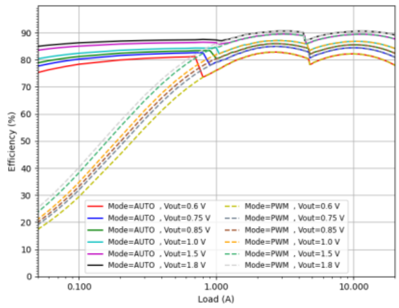


Figure 6: 4-Phase Efficiency (V_{IN} = 5.0 V)

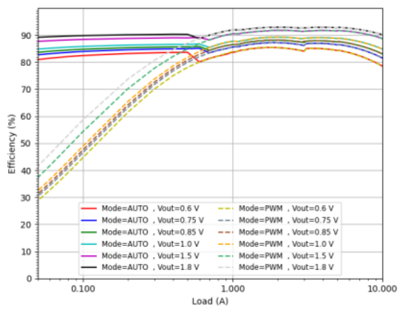


Figure 7: 2-Phase Efficiency (V_{IN} = 3.3 V)

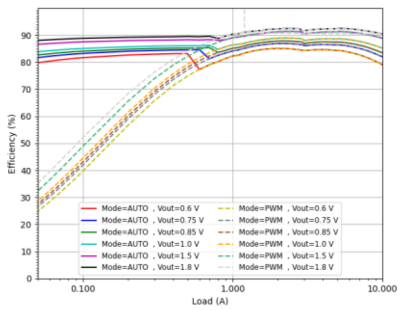


Figure 8: 2-Phase Efficiency (V_{IN} = 3.8 V)

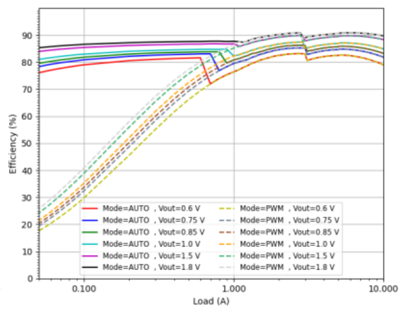


Figure 9: 2-Phase Efficiency (V_{IN} = 5.0 V)

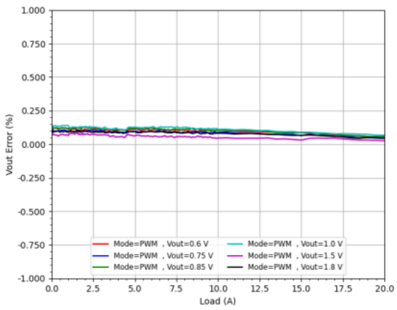


Figure 10: 4-Phase Load Regulation (V_{IN} = 3.3 V)

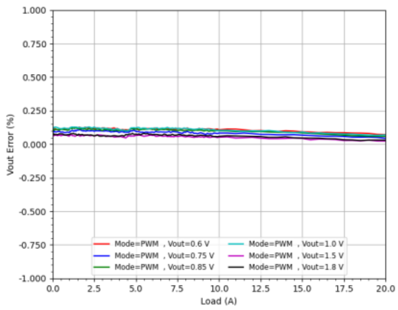


Figure 11: 4-Phase Load Regulation (V_{IN} = 3.8 V)

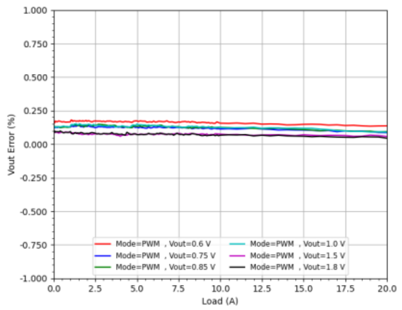


Figure 12: 4-Phase Load Regulation (V_{IN} = 5.0 V)

Unless otherwise noted, the operating conditions are: T_A = 25 °C, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, f_{SW} = 3 MHz, L = 100 nH, C_{OUT} = 10 x 10 µF (per phase), and Mode = AUTO.

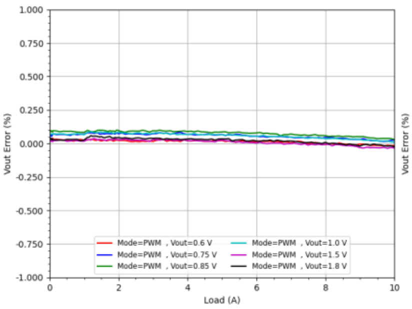


Figure 13: 2-Phase Load Regulation (V_{IN} = 3.3 V)

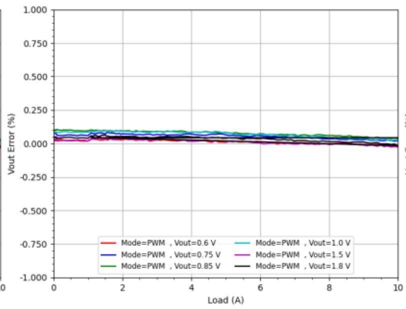


Figure 14: 2-Phase Load Regulation (V_{IN} = 3.8 V)

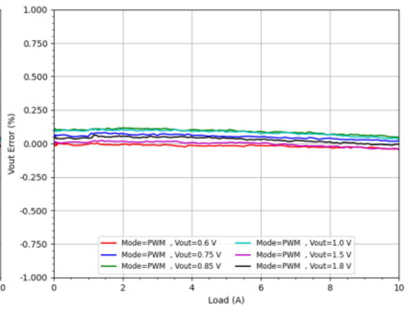


Figure 15: 2-Phase Load Regulation (V_{IN} = 5.0 V)

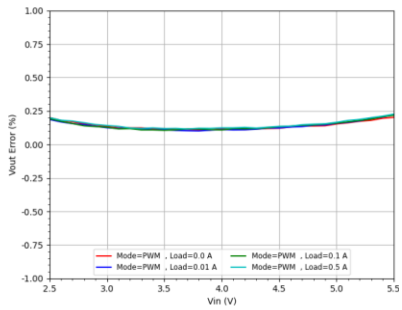


Figure 16: 4-Phase Line Regulation (V_{OUT} = 0.6 V)

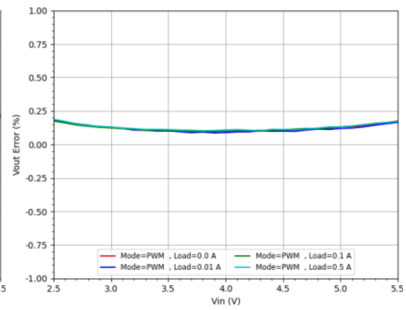


Figure 17: 4-Phase Line Regulation (V_{OUT} = 0.75 V)

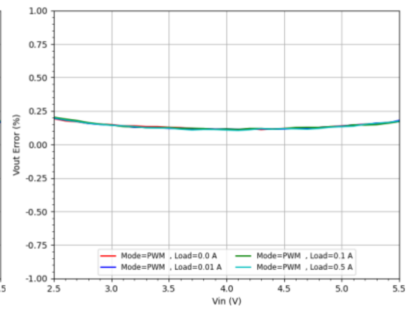


Figure 18: 4-Phase Line Regulation (V_{OUT} = 0.85 V)

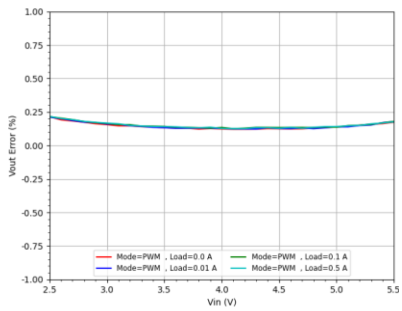


Figure 19: 4-Phase Line Regulation (V_{OUT} = 1.0 V)

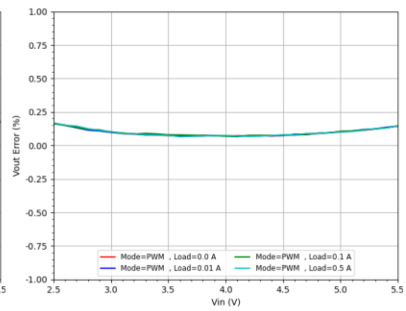


Figure 20: 4-Phase Line Regulation (V_{OUT} = 1.5 V)

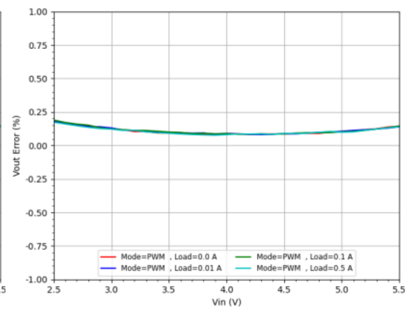


Figure 21: 4-Phase Line Regulation (V_{OUT} = 1.8 V)

Unless otherwise noted, the operating conditions are: T_A = 25 °C, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, f_{SW} = 3 MHz, L = 100 nH, C_{OUT} = 10 x 10 µF (per phase), and Mode = AUTO.

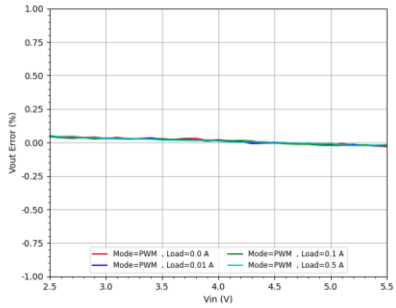


Figure 22: 2-Phase Line Regulation (V_{OUT} = 0.6 V)

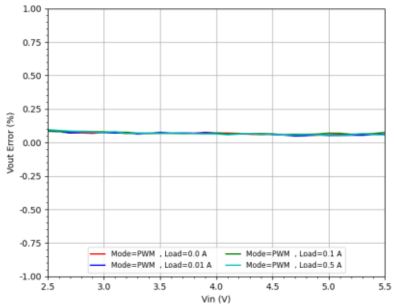


Figure 23: 2-Phase Line Regulation (V_{OUT} = 0.75 V)

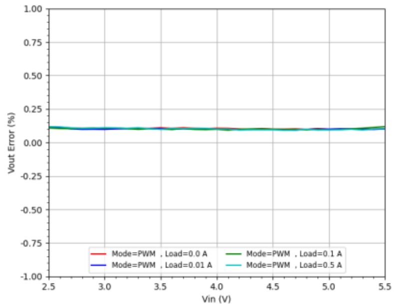


Figure 24: 2-Phase Line Regulation (V_{OUT} = 0.85 V)

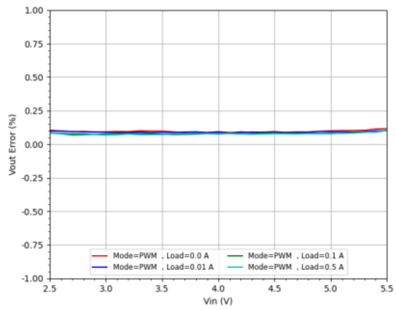


Figure 25: 2-Phase Line Regulation (V_{OUT} = 1.0 V)

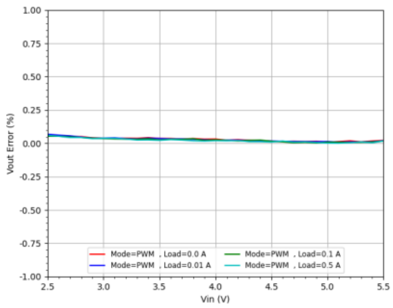


Figure 26: 2-Phase Line Regulation (V_{OUT} = 1.5 V)

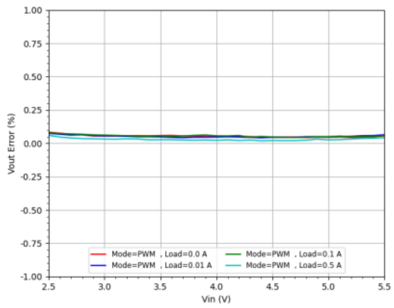


Figure 27: 2-Phase Line Regulation (V_{OUT} = 1.8 V)

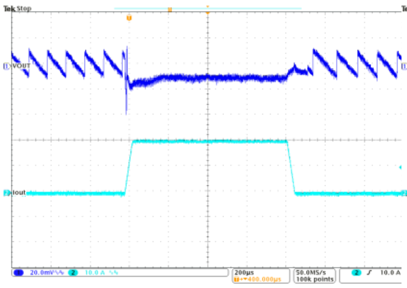


Figure 28: 4-Phase Load Transient (0.1 A to 20 A, 0.5 A/µs)

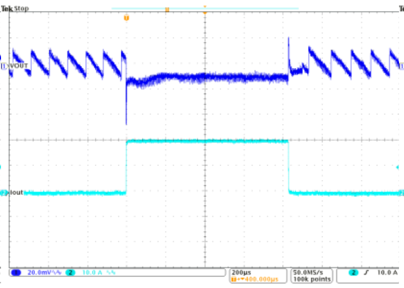


Figure 29: 4-Phase Load Transient (0.1 A to 20 A, 10 A/µs)

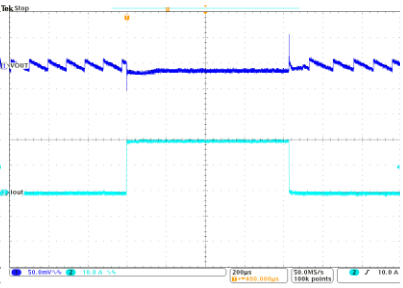


Figure 30: 4-Phase Load Transient (0.1 A to 20 A, 25 A/µs)

Unless otherwise noted, the operating conditions are: T_A = 25 °C, V_{IN} = 3.8 V, V_{OUT} = 1.1 V, f_{SW} = 3 MHz, L = 100 nH, C_{OUT} = 10 x 10 µF (per phase), and Mode = AUTO.

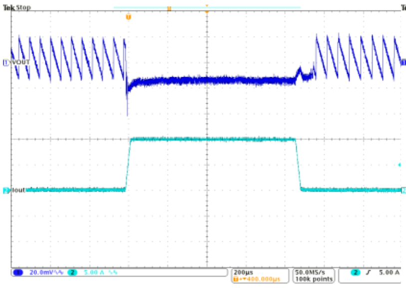


Figure 31: 2-Phase Load Transient (0.1 A to 10 A, 0.5 A/µs)

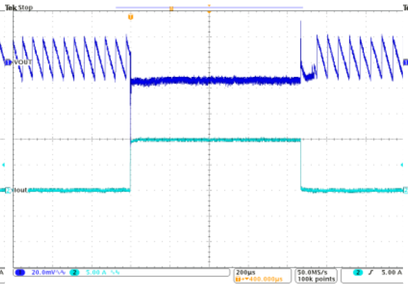


Figure 32: 2-Phase Load Transient (0.1 A to 10 A, 10 A/µs)

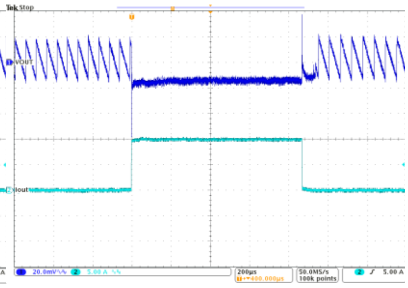


Figure 33: 2-Phase Load Transient (0.1 A to 10 A, 25 A/µs)

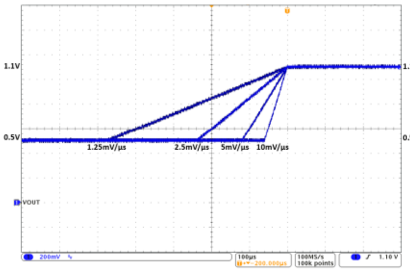


Figure 34: 2/4-Phase DVC (V_{OUT} = 0.5 V to 1.1 V, I_{OUT} = 10 A)

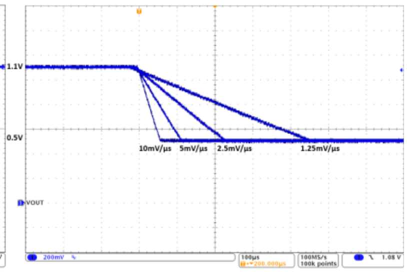


Figure 35: 2/4-Phase DVC (V_{OUT} = 1.1 V to 0.5 V, I_{OUT} = 10 A)

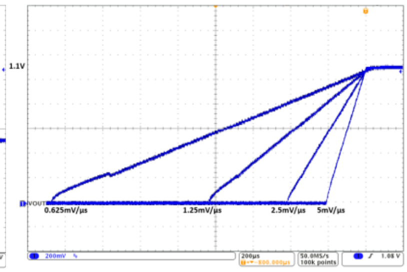


Figure 36: 2/4-Phase Soft-Start Slew-Rates (I_{OUT} = 0 A)

4 Functional Description

4.1 DC-DC Buck Converter

DA9092 operates as a single quad-phase buck converter when CONF is pulled down to GND and it operates as two dual-phase buck converters when CONF is pulled up to AVDD or floating (HiZ).

CONF can also be used to configure different I^{2}C slave IDs. It allows multiple DA9092 to be placed in the application sharing the same communication interface.

Output voltage is programmable in 5 mV steps in the range of 0.3 V to 1.275 V, or in 10 mV steps in the range of 0.6 V to 1.9 V by setting CH<x>_VSTEP to 1 (Note 1). The buck converter has two output voltage registers. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way, different application power modes can easily be supported. The output voltage selection can be operated either via external pin VSEL<x> or via I^{2}C interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored, and a power-good signal indicates that the buck output voltage has reached a level higher than the $V_{THR\_UV\_RISE}$ threshold. The power-good status is lost when the voltage drops below $V_{THR\_UV\_FALL}$ or rises above V_{THR_OV}. The status of the power good indicator can be read back via I^{2}C from the S_CH<x>_PG status bit. Output voltage UV and OV status can also be read back via I^{2}C from S_CH<x>_UV and S_CH<x>_OV status bit, respectively.

Note 1 The buck converter needs to be disabled (CH<x>_EN = 0) before CH<x>_VSTEP setting can be changed by I^{2}C write.

Table 11: An Example of Chip Configuration via CONF

		Chip1	Chip2	Chip3
CONF		**GND**	**AVDD**	**HiZ**
Configuration Mode		**1Ch-4Ph**	**2Ch-2Ph+2Ph**	**2Ch-2Ph+2Ph**
I^{2}C Slave ID (8-bit)		0xD2	0xD4	0xD6
VSEL1	Enable	Off	On	On
	Internal pull-down	Off	Off	Off
VSEL2	Enable	N/A	Off	Off
	Internal pull-down	On	Off	Off
EN1	Enable	On	On	On
	Internal pull-down	On	On	On
EN2	Enable	N/A	On	On
	Internal pull-down	On	On	On
CH1_VSTEP		5 mV	5 mV	5 mV
CH2_VSTEP		N/A	5 mV	5 mV
TW_N		TW	TW	TW
PB_N		PB of CH1	PB of CH1	PB of CH1

		VSEL	Chip1	Chip2	Chip3
CH1	VOUT	0	0.815 V	0.815 V	0.815 V
		1	0.815 V	0.815 V	0.815 V
	MAXPH	0	4	2	2

		VSEL	Chip1	Chip2	Chip3
		1	4	2	2
	MODE	0	AUTO	AUTO	AUTO
		1	AUTO	AUTO	AUTO
CH2	VOUT	0	N/A	0.815 V	0.815 V
		1		0.815 V	0.815 V
	MAXPH	0		2	2
		1		2	2
	MODE	0		AUTO	AUTO
		1		AUTO	AUTO

4.1.1 Buck Enable and Disable

The buck converter can be enabled by setting CH<x>_EN register bit to 1 or by toggling the external pin EN<x> from low to high.

EN<x>_EN = 1 indicates that the functionality of external pin EN<x> to control buck enable/disable is enabled. The functionality of external pin EN<x> is disabled by writing 0 to EN<x>_EN register bit.

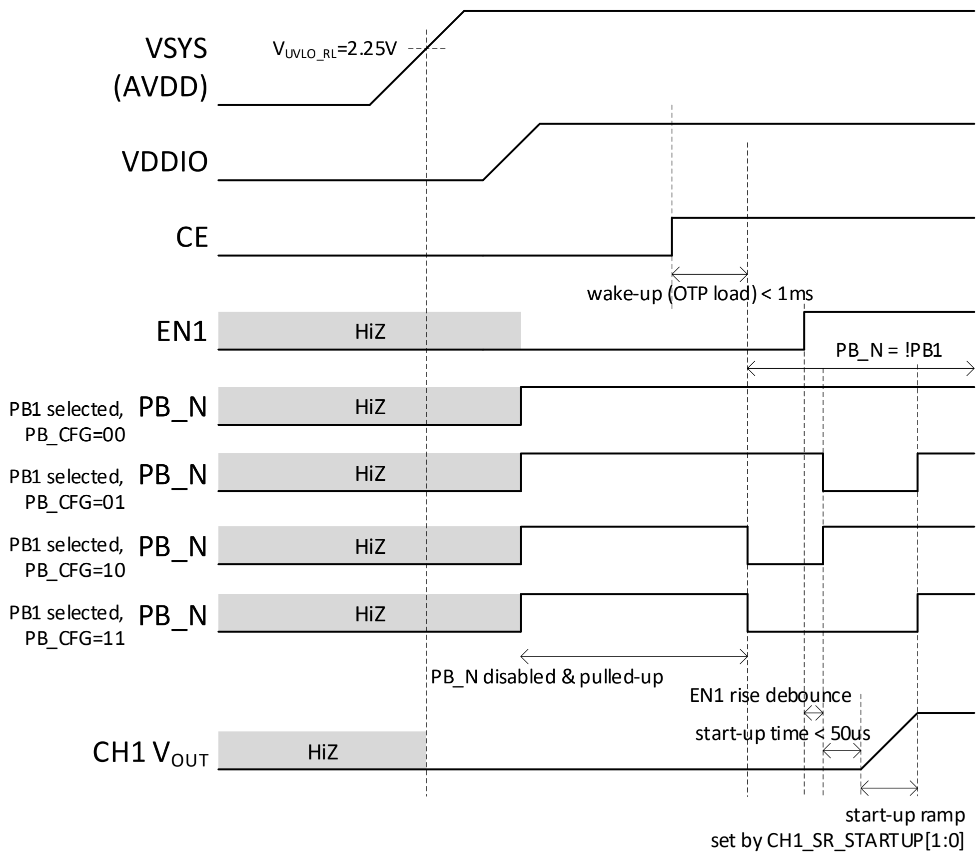


Figure 37: CH1 Start-Up Diagram (EN1_EN = 1)

The buck converter is disabled by writing 0 to CH<x>_EN or by toggling the external pin EN<x> from high to low. An internal output pull-down resistor at LX is enabled when CH<x>_EN = 0, unless it is disabled via CH<x>_DIS_PD.

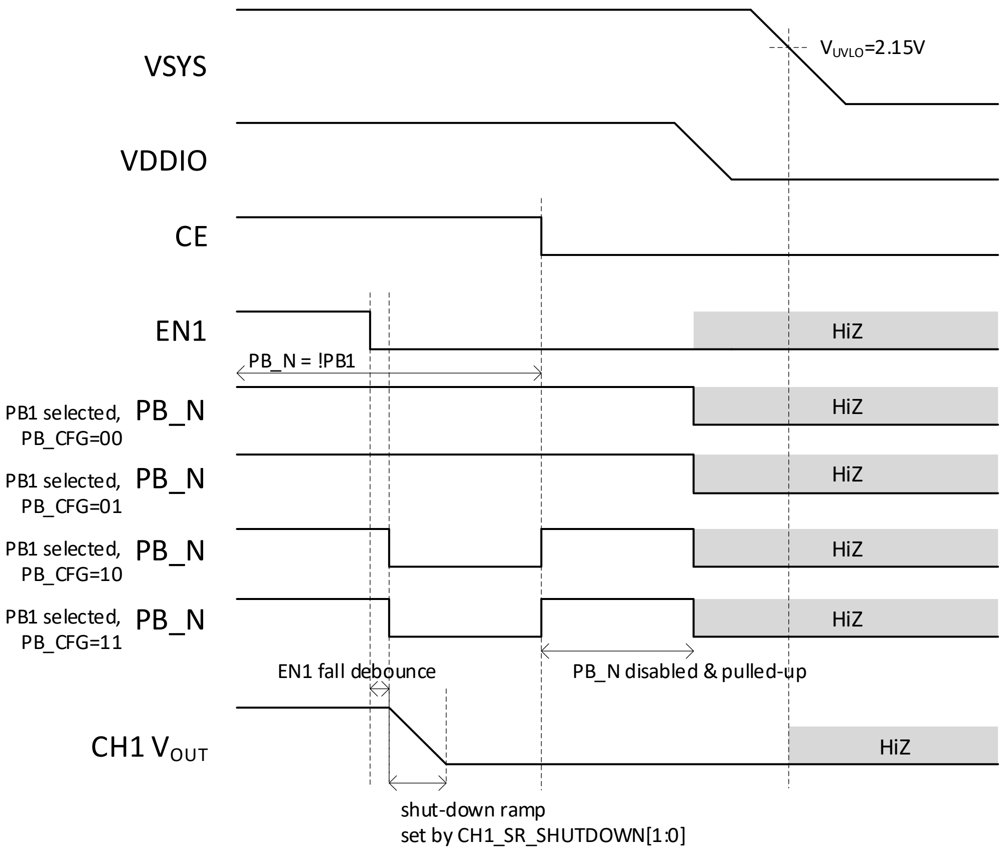


Figure 38: CH1 Shutdown Diagram (EN1_EN = 1)

4.1.2 Output Voltage Selection

For each buck converter two output voltages can be pre-configured inside CH<x>_VOUT_VSEL_LO and CH<x>_VOUT_VSEL_HI registers. The pre-configured output voltage setting can be selected by either toggling the external pin VSEL<x> or by changing the value of CH<x>_VSEL register bit.

Functionality of external pin VSEL<x> to select output voltage setting is disabled by writing 0 to VSEL<x>_EN register bit. Figure 39 and Figure 40 show interaction behaviors of external pin VSEL<x>, registers VSEL<x>_EN and CH<x>_VSEL in two different scenarios.

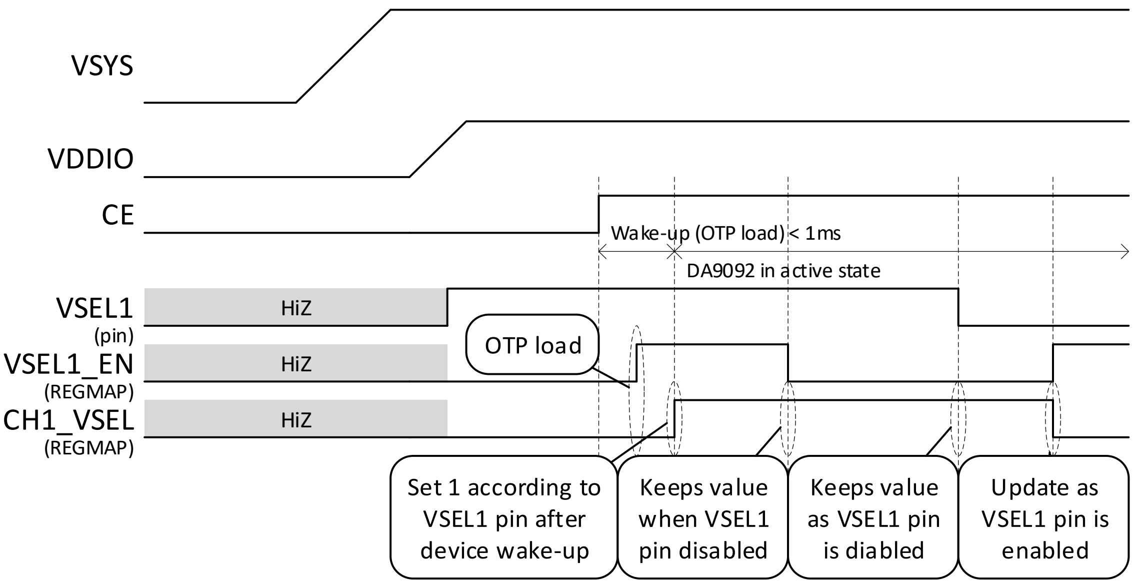


Figure 39: VSEL1 Pin, VSEL1_EN and CH1_VSEL Diagram (Scenario 1)

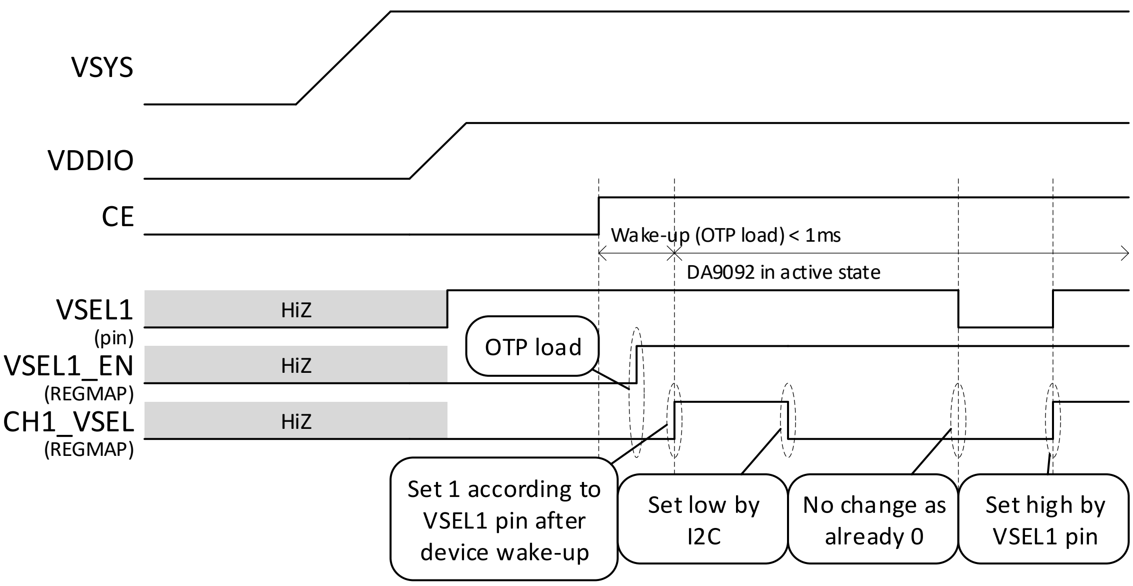


Figure 40: VSEL1 Pin, VSEL1_EN and CH1_VSEL Diagram (Scenario 2)

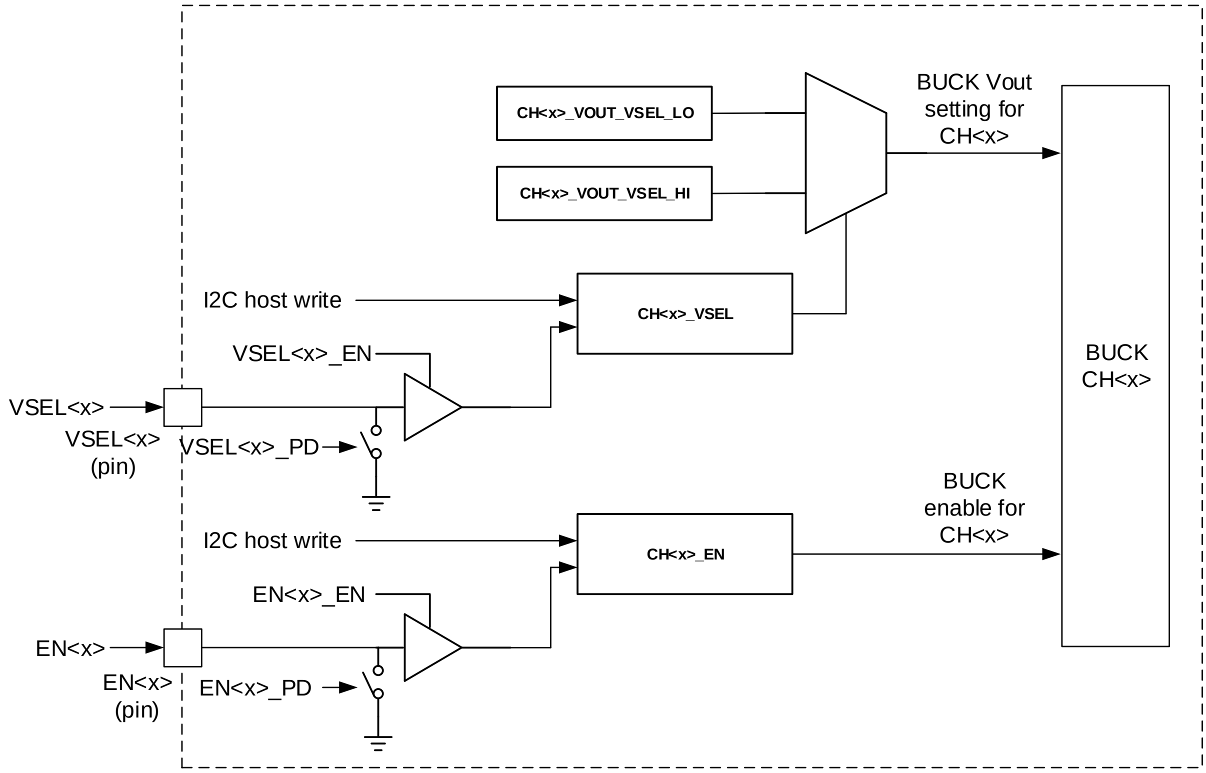


Figure 41: EN and VSEL Block Diagram

4.1.3 Switching Frequency

The buck switching frequency in PWM mode is selectable as an OTP option at typical 3.0 MHz or 4.0 MHz.

In PFM mode, DA9092 has an option to operate at switching above 25 kHz to avoid audible noise. This option is enabled by setting PFM_FREQ register bit to 1.

4.1.4 Operation Modes and Phase Selection

The buck converters can operate in PFM, full-phase PWM, PWM with phase-shedding, or auto-transition (AUTO) mode. The buck operation mode is selectable in CH<x>_MODE, or in CH<x>_MODE_VSEL_HI if VSEL<x>_EN is set to 1 and external pin VSEL<x> is pulled high.

External pin VSEL<x> can also be used to change buck operation mode when it is programmed to do so in OTP.

If AUTO is selected, the buck converter automatically changes between synchronous PWM mode and PFM depending on the load current. This improves the efficiency across the whole range of output load currents.

The maximum number of active phases in full-phase mode is adjustable in CH<x>_MAXPH. It can also be pre-configured by OTP and determined by external pin VSEL<x>.

Maximum number of active phases can be increased instantly, however, when the maximum number of active phases setting is reduced, the buck converter needs to operate in 1-phase mode (output current needs to decrease) first before it can actually be operating in less number of active phases in full-phase mode.

4.1.5 Soft Start-Up and Shutdown

To limit in-rush current from VSYS, the buck converter performs a soft start-up after being enabled.

The soft start-up and shutdown slew rates are selectable at (0.625, 1.25, 2.5, or 5.0) mV/µs in CH<x>_SR_STARTUP and CH<x>_SR_SHUTDOWN, respectively.

The buck converter follows shutdown slew-rate set in CH<x>_SR_SHUTDOWN when it is disabled by writing 0 to CH<x>_EN or by toggling the external pin EN<x> from high to low.

4.1.6 Dynamic Voltage Control

The buck converter is capable of supporting DVC transitions that occur when:

- the selected output voltage register is updated to a new target value
- the output voltage selection is changed using external pin VSEL<x>

The DVC controller operates in pulse width modulation (PWM) mode with synchronous rectification.

The slew rate of the DVC transition is programmable at (1.25, 2.5, 5.0, or 10.0) mV/µs in CH<x>_SR_UP for ramp-up and CH<x>_SR_DOWN for ramp-down.

4.1.7 Under-Voltage Lockout

The buck converter is shut down immediately if AVDD drops below the V_{UVLO} threshold. In this case, output voltage ramp-down is determined by load and pull-down resistor at LX (CH<x>_DIS_PD = 0). DA9092 will re-start with the default registers setting when AVDD increases above the UVLO release voltage threshold.

4.1.8 Current Limit and Short Protection

The integrated cycle-by-cycle peak-current detection protects the power stages and external coil from excessive current.

When the current limit is reached, the buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using M_CH<x>_OC in PMC_MASK_00 register.

A short protection is implemented in DA9092 to protect the device from an output short condition. The buck converter stops switching immediately when short protection is triggered. Short protection is triggered when the current limit is hit more than 16 cycles consecutively and the output voltage drops below short detection threshold. Output voltage ramp-down in this case is determined by load and pull-down resistor at LX (CH<x>_DIS_PD = 0).

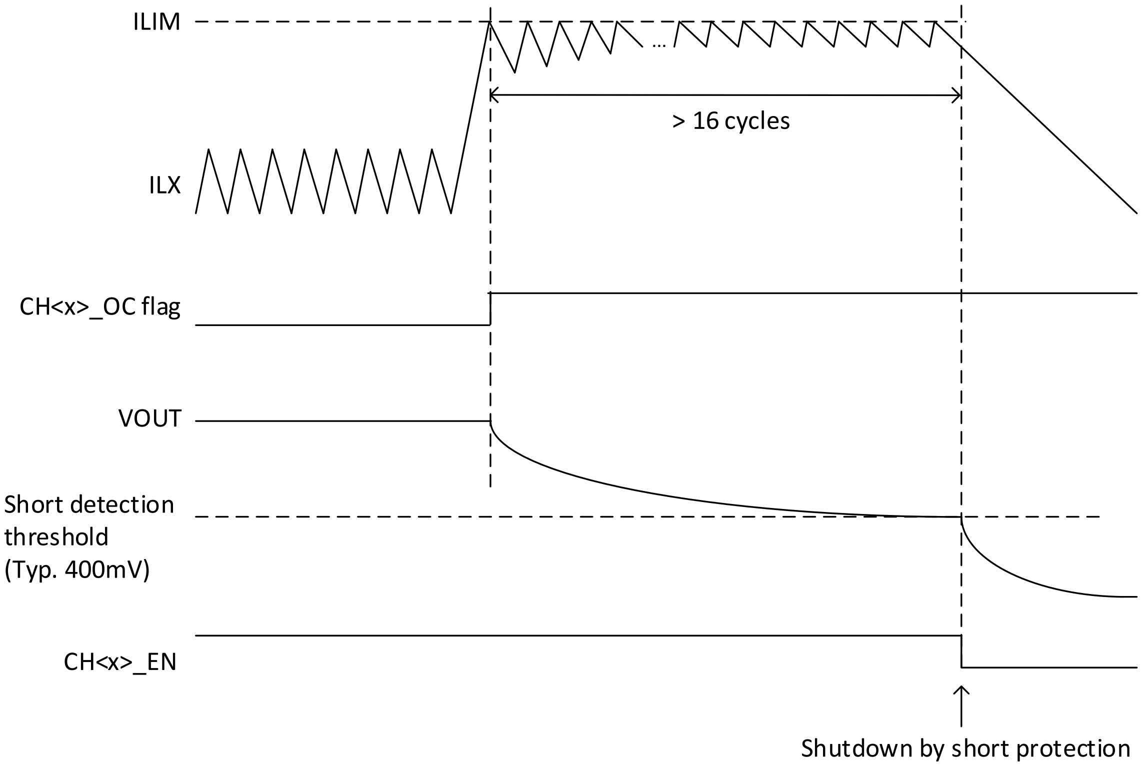


Figure 42: Current Limit and Short Protection

4.1.9 Thermal Protection

DA9092 is protected from internal overheating by thermal shutdown.

There are two kinds of flags concerning thermal protection: thermal warning and thermal critical. The warning flag is asserted when $T_J > T_{WARN}$ and the critical flag is asserted when $T_J > T_{CRIT}$. When the critical flag is asserted, the buck converter is shut down immediately and it enters a latch-off mode. In this case, output voltage ramp-down is determined by load and pull-down resistor at LX (CH<x>_DIS_PD = 0). To re-enable the buck, the critical status flag needs to be cleared and the EN signal needs to be set again by either toggling external pin EN<x> or writing 1 to CH<x>_EN register bit.

When the warning temperature or the critical temperature is reached, DA9092 generates an event and an interrupt is asserted unless the interrupt has been masked using M_TEMP_WARN or M_TEMP_CRIT in PMC_MASK_01 register.

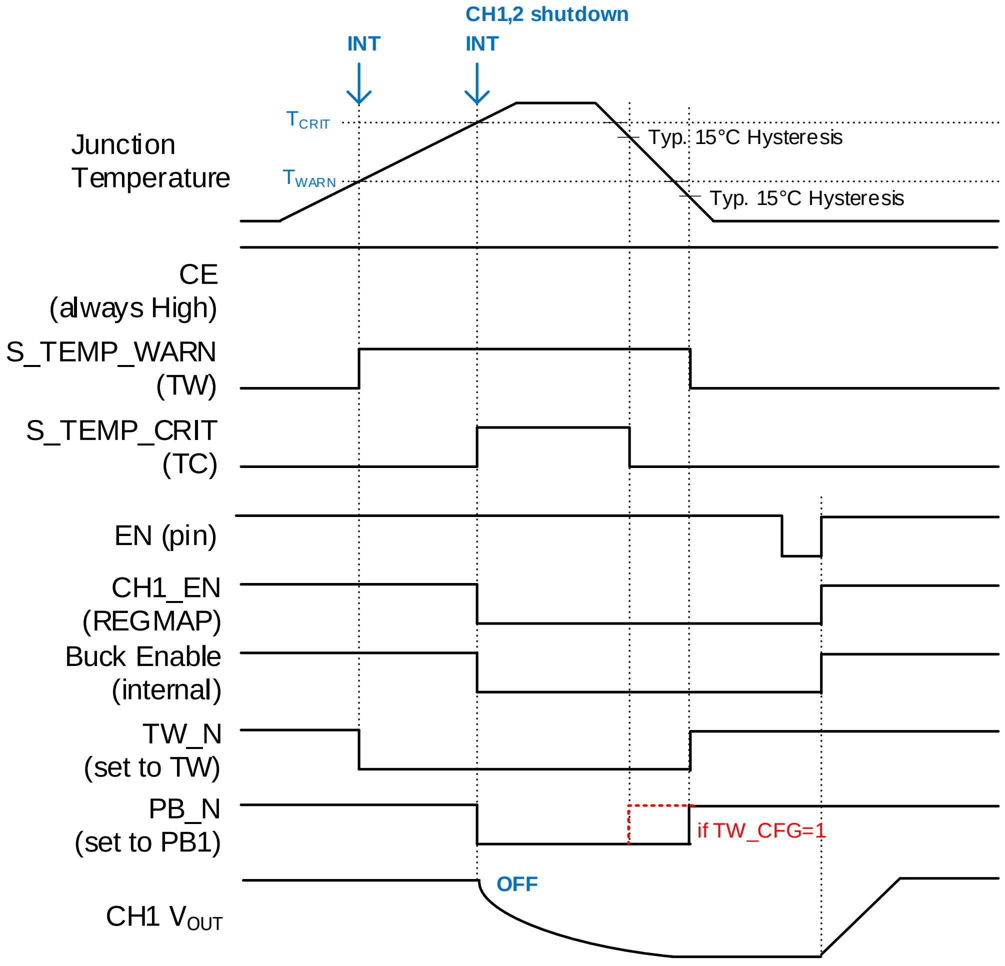


Figure 43: Buck Latch-Off Behavior by Temp Critical

4.2 Ports Description

4.2.1 CE

CE is chip (IC) enable/disable control input. When CE = 0, all blocks except for low IQ POR are powered down.

Except for event registers PMC_EVENT_00 and PMC_EVENT_01, registers reset values are loaded when CE goes from low to high. If it is preferable, event flags can also be cleared by CE rise when E_CLR_CFG is set to 1.

CE must never be left floating.

When the buck converter is shut down by pulling CE low, output voltage ramp-down is determined by load and the LX pull-down resistor (CH<x>_DIS_PD = 0), and not by the shutdown slew-rate.

4.2.2 CONF

CONF is used for configuration mode selection. It is a tri-state input (GND, AVDD, or HiZ) and it can be used to pre-configure I^2C Slave ID, CH<x>_VSTEP, EN<x>, VSEL<x>, TW_N and PB_N functionality (see Table 11).

4.2.3 EN1 and EN2

EN1 and EN2 can be used as enable/disable input of CH1 and CH2, respectively, if EN1_EN and EN2_EN register bits are set to 1.

Debounce time on falling and rising edge of EN1 and EN2 input are independently programmable via EN<x>_DEB_FALL and EN<x>_DEB_RISE at 10 µs, 100 µs, or 1 ms; it can also be disabled.

In case of 1Ch-4Ph configuration, EN2 should be pulled down to AGND.

As an alternative option, a typical 100 kΩ internal pull-down resistor on EN<x> port can be enabled by setting EN<x>_PD to 1. It is valid when CE is high and after initial OTP load.

4.2.4 VSEL1 and VSEL2

VSEL1 and VSEL2 can be used to change output voltage regulation setting, maximum number of active phases in full-phase mode, and operation mode of CH1 and CH2, respectively.

VSEL<x> functionality is disabled when VSEL<x>_EN register bit is 0.

Debounce time on falling and rising edge of VSEL1 and VSEL2 input are independently programmable via VSEL<x>_DEB_FALL and VSEL<x>_DEB_RISE at 10 µs, 100 µs, or 1 ms; it can also be disabled.

In case of 1Ch-4Ph configuration, VSEL2 should be pulled down to AGND.

As an alternative option, a typical 100 kΩ internal pull-down resistor on VSEL<x> port can be enabled by setting VSEL<x>_PD to 1. It is valid when CE is high and after initial OTP load.

CH<x>_VSEL update by VSEL<x> can be masked by setting VSEL<x>_PIN2REG_DIS=1. Clearing VSEL<x>_PIN2REG_DIS back to 0 updates CH<x>_VSEL to current VSEL<x> pin level.

4.2.5 TW_N

TW_N can be configured as thermal warning output signal of DA9092 by setting TW_SEL0 to 1. It is an open drain active-low output.

4.2.6 PB_N

PB_N can be configured as power-bad output signal of CH1 or CH2 via PB_SEL1 or PB_SEL2, respectively. It is an open drain active-low output. The power-bad output signal goes low when the output voltage drops below $V_{THR\_UV\_FALL}$ or rises above V_{THR_OV}, or when the buck converter is shut down by short protection or critical temperature. When the buck converter is shut down by short protection, PB_N stays low until either CE is pulled low or the buck converter is re-enabled by setting CH<x>_EN register bit to 1 via I²C or by toggling the external pin EN<x> from low to high.

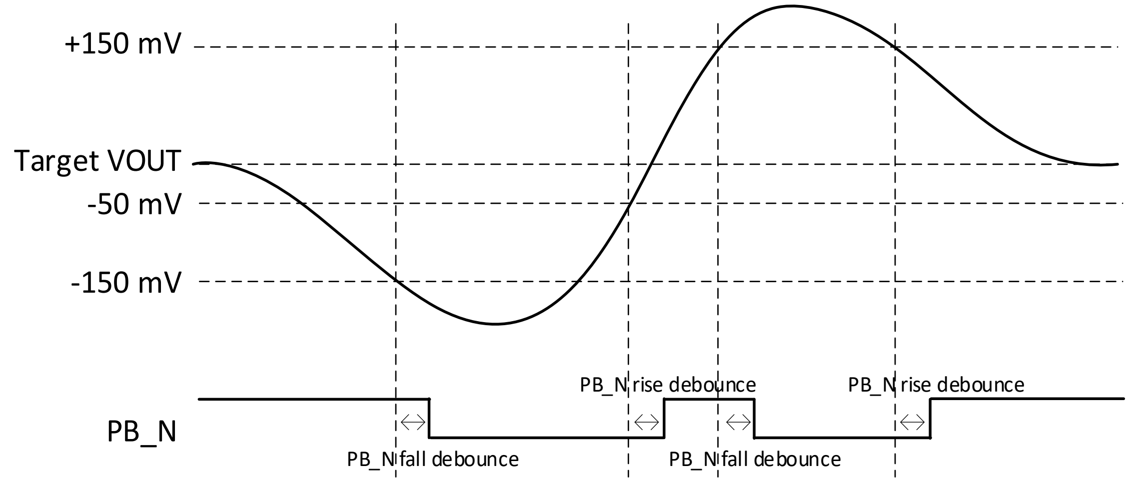


Figure 44: PB_N at Under-Voltage and Over-Voltage Condition

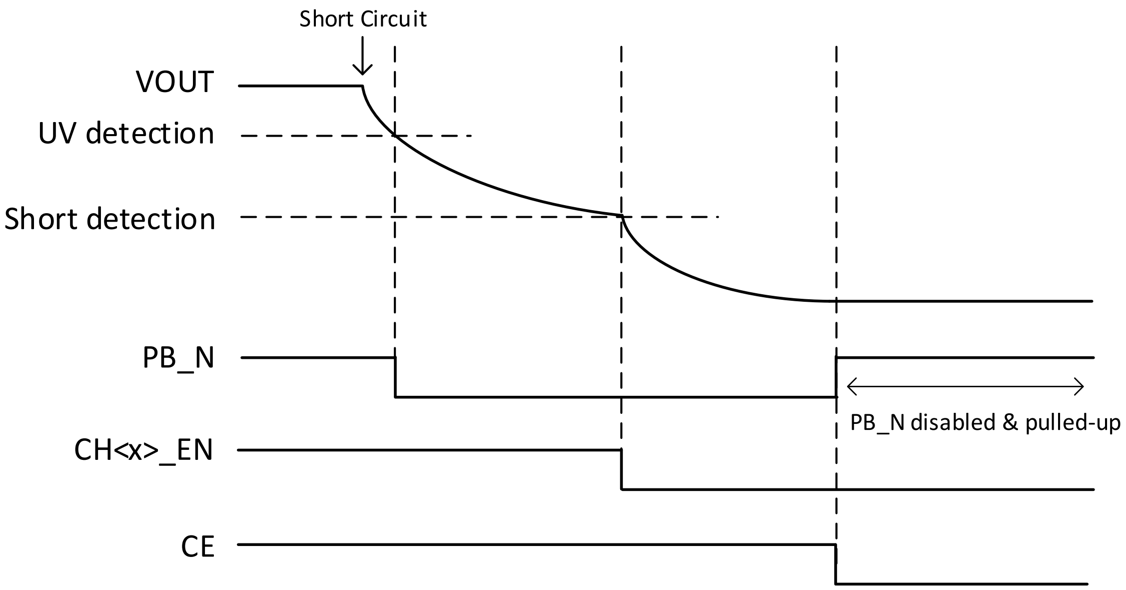


Figure 45: PB_N at Short Circuit Condition

4.2.7 INT_N

INT_N is an open drain active-low interrupt output signal which is asserted when either of the following events occur:

- Over-current
- Output under-voltage
- Output over-voltage
- Power-good
- Temperature warning
- Temperature critical
- Input under-voltage lockout

Once asserted, INT_N will be kept low until the event registers are cleared.

INT_N interrupt output signal of an event can be masked independently by setting the associated bit in PMC_MASK_00 and PMC_MASK_01 registers.

4.3 I²C Communication

DA9092 supports I²C compatible interface based on the following signals.

- SCL
  I²C bus serial clock generated by the host processor
- SDA
  I²C bus serial bidirectional data

SDA and SCL are open drain I/O terminals. The standard frequency of the I²C bus is 1 MHz in fast-mode plus or 400 kHz in fast-mode or 100 kHz in standard mode.

The I²C bus is used to control most functions and to change register values depending on the application requirements. The device is compatible with the standard I²C protocol but only operates as a slave. The transfer protocol is the same whether operating in fast-mode plus, fast-mode or standard-mode.

4.3.1 I²C Protocol

All data is transmitted across the I²C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one-byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).

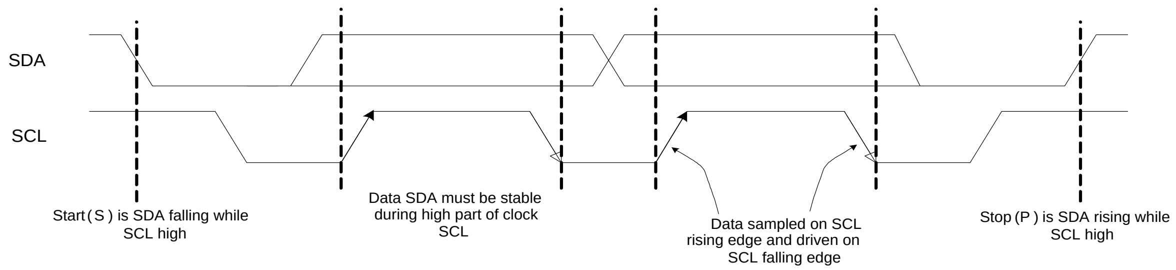


Figure 46: I²C START (S) and STOP (P)

The I²C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 47 and Figure 49).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9092 responds to all bytes with acknowledge (A), see Figure 47.

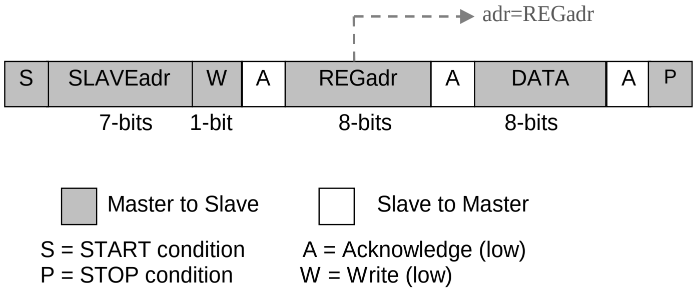


Figure 47: I²C Byte Write (SDA Line)

DA9092 also supports multiple byte writes, shown in Figure 48. By not sending a STOP command, data is written to consecutive addresses.

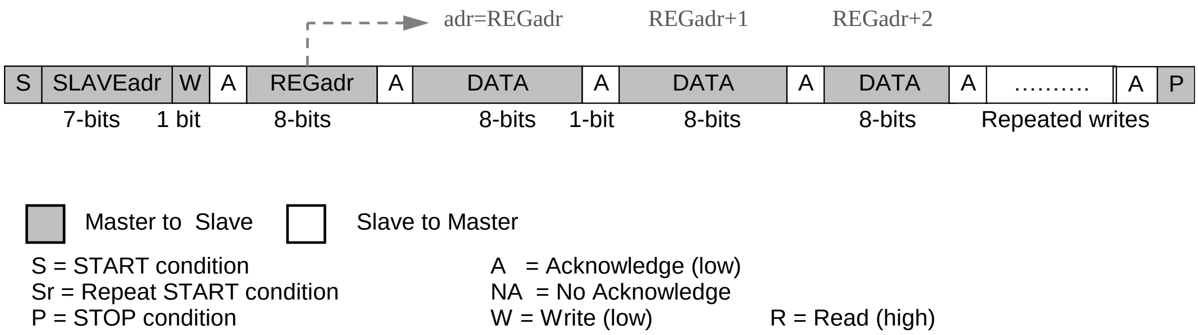


Figure 48: I²C Consecutive Write (SDA Line)

When the host reads data from a register, it first has to write to DA9092 with the target register address and then read from DA9092 with a repeated START, or alternatively a second START, condition. After receiving the data, the host sends no acknowledge (NA) and terminates the transmission with a STOP condition, see Figure 49.

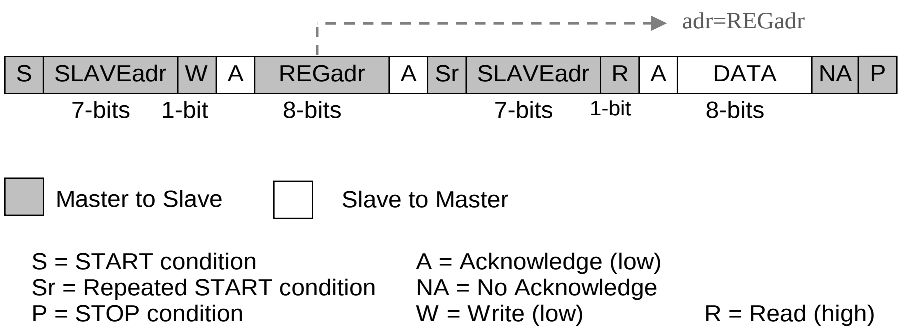


Figure 49: I²C Byte Read (SDA Line)

DA9092 also supports a multiple byte READ protocol. If the host responds to the returned data with an Acknowledge rather than Not Acknowledge and STOP, data will be read from sequential addresses until a Not Acknowledge and STOP command is sent by the host, as shown in Figure 50.

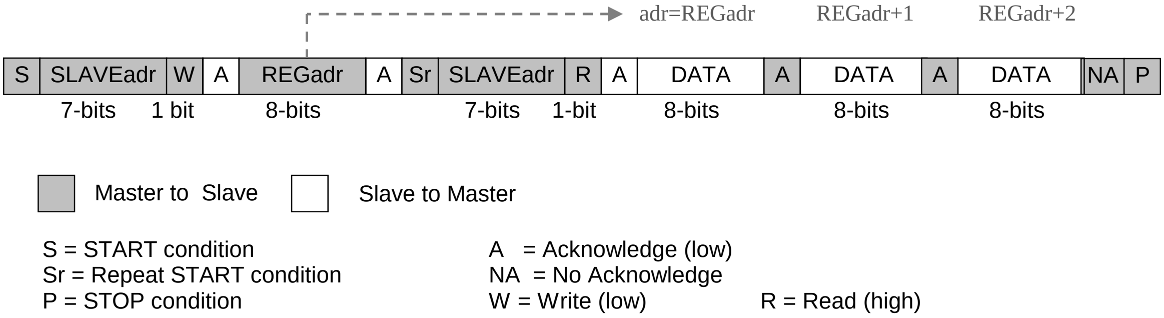


Figure 50: I²C Consecutive Read (SDA Line)

5 Register Definitions

5.1 Register Map

Table 12: Register Map

Address	Register	7	6	5	4	3	2	1	0	Reset
Functional registers										
Status										
0x0000	PMC_STATUS_00	S_CH2_OC	S_CH1_OC	S_CH2_OV	S_CH1_OV	S_CH2_UV	S_CH1_UV	S_CH2_PG	S_CH1_PG	0x00
0x0001	PMC_STATUS_01	Reserved	Reserved	Reserved	Reserved	Reserved	S_TEMP_WARN	S_TEMP_CRIT	S_VIN_UVLO	0x00
0x0002	PMC_EVENT_00	E_CH2_OC	E_CH1_OC	E_CH2_OV	E_CH1_OV	E_CH2_UV	E_CH1_UV	E_CH2_PG	E_CH1_PG	0x00
0x0003	PMC_EVENT_01	Reserved	Reserved	Reserved	Reserved	Reserved	E_TEMP_WARN	E_TEMP_CRIT	E_VIN_UVLO	0x00
0x0004	PMC_MASK_00	M_CH2_OC	M_CH1_OC	M_CH2_OV	M_CH1_OV	M_CH2_UV	M_CH1_UV	M_CH2_PG	M_CH1_PG	0xFF
0x0005	PMC_MASK_01	Reserved	Reserved	Reserved	Reserved	Reserved	M_TEMP_WARN	M_TEMP_CRIT	M_VIN_UVLO	0x07
Control										
0x0006	PMC_CTRL_00	Reserved	Reserved	Reserved	Reserved	Reserved	CHSEL	CONF<1:0>		0x04
0x0007	PMC_CTRL_01	CH2_VSTEP	CH1_VSTEP	CH2_DIS_PD	CH1_DIS_PD	CH2_VSEL	CH1_VSEL	CH2_EN	CH1_EN	0x00
0x0008	PMC_CTRL_02	VSEL2_PIN2REG_DIS	VSEL1_PIN2REG_DIS	CH2_MAXPH_VSEL_HI	CH2_MAXPH_VSEL_LO	CH1_MAXPH_VSEL_HI<1:0>		CH1_MAXPH_VSEL_LO<1:0>		0x3F
0x0009	PMC_CTRL_03	CH2_MODE_VSEL_HI<1:0>		CH2_MODE_VSEL_LO<1:0>		CH1_MODE_VSEL_HI<1:0>		CH1_MODE_VSEL_LO<1:0>		0xFF
VOUT										
0x000A	PMC_VOUT_CH1_00	CH1_VOUT_VSEL_LO<7:0>								0x8E
0x000B	PMC_VOUT_CH1_01	CH1_VOUT_VSEL_HI<7:0>								0x8E
0x000C	PMC_VOUT_CH2_00	CH2_VOUT_VSEL_LO<7:0>								0x8E
0x000D	PMC_VOUT_CH2_01	CH2_VOUT_VSEL_HI<7:0>								0x8E

Others										
0x000E	PMC_CFG_00	VSEL2_PD	VSEL1_PD	EN2_PD	EN1_PD	VSEL2_EN	VSEL1_EN	EN2_EN	EN1_EN	0x00
0x000F	PMC_CFG_01	Reserved	CH2_ILIM<2:0>			Reserved	CH1_ILIM<2:0>			0x44
0x0010	PMC_CFG_02	VSEL2_DEB_FALL<1:0>		VSEL2_DEB_RISE<1:0>		VSEL1_DEB_FALL<1:0>		VSEL1_DEB_RISE<1:0>		0x00
0x0011	PMC_CFG_03	EN2_DEB_FALL<1:0>		EN2_DEB_RISE<1:0>		EN1_DEB_FALL<1:0>		EN1_DEB_RISE<1:0>		0x55
0x0012	PMC_CFG_04	CH2_SR_SHUTDOWN<1:0>		CH2_SR_STARTUP<1:0>		CH1_SR_SHUTDOWN<1:0>		CH1_SR_STARTUP<1:0>		0xFF
0x0013	PMC_CFG_05	CH2_SR_DOWN<1:0>		CH2_SR_UP<1:0>		CH1_SR_DOWN<1:0>		CH1_SR_UP<1:0>		0xFF
0x0014	PMC_CFG_06	I2C_TMR_EN	VOUT_MAX_CFG	PG_OV_MASK	OC_DVC_MASK	PB_CFG<1:0>		PG_DVC_MASK<1:0>		0x00
0x0015	PMC_CFG_07	Reserved	E_CLR_CFG	PWM_FREQ	PFM_FREQ	SSPECTRUM	TW_CFG	TEMP_WARN_SEL<1:0>		0x00
0x0016	PMC_CFG_08	Reserved	PB_SEL2	PB_SEL1	PB_SEL0	Reserved	TW_SEL2	TW_SEL1	TW_SEL0	0x00
0x0017	PMC_CFG_09	PB_N_FALL<1:0>		PB_N_RISE<1:0>		TW_N_FALL<1:0>		TW_N_RISE<1:0>		0x55
0x0018	PMC_CFG_0A	I2C_SLAVE<6:0>							Reserved	0xD2
Device ID										
0x0019	PMC_DEV_ID	DEV_ID<7:0>								0xEA
0x001A	PMC_REV_ID	MRC_ID<3:0>				VRC_ID<3:0>				0x10
0x001B	PMC_CFG_REV	CFG_REV<7:0>								0x00

5.2 Register Descriptions

Except PMC_STATUS, PMC_EVENT, PMC_DEV_ID and PMC_REV_ID, default values of all other registers are defined by OTP.

The Type column in the register description tables maps to the Access shown in Table 13.

Table 13: Register Access Type

Datasheet Type	Access
RO	Read only
RW	Read / Write
RWC1	Read / Clear by writing 1

5.2.1 Status and Event

Table 14: PMC_STATUS_00 (0x00)

Bit	Type	Field Name	Description	Reset
[7]	RO	S_CH2_OC	CH2 current limit status. **Value** **Description** 0x0 CH2 output below current limit threshold. 0x1 CH2 output hitting current limit.	0x0
[6]	RO	S_CH1_OC	CH1 current limit status. **Value** **Description** 0x0 CH1 output below current limit threshold. 0x1 CH1 output hitting current limit.	0x0
[5]	RO	S_CH2_OV	CH2 output over-voltage status. **Value** **Description** 0x0 CH2 output below over-voltage threshold. 0x1 CH2 output above over-voltage threshold.	0x0
[4]	RO	S_CH1_OV	CH1 output over-voltage status. **Value** **Description** 0x0 CH1 output below over-voltage threshold. 0x1 CH1 output above over-voltage threshold.	0x0
[3]	RO	S_CH2_UV	CH2 output under-voltage status. **Value** **Description** 0x0 CH2 output above under-voltage threshold. 0x1 CH2 output below under-voltage threshold.	0x0

Bit	Type	Field Name	Description	Reset
[2]	RO	S_CH1_UV	CH1 output under-voltage status. **Value** **Description** 0x0 CH1 output above under-voltage threshold. 0x1 CH1 output below under-voltage threshold.	0x0
[1]	RO	S_CH2_PG	CH2 power-good status. Indicates CH2 output is at target voltage. **Value** **Description** 0x0 CH2 output not at target voltage. 0x1 CH2 output at target voltage.	0x0
[0]	RO	S_CH1_PG	CH1 power-good status. Indicates CH1 output is at target voltage. **Value** **Description** 0x0 CH1 output not at target voltage. 0x1 CH1 output at target voltage.	0x0

Table 15: PMC_STATUS_01 (0x01)

Bit	Type	Field Name	Description	Reset
[2]	RO	S_TEMP_WARN	Device junction temperature at warning level. **Value** **Description** 0x0 Not breached 0x1 Breached	0x0
[1]	RO	S_TEMP_CRIT	Device junction temperature at critical level. **Value** **Description** 0x0 Not breached 0x1 Breached	0x0
[0]	RO	S_VIN_UVLO	Input supply voltage at low level. **Value** **Description** 0x0 Not breached 0x1 Breached	0x0

Table 16: PMC_EVENT_00 (0x02)

Bit	Type	Field Name	Description	Reset
[7]	RWC1	E_CH2_OC	CH2_OC event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0

Bit	Type	Field Name	Description	Reset
[6]	RWC1	E_CH1_OC	CH1_OC event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[5]	RWC1	E_CH2_OV	CH2_OV event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[4]	RWC1	E_CH1_OV	CH1_OV event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[3]	RWC1	E_CH2_UV	CH2_UV event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[2]	RWC1	E_CH1_UV	CH1_UV event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[1]	RWC1	E_CH2_PG	CH2_PG event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[0]	RWC1	E_CH1_PG	CH1_PG event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0

Table 17: PMC_EVENT_01 (0x03)

Bit	Type	Field Name	Description	Reset
[2]	RWC1	E_TEMP_WARN	TEMP_WARN event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0

Bit	Type	Field Name	Description	Reset
[1]	RWC1	E_TEMP_CRIT	TEMP_CRIT event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0
[0]	RWC1	E_VIN_UVLO	VIN_UVLO event. Clear by write 1. **Value** **Description** 0x0 No event detected 0x1 Event detected	0x0

Table 18: PMC_MASK_00 (0x04)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_CH2_OC	INT_N mask for CH2_OC event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[6]	RW	M_CH1_OC	INT_N mask for CH1_OC event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[5]	RW	M_CH2_OV	INT_N mask for CH2_OV event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[4]	RW	M_CH1_OV	INT_N mask for CH1_OV event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[3]	RW	M_CH2_UV	INT_N mask for CH2_UV event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[2]	RW	M_CH1_UV	INT_N mask for CH1_UV event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1

Bit	Type	Field Name	Description	Reset
[1]	RW	M_CH2_PG	INT_N mask for CH2_PG event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[0]	RW	M_CH1_PG	INT_N mask for CH1_PG event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1

Table 19: PMC_MASK_01 (0x05)

Bit	Type	Field Name	Description	Reset
[2]	RW	M_TEMP_WARN	INT_N mask for TEMP_WARN event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[1]	RW	M_TEMP_CRIT	INT_N mask for TEMP_CRIT event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1
[0]	RW	M_VIN_UVLO	INT_N mask for VIN_UVLO event. **Value** **Description** 0x0 Not masked 0x1 Masked	0x1

5.2.2 Control

Table 20: PMC_CTRL_00 (0x06)

Bit	Type	Field Name	Description	Reset
[2]	RO	CHSEL	Channel operation mode. **Value** **Description** 0x0 Two channel mode, up to 2 phase per channel. 0x1 One channel mode, up to 4 phase.	0x1
[1:0]	RO	CONF	Device configuration by CONF input pin. **Value** **Description** 0x0 Config 0 (GND) 0x1 Config 1 (AVDD) 0x2 Config 2 (HiZ) 0x3 Reserved	0x0

Table 21: PMC_CTRL_01 (0x07)

Bit	Type	Field Name	Description	Reset
[7]	RW	CH2_VSTEP	VOUT step setting (mV), VOUT is doubled when set high, maximum is 1.9V. **Value** **Description** 0x0 5 0x1 10	0x0
[6]	RW	CH1_VSTEP	VOUT step setting (mV), VOUT is doubled when set high, maximum is 1.9V. **Value** **Description** 0x0 5 0x1 10	0x0
[5]	RW	CH2_DIS_PD	Disable pull-down of CH2 output while channel is not enabled. **Value** **Description** 0x0 Pull-down enabled when OFF. 0x1 Pull-down disabled.	0x0
[4]	RW	CH1_DIS_PD	Disable pull-down of CH1 output while channel is not enabled. **Value** **Description** 0x0 Pull-down enabled when OFF. 0x1 Pull-down disabled.	0x0
[3]	RW	CH2_VSEL	CH2 VOUT and operation select bit. Can be set/clear by VSEL2 input pin rise/fall. **Value** **Description** 0x0 low 0x1 high	0x0
[2]	RW	CH1_VSEL	CH1 VOUT and operation select bit. Can be set/clear by VSEL1 input pin rise/fall. **Value** **Description** 0x0 low 0x1 high	0x0
[1]	RW	CH2_EN	CH2 enable. Can be set/clear by EN2 pin rise/fall. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[0]	RW	CH1_EN	CH1 enable. Can be set/clear by EN1 pin rise/fall. **Value** **Description** 0x0 Disable 0x1 Enable	0x0

Table 22: PMC_CTRL_02 (0x08)

Bit	Type	Field Name	Description	Reset
[7]	RW	VSEL2_PIN2REG_DIS	Mask CH2_VSEL update by VSEL2 pin. CH2_VSEL is updated to VSEL2 pin level when this bit is cleared. **Value** **Description** 0x0 Enable 0x1 Disable	0x0
[6]	RW	VSEL1_PIN2REG_DIS	Mask CH1_VSEL update by VSEL1 pin. CH1_VSEL is updated to VSEL1 pin level when this bit is cleared. **Value** **Description** 0x0 Enable 0x1 Disable	0x0
[5]	RW	CH2_MAXPH_VSEL_HI	CH2 phase operation mode select, when CH2_VSEL is 1. **Value** **Description** 0x0 1 phase 0x1 Full phase	0x1
[4]	RW	CH2_MAXPH_VSEL_LO	CH2 phase operation mode select, when CH2_VSEL is 0. **Value** **Description** 0x0 1 phase 0x1 Full phase	0x1
[3:2]	RW	CH1_MAXPH_VSEL_HI	CH1 phase operation mode select, when CH1_VSEL is 1. **Value** **Description** 0x0 1 phase 0x1 2 phase 0x2 Reserved 0x3 Full phase	0x3
[1:0]	RW	CH1_MAXPH_VSEL_LO	CH1 phase operation mode select, when CH1_VSEL is 0. **Value** **Description** 0x0 1 phase 0x1 2 phase 0x2 Reserved 0x3 Full phase	0x3

Table 23: PMC_CTRL_03 (0x09)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH2_MODE_VSEL_HI	CH2 BUCK operation mode, when CH2_VSEL is 1. **Value** **Description** 0x0 PFM 0x1 Full-phase PWM 0x2 PWM mode, with auto-transition between single/full-phase (phase-shedding). 0x3 Auto-transition (AUTO) mode, with PFM, single, and full-phase transitions.	0x3
[5:4]	RW	CH2_MODE_VSEL_LO	CH2 BUCK operation mode, when CH2_VSEL is 0. **Value** **Description** 0x0 PFM 0x1 Full-phase PWM 0x2 PWM mode, with auto-transition between single/full-phase (phase-shedding). 0x3 Auto-transition (AUTO) mode, with PFM, single, and full-phase transitions.	0x3
[3:2]	RW	CH1_MODE_VSEL_HI	CH1 BUCK operation mode, when CH1_VSEL is 1. **Value** **Description** 0x0 PFM 0x1 Full-phase PWM 0x2 PWM mode, with auto-transition between single/full-phase (phase-shedding). 0x3 Auto-transition (AUTO) mode, with PFM, single, and full-phase transitions.	0x3
[1:0]	RW	CH1_MODE_VSEL_LO	CH1 BUCK operation mode, when CH1_VSEL is 0. **Value** **Description** 0x0 PFM 0x1 Full-phase PWM 0x2 PWM mode, with auto-transition between single/full-phase (phase-shedding). 0x3 Auto-transition (AUTO) mode, with PFM, single, and full-phase transitions.	0x3

5.2.3 Output Voltage

Table 24: PMC_VOUT_CH1_00 (0x0A)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH1_VOUT_VSEL_LO	CH1 output voltage setting (V), when CH1_VSEL is 0. (Note 1) **Value** **Description** 0x00 Reserved ... ... 0x3B Reserved 0x3C 0.300 0x3D 0.305 0x3E 0.310 ... ... 0xA2 0.810 0xA3 0.815 0xA4 0.820 ... ... 0xFE 1.270 0xFF 1.275	0xA3

Table 25: PMC_VOUT_CH1_01 (0x0B)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH1_VOUT_VSEL_HI	CH1 output voltage setting (V), when CH1_VSEL is 1. (Note 1) **Value** **Description** Value Description 0x00 Reserved ... ... 0x3B Reserved 0x3C 0.300 0x3D 0.305 0x3E 0.310 ... ... 0xA2 0.810 0xA3 0.815 0xA4 0.820 ... ... 0xFE 1.270 0xFF 1.275	0xA3

Table 26: PMC_VOUT_CH2_00 (0x0C)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH2_VOUT_VSEL_LO	CH2 output voltage setting (V), when CH2_VSEL is 0. (Note 2) **Value** **Description** Value Description 0x00 Reserved ... ... 0x3B Reserved 0x3C 0.300 0x3D 0.305 0x3E 0.310 ... ... 0xA2 0.810 0xA3 0.815 0xA4 0.820 ... ... 0xFE 1.270 0xFF 1.275	0xA3

Table 27: PMC_VOUT_CH2_01 (0x0D)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	CH2_VOUT_VSEL_HI	CH2 output voltage setting (V), when CH2_VSEL is 1. (Note 2) **Value** **Description** Value Description 0x00 Reserved ... ... 0x3B Reserved 0x3C 0.300 0x3D 0.305 0x3E 0.310 ... ... 0xA2 0.810 0xA3 0.815 0xA4 0.820 ... ... 0xFE 1.270 0xFF 1.275	0xA3

Note 1 When CH1_VSTEP = 1, output voltage is doubled and limited to 1.90 V (0xBE~0xFF = 1.90 V).

Note 2 When CH2_VSTEP = 1, output voltage is doubled and limited to 1.90 V (0xBE~0xFF = 1.90 V).

5.2.4 Others

Table 28: PMC_CFG_00 (0x0E)

Bit	Type	Field Name	Description	Reset
[7]	RW	VSEL2_PD	Enable pull-down of VSEL2 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[6]	RW	VSEL1_PD	Enable pull-down of VSEL1 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[5]	RW	EN2_PD	Enable pull-down of EN2 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[4]	RW	EN1_PD	Enable pull-down of EN1 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[3]	RW	VSEL2_EN	Enable VSEL2 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[2]	RW	VSEL1_EN	Enable VSEL1 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[1]	RW	EN2_EN	Enable EN2 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0
[0]	RW	EN1_EN	Enable EN1 pin. **Value** **Description** 0x0 Disable 0x1 Enable	0x0

Table 29: PMC_CFG_01 (0x0F)

Bit	Type	Field Name	Description	Reset
[6:4]	RW	CH2_ILIM	CH2 current limit setting per phase (A). **Value** **Description** 0x0 7.5 0x1 10.0 0x2 12.5 0x3 15.0 0x4 17.5 0x5 20.0 0x6 22.5 0x7 Reserved	0x4
[2:0]	RW	CH1_ILIM	CH1 current limit setting per phase (A). **Value** **Description** 0x0 7.5 0x1 10.0 0x2 12.5 0x3 15.0 0x4 17.5 0x5 20.0 0x6 22.5 0x7 Reserved	0x4

Table 30: PMC_CFG_02 (0x10)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	VSEL2_DEB_FALL	VSEL2 input pin debounce time on fall edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x0
[5:4]	RW	VSEL2_DEB_RISE	VSEL2 input pin debounce time on rise edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x0

Bit	Type	Field Name	Description	Reset
[3:2]	RW	VSEL1_DEB_FALL	VSEL1 input pin debounce time on fall edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x0
[1:0]	RW	VSEL1_DEB_RISE	VSEL1 input pin debounce time on rise edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x0

Table 31: PMC_CFG_03 (0x11)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	EN2_DEB_FALL	EN2 input pin debounce time on fall edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1
[5:4]	RW	EN2_DEB_RISE	EN2 input pin debounce time on rise edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1
[3:2]	RW	EN1_DEB_FALL	EN1 input pin debounce time on fall edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1

Bit	Type	Field Name	Description	Reset
[1:0]	RW	EN1_DEB_RISE	EN1 input pin debounce time on rise edge. **Value** **Description** 0x0 Off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1

Table 32: PMC_CFG_04 (0x12)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH2_SR_SHUTDOWN	CH2 active shutdown output voltage slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 0.625 0x1 1.25 0x2 2.50 0x3 5.00	0x3
[5:4]	RW	CH2_SR_STARTUP	CH2 soft-start output voltage slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 0.625 0x1 1.25 0x2 2.50 0x3 5.00	0x3
[3:2]	RW	CH1_SR_SHUTDOWN	CH1 active shutdown output voltage slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 0.625 0x1 1.25 0x2 2.50 0x3 5.00	0x3
[1:0]	RW	CH1_SR_STARTUP	CH1 soft-start output voltage slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 0.625 0x1 1.25 0x2 2.50 0x3 5.00	0x3

Note 1 Slew-rate is doubled when CH<x>_VSTEP = 1.

Table 33: PMC_CFG_05 (0x13)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CH2_SR_DOWN	CH2 DVC ramp-down slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 1.25 0x1 2.50 0x2 5.00 0x3 10.00	0x3
[5:4]	RW	CH2_SR_UP	CH2 DVC ramp-up slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 1.25 0x1 2.50 0x2 5.00 0x3 10.00	0x3
[3:2]	RW	CH1_SR_DOWN	CH1 DVC ramp-down slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 1.25 0x1 2.50 0x2 5.00 0x3 10.00	0x3
[1:0]	RW	CH1_SR_UP	CH1 DVC ramp-up slew-rate setting (mV/us). (Note 1) **Value** **Description** 0x0 1.25 0x1 2.50 0x2 5.00 0x3 10.00	0x3

Note 1 Slew-rate is doubled when CH<x>_VSTEP = 1.

Table 34: PMC_CFG_06 (0x14)

Bit	Type	Field Name	Description	Reset
[7]	RO	I2C_TMR_EN	Enable 30 ms timeout if SCL stops during I^{2}C transaction. (Note 1) **Value** **Description** 0x0 Disable I^{2}C timeout 0x1 Enable I^{2}C timeout	0x0

Bit	Type	Field Name	Description	Reset
[6]	RO	VOUT_MAX_CFG	VOUT limit setting when VSTEP = 0. (Note 2) **Value** **Description** 0x0 Max VOUT is 1.275 V 0x1 Max VOUT is 0.950 V	0x0
[5]	RW	PG_OV_MASK	Exclude OV from power-good condition. **Value** **Description** 0x0 OV condition sets PG low 0x1 OV condition has no effect on PG	0x0
[4]	RW	OC_DVC_MASK	Over-current event mask during DVC. **Value** **Description** 0x0 No mask 0x1 Mask OC during DVC	0x0
[3:2]	RW	PB_CFG	Power-bad (PB) output configuration. **Value** **Description** 0x0 Power-bad 0x1 Power-good with mask when disabled 0x2 Power-good with mask during start-up 0x3 Power-good	0x0
[1:0]	RW	PG_DVC_MASK	Power-good mask during DVC. **Value** **Description** 0x0 No mask 0x1 Mask as not power good during DVC 0x2 Mask as power good during DVC 0x3 Reserved	0x0

Note 1 Counting starts after Slave ID is detected. SCL toggle is being monitored.

Note 2 Invalid when VSTEP = 1.

Table 35: PMC_CFG_07 (0x15)

Bit	Type	Field Name	Description	Reset
[6]	RW	E_CLR_CFG	Event flag clear configuration. (Note 1) **Value** **Description** 0x0 Event flags are not cleared on CE rise nor UVLO release. 0x1 Event flags are cleared on CE rise or UVLO release.	0x0
[5]	RO	PWM_FREQ	BUCK PWM switching frequency option (MHz). **Value** **Description** 0x0 3 0x1 4	0x0

Bit	Type	Field Name	Description	Reset
[4]	RW	PFM_FREQ	BUCK PFM switching frequency option. **Value** **Description** 0x0 Frequency limiting off 0x1 Switching above 25kHz	0x0
[3]	RW	SSPECTRUM	PMIC operates on spread-spectrum clock. **Value** **Description** 0x0 Disabled 0x1 Enabled	0x0
[2]	RW	TW_CFG	Configuration for BUCK startup mask by junction temperature status. **Value** **Description** 0x0 BUCK start-up waits for S_TEMP_WARN to be cleared 0x1 BUCK start-up waits for S_TEMP_CRIT to be cleared	0x0
[1:0]	RW	TEMP_WARN_SEL	Junction temperature warning level select (degree-Celsius). **Value** **Description** 0x0 125 0x1 110 0x2 95 0x3 80	0x0

Note 1 AVDD lost causes event flag clear.

Table 36: PMC_CFG_08 (0x16)

Bit	Type	Field Name	Description	Reset
[6]	RW	PB_SEL2	PB_N pin output enable for CH2 power-bad. **Value** **Description** 0x0 Disabled 0x1 CH2 power-bad	0x0
[5]	RW	PB_SEL1	PB_N pin output enable for CH1 power-bad. **Value** **Description** 0x0 Disabled 0x1 CH1 power-bad	0x0
[4]	RW	PB_SEL0	PB_N pin output enable for S_TEMP_WARN. **Value** **Description** 0x0 Disabled 0x1 S_TEMP_WARN	0x0

Bit	Type	Field Name	Description	Reset
[2]	RW	TW_SEL2	TW_N pin output enable for CH2 power-bad. **Value** **Description** 0x0 Disabled 0x1 CH2 power-bad	0x0
[1]	RW	TW_SEL1	TW_N pin output enable for CH1 power-bad. **Value** **Description** 0x0 Disabled 0x1 CH1 power-bad	0x0
[0]	RW	TW_SEL0	TW_N pin output enable for S_TEMP_WARN. **Value** **Description** 0x0 Disabled 0x1 S_TEMP_WARN	0x0

Table 37: PMC_CFG_09 (0x17)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	PB_N_FALL	PB_N output pin debounce time on fall edge. **Value** **Description** 0x0 off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1
[5:4]	RW	PB_N_RISE	PB_N output pin debounce time on rise edge. **Value** **Description** 0x0 off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1
[3:2]	RW	TW_N_FALL	TW_N output pin debounce time on fall edge. **Value** **Description** 0x0 off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1

Bit	Type	Field Name	Description	Reset
[1:0]	RW	TW_N_RISE	TW_N output pin debounce time on rise edge. **Value** **Description** 0x0 off 0x1 10 us 0x2 100 us 0x3 1 ms	0x1

Table 38: PMC_CFG_0A (0x18)

Bit	Type	Field Name	Description	Reset
[7:1]	RO	I2C_SLAVE	I2C slave ID.	0x69

5.2.5 Device ID

Table 39: PMC_DEV_ID (0x19)

Bit	Type	Field Name	Description	Reset
[7:0]	RO	DEV_ID	Device ID.	0xEA

Table 40: PMC_REV_ID (0x1A)

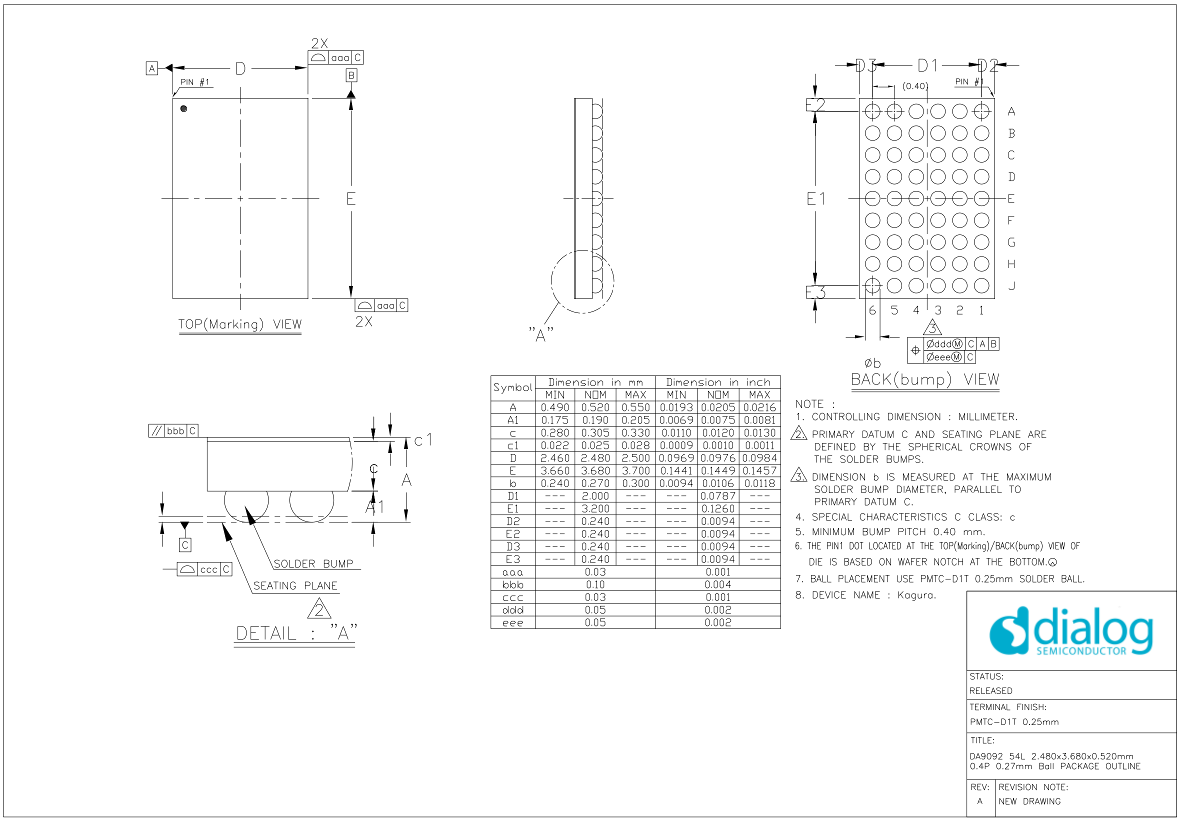
Bit	Type	Field Name	Description	Reset
[7:4]	RO	MRC_ID	Mask revision code.	0x2
[3:0]	RO	VRC_ID	Chip variant code; e.g. package variants.	0x0

Table 41: PMC_CFG_REV (0x1B)

Bit	Type	Field Name	Description	Reset
[7:0]	RO	CFG_REV	OTP variant code.	0x0

6 Package Information

6.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.490	0.520	0.550	0.0193	0.0205	0.0216
A1	0.175	0.190	0.205	0.0069	0.0075	0.0081
c	0.280	0.305	0.330	0.0110	0.0120	0.0130
c1	0.022	0.025	0.028	0.0009	0.0010	0.0011
D	2.460	2.480	2.500	0.0969	0.0976	0.0984
E	3.660	3.680	3.700	0.1441	0.1449	0.1457
b	0.240	0.270	0.300	0.0094	0.0106	0.0118
D1	---	2.000	---	---	0.0787	---
E1	---	3.200	---	---	0.1260	---
D2	---	0.240	---	---	0.0094	---
E2	---	0.240	---	---	0.0094	---
D3	---	0.240	---	---	0.0094	---
E3	---	0.240	---	---	0.0094	---
aaa	0.03			0.001		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.05			0.002		
eee	0.05			0.002		

Figure 51: WLCSP6x9 Package Outline Drawing

6.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 42.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The DA9092 package is qualified for MSL1.

Table 42: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

6.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore, a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

6.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

7 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 43: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9092-xxOV2	WLCSP 54L	2.48 x 3.68	Reel	10,000 pcs

Part Number Legend:

DA9092-xxOV2

xx: OTP variant

8 Application Information

The following recommended components and typical buck performance are references selected from requirements of a typical application.

8.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 44: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tol. (%)	V-Rate	Type
V_{OUT} output bypass	10 µF	0402	X5R	±20	6.3 V	Murata GRM155R60J106ME15D
VDDx bypass	0.1 µF	0402	X7R	±10	16 V	Murata GCM155R71C104KA55D
	10 µF	0402	X5R	±20	10 V	Samsung Electro-Mechanics CL05A106MP8NUB8
AVDD bypass	1 µF	0201	X5R	±20	10 V	Murata GRM033R61A105ME15D

8.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current

  Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance

  Critical for the converter efficiency and should therefore be minimized.

Fully shielded inductor is highly recommended to use. The typical recommended output inductance is 0.1 µH per phase. Use of larger output inductance degrades the load transient performance of the buck converter.

Table 45: Recommended Inductor Types

Value (µH)	Size (mm)	I_{MAX} (DC) (A)	I_{SAT} (A)	Tol. (%)	DC Resistance (mΩ)	Type
0.1	2.5 x 2.0 x 1.2	12	12	±20	4.0	TDK TMS252012ALM-R10MTAA

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

High-Performance Multi-Phase DC-DC Buck Converter

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

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