2.5 A Companion Charger for Rapid Charging

General Description

DA9155M offers a small solution that can be easily added on to existing main charger circuits and solves the heat dissipation problem created when the rapid charging feature is adopted. DA9155M is compatible to all rapid charging technologies using high voltage input.

DA9155M features a Buck converter capable of 2.5 A constant output current and regulates the output current with ±5 % accuracy for single cell Li-Ion batteries. Current sensing is performed with a fully integrated circuit.

The peak efficiency of the Buck converter is 92 %.

Key Features

- Input voltage 4.3 V to 13.5 V
- Input voltage monitoring
- Buck converter with output current regulation
  - Output current 2.5 A
  - ±5 % current regulation accuracy
  - Selectable switching frequency
- Fault detection (V_{IN} and V_{BAT} monitoring)
- Safety timer
- Junction temperature monitoring
- -40 °C to +85 °C temperature range
- WLCSP, 0.4 mm pitch

Applications

- Companion charger in smartphone and tablet platforms
- Companion charger for all single cell Li-Ion battery powered devices

1 Block Diagram

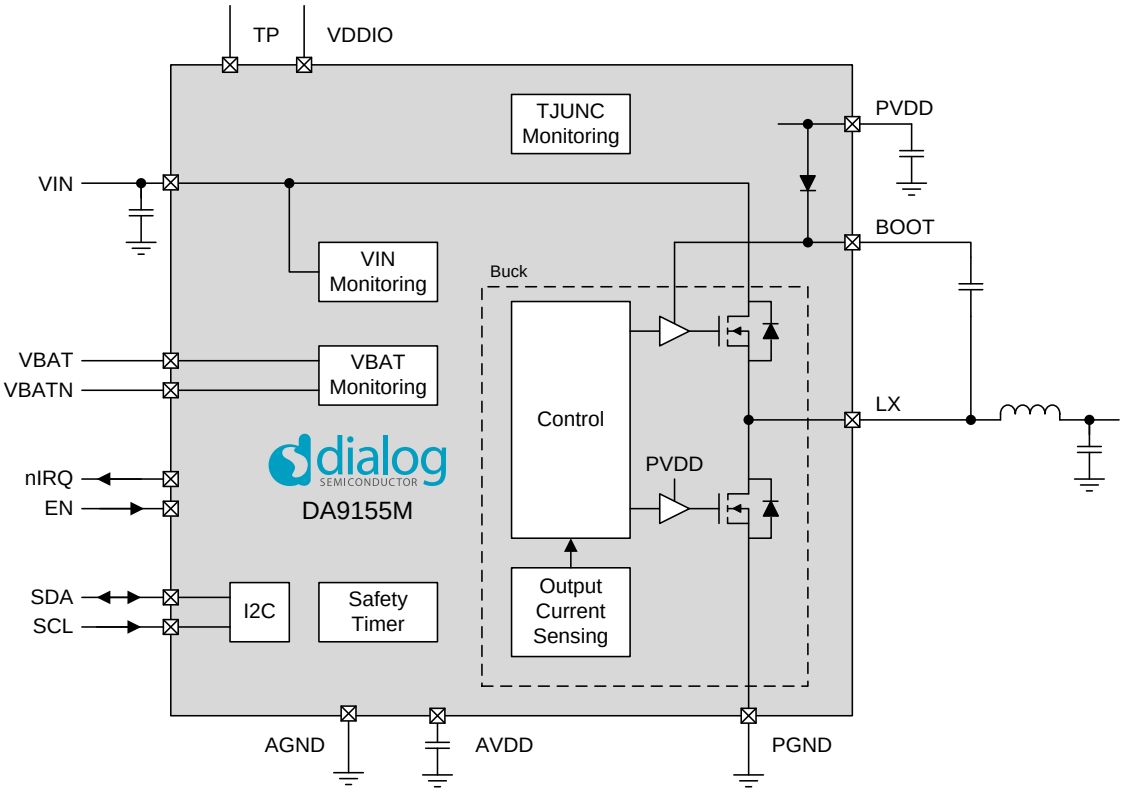

Figure 1: DA9155M Block Diagram.

2 Revision History

Revision	Date	Changes
3.1	04-May-2017	Document formatting changes
3.06	21-Dec-2016	Added thermal resistance to Recommended Operating Conditions Additional description in TIMER_B register definition table Additional description in Pin list for AVDD and PVDD Changes to Description
3.05	22-July-2016	Updated first page
3.04	10-May-2016	Added max value of V_{IN_OVLO} Updated max value of V_{IN_UVLO} Updated typ value of L_{ESR} Added min value in Output current range Added min and max values of I_{LIM} Updated test condition for V_{BAT_OV} Updated test condition for $I_{Q\_DIS\_VIN}$ Updated description of Bit E_RDY in EVENT_B (0x004) register
3.03	24-Mar-2016	Update Specs for $I_{Q\_NO\_PWR\_VBAT}$ and removed V_{OH}
3.02	01-Mar-2016	Updated Specs for V_{IN2BAT}, V_{IN2BAT_HYST}, $V_{IN\_DROP\_HYST}$, $V_{IN\_DROP\_ACC}$, $V_{BAT\_UV\_ACC}$, $V_{BAT\_OV\_ACC}$
3.01	15-Jan-2016	Update Figure 2 for LF35
3.00	09-Nov-2015	Final Datasheet Release

3 Ordering Information

The order number consists of the part number followed by a suffix indicating the packing method. For details, please consult the customer portal on the Dialog website or your local sales representative.

Table 1: Ordering Information

Part number	Package	Package description
DA9155M-xxU72	30 WL-CSP	Tape and Reel, 4500pcs

Contents

4 Pin List

Table 2: DA9155M Pin Description

Pin	Name	Type	Description
C1	VDDIO	PS	IO supply
B2, B3, B4, C2, C3, D1, D2, D3	AGND	GND	Analog ground
A2	AVDD	AIO	Internal supply, typical 4 V
A3	PVDD	AIO	Internal supply, typical 4 V
E2	SDA	DIO	Data signal of the 2-wire interface (GPIO)
E1	SCL	DI	Clock signal of the 2-wire interface (GPIO)
E4	EN	DI	Control signal for the output current/voltage (GPIO)
E3	nIRQ	DO	Interrupt signal to host processor (GPIO)
A5, A6	VIN	PS	Input supply
B5, B6, C5, C6, D5, D6	VLX	AO	Switching node of Buck
A4	BOOT	AIO	Supply of the high-side driver
B1	VBAT	AI	Battery voltage sense, positive terminal
A1	VBATN	AI	Battery voltage sense, negative terminal
E5, E6	PGND	GND	Power grounds of the Buck, digital ground
C4, D4	NC		Not connected. Short to ground.

Table 3: Pin Type Definitions

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analogue Input
DO	Digital Output	AO	Analogue Output
DIO	Digital Input/Output	AIO	Analogue Input/Output
PS	Power Supply	GND	Ground connection

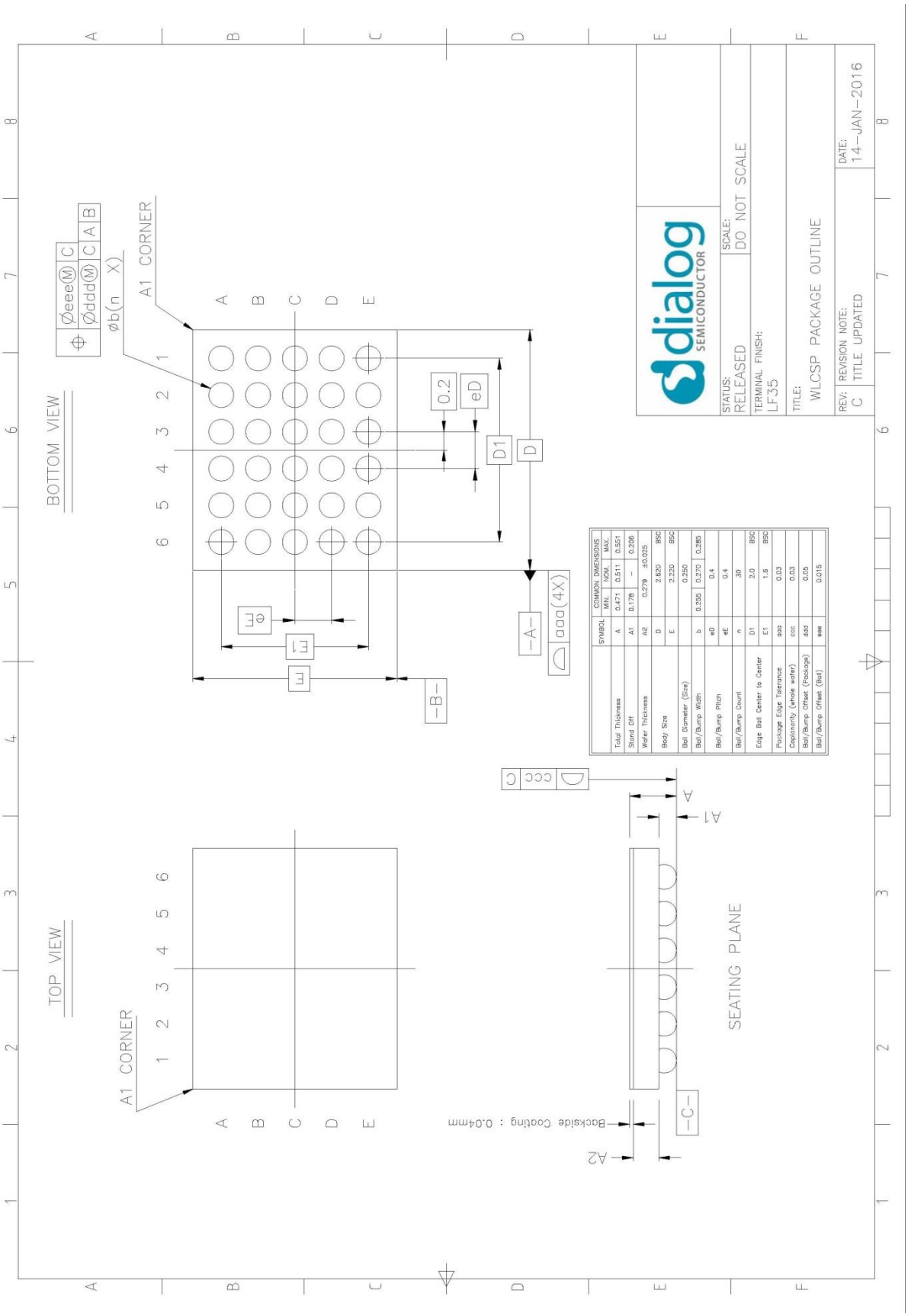

Figure 2: DA9155M Package Outline Drawing

5 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings of the device. Stressing the device beyond these ratings may cause permanent damage to the device. Functionality of the device is only guaranteed in conditions listed in sections 6 and 7. Operating the device in conditions exceeding those listed in sections 6 and 7, but still complying with the absolute maximum ratings listed in Table 4, for extended periods of time may affect device reliability.

Table 4: Absolute Maximum Ratings

Parameter	Symbol	Note	Min	Max	Unit
Storage temperature			-60	+150	°C
Operating temperature	T_A		-40	+85	°C
Terminal voltage (referenced to PGND, unless otherwise noted)	VIN	The device is not operational above V_{IN_OVLO}.	-0.3	20	V
	VLX		-0.3	VIN	V
	BOOT		-0.3	VLX+5.5	V
	VBATP	Referenced to VBATN	-0.3	6	V
	All other terminals	Referenced to AGND	-0.3	5.5	V
ESD tolerance		HBM		2	kV

6 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating temperature	T_A	-40	+85	°C
Supply voltage	V_{IN}	4.3	13.5	V
Supply voltage IO	V_{DDIO}	1.5	3.6	V
Thermal resistance (junction to ambient) Note 1	θ_{JA}		37.42	ºC/W

Note 1 Multilayer JEDEC standard, still air, ambient temperature 27 ºC, simulated value

7 Electrical Characteristics

7.1 Digital I/O

Unless otherwise noted, the following is valid for T_A = -40 to +85 ºC, V_{IN} = 4.3 to 13.5 V, V_{BAT} = 2.6 to 4.4 V

Table 6: Digital I/O

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input high voltage (EN, SCL, SDA)	V_{IH}		0.7 × VDDIO			V
Input low voltage (EN, SCL, SDA)	V_{IL}				0.3 × VDDIO	V
Output low voltage (nIRQ, SDA)	V_{OL}				0.3	V
Input capacitance (SCL, SDA)	C_{IN}				10	pF

7.2 V_{IN} Monitoring

Unless otherwise noted, the following is valid for T_A = -40 to +85 ºC, V_{IN} = 4.3 to 13.5 V, V_{BAT} = 2.6 to 4.4 V

Table 7: V_{IN} Monitoring

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
V_{IN} to V_{BAT} threshold	V_{IN2BAT}	Falling threshold	225	275	330	mV
V_{IN} to V_{BAT} hysteresis	V_{IN2BAT_HYST}			130		mV
V_{IN} overvoltage threshold	V_{IN_OVLO}	Rising threshold, pulse width greater than 3 µs	13.5		15	V
V_{IN} overvoltage hysteresis	$V_{IN\_OVLO\_HYST}$			2%		
V_{IN} undervoltage threshold	V_{IN_UVLO}	Falling threshold	4.085	4.3	4.5	V
V_{IN} undervoltage hysteresis	$V_{IN\_UVLO\_HYST}$			2%		
V_{IN} drop threshold range	V_{IN_DROP}	Falling threshold. V_{IN_DROP}=0x3B		12		V
		Falling threshold. V_{IN_DROP}=0x37		11.6		V
		Falling threshold. V_{IN_DROP}=0x23		8.6		V
		Falling threshold V_{IN_DROP}=0x00		4.3		V
V_{IN} drop hysteresis	$V_{IN\_DROP\_HYST}$			1.5%		
V_{IN} drop accuracy	$V_{IN\_DROP\_ACC}$	Vin_drop <= 5.4V	-1.6%		+1.6%	
		Vin_drop > 5.4V	-1.9%		+1.9%	

7.3 Buck Converter

Table 8: External Components

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input capacitor	C_{IN}			10		µF
Output capacitor	C_{OUT}	Nominal	10	22		µF
Output capacitor ESR	C_{ESR}			3		mΩ
Inductor value	L_{BUCK}			0.47		µH
Inductor resistance	L_{ESR}			24		mΩ

Unless otherwise noted, the following is valid for T_A = -40 to +85 ºC, V_{IN} = 4.3 to 13.5 V, V_{BAT} = 2.6 to 4.4 V

Table 9: Buck Converter

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage range	V_{IN}	V_{IN} has to be above V_{BAT} (Section 7.2)	4.3		13.5	V
Output current range			400		2500	mA
Output current	I_{OUT}	BUCK_IOUT = 0x32		750		mA
		BUCK_IOUT = 0x7D		1500		mA
		BUCK_IOUT = 0xE1		2500		mA
Output current regulation accuracy	I_{OUT_ACC}	I_{OUT} = 2.5 A, D ≤ 80%, V_{IN} = 5V to 12V, T_A = 0 to 85 ºC (Note 2)	-5%		+5%	
		1.5 A ≤ I_{OUT} < 2.5 A, D ≤ 80%, V_{IN} = 5V to 12V, T_A = 25 ºC (Note 2)	-5%		+5%	
		500 mA ≤ I_{OUT} < 1.5 A, D ≤ 80%, V_{IN} = 5V to 12V, T_A = 25 ºC (Note 2)	-10%		+10%	
Efficiency	η	V_{IN} = 5 V, V_{BAT} = 4.4 V, I_{OUT} = 2.5 A		96%		
		V_{IN} = 9 V, V_{BAT} = 4.4 V, I_{OUT} = 2.5 A		92%		
		V_{IN} = 12 V, V_{BAT} = 4.4 V, I_{OUT} = 2.5 A		90%		
Switching frequency	f	OSC_TUNE = 0x0 BUCK_FSW = 0x0 (Note 3)		1.2		MHz
		OSC_TUNE = 0x0 BUCK_FSW = 0x2 (Note 3)		1.5		MHz
		OSC_TUNE = 0x0 BUCK_FSW = 0x3 (Note 3)		1		MHz
Duty cycle	D	VIN ≥ 5 V, f=1.5 MHz	15%		85%	
		Switching frequency is stepwise reduced above 85% duty cycle			95%	
Minimum off-time	t_{MIN_OFF}			100		ns
High-side R_{DSON}	$R_{DSON-HS}$	Including pin and routing		25		mΩ
Low-side R_{DSON}	$R_{DSON-LS}$	Including pin and routing		25		mΩ
Peak current limit	I_{LIM}	BUCK_ILIM = 0x19	4400	5500	6600	mA
		BUCK_ILIM = 0x14	4000	5000	6000	mA
		BUCK_ILIM = 0x0	2050	3000	3820	mA

Note 2 Accuracy may decrease by 5% at D > 80%

Note 3 1 MHz is recommended for V_{IN} ≤ 6.5 V and 1.5 MHz for V_{IN} > 6.5 V

7.4 2-Wire Interface

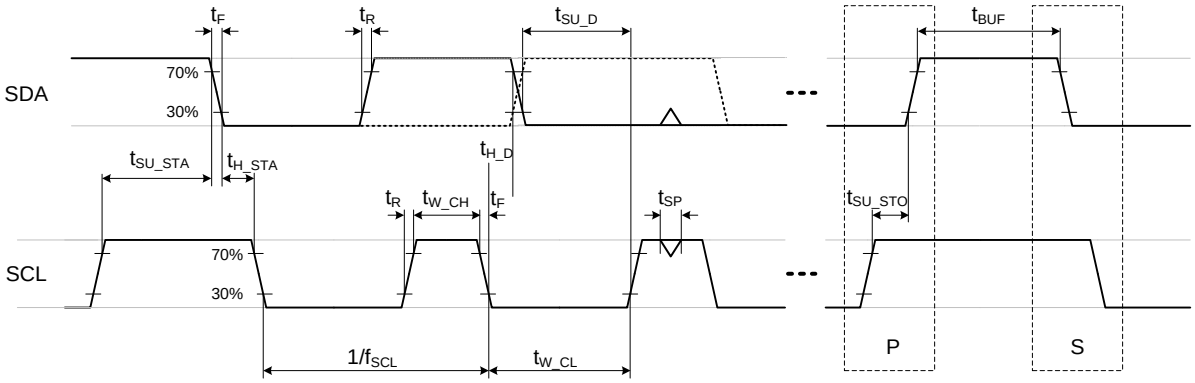

Figure 3: 2-Wire Interface Timing

Unless otherwise noted, the following is valid for T_A = -40 to +85 ºC, V_{IN} = 4.3 to 13.5 V, V_{BAT} = 2.6 to 4.4 V

Table 10: 2-Wire Interface

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Spike suppression (SCL, SDA)	t_{SP}	Fast/fast+ mode	0		50	ns
		High speed mode	0		10	ns
Bus free time from STOP to START condition	t_{BUF}		0.5			µs
Bus line capacitive load					150	pF
Standard/Fast/Fast+ mode						
SCL clock frequency	f_{SCL}	Note 4	0		1000	kHz
Start condition setup time	t_{SU_STA}		0.26			us
Start condition hold time	t_{H_STA}		0.26			us
SCL low time	t_{W_CL}		0.5			us
SCL high time	t_{W_CH}		0.26			us
2-wire SCL and SDA rise time	t_R				1000	ns
2-wire SCL and SDA fall time	t_R				300	ns
Data setup time	t_{SU_D}		50			ns
Data hold-time	t_{H_D}		0			ns
Stop condition setup time	t_{SU_STO}		0.26			us
High speed mode						
SCL clock frequency	f_{SCL}	Requires V_{DDIO} ≥ 1.8 V (Note 4)	0		3400	kHz
Start condition setup time	t_{SU_STA}		160			ns

Start condition hold time	t_{H_STA}		160			ns
SCL low time	t_{SCL_LO}		160			ns
SCL high time	t_{SCL_HI}		60			ns
2-wire SCL and SDA rise/fall time	t_R				160	ns
Data setup time	t_{SU_D}		10			ns
Data hold-time	t_{H_D}		0			ns
Stop condition setup time	t_{SU_STO}		160			ns

Note 4 Minimum clock frequency is 10 kHz if 2W_TO is enabled

7.5 Temperature Supervision

Unless otherwise noted, the following is valid for V_{IN} = 4.3 to 13.5 V, V_{BAT} = 2.6 to 4.4 V

Table 11: Temperature Supervision

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
POR temperature threshold	T_{JUNC_POR}			150		°C
Critical temperature threshold	T_{JUNC_CRIT}			140		°C
Warning temperature threshold	T_{JUNC_WARN}	Rising threshold TJUNC_WARN=0xB		125		°C
		Rising threshold TJUNC_WARN=0x0		70		°C

7.6 V_{BAT} Monitoring

Unless otherwise noted, the following is valid for TA = -40 to +85 ºC

Table 12: V_{BAT} Monitoring

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Overvoltage threshold	V_{BAT_OV}	Rising threshold, VBAT_OV = 0x3C		5.1		V
		Rising threshold, VBAT_OV = 0x20		4.4		V
		Rising threshold, VBAT_OV = 0x00		3.6		V
Undervoltage threshold	V_{BAT_UV}	Falling threshold, VBAT_UV = 0x32		3.25		V
		Falling threshold, VBAT_UV = 0x18		2.6		V
		Falling threshold, VBAT_UV = 0x0		2.0		V
VBAT monitoring hysteresis	$V_{BAT\_MON\_HYS}$			1.5%		
V_{BAT_UV} accuracy	$V_{BAT\_UV\_ACC}$		-3%		+3%	
V_{BAT_OV} accuracy	$V_{BAT\_OV\_ACC}$		-1.6%		+1.6%	

7.7 Current Consumption

Unless otherwise noted, the following is valid for T_A = -40 to +85 ºC

Table 13:Current Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current (no-power mode)	$I_{Q\_NO\_PWR\_VBAT}$	V_{BAT} = 3.6 V	1	5	12	µA
Current (disabled mode)	$I_{Q\_DIS\_VIN}$	V_{IN} = 5 V, V_{BAT} = 2.6 to 4.4 V	100	250	400	µA

8 Typical Characteristics

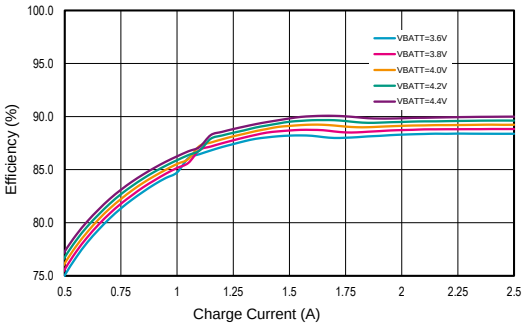

Figure 4: Efficiency V_{IN} = 12 V

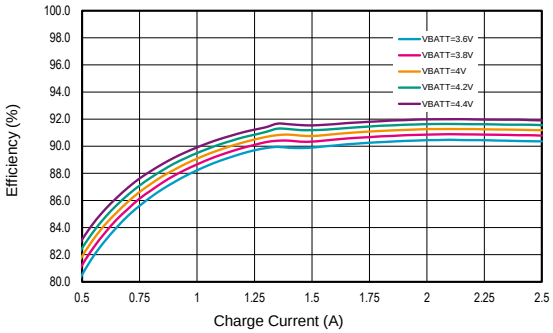

Figure 5: Efficiency V_{IN} = 9 V

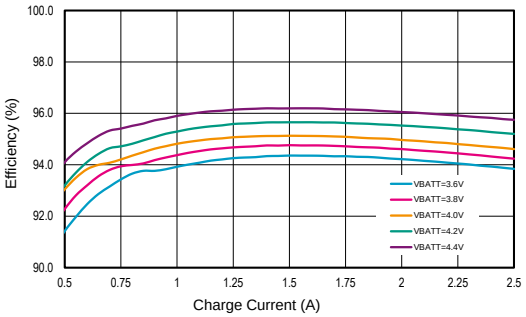

Figure 6: Efficiency V_{IN} = 5 V

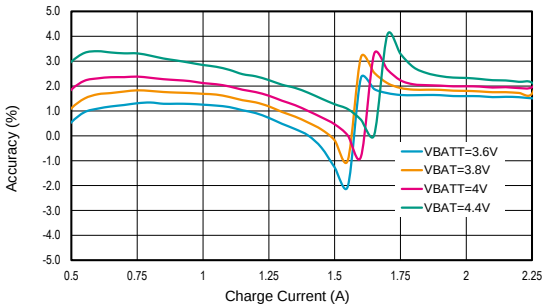

Figure 7: Accuracy V_{IN} = 12 V

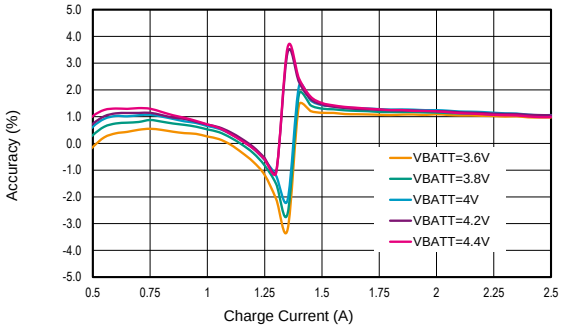

Figure 8: Accuracy V_{IN} = 9 V

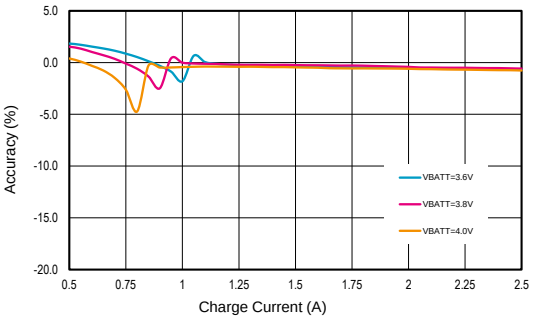

Figure 9: Accuracy V_{IN} = 5 V

9 System Block Diagram

A block diagram of a typical application is illustrated in Figure 10.

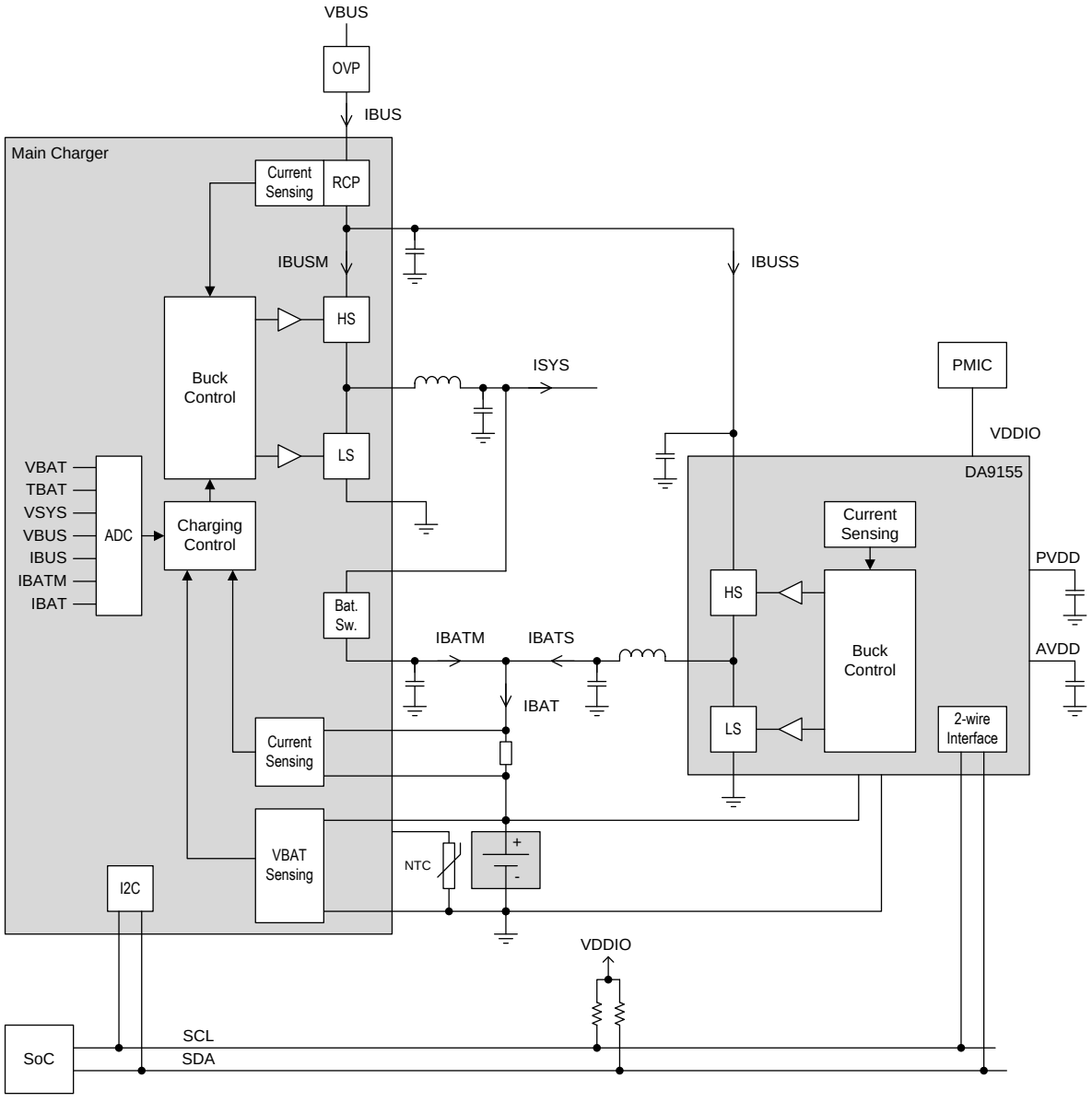

Figure 10: DA9155M System Block Diagram

2.5 A Companion Charger for Rapid Charging

9.1 Main Charger

The main charger is a fully featured charger that can operate as a stand-alone device. It is also designed to support an external slave charger. The main charger is responsible for the following functions:

- Charging control (pre-charge, CC, CV, JEITA)
- Battery detection
- Battery activation
- Battery pre-charge
- CV-phase
- IBUS sensing (IBUSM + IBUSS)
- Reverse-current protection
- IBATM regulation
- IBAT sensing (IBATM + IBATS)
- Battery isolation
- TBAT monitoring
- VBAT sensing

9.2 Slave Charger

The slave charger provides a regulated current (IBATS) and it is enabled only in the CC-phase of charging. The slave charger does not feature a VBAT regulation loop, and therefore, does not operate during CV-phase of charging. It is controlled by the application processor. The slave charger is responsible for the following functions:

- IBATS regulation
- Hazard detection (VBAT over- and undervoltage)

For more details about the slave charger operation and the system integration, please refer to the application note.

10 Functional Description

10.1 Control Signals

10.1.1 EN

The EN pin controls the BUCK_EN register. A rising edge sets the register and a falling edge clears it. The rising edge of the EN pin has to occur when DA9155M is in the disabled mode. The application processor can start the Buck by asserting the EN pin or by setting the BUCK_EN bit through the 2-wire interface.

The level of the EN pin can be read from S_EN_PIN register.

A fault condition in the system (VIN_DROP, VIN_OV, VIN_UV, VBAT_OV, VBAT_UV, VIO_UV, TJUNC_CRIT) de-asserts BUCK_EN and triggers a transition to the disabled mode. If a rising edge of the EN pin occurs while the fault condition remains, the Buck is not enabled and an event indicating a blocked enable is triggered (E_EN_BLOCK). Re-enabling the Buck after a fault condition requires that status and event bits are cleared.

The EN pin can be shorted to ground when not used.

10.1.2 nIRQ

nIRQ is a level sensitive interrupt signal. It can be configured either as a push-pull or as an open drain output (IRQ_TYPE), and the polarity can be selected (IRQ_LEVEL). The structure of the interrupt logic is depicted in Figure 11.

nIRQ is asserted when an un-masked event is asserted. The nIRQ will not be released until all event registers have been cleared. New events that occur during reading an event register will be held until the event register has been cleared, ensuring that the host processor does not miss them.

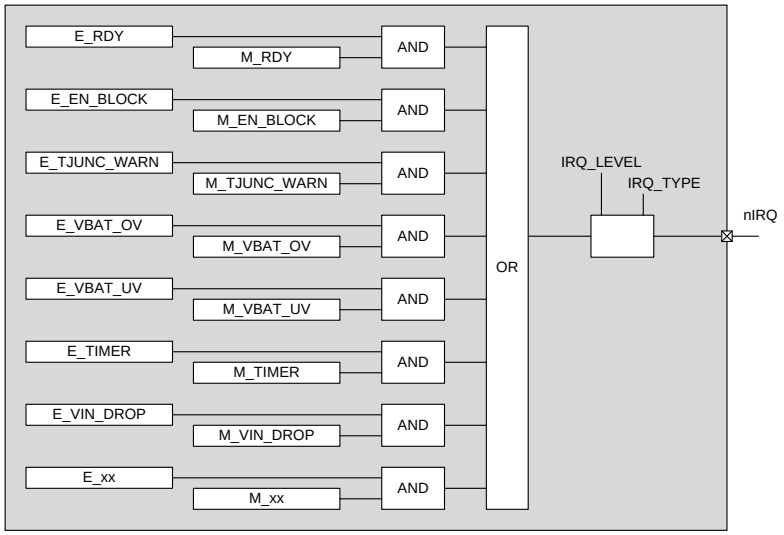

Figure 11: DA9155M Interrupt Logic

10.2 2-Wire Interface

The 2-wire interface provides access to control and status registers. The interface supports operations compatible to standard, fast, fast-plus and high speed mode of the I^2C bus specification Rev. 3.

Communication on the 2-wire bus is always between two devices, one acting as the master and the other as the slave. The DA9155M will only operate as a slave.

SCL carries the 2-wire clock and SDA carries the bi-directional data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 –20 kΩ). These are often shared between multiple devices connected to the interface. The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the DA9155M internal clock signals. DA9155M will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered in case the clock signal ceases to toggle for >35 ms (controlled in 2W_TO).

Bus clear, if the SDA is stuck, is achieved after receiving 9 clock pulses. Operation in high speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable spike suppression and slope control characteristics compatible to the I^2C specification. The high speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. The DA9155M does not make a use of clock stretching and delivers read data without additional delay up to 3.4 MHz.

Alternatively the interface can be configured to use high speed mode continuously via PM_IF_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus, but limits the attachable bus slaves to compatible devices.

10.2.1 Register Map Paging

The 2-wire interface has direct access to two pages of the register map (up to 256 addresses). The register at address zero on each page is used as a page control register (the LSB of the PAGE register is ignored). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting the REVERT register.

Alternatively, DA9155M offers a way to access register pages which avoids changing the active page via the PAGE register. DA9155M can respond to multiple consecutive slave addresses and update the PAGE register automatically based on the slave address. For example, when IF_BASE_ADDR = 0x58, the PAGE register responds to the slave address as follows:

Slave address = 0x58 ⇨ PAGE = 0x00

Slave address = 0x59 ⇨ PAGE = 0x02

Slave address = 0x5A ⇨ PAGE = 0x04

Slave address = 0x5B ⇨ PAGE = 0x06

The consecutive addresses are obtained by replacing the two LSB in IF_BASE_ADDR with “00”, “01”, “10”, or “11”. This feature can be enabled in the I2C_EXTEND_EN register.

10.2.2 Details of the 2-Wire Protocol

All data is transmitted across the 2-wire bus in 8-bit groups. To send a bit the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver’s shift register.

A two-byte serial protocol is used containing one address byte and one data byte. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in the high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in the high state. The START and STOP conditions are illustrated in Figure 12.

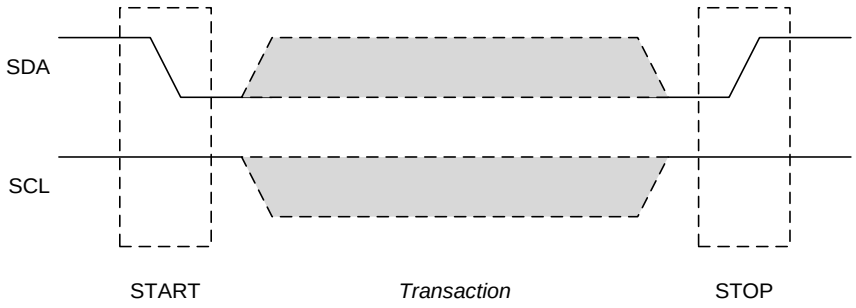

Figure 12: Timing of the START and STOP Conditions

The 2-wire bus will be monitored by DA9155M for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with ‘A’ in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. DA9155M responds to all bytes with an ACK. A register write operation is illustrated in Figure 13.

2.5 A Companion Charger for Rapid Charging

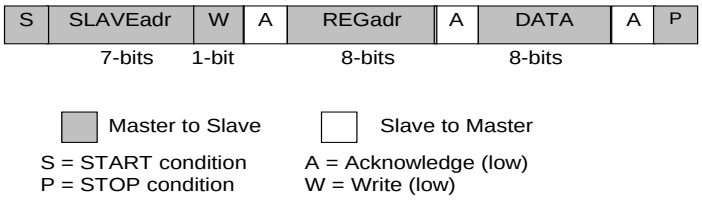

Figure 13: Byte Write Operation

When the host reads data from a register it first has to write-access DA9155M the target register address and then read-access DA9155M with a repeated START or alternatively a second START condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition. This is illustrated in Figure 14.

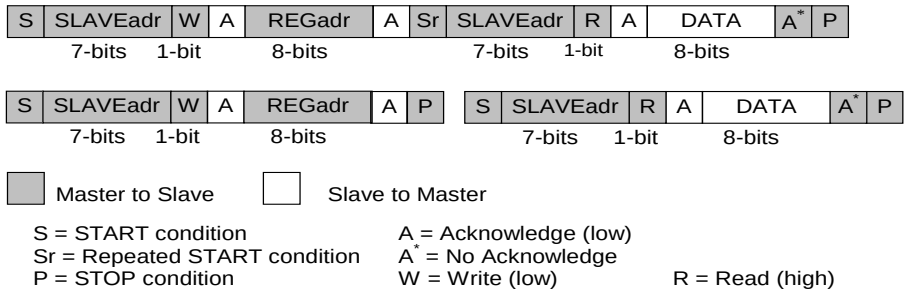

Figure 14: Examples of Byte Read Operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see Figure 15. The 2-wire control block then increments the address pointer to the next register address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK directly after receiving the data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then the DA9155M will return code zero.

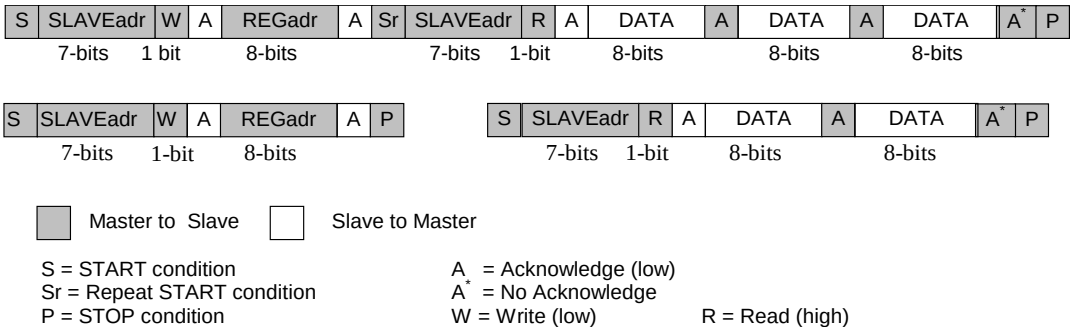

Figure 15: 2-Wire Page Read

The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in Figure 16.

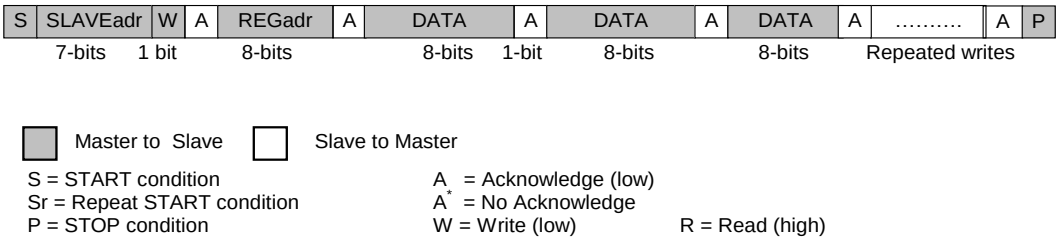

Figure 16: 2-Wire Page Write

Via control WRITE_MODE, a repeated write mode can be enabled. In this mode, the master can execute back-to-back write operations to non-consecutive addresses. This is achieved by transmitting register address and data pairs. The data will be stored in the address specified by the preceding byte. The repeated write mode is illustrated in Figure 17.

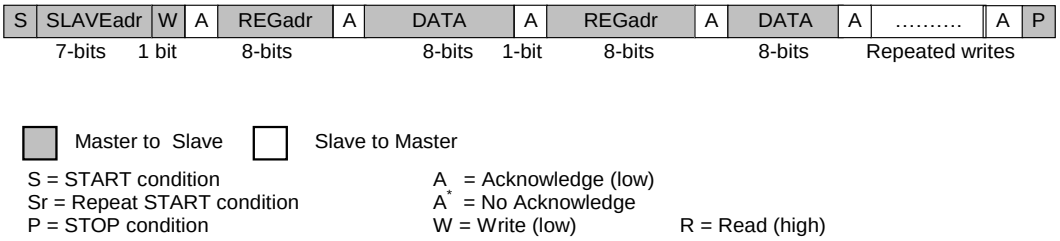

Figure 17: 2-Wire Repeated Write

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

10.3 Buck Converter

DA9155M features a Buck converter that provides up to 2.5 A of regulated output current, with I_{OUT_ACC} regulation accuracy.

The output current of the Buck can be selected from a control register (BUCK_IOUT). In order to limit inrush current from the power supply, the Buck converter features a soft-start function. Whenever the Buck is enabled or the output current is changed, the output current is ramped to the target value by running through the BUCK_IOUT steps at a rate defined by the START_SLEW and DEF_SLEW_RATE registers. As the names imply, START_SLEW is used when the Buck is enabled and DEF_SLEW_RATE is used when disabling the Buck or changing between IOUT settings. The slew rate timings are summarized in Table 14.

Table 14: Slew Rate Timings with Different Register Settings

SLEW[2:0]	Time per IOUT Step [µs]	Ramp Rate [mA/µs]	Ramp Time 250 mA to 2.5 A [µs]
0x5	10.67	0.938	2400
0x6	21.30	0.469	4800
0x7	42.70	0.234	9600

The Buck features a programmable peak current limit (BUCK_ILIM), which protects the pass devices and the inductor. Hitting the limit triggers an E_BUCK_ILIM event. During normal operation the E_BUCK_ILIM event should not occur. However, the event can be used as an indication of abnormal system behaviour.

The Buck is enabled either by writing directly to a control register BUCK_EN or asserting the EN input. The soft-start feature described above is effective when the Buck is enabled or disabled.

The switching frequency is chosen high enough to allow the use of a small 0.47 µH inductor. Furthermore, the switching frequency can be adjusted with the BUCK_FSW and OSC_FRQ registers in order to avoid interference to/from the main charger. The Buck also features an automatic

frequency fold back mode, where the switching frequency is stepwise reduced until a required duty cycle can be achieved. Without the frequency fold back the duty cycle is limited by the Buck's minimum off-time.

It is recommended to configure the switching frequency to 1 MHz when operating with 5 V V_{IN}.

10.4 Safety Timer

DA9155M features a safety timer that is intended to disable the Buck converter in the event of system malfunction during charging.

Whenever the Buck is enabled, either through the EN pin or from a register, the safety timer is loaded with a pre-programmed value (TIMER_LOAD) and it starts decrementing. In normal operation the application processor should periodically re-initialize the safety timer by writing a new value to the TIMER_LOAD register. The value of the counter can be read from the TIMER_COUNT register. However, if the timer reaches zero an event is asserted, and the Buck is automatically disabled. The BUCK_EN register is cleared and the Buck is stopped by ramping down the output current at a rate defined in SLEW_RATE. Resuming normal operation requires that the event is cleared.

10.5 V_{IN} Monitoring

V_{IN} is monitored to detect a power supply insertion, and to ensure that V_{IN} is within an acceptable voltage range. The monitoring is illustrated in Figure 18.

When V_{IN} is below the VIN2BAT threshold DA9155M stays in the no-power mode. When V_{IN} rises above the VIN2BAT threshold, DA9155M moves to the reset mode where the internal supply and reference are enabled.

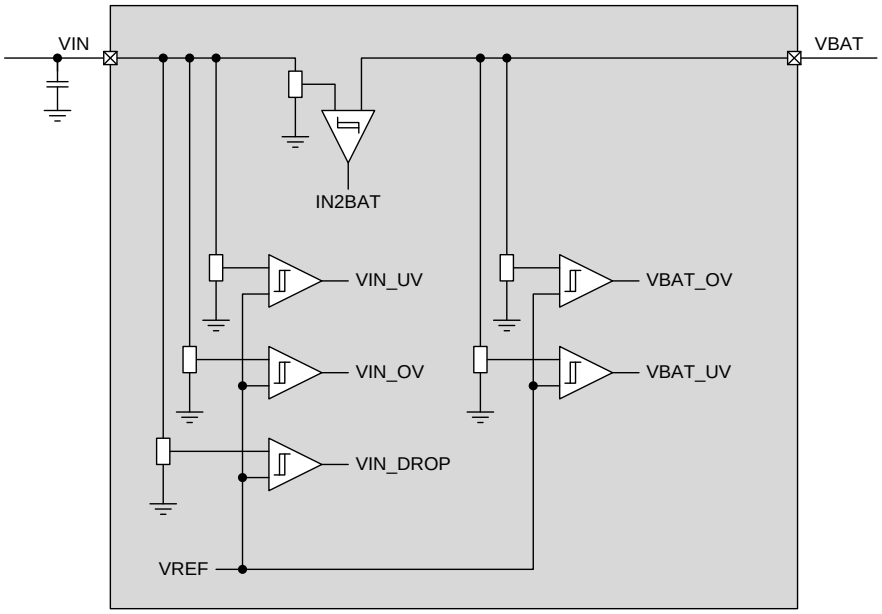

Figure 18: V_{IN} Monitoring of DA9155M

In reset, disabled, and active mode, V_{IN} is monitored against over- and undervoltage. If over- or undervoltage is detected, an event is triggered (E_VIN_OV, E_VIN_UV), the BUCK_EN register is cleared, and DA9155M moves to disabled mode. Re-enabling the Buck requires that the status and event bits are cleared.

During charging V_{IN} is monitored for weak charger or high impedance USB cable detection. If V_{IN} drops below the threshold V_{IN_DROP}, an event is triggered (E_VIN_DROP) and the Buck is automatically disabled. The BUCK_EN register is cleared and the Buck is stopped by ramping down the output current at a rate defined in DEF_SLEW_RATE. The Buck does not start automatically when the V_{IN} rises above the threshold. Resuming normal operation requires that the status and event bits are cleared. This feature is targeted for use cases where the V_{IN} is above the standard

V_{BUS}, in which case the undervoltage lockout is too low to detect a weak supply. By default, V_{IN_DROP} is set to the same voltage as the V_{IN_UVLO}, which effectively disables the V_{IN_DROP}.

The status of the V_{IN} monitoring comparators can be read out from the status registers (S_VIN_UV, S_VIN_OV, S_VIN_DROP).

10.6 V_{BAT} Monitoring

The V_{BAT} monitoring is illustrated in Figure 18. The slave charger has to monitor the battery voltage in case of fault conditions during charging, meaning that battery over- and undervoltage have to be detected.

DA9155M features two factory programmable settings for handling the monitoring:

1. An overvoltage or undervoltage event triggers an event (E_VBAT_OV, E_VBAT_UV) and the BUCK_EN register is de-asserted. Resuming normal operation requires that V_{BAT} is within normal range and the events are cleared. The supervision of the battery voltage V_{BAT} is done by comparators.
2. An overvoltage or undervoltage event does not disable the Buck converter. Only the status registers are updated (default).

The V_{BAT} monitoring status comparators can always be read out from the status registers (S_VBAT_UV, S_VBAT_OV).

10.7 Junction Temperature Supervision

To protect DA9155M from damage due to excessive power dissipation the junction temperature is monitored continuously. The monitoring is split into three temperature ranges T_{JUNC_WARN} (125 °C), T_{JUNC_CRIT} (140 °C), and T_{JUNC_POR} (150 °C).

If the junction temperature rises above the first threshold (TJUNC_WARN), the event E_TJUNC_WARN is asserted. If the event is not masked, this will fire an interrupt. This first level of temperature supervision is intended for non-invasive temperature control, where the necessary measures for cooling the system down are left to the host software. The status of the T_{JUNC_WARN} comparator can be read from S_TJUNC_WARN. The interrupt is only generated when the temperature crosses the threshold from low to high. After the interrupt, the application processor can read out the comparator status to detect when the temperature drops below the threshold.

If the junction temperature continues to rise and crosses the second threshold (T_{JUNC_CRIT}), an event is fired (E_TJUNC_CRIT), the BUCK_EN is de-asserted, and DA9155M moves to the disabled mode. Resuming normal operation requires that T_{JUNC} drops below T_{JUNC_CRIT} and the event is cleared.

There is also a third temperature threshold (T_{JUNC_POR}) which causes DA9155M to enter the reset mode. DA9155M stays in the reset mode as long as the junction temperature is above T_{JUNC_CRIT}.

2.5 A Companion Charger for Rapid Charging

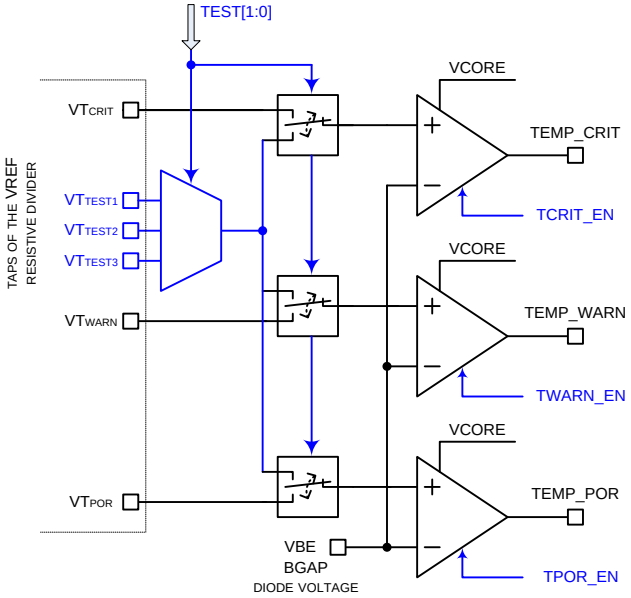

Figure 19: Junction Temperature Monitoring of DA9155M

10.8 Power Modes

The power modes of DA9155M are illustrated in Figure 20.

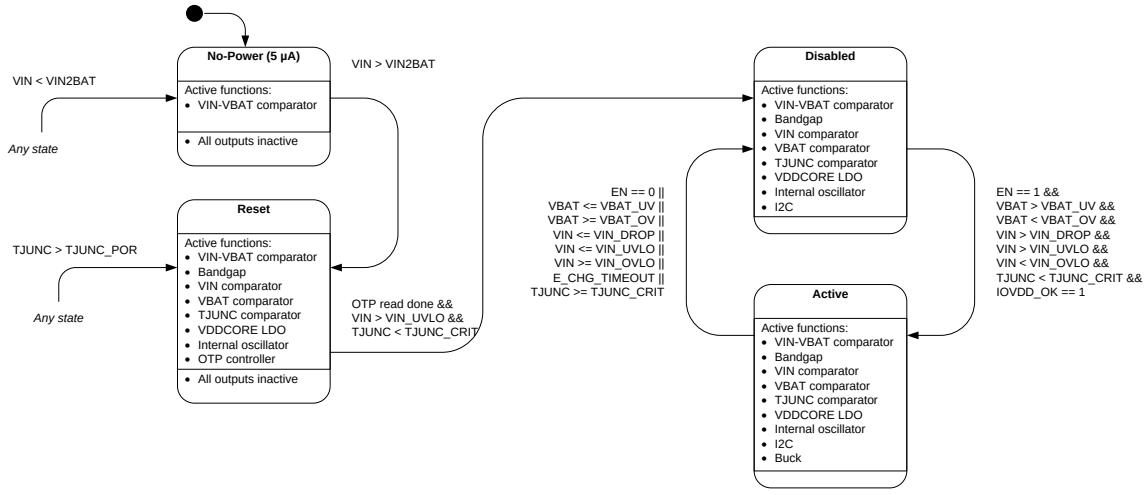

Figure 20: Power Modes of DA9155M.

Note 1 The conditions for state transitions follow the C-language syntax.

10.8.1 No-Power

The no-power mode is the initial state of DA9155M. Only the V_{IN}-V_{BAT} comparator is active in this state. When V_{IN} rises above V_{BAT}, DA9155M enters the reset mode. All IOs are in their inactive state. The no-power mode is entered whenever V_{IN} drops below V_{BAT}.

10.8.2 Reset

DA9155M enters the reset mode when a power supply is attached and V_{IN} rises above V_{BAT}. In the reset mode, DA9155M will enable the internal reference, the internal supply, execute the reset sequence, and read the OTP. Once the OTP is read and all the V_{IN} conditions are met, DA9155M moves automatically to the disabled mode.

The junction temperature monitoring is also enabled in the reset mode. If a junction over-temperature is detected during operation (TJUNC ≥ TJUNC_POR), DA9155M moves back to the reset mode.

10.8.3 Disabled

In the disabled mode DA9155M is fully functional but the Buck has not been enabled. An event is fired when entering the disabled mode to notify the application processor that the slave charger is ready for operation. If a fault condition exists (T_{JUNC}, V_{BAT}, or V_{IN}), the enable signal is blocked, DA9155M stays in the disabled mode, and an event is triggered.

DA9155M moves to the active mode when the Buck is enabled either by asserting the EN signal or by setting the BUCK_EN register.

10.8.4 Active

In the active mode DA9155M is fully functional and the Buck is running.

DA9155M moves back to the disabled mode if the Buck is disabled, the safety timer expires, or if there is a fault condition (T_{JUNC}, V_{BAT}, or V_{IN}).

11 Register Map

11.1 Overview

Addr	Register	7	6	5	4	3	2	1	0
Page Control									
0x000	PAGE_CTRL_0	REVERT	WRITE_MODE	PAGE					
Status And Events									
0x001	STATUS_A	S_EN_BLOCK	S_VIN_OV	S_VIN_DROP	S_VIN_UV	S_VBAT_OV	S_VBAT_UV	S_TJUNC_CRIT	S_TJUNC_WARN
0x002	STATUS_B						S_BUCK_ILIM	S_EN_PIN	MODE
0x003	EVENT_A	E_EN_BLOCK	E_VIN_OV	E_VIN_DROP	E_VIN_UV	E_VBAT_OV	E_VBAT_UV	E_TJUNC_CRIT	E_TJUNC_WARN
0x004	EVENT_B				E_TJUNC_POR	E_VDDIO_UV	E_TIMER	E_BUCK_ILIM	E_RDY
0x005	IRQ_MASK_A	M_EN_BLOCK	M_VIN_OV	M_VIN_DROP	M_VIN_UV	M_VBAT_OV	M_VBAT_UV	M_TJUNC_CRIT	M_TJUNC_WARN
0x006	IRQ_MASK_B				M_TJUNC_POR	M_VDDIO_UV	M_TIMER	M_BUCK_ILIM	M_RDY
VIN And VBAT Monitoring									
0x007	CONTROL_A	VIN_DROP							
0x008	CONTROL_B			VBAT_UV					
0x009	CONTROL_C			VBAT_OV					
Configuration									
0x00A	CONTROL_D		START_SLEW				DEF_SLEW_RATE		
0x00B	CONTROL_E				TIMER_DIS	TJUNC_WARN			
Safety Timer									
0x00C	TIMER_A	TIMER_COUNT							
0x00D	TIMER_B	TIMER_LOAD							
Buck Control									
0x00E	BUCK_CTRL								BUCK_EN
0x00F	BUCK_ILIM				BUCK_ILIM				
0x010	BUCK_IOUT	BUCK_IOUT							
Interface									
0x011	INTERFACE	IF_BASE_ADDR							
0x012	CONFIG_A	VDDIO_CONF		I2C_EXTEND_EN	2W_TO	2W_IF_HSM		IRQ_LEVEL	IRQ_TYPE
Configuration									
0x013	CONFIG_B	OSC_FRQ						BUCK_FSW	
Page Control									
0x080	PAGE_CTRL_1	REVERT	WRITE_MODE	PAGE					
Page Control									
0x100	PAGE_CTRL_2	REVERT	WRITE_MODE	PAGE					
Page Control									
0x180	PAGE_CTRL_3	REVERT	WRITE_MODE	PAGE					
Page Control									
0x200	PAGE_CTRL_4	REVERT	WRITE_MODE	PAGE					
Page Control									
0x280	PAGE_CTRL_5	REVERT	WRITE_MODE	PAGE					
Page Control									
0x300	PAGE_CTRL_6	REVERT	WRITE_MODE	PAGE					
Trimming and Engineering									
0x319	ANA_ENG_OTP_9	ENG_VDDIO_UV_DIS		ENG_TJUNC_CRIT_DIS	ENG_VBAT_OV_DIS	ENG_VBAT_UV_DIS		ENG_VIN_DROP_DIS	

11.2 Register Descriptions
11.3 Page 0

11.3.1 Page Control

PAGE_CTRL_0 (0x000)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.3.2 Status and Events

STATUS_A (0x001)

Field	Slice	Description
S_EN_BLOCK	7:7	A status bit in STATUS_A is blocking the buck from being enabled.
S_VIN_OV	6:6	VIN overvoltage comparator status
S_VIN_DROP	5:5	VIN DROP comparator status
S_VIN_UV	4:4	VIN undervoltage comparator status
S_VBAT_OV	3:3	VBAT overvoltage comparator status
S_VBAT_UV	2:2	VBAT undervoltage comparator status.
S_TJUNC_CRIT	1:1	TJUNC CRIT comparator status
S_TJUNC_WARN	0:0	TJUNC_WARN comparator status

STATUS_B (0x002)

Field	Slice	Description
Reserved	8:3	
S_BUCK_ILIM	2:2	Status (debounced) of the peak current comparator.
S_EN_PIN	1:1	Status of the EN pin.
MODE	0:0	DA9155M mode: disabled (0) or active (1).

EVENT_A (0x003)

Field	Slice	Description
E_EN_BLOCK	7:7	An enable signal was blocked. The reason for the blocking can be read out from the STATUS_A register.
E_VIN_OV	6:6	VIN exceeded the VIN_OVLO threshold.
E_VIN_DROP	5:5	VIN dropped below the VIN_DROP threshold.
E_VIN_UV	4:4	VIN dropped below the VIN_UVLO threshold.
E_VBAT_OV	3:3	The battery voltage exceeded the VBAT_OV threshold.
E_VBAT_UV	2:2	The battery voltage dropped below the VBAT_UV threshold.

E_TJUNC_CRIT	1:1	The junction temperature exceeded the TJUNC_CRIT threshold.
E_TJUNC_WARN	0:0	Junction temperature crossed the TJUNC_WARN threshold. Only a low-to-high transition triggers the event.

EVENT_B (0x004)

Field	Slice	Description
Reserved	7:5	
E_TJUNC_POR	4:4	The junction temperature crossed the TJUNC_POR threshold and caused an entry to the reset mode. This bit is only reset upon a transition from the no-power mode to the reset mode.
E_VDDIO_UV	3:3	VDDIO dropped below a threshold. This event causes the I2C interface to be reset.
E_TIMER	2:2	The safety timer expired.
E_BUCK_ILIM	1:1	The peak output current exceeded the limit BUCK_ILIM.
E_RDY	0:0	DA9155M moved to the disabled mode. The event is not generated if VDDIO is below the monitoring threshold (VDDIO_CONF).

IRQ_MASK_A (0x005)

Field	Slice	Description
M_EN_BLOCK	7:7	Mask bit for E_EN_BLOCK
M_VIN_OV	6:6	Mask bit for E_VIN_OV
M_VIN_DROP	5:5	Mask bit for E_VIN_DROP
M_VIN_UV	4:4	Mask bit for E_VIN_UV
M_VBAT_OV	3:3	Mask bit for E_VBAT_OV
M_VBAT_UV	2:2	Mask bit for E_VBAT_UB
M_TJUNC_CRIT	1:1	Mask bit for E_TJUNC_CRIT
M_TJUNC_WARN	0:0	Mask bit for E_TJUNC_WARN

IRQ_MASK_B (0x006)

Field	Slice	Description
Reserved	7:5	
M_TJUNC_POR	4:4	Mask bit for E_TJUNC_POR
M_VDDIO_UV	3:3	Mask bit for E_VDDIO_UV
M_TIMER	2:2	Mask bit for E_TIMER
M_BUCK_ILIM	1:1	Mask bit for E_BUCK_ILIM
M_RDY	0:0	Mask bit for E_RDY

11.3.3 VIN and VBAT Monitoring

CONTROL_A (0x007)

Field	Slice	Description
VIN_DROP	7:0	VIN drop threshold. N=0x0,0x1,...,0xE: VIN_DROP=4.3+(N×0.05) V

		N=0xF,0x10,...,0x1D: VIN_DROP=5.0+((N-0xE)×0.2) V N=0x1E,0x1F,...,0x27: VIN_DROP=8.0+((N-0x1D)×0.1) V N=0x28,0x29,...,0x31: VIN_DROP=9.0+((N-0x27)×0.2) V N=0x32,0x33,...,0x3B: VIN_DROP=11.0+((N-0x31)×0.1) V The maximum value is 12.0 V (0x3B). Any value greater than the maximum will be stored in the register but limited to the maximum at the output.

CONTROL_B (0x008)

Field	Slice	Description
Reserved	7:6	
VBAT_UV	5:0	VBAT undervoltage. VBAT_UV=2.0+(N×0.025) V.

CONTROL_C (0x009)

Field	Slice	Description
Reserved	7:6	
VBAT_OV	5:0	VBAT overvoltage. VBAT_OV=3.6+(N×0.025) V.

11.3.4 Configuration

CONTROL_D (0x00A)

Field	Slice	Description
Reserved	7:7	
START_SLEW	6:4	Slew rate control for the buck start. The enumeration is the same as DEF_SLEW_RATE
Reserved	3:3	
DEF_SLEW_RATE	2:0	Slew rate control for the output current changes. Each output current step (10 mA) is delayed with T_STEP=OSC/(2^N1), where OSC is the high frequency oscillator (6 MHz default). The minimum value for N is 5 (101). The effective slew rate is then given by the current change (I_DELTA), the number of steps required for the change (I_DELTA/10 mA), and the time spend in each step (T_STEP): SLEW_RATE=I_DELTA/((I_DELTA/10 mA)×T_STEP)

CONTROL_E (0x00B)

Field	Slice	Description
Reserved	7:5	
TIMER_DIS	4:4	Disables the safety timer. 1 = Safety timer disabled 0 = safety timer enabled
TJUNC_WARN	3:0	Junction temperature warning threshold. TJUNC_WARN=70+(N×5) °C

11.3.5 Safety Timer

TIMER_A (0x00C)

Field	Slice	Description
TIMER_COUNT	7:0	Countdown value of the safety timer. Decremented at 1 s intervals. Reading the register gives the current timer value. Writing the register has no affect.

TIMER_B (0x00D)

Field	Slice	Description
TIMER_LOAD	7:0	Safety timer pre-load and re-load. Writing the register when the buck is not enabled sets the pre-load value. The pre-load value is automatically loaded in to TIMER_COUNT the next time the buck is enabled. Writing the register during buck operation loads the written value in to TIMER_COUNT. TIMER_LOAD provides the time in seconds. The minimum value is 0 s (0x00). The maximum value is 255 s (0xFF). The default is set to the maximum time (0xFF).

11.3.6 Buck Control

BUCK_CTRL (0x00E)

Field	Slice	Description
Reserved	7:1	
BUCK_EN	0:0	Buck enable. The register is also set at the rising edge of the EN pin and cleared at the falling edge.

BUCK_ILIM (0x00F)

Field	Slice	Description
Reserved	7:5	
BUCK_ILIM	4:0	Peak current limit. BUCK_ILIM=(3000+N×100) mA The maximum value is 5.5 A (0x19). Any value greater than the maximum will be stored in the register but limited to the maximum at the output

BUCK_IOUT (0x010)

Field	Slice	Description
BUCK_IOUT	7:0	Buck output current. IOUT=250+(N×10) mA The minimum value is 400 mA (0x0F). The maximum value is 2.5 A (0xE1). Any value greater than the maximum will be stored in the register but limited to the maximum at the output.

11.3.7 Interface

INTERFACE (0x011)

Field	Slice	Description
IF_BASE_ADDR	7:1	Slave address of DA9155M.
Reserved	0:0	

CONFIG_A (0x012)

Field	Slice	Description
VDDIO_CONF	7:6	VDDIO monitoring threshold. 00: 1.5 V 01: 1.8 V 10: 3.3 V 11: 3.6 V
I2C_EXTEND_EN	5:5	Enable PAGE decoding from the 3 LSBs of the incoming slave address. 0: DA9155M responds normally to the I2C slave address programmed in IF_BASE_ADDR. The register map page is changed by writing to the PAGE register. 1: DA9155M will respond to multiple the slave addresses and decode the PAGE from the 3 LSBs. IF_BASE_ADDR[7:4] + 0: PAGE = 0x00 IF_BASE_ADDR[7:4] + 1: PAGE = 0x02 IF_BASE_ADDR[7:4] + 2: PAGE = 0x04 IF_BASE_ADDR[7:4] + 3: PAGE = 0x06.
2W_TO	4:4	Enable 35 ms timeout for the 2-wire interface.
2W_IF_HSM	3:3	Puts the 2-wire interface permanently in high-speed mode.
Reserved	2:2	
IRQ_LEVEL	1:1	Selects the polarity of nIRQ: active low (0) or active high (1).
IRQ_TYPE	0:0	Select the type of nIRQ output: open-drain (0) or push-pull (1).

11.3.8 Configuration

CONFIG_B (0x013)

Field	Slice	Description
OSC_FRQ	7:4	Oscillator frequency tuning: 0000: no tune 0001: +200 kHz 0010: +400 kHz 0011: +600 kHz 0100: +800 kHz 0101: +1000 kHz 0110: +1200 kHz 0111: no tune 1000: no tune 1001: -200 kHz 1010: -400 kHz 1011: -600 kHz

		1100: -800 kHz 1101: -1000 kHz 1110: -1200 kHz 1111: no tune
Reserved	3:2	
BUCK_FSW	1:0	Switching frequency of the buck converter. The buck clock is a divided version of the tuned oscillator frequency OSC. 00: OSC/5 01: OSC/3 10: OSC/4 11: OSC/6

11.4 Page 1

11.4.1 Page Control

PAGE_CTRL_1 (0x080)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.5 Page 2

11.5.1 Page Control

PAGE_CTRL_2 (0x100)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.6 Page 3

11.6.1 Page Control

PAGE_CTRL_3 (0x180)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access

WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.7 Page 4

11.7.1 Page Control

PAGE_CTRL_4 (0x200)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.8 Page 5

11.8.1 Page Control

PAGE_CTRL_5 (0x280)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.9 Page 6

11.9.1 Page Control

PAGE_CTRL_6 (0x300)

Field	Slice	Description
REVERT	7:7	0: PAGE maintains its value until re-written 1: PAGE reverts to 0 after one access
WRITE_MODE	6:6	Behavior upon sequential write accesses over the 2-wire interface 0: Write data to consecutive addresses 1: Write data to arbitrary addresses using address-data pairs
PAGE	5:0	Top 6 bits of the register address.

11.9.2 Trimming and Engineering

ANA_END_OTP_9 (0x319)

Field	Slice	Description
ENG_VDDIO_UV_DIS	7:7	0: VDDIO monitoring is enabled 1: VDDIO monitoring is disabled
Reserved	6:6	
ENG_TJUNC_CRIT_DIS	5:5	0: TJUNC CRIT comparator is enabled 1: TJUNC CRIT comparator is disabled
ENG_VBAT_OV_DIS	4:4	0: VBAT over voltagecomparator is enabled 1: VBAT overvoltage comparator is disabled
ENG_VBAT_UV_DIS	3:3	0: VBAT undervoltage comparator is enabled 1: VBAT undervoltage comparator is disabled
Reserved	2:2	
ENG_VIN_DROP_DIS	1:1	0: VIN DROP comparator is enabled 1: VIN DROP comparator is disabled
Reserved	0:0	

12 Application Information

12.1 PCB Layout

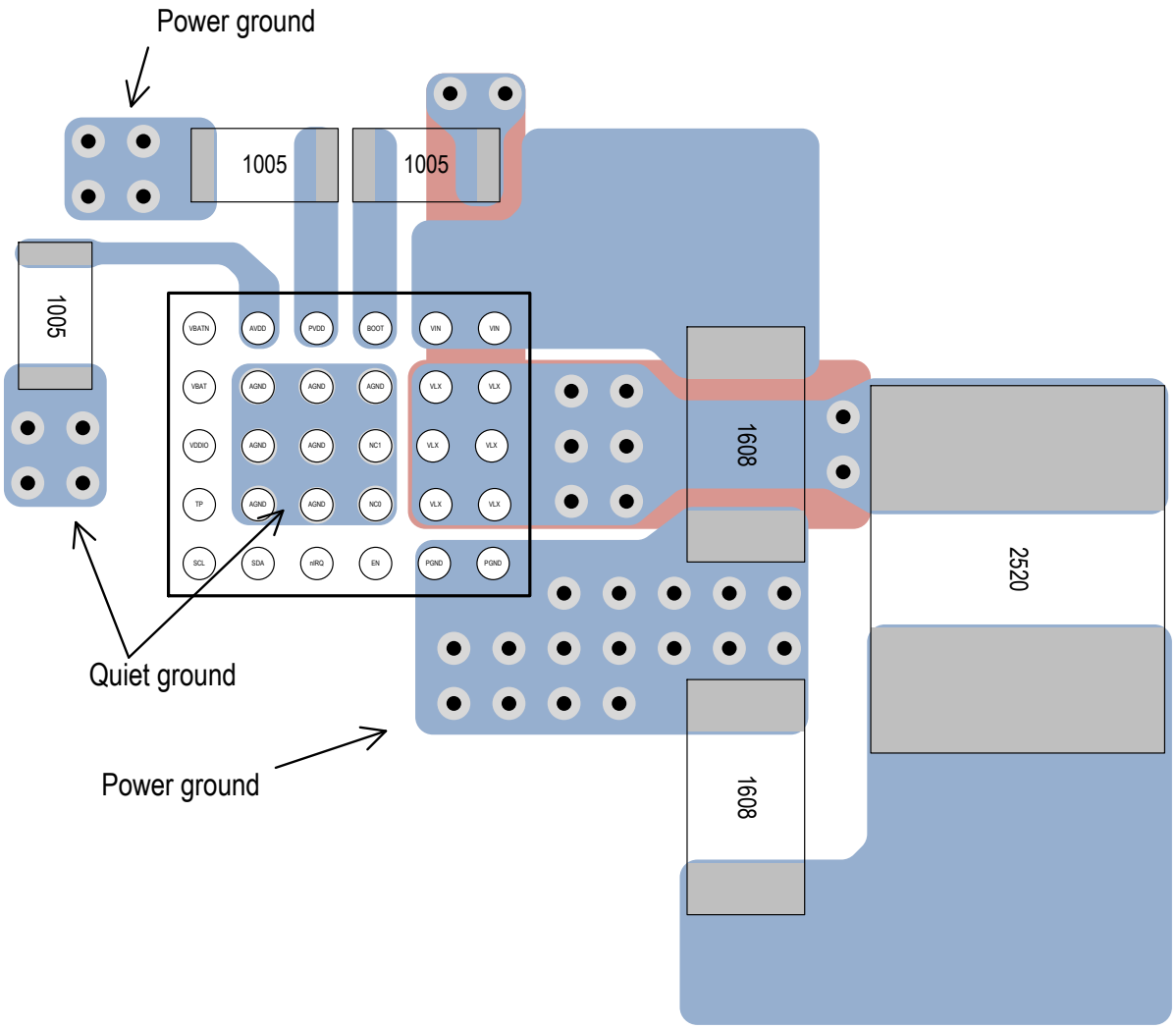

Figure 21: Preliminary PCB Layout for DA9155M

Note 1 Component sizes in mm.

It is recommended to create a separate quiet ground for the AVDD capacitor connection. The PCB layout should ensure this ground is kept quiet, for example, they should be separated from the main noisy power ground return path. The quiet ground can then be connected to the main ground at the ground plane.

12.2 Component Selection

12.2.1 Capacitors

Ref	Value	Size Code [mm]	Temp. Char.	Tol.	Rating	Part
Buck input bypass	10 µF	1608	X5R	±20%	25 V	CL10A106MA8NRNC
	10 µF	1608	X5R	±20%	25 V	Murata GRM188R61E106MA73
Buck output	22 µF	1608	X5R	±20%	6.3 V	Murata GRM188R60J226MEA0

Ref	Value	Size Code [mm]	Temp. Char.	Tol.	Rating	Part
bypass	10 µF	1608	X5R	±20%	6.3 V	GRM188R60J106ME84
Buck bootstrap	10 nF	0603	X5R	±10%	16 V	CL03A103KO3NNNC
	10 nF	1005	X7R	±10%	16 V	Murata GRM15XR71C103KA86
AVDD output bypass	2.2 µF	1005	X5R	±20%	6.3 V	CL05A225MQ5NSDC
	2.2 µF	1005	X5R	±20%	6.3 V	Murata GRM155R60J225ME95
PVDD output bypass	2.2 µF	1005	X5R	±20%	6.3 V	CL05A225MQ5NSDC
	2.2 µF	1005	X5R	± 20%	6.3 V	Murata GRM155R60J225ME95

12.2.2 Inductor

Ref	Value	ISAT [A]	IRMS [A]	DCR (typ) [mΩ]	Size (L×W×H) [mm]	Part
Buck	0.47 µH	6.0	4.5	24	2.5×2.0×1.0	CIGT252010LMR47MNE

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This data sheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This data sheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This data sheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing, and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This data sheet contains the specifications for discontinued products. The information is provided for reference only.

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Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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