8 Channel System PMIC supporting DDR VTT

General Description

DA9281 is an 8-channel power management integrated circuit (PMIC) with 4 buck regulators, 3 LDOs and 1 voltage buffer to support DDR VTT termination.

Key functions for power applications, such as soft-start, selectable preset output voltage, flexible power-up and power-down sequences are provided on chip and are programmable via the I²C interface with non-volatile memory defaults.

All 8 channels have an output discharge function and protections features such as over-current protection (OCP), over voltage protection (OVP), and under voltage protection (UVP).

Key Features

- 4.5 V to 5.5 V input voltage
- BUCK (CH1 to CH4)
  - Output current 5.0 A at 0.8 to 3.0 V (CH1)
  - Output current 2.5 A at 0.8 to 3.3 V (CH2)
  - Output current 2.5 A at 0.8 to 3.6 V (CH3)
  - Output current 2.5 A at 0.8 to 3.3 V (CH4)
  - Operation frequency 2 MHz
  - Discharge function
  - Soft-start function
- LDO (CH6 to CH8)
  - Output current 0.2 A at 2.5 V (CH6)
  - Output current 0.2 A at 1.8/3.3 V (CH7)
  - Output current 1.6 A at 1.8 V (CH8)
  - Discharge function
  - Soft-start function
- Termination Voltage Regulator (CH5)
  - Output current -0.5 A to 0.5 A at CH4 = 1.2 V or CH4 = 1.35 V
  - Discharge function
  - Soft-start function
- I²C digital interface
- Protection features: OCP, OVP, UVP for all channels
- Parameters of output voltage can be changed by I²C control
- Programmable sequencer by I²C control
- -40 °C to +85 °C ambient temperature range
- QFN-40 5 mm x 5 mm 0.4 mm pitch package

System Diagram

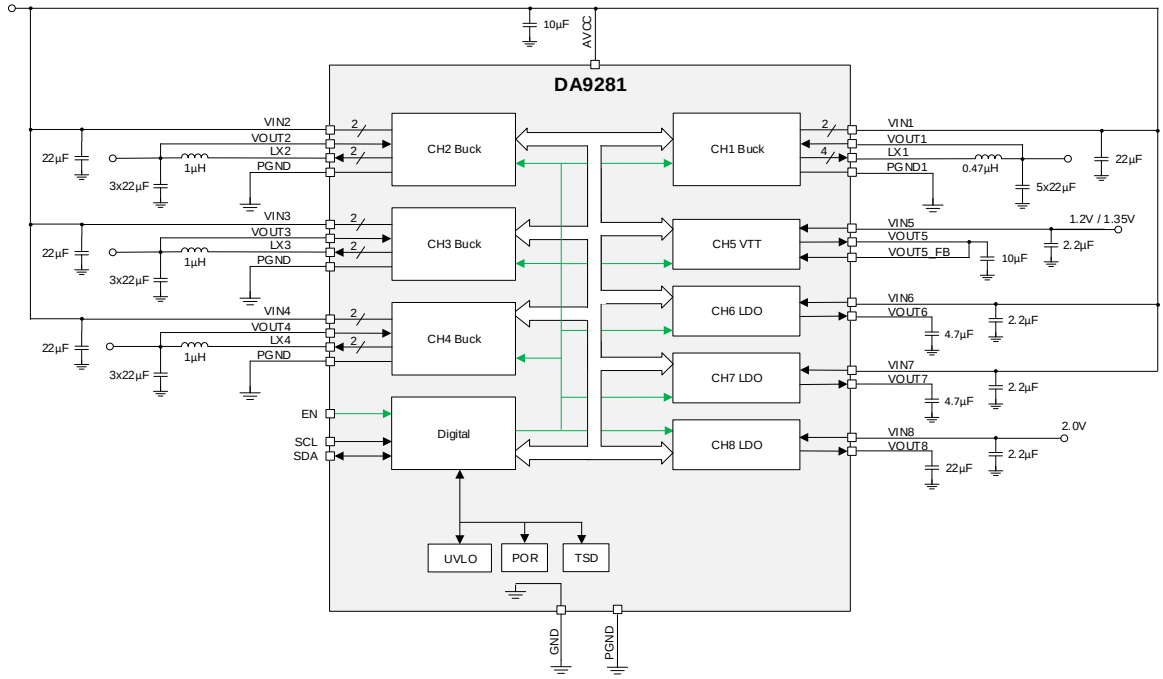

Figure 1: System Diagram

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1 Terms and Definitions

OCP	Over-current protection
OVP	Over-voltage protection
PMIC	Power management integrated circuit
POR	Power on reset
TSD	Thermal shutdown sequence
UVLO	Under-voltage lockout
UVP	Under-voltage protection
VTT	Termination voltage regulator

2 Block Diagram

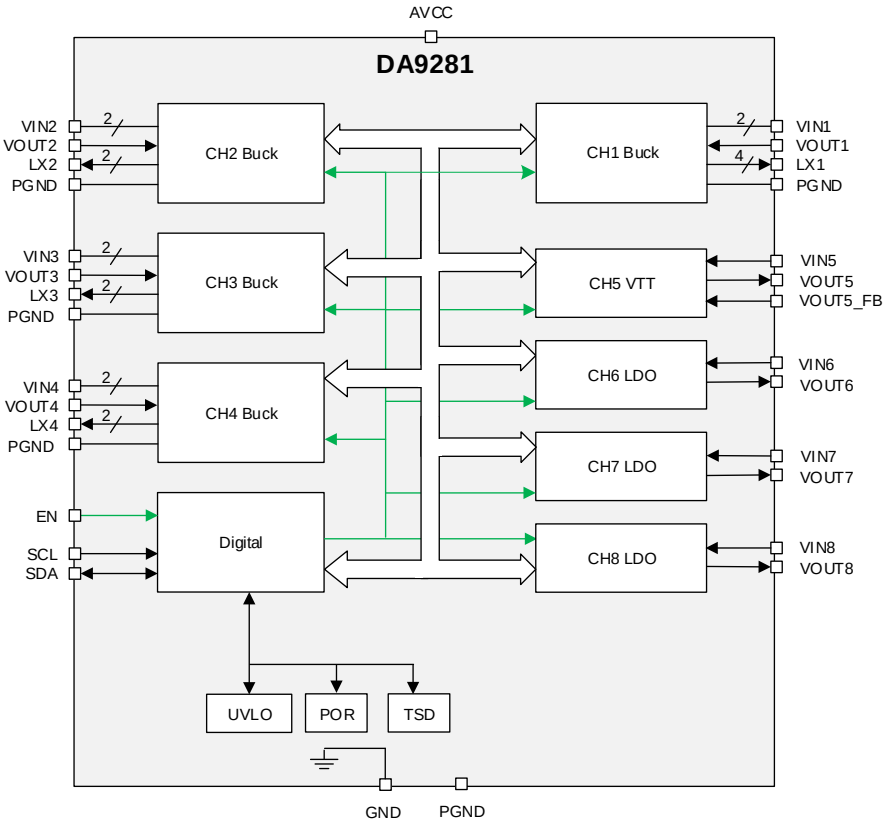


Figure 2: Block Diagram

3 Pinout

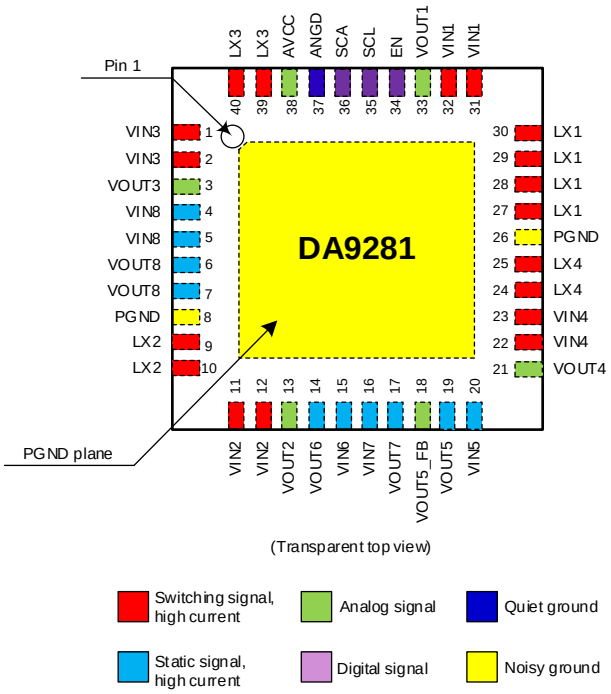


Figure 3: 40 Lead QFN 0.4 mm Pitch Package Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Max Voltage (V)	Max Current (A)	Description
1,2	VIN3	PWR			Input voltage for CH3 buck converter
3	VOUT3	AI			Output voltage feedback of CH3 buck converter
4,5	VIN8	PWR			Input voltage for CH8 LDO
6,7	VOUT8	AO			Output voltage of CH8 LDO
8	PGND	GND			Power ground
9,10	LX2	AO			SW node of CH2 buck converter
11,12	VIN2	PWR			Input voltage for CH2 buck converter
13	VOUT2	AI			Output voltage feedback of CH2 buck converter
14	VOUT6	AO			Output voltage of CH6 LDO
15	VIN6	PWR			Input voltage for CH6 LDO
16	VIN7	PWR			Input voltage for CH7 LDO
17	VOUT7	AO			Output voltage of CH7 LDO
18	VOUT5_FB	AI			Output voltage feedback of CH5 regulator
19	VOUT5	AO			Output voltage of CH5 regulator
20	VIN5	PWR			Input voltage for CH5 regulator
21	VOUT4	AI			Output voltage feedback of CH4 buck converter
22,23	VIN4	PWR			Input voltage for CH4 buck converter
24,25	LX4	AO			SW node of CH4 buck converter

Pin #	Pin Name	Type (Table 2)	Max Voltage (V)	Max Current (A)	Description
26	PGND	GND			Power ground
27-30	LX1	AO			SW node of CH1 buck converter
31,32	VIN1	PWR			Input voltage for CH1 buck converter
33	VOUT1	AI			Output voltage feedback of CH1 buck converter
34	EN	DI			Enable pin
35	SCL	DI			2-wire I^2C clock
36	SDA	DIO			2-wire I^2C data input/output
37	AGND	GND			Quiet analog ground
38	AVCC	PWR			Quiet analog supply
39,40	LX3	AO			SW node of CH3 buck converter
Paddle	PGND	GND			Common ground for all channels

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection
PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-60	+150	°C
T_A	Operating temperature		-40	+85	°C
T_J	Junction temperature		-40	+125	°C
A_{VCC}	Power supply input		-0.3	6.0	V
V_{INx}	Power supply inputs		-0.3	V_{AVCC} + 0.3 Note 1	V
LX_X	SW node		-0.3	V_{INX} + 0.3 Note 2	V
V_{OUTx}	LDO output pins		-0.3	V_{INX} + 0.3 Note 2	V
SCL/SDA	Digital input pins		-0.3	6.0	V
	Max. input voltage	All other pins	-0.3	V_{AVCC} + 0.3 Note 1	V
	Max. power dissipation	T_A = 85°C		1.43	W
	Package thermal resistance		28		°C/W
	ESD tolerance	HBM		2	kV
	ESD tolerance	CDM		500	V

Note 1 Voltage must not exceed 6.0 V.

Note 2 Voltage must not exceed 6.0 V and must not exceed V_{AVCC} + 0.3 V.

4.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating temperature		-40		+85	°C
V_{AVCC}	Supply voltage (AVCC)		4.5	5	5.5	V
V_{INX}	Supply voltages	X=1,2,3,4,6,7	4.5	5	5.5	V
V_{IN5}	Supply voltage (CH5)	V_{OUT4} = 1.2 V	1.176	1.2	1.224	V
		V_{OUT4} = 1.35 V	1.323	1.35	1.377	
V_{IN8}	Supply voltage (CH8)		1.98	2	2.12	V

4.3 Electrical Characteristics

4.3.1 Current Consumption Characteristics

Table 5: Current Consumption Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$I_{VIN\_AVCC\_OFF}$	Current in OFF state (EN = LOW)	Total current from all VIN pins and AVCC pin V_{AVCC} = 5 V T_A = 85 °C for maximum spec		20	50	µA
$I_{VIN\_AVCC\_ACTIVE}$	Current in ACTIVE state (EN = HIGH)	Total current from all VIN pins and AVCC pin No load, no switching V_{AVCC} = 5 V T_A = 85 °C for maximum spec		600	2000	µA

4.3.2 Supervisory Characteristics

Table 6: Supervisory Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
Under-Voltage Lockout						
V_{UVLO_FALL}	UVLO falling threshold	At AVCC (Shutdown sequence is triggered)	3.7	3.8	3.9	V
V_{UVLO_HYS}	UVLO hysteresis	At AVCC	80	100	120	mV
V_{POR_FALL}	POR falling threshold	At AVCC (All channels are disabled immediately)	3.05		3.5	V
V_{DIGPOR_FALL}	Digital POR falling threshold	At AVCC (Digital Core Power-On-Reset)	2.5		3.05	V
V_{DIGPOR_HYS}	Digital POR hysteresis	At AVCC		175		mV
Under-Voltage Protection						
V_{UVP_FALL}	Under-voltage protection threshold	All channels	65	70	75	%
t_{UVP_DET}	UVP detect time			100		µs
Over-Voltage Protection						
V_{OVP_RISE}	Over-voltage protection threshold	All channels	115	120	125	%
t_{OVP_DET}	OVP detect time			100		µs
Thermal Shutdown						
T_{SHDN}	Thermal shutdown rising threshold			140	150	°C
T_{SHDN_HYS}	Thermal shutdown hysteresis			15		°C

4.3.3 CH1 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN1} ≤ 5.5 V.

Table 7: CH1 Buck Converter Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN1}	Input voltage	At VIN1 pin	4.5	5	5.5	V
C_{OUT}	Output Capacitance	Including voltage and temperature coefficient	44	88	105.6	µF
ESR_{COUT}	ESR of C_{OUT}	f > 100 kHz + track impedance			10	mΩ
L	Inductor value	Including current and temperature dependence	0.22	0.47	0.57	µH
ESR_{LBUCK}	Inductor resistance			23		mΩ
Electrical Performance						
V_{OUT}	Output voltage	BUCK1_OPT_CTRL6 = 0b 10 mV step	0.8		2.2	V
		BUCK1_OPT_CTRL6 = 1b 20 mV step	1.6		3.0	V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation PWM operation	-2.5		2.5	%
$V_{OUT\_ACC\_PFM}$	Overall output accuracy	Including load and line regulation PFM operation	-2.5		4.5	%
V_{OUT_RPL}	Output voltage ripple	PWM operation	-10		10	mV
$V_{OUT\_RPL\_LLD}$	Output voltage ripple at light load	PFM operation	-25		25	mV
$V_{OUT\_TR\_LD\_1500}$	Output voltage load transient Including DC accuracy	I_{OUT} = 0.1 to 1.5 A dI/dt = 0.5 A/µs	-5		5	%
$V_{OUT\_TR\_LD\_4500}$	Output voltage load transient Including DC accuracy	I_{OUT} = 2.4 to 4.5 A dI/dt = 0.5 A/µs	-5		5	%
I_{OUT_MAX}	Maximum output current		5			A
I_{POSLIM}	Positive current limit			7		A
I_{NEGLIM}	Negative current limit			-2.4		A
f_{SW}	Switching frequency (PWM operation)		1.8	2	2.2	MHz
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{DIS_D}	Disable delay	Programmable	0		10	ms
R_{PD_FB}	Feedback pull-down resistor	V_{OUT} = 0.5 V Disabled by OTP		15		Ω
η_{100}	Efficiency	V_{IN1} = 5.0 V V_{OUT} = 3.3 V I_{OUT} = 10 mA to 100 mA Note 1		75		%
η_{3000}	Efficiency	V_{IN1} = 5.0 V V_{OUT} = 3.3 V I_{OUT} = 100 mA to 3 A		80		%
η_{4000}	Efficiency	V_{IN1} = 5.0 V V_{OUT} = 3.3 V I_{OUT} = 3 A to 4 A		75		%
η_{5000}	Efficiency	V_{IN1} = 5.0 V V_{OUT} = 3.3 V I_{OUT} = 4 A to 5 A		70		%

Note 1 V_{IN1} current only

4.3.4 CH2 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN2} ≤ 5.5 V.

Table 8: CH2 Buck Converter Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN2}	Input voltage	At VIN2 pin	4.5	5	5.5	V
C_{OUT}	Output Capacitance	Including voltage and temperature coefficient	22	44	52.8	µF
ESR_{COUT}	ESR of C_{OUT}	f > 100 kHz + track impedance			10	mΩ
L	Inductor value	Including current and temperature dependence	0.5	1	1.2	µH
ESR_{LBUCK}	Inductor resistance			40		mΩ
Electrical Performance						
V_{OUT}	Output voltage	BUCK2_OPT_CTRL6 = 0b 10 mV step	0.8		2.2	V
		BUCK2_OPT_CTRL6 = 1b 20 mV step	1.6		3.3	V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation PWM operation	-2		2	%
$V_{OUT\_ACC\_PFM}$	Overall output accuracy	Including load and line regulation PFM operation	-2		3.5	%
V_{OUT_RPL}	Output voltage ripple	PWM operation	-10		10	mV
$V_{OUT\_RPL\_LLD}$	Output voltage ripple at light load	PFM operation	-20		20	mV
$V_{OUT\_TR\_LD}$	Output voltage load transient	I_{OUT} = 0.5 to 2.5 A dI/dt = 0.5 A/µs Including DC accuracy	-5		5	%
I_{OUT_MAX}	Maximum output current		2.5			A
I_{POSLIM}	Positive current limit			3.75		A
I_{NEGLIM}	Negative current limit			-1.4		A
f_{SW}	Switching frequency (PWM operation)		1.8	2	2.2	MHz
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms
t_{DIS_D}	Disable delay	Programmable	0		10	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PD_FB}	Feedback pull-down resistor	V_{OUT} = 0.5V Disabled by OTP		30		Ω
η_{100}	Efficiency	V_{IN2} = 5.0 V V_{OUT} = 2.5 V I_{OUT} = 1 mA to 100 mA Note 1		90		%
η_{1000}	Efficiency	V_{IN2} = 5.0 V V_{OUT} = 2.5 V I_{OUT} = 100 mA to 1 A		90		%
η_{2000}	Efficiency	V_{IN2} = 5.0 V V_{OUT} = 2.5 V I_{OUT} = 1 A to 2 A		85		%
η_{2500}	Efficiency	V_{IN2} = 5.0 V V_{OUT} = 2.5 V I_{OUT} = 2 A to 2.5 A		85		%

Note 1 V_{IN2} current only

4.3.5 CH3 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN3} ≤ 5.5 V.

Table 9: CH3 Buck Converter Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN3}	Input voltage	At VIN3 pin	4.5	5	5.5	V
C_{OUT}	Output Capacitance	Including voltage and temperature coefficient	22	44	52.8	µF
ESR_{COUT}	ESR of C_{OUT}	f > 100 kHz + track impedance			10	mΩ
L	Inductor value	Including current and temperature dependence	0.5	1	1.2	µH
ESR_{LBUCK}	Inductor resistance			40		mΩ
Electrical Performance						
V_{OUT}	Output voltage	BUCK3_OPT_CTRL6 = 0b 10 mV step	0.8		2.2	V
		BUCK3_OPT_CTRL6 = 1b 20 mV step	1.6		3.6	V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation PWM operation	-2		2	%
$V_{OUT\_ACC\_PFM}$	Overall output accuracy	Including load and line regulation PFM operation	-2		3.5	%
V_{OUT_RPL}	Output voltage ripple	PWM operation	-10		10	mV
$V_{OUT\_RPL\_LLD}$	Output voltage ripple at light load	PFM operation V_{OUT} ≤ 3.3 V	-20		20	mV
$V_{OUT\_TR\_LD}$	Output voltage load transient	V_{OUT} ≤ 3.3 V I_{OUT} = 0.5 to 2.5 A dI/dt = 0.5 A/µs Including DC accuracy	-5		5	%
I_{OUT_MAX}	Maximum output current	V_{OUT} ≤ 3.3 V	2.5			A
I_{POSLIM}	Positive current limit threshold			3.75		A
I_{NEGLIM}	Negative current limit			- 1.4		A
f_{SW}	Switching frequency (PWM operation)		1.8	2	2.2	MHz
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{DIS_D}	Disable delay	Programmable	0		10	ms
R_{PD_FB}	Feedback pull-down resistor	V_{OUT} = 0.5 V Disabled by OTP		30		Ω
η_{100}	Efficiency	V_{IN3} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 1 mA to 100 mA Note 1		85		%
η_{1000}	Efficiency	V_{IN3} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 100 mA to 1 A		85		%
η_{2000}	Efficiency	V_{IN3} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 1 A to 2 A		80		%
η_{2500}	Efficiency	V_{IN3} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 2 A to 2.5 A		75		%

Note 1 V_{IN3} current only

4.3.6 CH4 Buck Converter Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN4} ≤ 5.5 V.

Table 10: CH4 Buck Converter Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN4}	Input voltage	At VIN4 pin	4.5	5	5.5	V
C_{OUT}	Output Capacitance	Including voltage and temperature coefficient	22	44	52.8	µF
ESR_{COUT}	ESR of C_{OUT}	f > 100 kHz + track impedance			10	mΩ
L	Inductor value	Including current and temperature dependence	0.5	1	1.2	µH
ESR_{LBUCK}	Inductor resistance			40		mΩ
Electrical Performance						
V_{OUT}	Output voltage	BUCK4_OPT_CTRL6 = 0b 10 mV step	0.8		2.2	V
		BUCK4_OPT_CTRL6 = 1b 20 mV step	1.6		3.3	V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation PWM operation	-2		2	%
$V_{OUT\_ACC\_PFM}$	Overall output accuracy	Including load and line regulation PFM operation	-2		3.5	%
V_{OUT_RPL}	Output voltage ripple	PWM operation	-10		10	mV
$V_{OUT\_RPL\_LLD}$	Output voltage ripple at light load	PFM operation	-20		20	mV
$V_{OUT\_TR\_LD\_2000}$	Output voltage transient load regulation	I_{OUT} = 0.5 A to 2.0 A dI/dt = 0.5 A/µs Including DC accuracy	-5		5	%
I_{OUT_MAX}	Maximum output current		2.5			A
I_{POSLIM}	Positive current limit threshold			3.5		A
I_{NEGLIM}	Negative current limit			-1.4		A
f_{SW}	Switching frequency (PWM operation)		1.8	2	2.2	MHz
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms
t_{DIS_D}	Disable delay	Programmable	0		10	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PD_FB}	Feedback pull-down resistor	V_{OUT} = 0.5 V Disabled by OTP		30		Ω
η_{100}	Efficiency	V_{IN4} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 1 mA to 100 mA Note 1		85		%
η_{1000}	Efficiency	V_{IN4} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 100 mA to 1 A		85		%
η_{2000}	Efficiency	V_{IN4} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 1 A to 2 A		80		%
η_{2500}	Efficiency	V_{IN4} = 5.0 V V_{OUT} = 1.2 V I_{OUT} = 2 A to 2.5 A		75		%

Note 1 V_{IN4} current only

4.3.7 CH5 Voltage Regulator Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 1.176 V ≤ V_{IN5} ≤ 1.377 V.

Table 11: CH5 Voltage Regulator Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN5}	Input voltage	CH4 output	1.176	1.2	1.224	V
			1.323	1.35	1.377	
C_{OUT}	Output Capacitor	Including voltage and temperature coefficient	5	10	12	µF
ESR_{COUT}	ESR of C_{OUT}	f > 1 MHz including track impedance			10	mΩ
Electrical Performance						
V_{OUT}	Output voltage	V_{OUT4} = 1.2 V or 1.35 V		V_{OUT4}/2		V
V_{OUT_ACC}	Overall output accuracy		-2		2	%
I_{OUT_SINK}	Maximum sink current		500			mA
I_{OUT_SRC}	Maximum source current				-500	mA
I_{LIM_SINK}	Sink current limit			700		mA
I_{LIM_SRC}	Source current limit			-700		mA
$V_{OUT\_TR\_LD}$	Transient load regulation	I_{OUT} = -300 mA to 300 mA dI/dt = 0.1 A/µs Including DC accuracy	-5		5	%
t_{EN_D}	Enable delay	Note 1	0	100		µs
$t_{SOFTSTART}$	Soft-start time	Programmable in 200 µs steps	0.4		0.8	ms
$t_{SOFTSTART\_ACC}$	Soft-start time accuracy		-0.1		0.1	ms
R_{PD}	Pull-down resistance in OFF mode	V_{OUT} = 0.5 V Disable by OTP		100		Ω

Note 1 CH5 start-up triggered by CH4 soft-start completion.

4.3.8 CH6 LDO Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN6} ≤ 5.5 V.

Table 12: CH6 LDO Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN6}	Input voltage	Power stage supplied	4.5	5	5.5	V
C_{OUT}	Output Capacitor	Including voltage and temperature coefficient	2.35	4.7	5.64	µF
ESR_{COUT}	ESR of C_{OUT}	f > 1 MHz including track impedance			10	mΩ
Electrical Performance						
V_{OUT}	Output voltage at lowest V_{OUT} setting			2.5		V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation	-2		2	%
I_{OUT_MAX}	Maximum output current		200			mA
I_{LIM}	Current limit			350		mA
$V_{OUT\_TR\_LD}$	Transient load regulation	10 mA to 150 mA dI/dt = 0.05 A/µs Including DC accuracy	-5		5	%
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms
$t_{SOFTSTART}$	Soft-start time	Programmable in 200 µs steps	0.4		0.8	ms
$t_{SOFTSTART\_ACC}$	Soft-start time accuracy		-0.1		0.1	ms
t_{DIS_D}	Disable delay	Programmable	0		10	ms
R_{PD}	Pull-down resistance in OFF mode	V_{OUT} = 0.5 V Disable by OTP		400		Ω

4.3.9 CH7 LDO Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 4.5 V ≤ V_{IN7} ≤ 5.5 V.

Table 13: CH7 LDO Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN7}	Input voltage		4.5	5	5.5	V
C_{OUT}	Output Capacitor	Including voltage and temperature coefficient	2.35	4.7	5.64	µF
ESR_{COUT}	ESR of C_{OUT}	f > 1 MHz including track impedance			10	mΩ
Electrical Performance						
V_{OUT_SEL0}	Output voltage	CH7_VOUT = 0x0		1.8		V
V_{OUT_SEL1}	Output voltage	CH7_VOUT = 0x1		3.3		V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation	-2		2	%
I_{OUT_MAX}	Maximum output current		200			mA
I_{LIM}	Current limit			350		mA
$V_{OUT\_TR\_LD}$	Transient load regulation	V_{OUT} = 1.8 V, 3.3 V 10 mA to 150 mA dI/dt = 0.05 A/µs Including DC accuracy	-5		5	%
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms
$t_{SOFTSTART}$	Soft-start time	Programmable in 200 µs steps	0.4		0.8	ms
$t_{SOFTSTART\_ACC}$	Soft-start time accuracy		-0.1		0.1	ms
t_{DIS_D}	Disable delay	Programmable	0		10	ms
R_{PD}	Pull-down resistance in OFF mode	V_{OUT} = 0.5 V Disable by OTP		400		Ω

4.3.10 CH8 LDO Characteristics

Unless otherwise noted, the following is valid for -40 °C ≤ T_A ≤ +85 °C, 1.98 V ≤ V_{IN8} ≤ 2.12 V.

Table 14: CH8 LDO Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN8}	Input voltage		1.98	2	2.12	V
C_{OUT}	Output Capacitor	Including voltage and temperature coefficient	11	22	26.4	µF
ESR_{COUT}	ESR of C_{OUT}	f > 1 MHz including track impedance			10	mΩ
Electrical Performance						
V_{OUT}	Output voltage			1.8		V
V_{OUT_ACC}	Overall output accuracy	Including load and line regulation	-2		2	%
I_{OUT_MAX}	Maximum output current		1.6			A
I_{LIM}	Current limit			2.5		A
$V_{OUT\_TR\_LD}$	Transient load regulation	0.1 A to 1.46 A dI/dt = 0.5 A/µs Including DC accuracy	-5		5	%
$V_{DROPOUT}$	Dropout voltage Note 1	V_{OUT} = V_{OUT_SET} - 10 mV I_{OUT} = I_{OUT_MAX}			180	mV
t_{EN_D}	Enable delay	Programmable in 800 µs steps	0		2.4	ms
$t_{SOFTSTART}$	Soft-start time	Programmable in 200 µs steps	0.4		0.8	ms
$t_{SOFTSTART\_ACC}$	Soft-start time accuracy		-0.1		0.1	ms
t_{DIS_D}	Disable delay	Programmable	0		10	ms
R_{PD}	Pull-down resistance in OFF mode	V_{OUT} = 0.5 V Disable by OTP		50		Ω

Note 1 Difference between input and output of the LDO should exceed this parameter.

4.4 Timing Characteristics

Table 15: I2C Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{BUS}	Bus free time between a STOP and START condition		1.3			µs
C_{BUS}	Bus line capacitive load				400	pF
f_{SCL}	SCL clock frequency				400	kHz
t_{LO_SCL}	SCL low time		0.6			µs
t_{HI_SCL}	SCL high time		0.6			µs
t_{RISE}	SCL and SDA rise time. Requirement for input.				300	ns
t_{FALL}	SCL and SDA fall time. Requirement for input.				300	ns
t_{SETUP_START}	Start condition setup time		0.6			µs
t_{HOLD_START}	Start condition hold time		0.6			µs
t_{SETUP_STOP}	Stop condition setup time		0.6			µs
t_{SETUP_DATA}	Data setup time		100			ns
t_{HOLD_DATA}	Data hold time		0			ns
t_{SPIKE}	Spike suppression pulse width		0		50	ns

5 Functional Description

DA9281 is an 8-channel PMIC optimized for supplying system, I/O, and peripheral rails.

DA9281 features four buck regulators. High efficiency is achieved over a wide load range by implementing auto mode. All switches are fully integrated so that external Schottky Diodes are not required. There are also three LDO regulators. In addition, there is a termination voltage regulator (VTT). All eight channels have an output discharge function and protection features such as OCP, UVP and OVP.

DA9281 features a programmable power sequencer that handles start-up and shutdown sequences.

These functions are programmed using the I^2C interface.

5.1 POWER_OFF, SHUTDOWN, OPERATING, UVLO, and Thermal Shutdown State Transitions

5.1.1 State Diagram

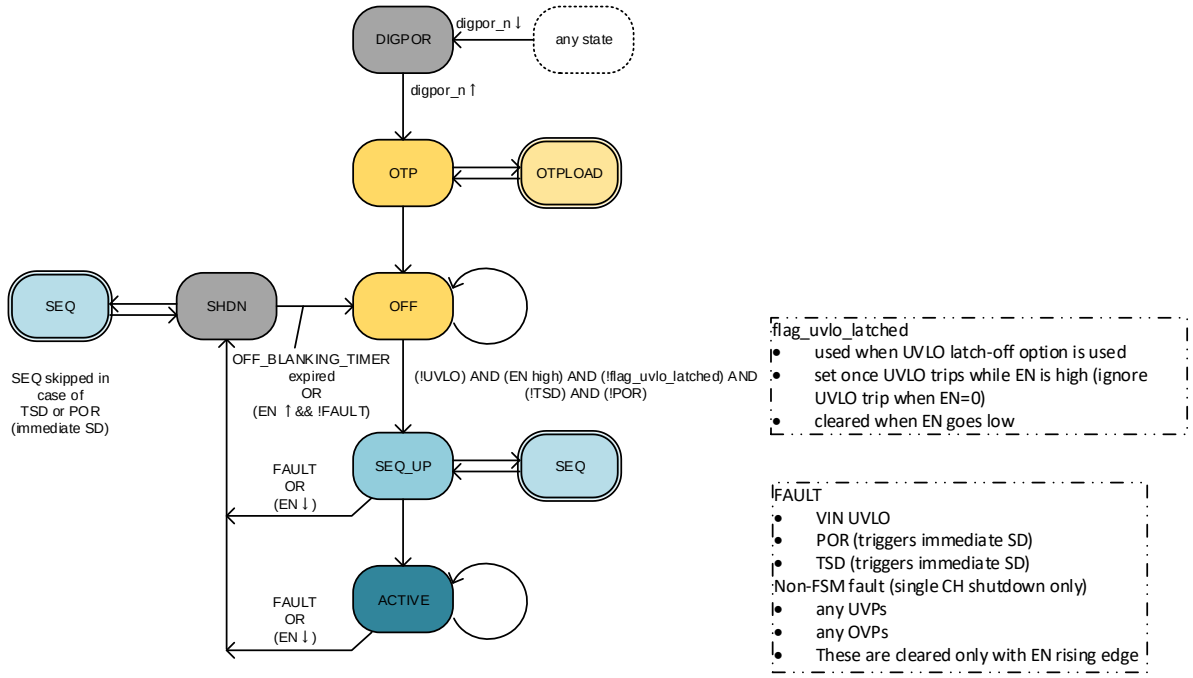


Figure 4: State Transitions Diagram

5.1.2 Mode Description

- **DIGPOR**: The digital circuit is in POR. Once DIGPOR is released, the FSM automatically transitions to the OTP load state.
- **OTP**: In the OTP state the OTP load is handled by the sub-FSM for OTP load. All OTP programmable registers are configured with the data from OTP in this phase. Once all registers have been configured, the FSM moves to OFF.
- **OFF**: In the OFF state the device waits for all conditions to allow enabling the channels. The VIN must not be in a UV condition (UVLO or POR) and the UVLO stored flag must not be set (in case the latch-off option is used), the junction temperature must be below the temperature shutdown threshold minus the hysteresis and in addition the EN pin needs to be high.
- **SEQ_UP**: In this state the channels are being enabled according to their delay configurations by the SEQ sub-FSM. The channels also run through their soft-start before exiting this state towards ACTIVE. This state is left immediately towards SHDN in case of a fault (VIN UVLO, POR, TSD) or if the EN pin is set low.

- **ACTIVE**: All channels are enabled. This state is left towards SHDN in case of a fault (UVLO, POR, TSD) or if the EN pin is set low.
- **SHDN**: In SHDN the SEQ sub-FSM takes care of disabling the channels according to their configured timing. In case of TSD or POR the channel shutdown happens immediately. After shutting down the channels a 10ms wait time (OFF_BLANKING_TIMER) needs to pass before going back to OFF. This is done to allow the channels to be adequately discharged. This wait time can be skipped or shortened, if the transition to OFF was triggered by the EN pin going low, no fault conditions present in the shutdown and the EN pin goes high again.

5.2 Startup and Shutdown Sequences

5.2.1 CH1, CH2, CH3, CH4 Soft Start-Up

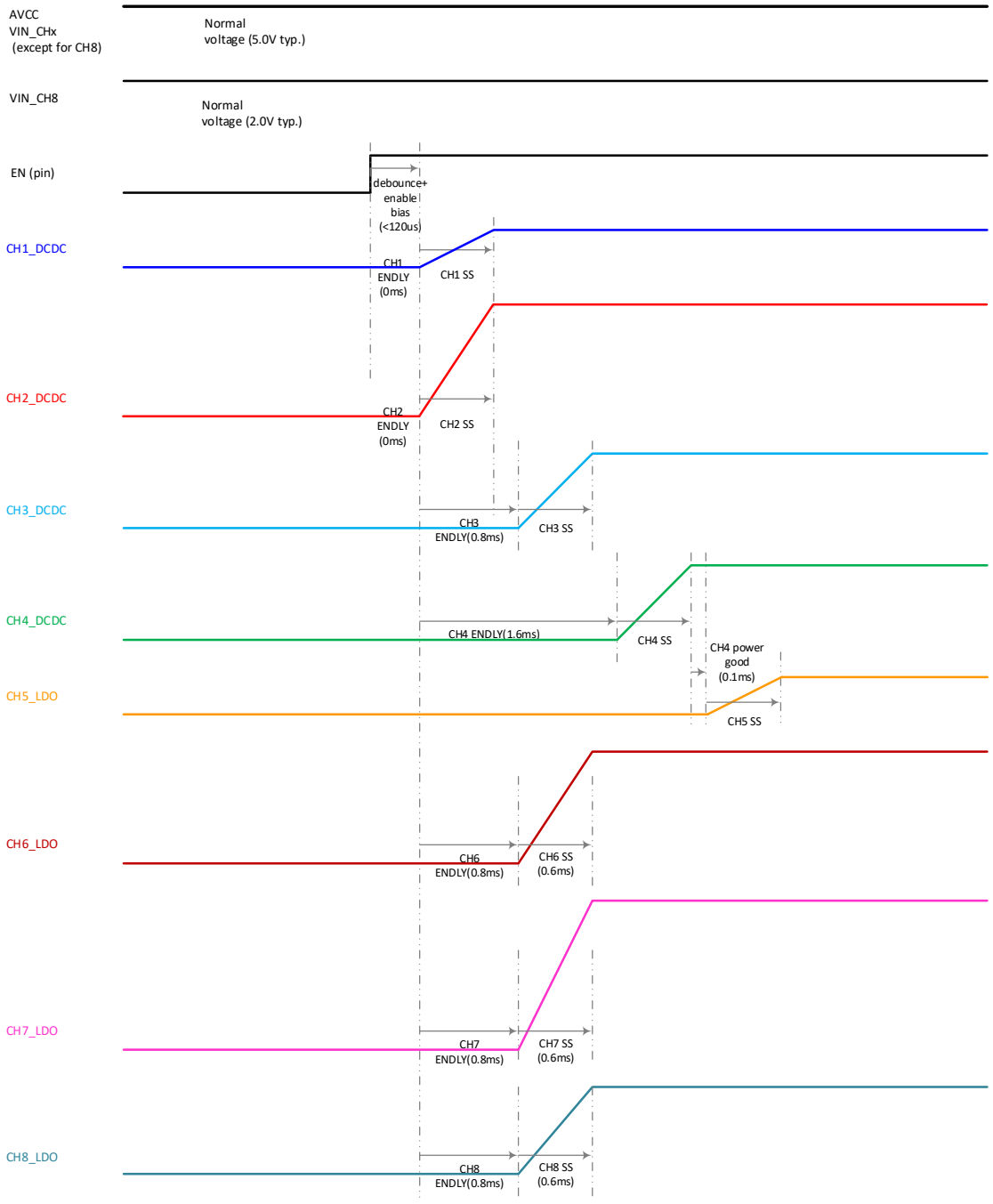
To limit in-rush current from V_{INx}, the buck converters (CH1 to CH4) perform a soft start-up after being enabled.

The soft start-up slew rates are selectable as shown below in CH<x>_SS:

Table 16: CH<x> Slew Rates

CH<x>_SS	CH1 Slew Rate	CH2 Slew Rate	CH3 Slew Rate	CH4 Slew Rate
0.4 ms	10 mV / 5 µs	10 mV / 3.25 µs		
0.6 ms	10 mV / 7.5 µs	10 mV / 5 µs		
0.8 ms	10 mV / 10 µs	10 mV / 6.75 µs		

5.2.2 Normal Startup Sequence



CH1_ENDLY = 00b : 0.0ms (default)
CH2_ENDLY = 00b : 0.0ms (default)
CH3_ENDLY = 01b : 0.8ms (default)
CH4_ENDLY = 10b : 1.6ms (default)
CH6_ENDLY = 01b : 0.8ms (default)
CH7_ENDLY = 01b : 0.8ms (default)
CH8_ENDLY = 01b : 0.8ms (default)

Figure 5: Normal Startup Sequence

5.2.3 Normal Shutdown Sequence

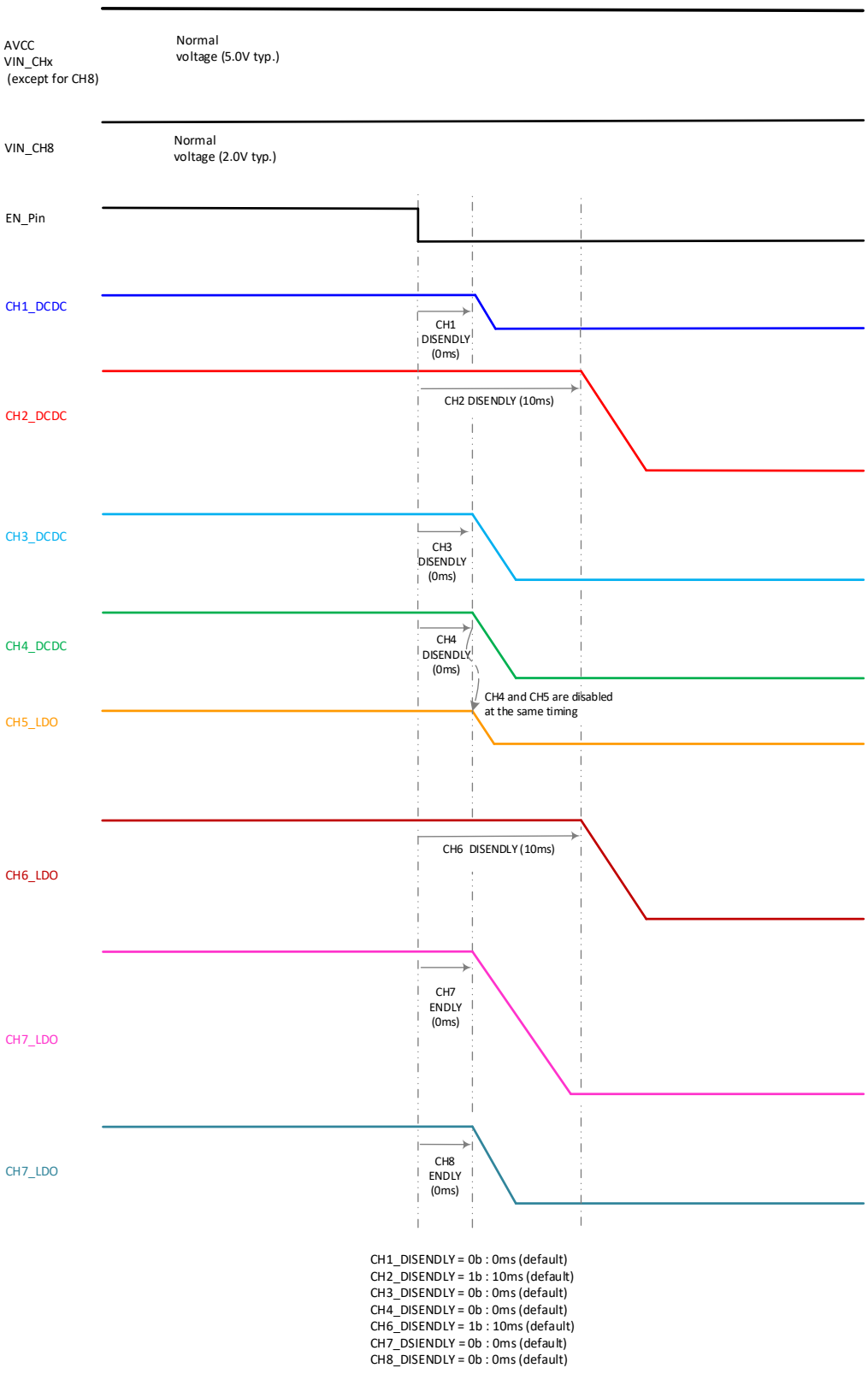


Figure 6: Normal Shutdown Sequence

5.2.4 UVLO Falling Shutdown

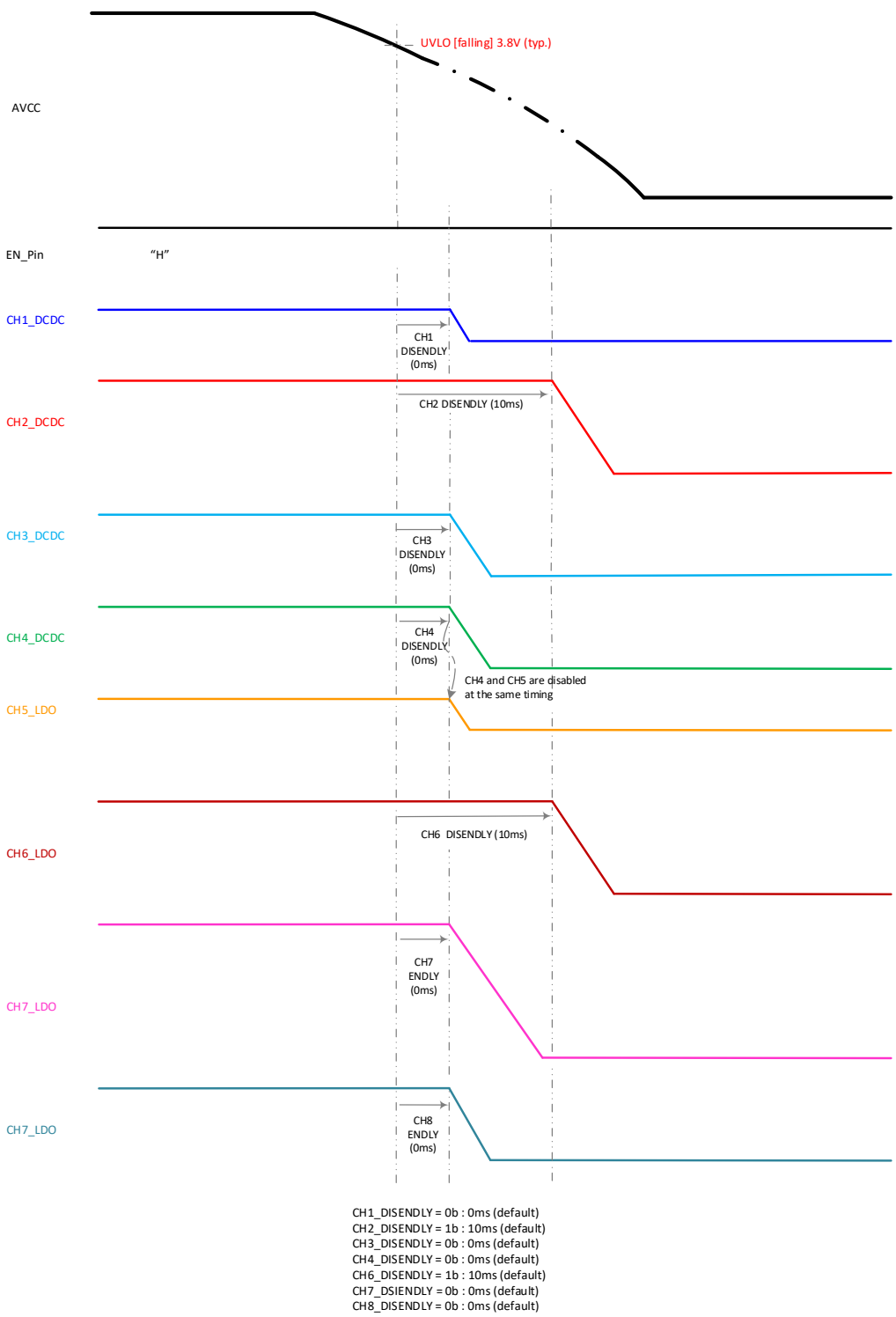


Figure 7: UVLO Falling Shutdown Sequence 1

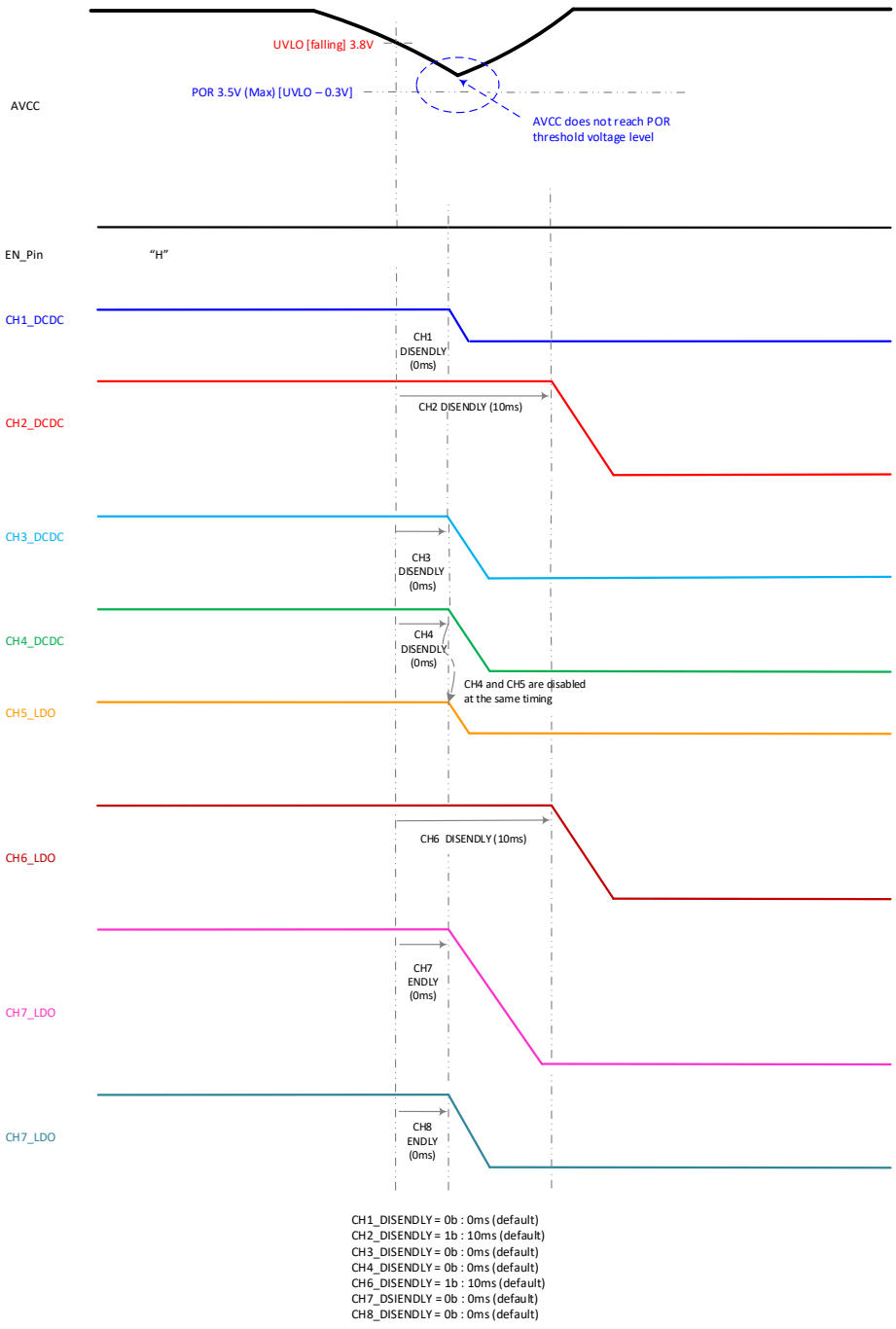


Figure 8: UVLO Falling Shutdown Sequence 2

5.2.5 POR Falling Shutdown

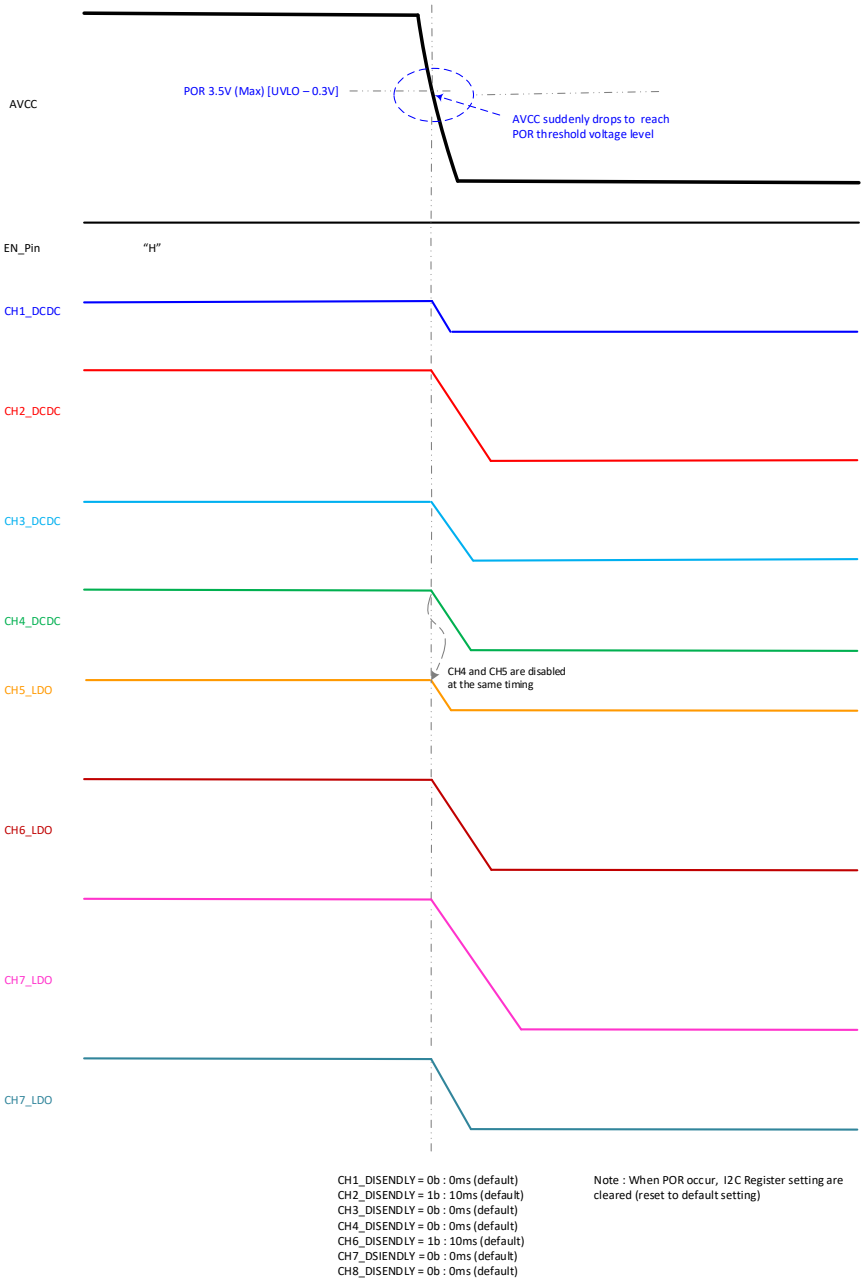


Figure 9: POR Falling Shutdown

5.2.6 TSD Thermal Shutdown Sequence

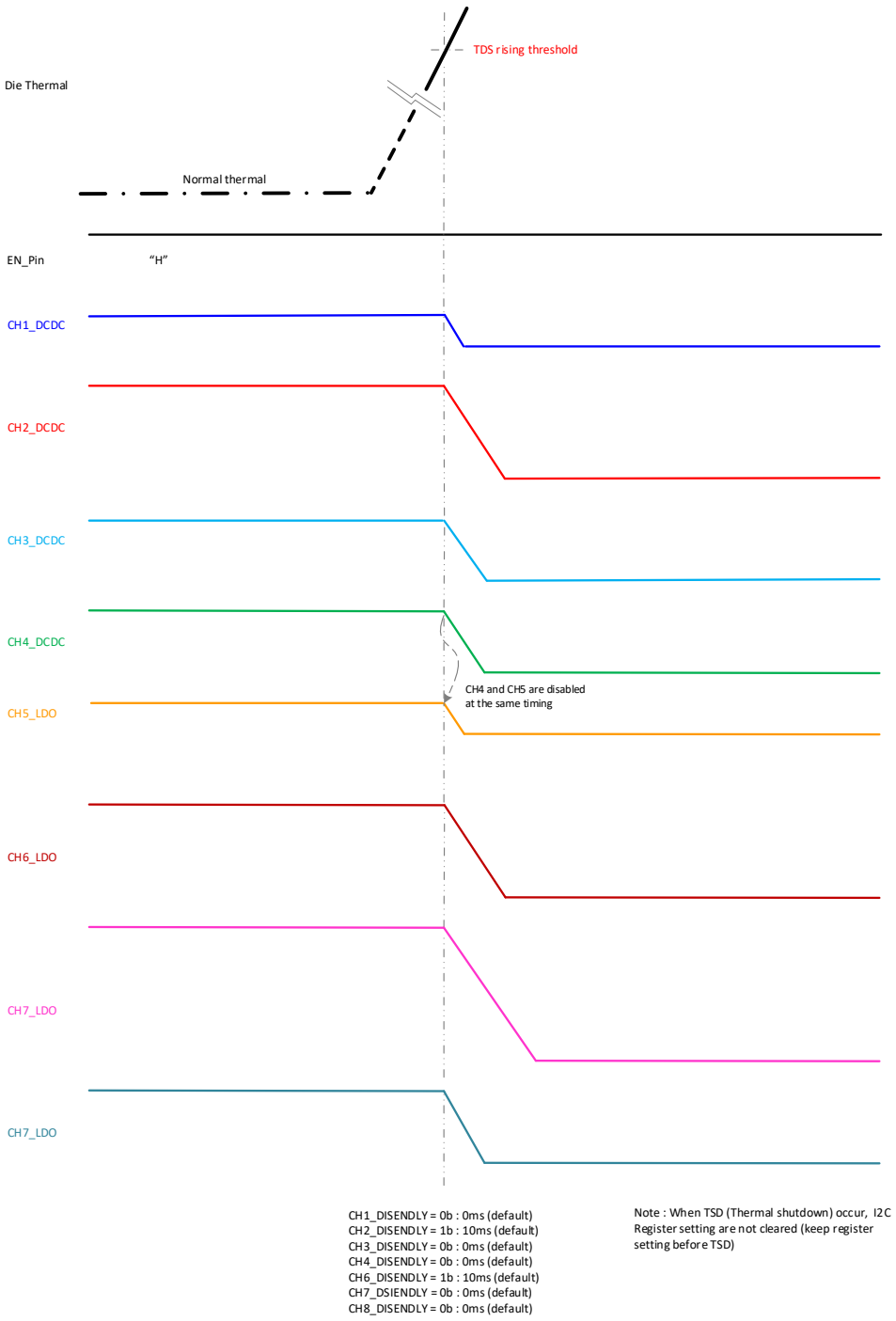
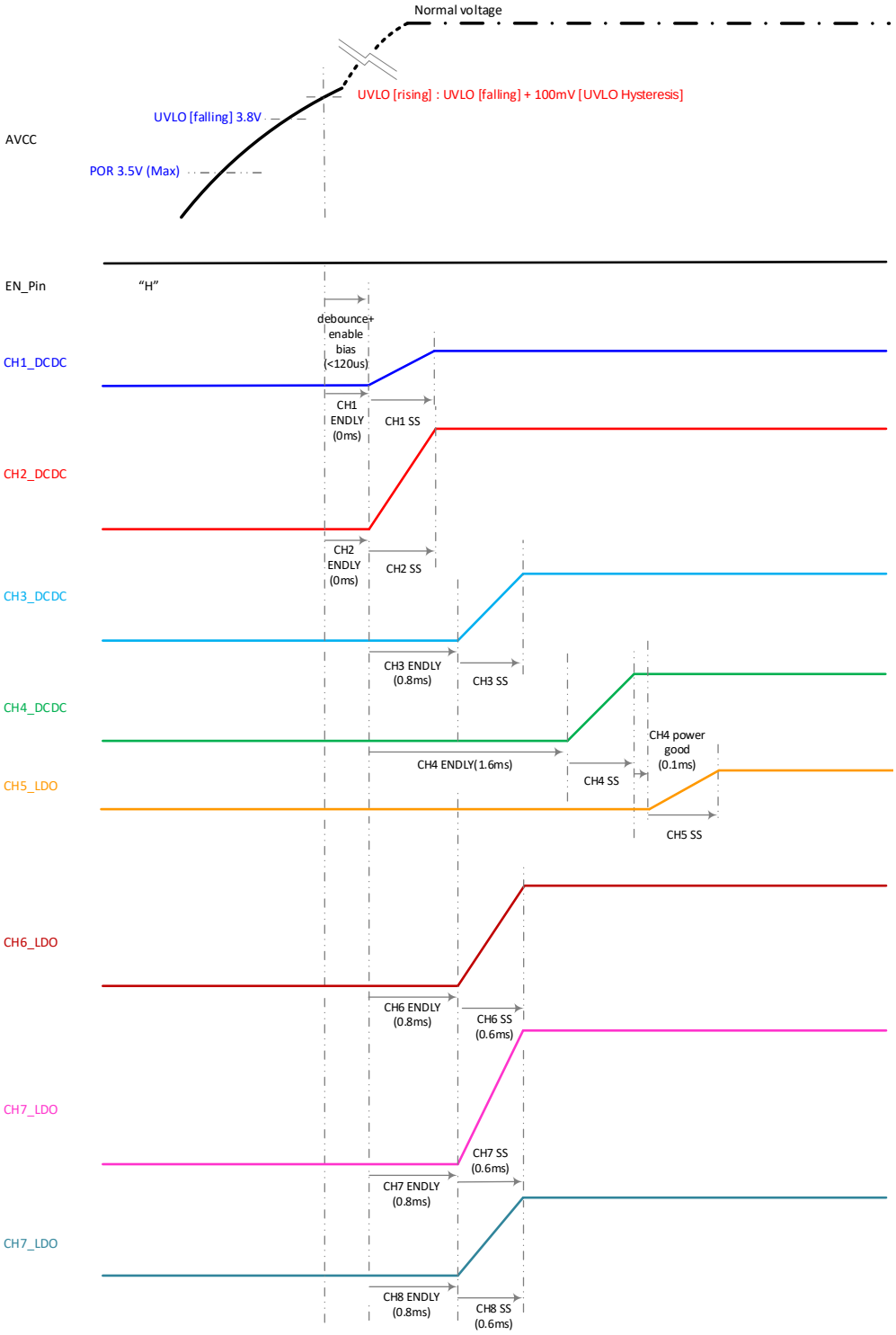


Figure 10: TSD Shutdown

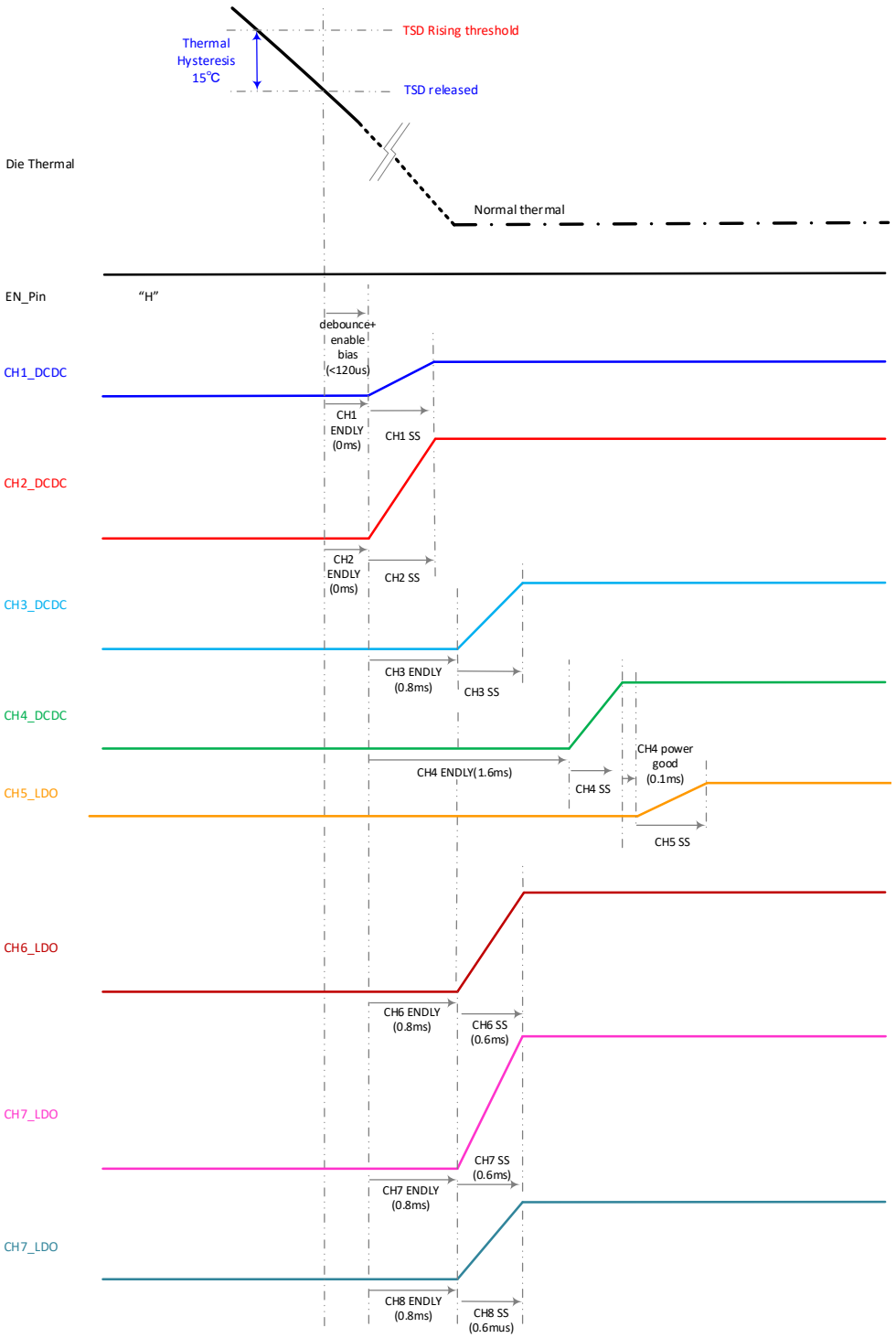
5.2.7 Restart Sequence POR Released



CH1_ENDLY = 00b : 0.0ms (default)
CH2_ENDLY = 00b : 0.0ms (default)
CH3_ENDLY = 01b : 0.8ms (default)
CH4_ENDLY = 10b : 1.6ms (default)
CH6_ENDLY = 01b : 0.8ms (default)
CH7_ENDLY = 01b : 0.8ms (default)
CH8_ENDLY = 01b : 0.8ms (default)

Figure 11: Restart Sequence after POR Released

5.2.8 Restart Sequence TSD Released



CH1_ENDLY = 00b : 0.0ms (default)
CH2_ENDLY = 00b : 0.0ms (default)
CH3_ENDLY = 01b : 0.8ms (default)
CH4_ENDLY = 10b : 1.6ms (default)
CH6_ENDLY = 01b : 0.8ms (default)
CH7_ENDLY = 01b : 0.8ms (default)
CH8_ENDLY = 01b : 0.8ms (default)

Figure 12: Restart Sequence after TSD Released

5.3 Supervisory and Protection Functions

5.3.1 Under-Voltage Lockout

DA9281 has an under-voltage lockout (UVLO) function circuit to monitor the input voltage state at the AVCC power supply and control internal circuit operation.

Whilst operating, the supply voltage at AVCC decreases and when it falls below UVLO detection voltage falling threshold (3.8 V typ. as default), all channels (buck regulators (CH1-CH4), LDOs (CH6, CH7, and CH8) and VTT regulator (CH5)) are sequentially disabled and then the output capacitors are discharged using pull-down resistances, in order to prevent malfunction.

The following behavior when AVCC increases after UVLO is programmable (UVLO latch-off turned “off” or “on” is set by OTP). The current sample device is set to UVLO latch-off turned “on”.

- With UVLO latch-off turned “off”: When the power supply voltage at AVCC increases and exceeds the UVLO release voltage including hysteresis (100 mV typ.), UVLO is released, and then all channels restart automatically.
- With UVLO latch-off turned “on”: The chip cannot restart directly, but the enable pin EN needs to be pulled “low” first to clear the UVLO flag. Only then, with EN “high”, the chip will power up the channels again.

5.3.2 Thermal Shutdown

DA9281 has a Thermal Shutdown (TSD) function circuit to monitor the terminal temperature on the device and to control internal circuit operation.

Whilst operating, the terminal temperature increases and when it exceeds thermal rising threshold (140 °C typ.) all channels (buck regulators (CH1-CH4), LDOs (CH6, CH7, and CH8) and VTT regulator (CH5)) are disabled immediately and then the output capacitors are discharged using pull down resistances, in order to prevent malfunction.

When the terminal temperature decreases and becomes lower than thermal hysteresis (15 °C typ.), TSD is released, and then all channels restart.

5.3.3 Over-Current Protection

All channels (from CH1 to CH8) on DA9281 have an OCP function circuit to monitor over-current.

This function automatically limits the output current when it exceeds the regulated (current limit) value.

If it returns to the regulated (current limit) value or less than current limit value, it automatically returns to normal operation.

Although the shutdown operation is not executed by this function, if the current is exceeding the regulated (current limit) value, the output voltage will fall with the function (over-current limitation). As a result, UVP may be detected and the output is shut down.

5.3.4 Under-Voltage Protection

All channels (from CH1 to CH8) on DA9281 have an UVP function circuit to monitor under-voltage.

Channels CH1 to CH8 output is shut down after detecting voltage lower than the reference voltage (70 % typ.) for the regulation period time (100 µs typ.)

To restart the channel after UVP, the EN pin must be first set to “low”. The channels can power up again from the rising edge of the EN pin.

5.3.5 Over-Voltage Protection

Channels CH1 to CH8 on DA9281 have an OVP function circuit to monitor over-voltage.

Channels CH1 to CH8 output is shut down after detecting voltage higher than the reference voltage (120 % typ.) for the regulation period time (100 µs typ.).

To restart the channel after OVP, the EN pin must be first set to “low”. The channels can power up again from the rising edge of the EN pin.

5.3.6 DC-DC Latch Off Protection

Figure 13 shows the function operation of latch off protection on CH1-CH4 DC-DC converter which are enabled by the EN pin, the example shown is CH1 DC-DC.

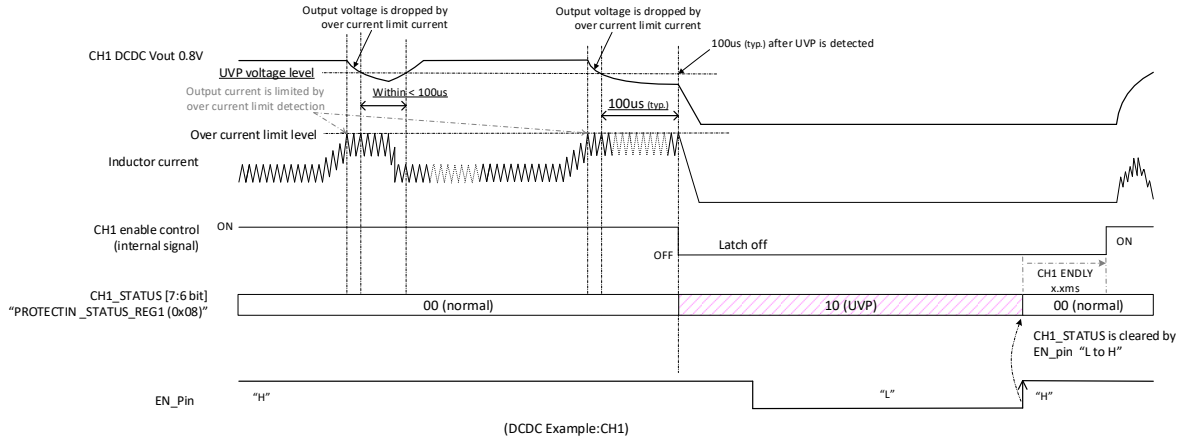


Figure 13: DC-DC Shutdown due to OCP/UVP

5.3.7 LDO Latch Off Protection

Figure 14 shows the function operation of latch off protection on CH5 and CH6 LDOs, which are enabled by the EN pin, the example shown is CH6 LDO.

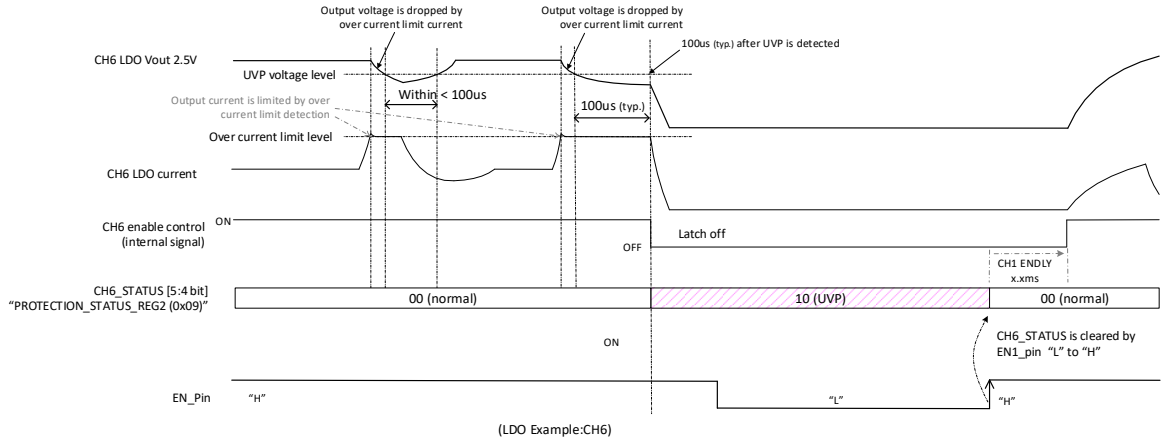


Figure 14: LDO Shutdown due to OCP/UVP

5.3.8 UVP Behavior during Soft-Start

During Soft-Start of all channels CH1-CH8, the UVP are masked so that no incorrect UVP flags are generated. The masking ends 100 µs after the end of the Soft-Start period. If the channel did not start up correctly, the UVP flag is raised 200 µs after the end of Soft-Start since this includes the 100 µs delay for the UVP masking release plus 100 µs minimum observe time before the flag is raised.

An example is shown in Figure 15.

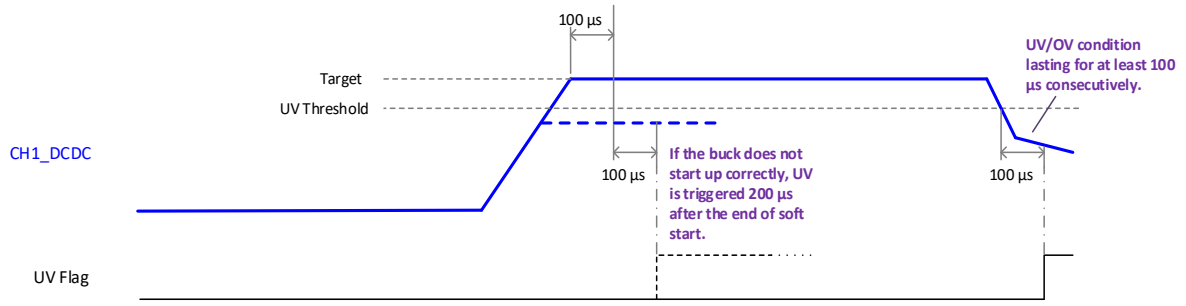


Figure 15: UVP Behavior during Soft-Start

5.4 I²C Communication

DA9281 includes an I²C-compatible 2-wire serial interface to access the internal registers. Using the I²C interface, the host processor can control each channel and read back the system status. DA9281 only operates as a slave device. For detailed information about each register, see Section 0.

The host processor provides the serial clock at the SCL pin. DA9281 supports I²C standard-mode (100 Kbit/s) and up to 400 Kbit/s (fast-mode) as described in the I²C-bus specification Rev 06 (UM1010204, issued on 4 April 2014).

The DA9281 8-bit SLAVE address is 0xA2h (default).

The I²C data pin, SDA, is open drain allowing multiple devices to share a communication line.

The I²C interface uses a two-byte serial protocol containing one byte for address and one byte for data. The data and address are transferred with MSB transmitted first for both read and write operations.

All transmissions begin with a START condition issued from the master while the bus is in an IDLE state (that is, the bus is free). The START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state. A STOP condition is indicated by a low to high transition on the SDA line while the SCL line is in the high state.

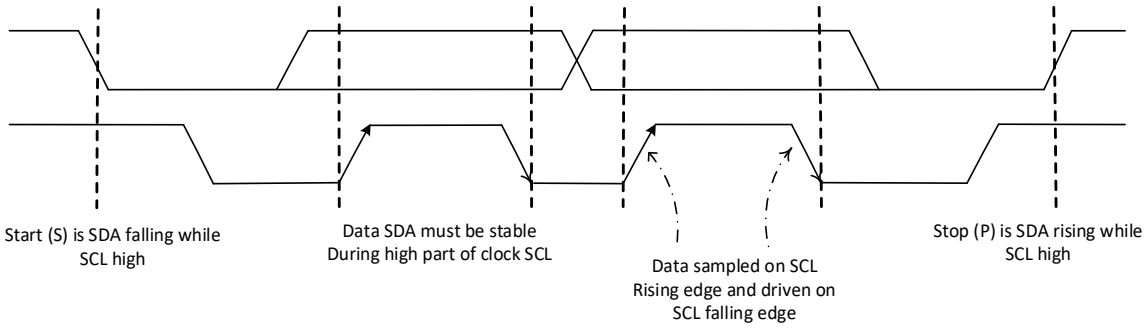


Figure 16: I²C Start (S) and Stop (P)

DA9281 monitors the serial bus for a valid SLAVE address whenever the interface is enabled. When it receives its own slave address, it immediately gives an acknowledge signal to the host by pulling the SDA line low during the following clock cycle.

A Not Acknowledge signal is given by the logic 1, not pulling down the SDA line.

A single-byte write is shown in Figure 17. The slave address is followed by a WRITE bit (low), the register address, and the data. The transaction is terminated with a STOP.

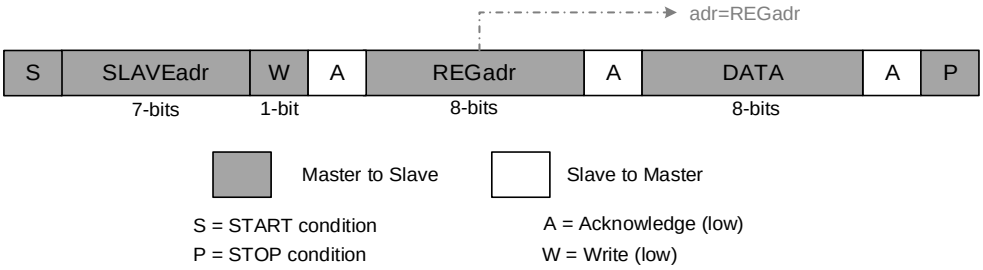


Figure 17: Single Write Command

DA9281 also supports multiple byte writes, see Figure 18. By not sending the STOP command, data is written to consecutive addresses.

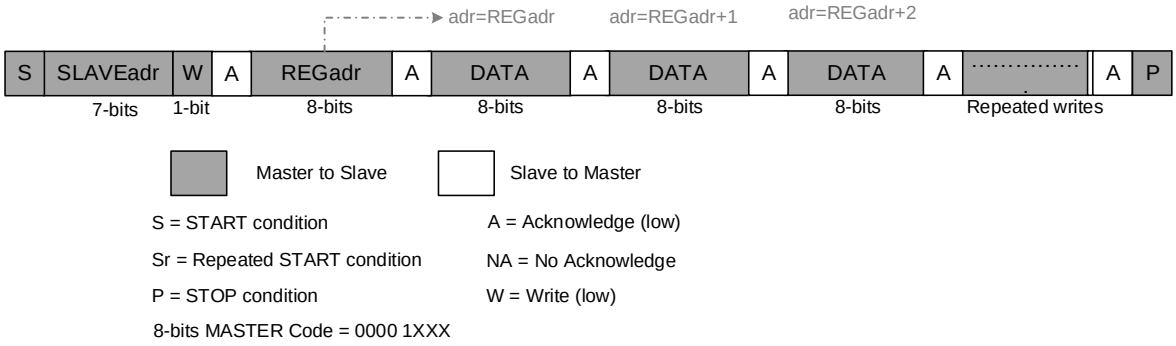


Figure 18: Consecutive Write Command

The data READ protocol does not have a register address immediately preceding it. To read from a specific address, the register address is given by using a write command followed by a Repeated START. A single byte read is shown in Figure 19. A Repeated START is followed by the slave address and a READ bit. After the READ data is returned to the host, the host responds with a Not Acknowledge and a STOP.

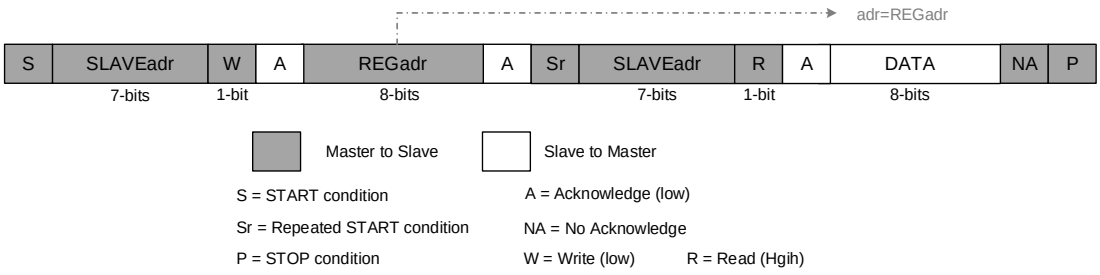


Figure 19: Single Read Command

DA9281 also supports a multiple byte reads. If the host responds to the returned data with an Acknowledge rather than a No Acknowledge and a STOP, then data will be read from sequential addresses until a No Acknowledge and a STOP command are given, as shown in Figure 20. If a READ address is given with a WRITE and Repeated START, consecutive addresses are read from the WRITE address.

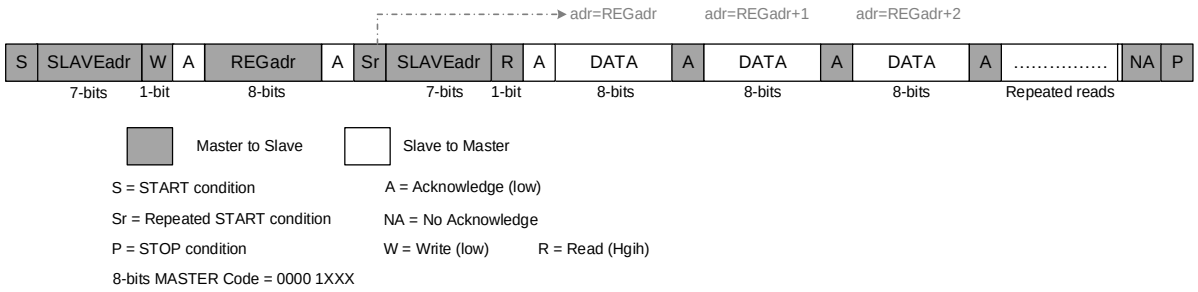


Figure 20: Consecutive Read Command

6 Register Definitions

NOTE
The following registers are password protected. ● PMC_VOUT_ADJUST ● PMC_CONTROL_00 ● PMC_CONTROL_01 ● PMC_CONTROL_02 ● PMC_CH1_VOUT_INT ● PMC_CH2_VOUT_INT ● PMC_CH3_VOUT_INT ● PMC_CH4_VOUT_INT ● PMC_CONFIG_00 ● PMC_CONFIG_0B ● BUCK_BUCK_OTP_04 ● BUCK_BUCK_OTP_05 ● BUCK_BUCK_OTP_06 ● BUCK_BUCK_OTP_07 I^2C access is required to unlock those registers. Write the following sequence: Write 0x00 to address 0x3E Write 0xB0 to address 0x3F Write 0xA9 to address 0x3F Write 0x8A to address 0x3F Write 0xA7 to address 0x3F Write 0xA8 to address 0x3F Write 0xB1 to address 0x3F To lock those registers, write the following sequence: Write 0x00 to address 0x3E Write 0x00 to address 0x3F

6.1 Register Map

Table 17: Register Map

Address	Register	Description
0x01	PMC_VOUT_ADJUST	Output voltage selection for CH7
0x02	PMC_DISCHARGE	Pulldown selection
0x03	PMC_SOFT_START_1	Soft-start time select for CH1, CH2, CH3, CH4
0x04	PMC_SOFT_START_2	Soft-start time select for CH5, CH6, CH7, CH8
0x05	PMC_ENABLE_DELAY_1	Enable delay for CH1, CH2, CH3, CH4
0x06	PMC_ENABLE_DELAY_2	Enable delay for CH6, CH7, CH8
0x07	PMC_DISENDLY	Disable delay for CH1, CH2, CH3, CH4, CH6, CH7, CH8
0x08	PMC_PROT_STATUS_1	OVP/UVP status of CH1, CH2, CH3, CH4
0x09	PMC_PROT_STATUS_2	OVP/UVP status of CH5, CH6, CH7, CH8
0x0A	PMC_STATUS	PG status for CH1, CH2, CH3, CH4; UVLO, VDD_FAULT and TEMP_CRIT status
0x0C	PMC_CONTROL_00	Enable for CH1, CH2, CH3, CH4, CH5, CH6, CH7, CH8
0x0D	PMC_CONTROL_01	Operating mode for CH1, CH2, CH3, CH4
0x0E	PMC_CONTROL_02	Sequence enable for CH1, CH2, CH3, CH4, CH5, CH6, CH7, CH8
0x0F	PMC_CH1_VOUT_INT	VOUT setting for CH1
0x10	PMC_CH2_VOUT_INT	VOUT setting for CH2
0x11	PMC_CH3_VOUT_INT	VOUT setting for CH3
0x12	PMC_CH4_VOUT_INT	VOUT setting for CH4
0x14	PMC_CONFIG_00	I2C slave address
0x1F	PMC_CONFIG_0B	Sequencer enable
0x41	OTP_VARIANT_ID	Silicon revision
0x42	OTP_CUSTOMER_ID	OTP file version
0x43	OTP_CONFIG_ID	OTP variant
0x4C	BUCK_BUCK_OTP_04	Divider mode enable for CH1
0x4D	BUCK_BUCK_OTP_05	Divider mode enable for CH2
0x4E	BUCK_BUCK_OTP_06	Divider mode enable for CH3
0x4F	BUCK_BUCK_OTP_07	Divider mode enable for CH4

6.2 Register Details

Table 18: Register Details

Address	Register	Bit	Type	Function	Detail	Default
0x01	PMC_VOUT_ADJUST	[7:6]	R/W	RESERVED	-	00b
		[5:2]	R/W	RESERVED<	-	0000b
		[1:1]	R/W	CH7_VOUT	0: 1.8 V 1: 3.3 V	1b
		[0:0]	R/W	RESERVED	-	0b
0x02	PMC_DISCHARGE	7	R/W	CH1_DISCH	0: Discharge Disable 1: Discharge enable	1b
		6	R/W	CH2_DISCH	0: Discharge Disable 1: Discharge enable	1b
		5	R/W	CH3_DISCH	0: Discharge Disable 1: Discharge enable	1b
		4	R/W	CH4_DISCH	0: Discharge Disable 1: Discharge enable	1b
		3	R/W	CH5_DISCH	0: Hi-Z 1: Discharge enable	1b
		2	R/W	CH6_DISCH	0: Discharge Disable 1: Discharge enable	1b
		1	R/W	CH7_DISCH	0: Discharge Disable 1: Discharge enable	1b
		0	R/W	CH8_DISCH	0: Discharge Disable 1: Discharge enable	1b
0x03	PMC_SOFT_START_1	[7:6]	R/W	CH1_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
		[5:4]	R/W	CH2_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b

Address	Register	Bit	Type	Function	Detail	Default
		[3:2]	R/W	CH3_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
		[1:0]	R/W	CH4_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
0x04	PMC_SOFT_START_2	[7:6]	R/W	CH5_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
		[5:4]	R/W	CH6_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
		[3:2]	R/W	CH7_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
		[1:0]	R/W	CH8_SS	00: 0.4 ms 01: 0.6 ms 10: 0.8 ms 11: Reserved	01b
0x05	PMC_ENABLE_DELAY_1	[7:6]	R/W	CH1_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
		[5:4]	R/W	CH2_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
		[3:2]	R/W	CH3_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
		[1:0]	R/W	CH4_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
0x06	PMC_ENABLE_DELAY_2	[7:6]	R/W	Reserved		
		[5:4]	R/W	CH6_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
		[3:2]	R/W	CH7_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b

Address	Register	Bit	Type	Function	Detail	Default
		[1:0]	R/W	CH8_ENDLY	00: 0.0 ms 01: 0.8 ms 10: 1.6 ms 11: 2.4 ms	00b
0x07	PMC_DISENDLY	7	R/W	CH1_DISENDLY	0: 0 ms 1: 10 ms	0b
		6	R/W	CH2_DISENDLY	0: 0 ms 1: 10 ms	0b
		5	R/W	CH3_DISENDLY	0: 0 ms 1: 10 ms	0b
		4	R/W	CH4_DISENDLY	0: 0 ms 1: 10 ms	0b
		3	R/W	RESERVED	-	0b
		2	R/W	CH6_DISENDLY	0: 0 ms 1: 10 ms	0b
		1	R/W	CH7_DISENDLY	0: 0 ms 1: 10 ms	0b
		0	R/W	CH8_DISENDLY	0: 0ms 1: 10ms	0b
0x08	PMC_PROT_STATUS_1	[7:6]	R	CH1_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
		[5:4]	R	CH2_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
		[3:2]	R	CH3_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
		[1:0]	R	CH4_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
0x09	PMC_PROT_STATUS_2	[7:6]	R	CH5_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
		[5:4]	R	CH6_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
		[3:2]	R	CH7_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b

Address	Register	Bit	Type	Function	Detail	Default
		[1:0]	R	CH8_STATUS	00: Normal 01: Reserved 10: UVP 11: OVP	00b
0x0A	PMC_STATUS_00	7	R	S_CH1_PG	CH1 PG status	0b
		6	R	S_CH2_PG	CH2 PG status	0b
		5	R	S_CH3_PG	CH3 PG status	0b
		4	R	S_CH4_PG	CH4 PG status	0b
		3	R	RESERVED	-	0b
		2	R	S_UVLO	VIN UV status	0b
		1	R	S_VDD_FAULT	VDD_FAULT status	0b
		0	R	S_TEMP_CRIT	Thermal shutdown status	0b
0x0C	PMC_CONTROL_00	7	R/W	CH1_EN	CH1 enable	0b
		6	R/W	CH2_EN	CH2 enable	0b
		5	R/W	CH3_EN	CH3 enable	0b
		4	R/W	CH4_EN	CH4 enable	0b
		3	R/W	CH5_EN	CH5 enable	0b
		2	R/W	CH6_EN	CH6 enable	0b
		1	R/W	CH7_EN	CH7 enable	0b
		0	R/W	CH8_EN	CH8 enable	0b
0x0D	PMC_CONTROL_01	7	R/W	RESERVED	-	0b
		6	R/W	RESERVED	-	0b
		5	R/W	RESERVED	-	0b
		4	R/W	RESERVED	-	0b
		3	R/W	CH1_MODE	CH1 Mode 0: Auto-mode 1: Force-PWM	0b
		2	R/W	CH2_MODE	CH2 Mode 0: Auto-mode 1: Force-PWM	0b
		1	R/W	CH3_MODE	CH3 Mode 0: Auto-mode 1: Force-PWM	0b
		0	R/W	CH4_MODE	CH4 Mode 0: Auto-mode 1: Force-PWM	0b
0x0E	PMC_CONTROL_02	7	R/W	CH1_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		6	R/W	CH2_SEQ_DIS	0: Enabled by sequencer	0b

Address	Register	Bit	Type	Function	Detail	Default
					1: Not enabled by sequencer	
		5	R/W	CH3_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		4	R/W	CH4_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		3	R/W	CH5_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		2	R/W	CH6_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		1	R/W	CH7_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
		0	R/W	CH8_SEQ_DIS	0: Enabled by sequencer 1: Not enabled by sequencer	0b
0x0F	PMC_CH1_VOUT	[7:0]	R/W	CH1_VOUT_INT	CH1 output voltage (V) Format is (without divider)/(with divider) **Value Description** 0x00: Reserved … 0x4F: Reserved 0x50: 0.80/1.60 0x51: 0.81/1.62 0x52: 0.82/1.64 0x53: 0.83/1.66 0x54: 0.84/1.68 0x55: 0.85/1.70 0x56: 0.86/1.72 0x57: 0.87/1.74 0x58: 0.88/1.76 0x59: 0.89/1.78 0x5A: 0.90/1.80 0x5B: 0.91/1.82 0x5C: 0.92/1.84 0x5D: 0.93/1.86 0x5E: 0.94/1.88 0x5F: 0.95/1.90 0x60: 0.96/1.92 0x61: 0.97/1.94	50b

Address	Register	Bit	Type	Function	Detail	Default
					0x62: 0.98/1.96 0x63: 0.99/1.98 0x64: 1.00/2.00 0x65: 1.01/2.02 0x66: 1.02/2.04 0x67: 1.03/2.06 0x68: 1.04/2.08 0x69: 1.05/2.10 0x6A: 1.06/2.12 0x6B: 1.07/2.14 0x6C: 1.08/2.16 0x6D: 1.09/2.18 0x6E: 1.10/2.20 0x6F: 1.11/2.22 0x70: 1.12/2.24 0x71: 1.13/2.26 0x72: 1.14/2.28 0x73: 1.15/2.30 0x74: 1.16/2.32 0x75: 1.17/2.34 0x76: 1.18/2.36 0x77: 1.19/2.38 0x78: 1.20/2.40 0x79: 1.21/2.42 0x7A: 1.22/2.44 0x7B: 1.23/2.46 0x7C: 1.24/2.48 0x7D: 1.25/2.50 0x7E: 1.26/2.52 0x7F: 1.27/2.54 0x80: 1.28/2.56 0x81: 1.29/2.58 0x82: 1.30/2.60 0x83: 1.31/2.62 0x84: 1.32/2.64 0x85: 1.33/2.66 0x86: 1.34/2.68 0x87: 1.35/2.70 0x88: 1.36/2.72 0x89: 1.37/2.74 0x8A: 1.38/2.76 0x8B: 1.39/2.78 0x8C: 1.40/2.8 0x8D: 1.41/2.82 0x8E: 1.42/2.84 0x8F: 1.43/2.86 0x90: 1.44/2.88 0x91: 1.45/2.9 0x92: 1.46/2.92 0x93: 1.47/2.94	

Address	Register	Bit	Type	Function	Detail	Default
					0x94: 1.48/2.96 0x95: 1.49/2.98 0x96: 1.50/3 0x97: 1.51/Reserved 0x98: 1.52/Reserved 0x99: 1.53/Reserved 0x9A: 1.54/Reserved 0x9B: 1.55/Reserved 0x9C: 1.56/Reserved 0x9D: 1.57/Reserved 0x9E: 1.58/Reserved 0x9F: 1.59/Reserved 0xA0: 1.60/Reserved 0xA1: 1.61/Reserved 0xA2: 1.62/Reserved 0xA3: 1.63/Reserved 0xA4: 1.64/Reserved 0xA5: 1.65/Reserved 0xA6: 1.66/Reserved 0xA7: 1.67/Reserved 0xA8: 1.68/Reserved 0xA9: 1.69/Reserved 0xAA: 1.7/Reserved 0xAB: 1.71/Reserved 0xAC: 1.72/Reserved 0xAD: 1.73/Reserved 0xAE: 1.74/Reserved 0xAF: 1.75/Reserved 0xB0: 1.76/Reserved 0xB1: 1.77/Reserved 0xB2: 1.78/Reserved 0xB3: 1.79/Reserved 0xB4: 1.8/Reserved 0xB5: 1.81/Reserved 0xB6: 1.82/Reserved 0xB7: 1.83/Reserved 0xB8: 1.84/Reserved 0xB9: 1.85/Reserved 0xBA: 1.86/Reserved 0xBB: 1.87/Reserved 0xBC: 1.88/Reserved 0xBD: 1.89/Reserved 0xBE: 1.9/Reserved 0xBF: 1.91/Reserved 0xC0: 1.92/Reserved 0xC1: 1.93/Reserved 0xC2: 1.94/Reserved 0xC3: 1.95/Reserved 0xC4: 1.96/Reserved 0xC5: 1.97/Reserved	

Address	Register	Bit	Type	Function	Detail	Default
					0xC6: 1.98/Reserved 0xC7: 1.99/Reserved 0xC8: 2/Reserved 0xC9: 2.01/Reserved 0xCA: 2.02/Reserved 0xCB: 2.03/Reserved 0xCC: 2.04/Reserved 0xCD: 2.05/Reserved 0xCE: 2.06/Reserved 0xCF: 2.07/Reserved 0xD0: 2.08/Reserved 0xD1: 2.09/Reserved 0xD2: 2.1/Reserved 0xD3: 2.11/Reserved 0xD4: 2.12/Reserved 0xD5: 2.13/Reserved 0xD6: 2.14/Reserved 0xD7: 2.15/Reserved 0xD8: 2.16/Reserved 0xD9: 2.17/Reserved 0xDA: 2.18/Reserved 0xDB: 2.19/Reserved 0xDC: 2.2/Reserved 0xDD: Reserved … 0xFF: Reserved	
0x10	PMC_CH2_VOUT	[7:0]	R/W	CH2_VOUT_INT	CH2 output voltage (V) Format is (without divider)/(with divider) **Value Description** 0x00: Reserved … 0x4F: Reserved 0x50: 0.80/1.60 0x51: 0.81/1.62 0x52: 0.82/1.64 0x53: 0.83/1.66 0x54: 0.84/1.68 0x55: 0.85/1.70 0x56: 0.86/1.72 0x57: 0.87/1.74 0x58: 0.88/1.76 0x59: 0.89/1.78 0x5A: 0.90/1.80 0x5B: 0.91/1.82 0x5C: 0.92/1.84 0x5D: 0.93/1.86 0x5E: 0.94/1.88 0x5F: 0.95/1.90	50b

Address	Register	Bit	Type	Function	Detail	Default
					0x60: 0.96/1.92 0x61: 0.97/1.94 0x62: 0.98/1.96 0x63: 0.99/1.98 0x64: 1.00/2.00 0x65: 1.01/2.02 0x66: 1.02/2.04 0x67: 1.03/2.06 0x68: 1.04/2.08 0x69: 1.05/2.10 0x6A: 1.06/2.12 0x6B: 1.07/2.14 0x6C: 1.08/2.16 0x6D: 1.09/2.18 0x6E: 1.10/2.20 0x6F: 1.11/2.22 0x70: 1.12/2.24 0x71: 1.13/2.26 0x72: 1.14/2.28 0x73: 1.15/2.30 0x74: 1.16/2.32 0x75: 1.17/2.34 0x76: 1.18/2.36 0x77: 1.19/2.38 0x78: 1.20/2.40 0x79: 1.21/2.42 0x7A: 1.22/2.44 0x7B: 1.23/2.46 0x7C: 1.24/2.48 0x7D: 1.25/2.50 0x7E: 1.26/2.52 0x7F: 1.27/2.54 0x80: 1.28/2.56 0x81: 1.29/2.58 0x82: 1.30/2.60 0x83: 1.31/2.62 0x84: 1.32/2.64 0x85: 1.33/2.66 0x86: 1.34/2.68 0x87: 1.35/2.70 0x88: 1.36/2.72 0x89: 1.37/2.74 0x8A: 1.38/2.76 0x8B: 1.39/2.78 0x8C: 1.40/2.8 0x8D: 1.41/2.82 0x8E: 1.42/2.84 0x8F: 1.43/2.86 0x90: 1.44/2.88 0x91: 1.45/2.9	

Address	Register	Bit	Type	Function	Detail	Default
					0x92: 1.46/2.92 0x93: 1.47/2.94 0x94: 1.48/2.96 0x95: 1.49/2.98 0x96: 1.50/3 0x97: 1.51/3.02 0x98: 1.52/3.04 0x99: 1.53/3.06 0x9A: 1.54/3.08 0x9B: 1.55/3.1 0x9C: 1.56/3.12 0x9D: 1.57/3.14 0x9E: 1.58/3.16 0x9F: 1.59/3.18 0xA0: 1.60/3.2 0xA1: 1.61/3.22 0xA2: 1.62/3.24 0xA3: 1.63/3.26 0xA4: 1.64/3.28 0xA5: 1.65/3.3 0xA6: 1.66/Reserved 0xA7: 1.67/Reserved 0xA8: 1.68/Reserved 0xA9: 1.69/Reserved 0xAA: 1.7/Reserved 0xAB: 1.71/Reserved 0xAC: 1.72/Reserved 0xAD: 1.73/Reserved 0xAE: 1.74/Reserved 0xAF: 1.75/Reserved 0xB0: 1.76/Reserved 0xB1: 1.77/Reserved 0xB2: 1.78/Reserved 0xD0: 2.08/Reserved 0xD1: 2.09/Reserved 0xD2: 2.1/Reserved 0xD3: 2.11/Reserved 0xD4: 2.12/Reserved 0xD5: 2.13/Reserved 0xD6: 2.14/Reserved 0xD7: 2.15/Reserved 0xD8: 2.16/Reserved 0xD9: 2.17/Reserved 0xDA: 2.18/Reserved 0xDB: 2.19/Reserved 0xB3: 1.79/Reserved 0xB4: 1.8/Reserved 0xB5: 1.81/Reserved 0xB6: 1.82/Reserved 0xB7: 1.83/Reserved	

Address	Register	Bit	Type	Function	Detail	Default
					0xB8: 1.84/Reserved 0xB9: 1.85/Reserved 0xBA: 1.86/Reserved 0xBB: 1.87/Reserved 0xBC: 1.88/Reserved 0xBD: 1.89/Reserved 0xBE: 1.9/Reserved 0xBF: 1.91/Reserved 0xC0: 1.92/Reserved 0xC1: 1.93/Reserved 0xC2: 1.94/Reserved 0xC3: 1.95/Reserved 0xC4: 1.96/Reserved 0xC5: 1.97/Reserved 0xC6: 1.98/Reserved 0xC7: 1.99/Reserved 0xC8: 2/Reserved 0xC9: 2.01/Reserved 0xCA: 2.02/Reserved 0xCB: 2.03/Reserved 0xCC: 2.04/Reserved 0xCD: 2.05/Reserved 0xCE: 2.06/Reserved 0xCF: 2.07/Reserved 0xDC: 2.2/Reserved 0xDD: Reserved … 0xFF: Reserved	
0x11	PMC_CH3_VOUT	[7:0]	R/W	CH3_VOUT_INT	CH3 output voltage (V) Format is (without divider)/(with divider) **Value Description** 0x00: Reserved … 0x4F: Reserved 0x50: 0.80/1.60 0x51: 0.81/1.62 0x52: 0.82/1.64 0x53: 0.83/1.66 0x54: 0.84/1.68 0x55: 0.85/1.70 0x56: 0.86/1.72 0x57: 0.87/1.74 0x58: 0.88/1.76 0x59: 0.89/1.78 0x5A: 0.90/1.80 0x5B: 0.91/1.82 0x5C: 0.92/1.84	50b

Address	Register	Bit	Type	Function	Detail	Default
					0x5D: 0.93/1.86 0x5E: 0.94/1.88 0x5F: 0.95/1.90 0x60: 0.96/1.92 0x61: 0.97/1.94 0x62: 0.98/1.96 0x63: 0.99/1.98 0x64: 1.00/2.00 0x65: 1.01/2.02 0x66: 1.02/2.04 0x67: 1.03/2.06 0x68: 1.04/2.08 0x69: 1.05/2.10 0x6A: 1.06/2.12 0x6B: 1.07/2.14 0x6C: 1.08/2.16 0x6D: 1.09/2.18 0x6E: 1.10/2.20 0x6F: 1.11/2.22 0x70: 1.12/2.24 0x71: 1.13/2.26 0x72: 1.14/2.28 0x73: 1.15/2.30 0x74: 1.16/2.32 0x75: 1.17/2.34 0x76: 1.18/2.36 0x77: 1.19/2.38 0x78: 1.20/2.40 0x79: 1.21/2.42 0x7A: 1.22/2.44 0x7B: 1.23/2.46 0x7C: 1.24/2.48 0x7D: 1.25/2.50 0x7E: 1.26/2.52 0x7F: 1.27/2.54 0x80: 1.28/2.56 0x81: 1.29/2.58 0x82: 1.30/2.60 0x83: 1.31/2.62 0x84: 1.32/2.64 0x85: 1.33/2.66 0x86: 1.34/2.68 0x87: 1.35/2.70 0x88: 1.36/2.72 0x89: 1.37/2.74 0x8A: 1.38/2.76 0x8B: 1.39/2.78 0x8C: 1.40/2.8 0x8D: 1.41/2.82 0x8E: 1.42/2.84	

Address	Register	Bit	Type	Function	Detail	Default
					0x8F: 1.43/2.86 0x90: 1.44/2.88 0x91: 1.45/2.9 0x92: 1.46/2.92 0x93: 1.47/2.94 0x94: 1.48/2.96 0x95: 1.49/2.98 0x96: 1.50/3 0x97: 1.51/3.02 0x98: 1.52/3.04 0x99: 1.53/3.06 0x9A: 1.54/3.08 0x9B: 1.55/3.1 0x9C: 1.56/3.12 0x9D: 1.57/3.14 0x9E: 1.58/3.16 0x9F: 1.59/3.18 0xA0: 1.60/3.2 0xA1: 1.61/3.22 0xA2: 1.62/3.24 0xA3: 1.63/3.26 0xA4: 1.64/3.28 0xA5: 1.65/3.3 0xA6: 1.66/3.32 0xA7: 1.67/3.34 0xA8: 1.68/3.36 0xA9: 1.69/3.38 0xAA: 1.70/3.4 0xAB: 1.71/3.42 0xAC: 1.72/3.44 0xAD: 1.73/3.46 0xAE: 1.74/3.48 0xAF: 1.75/3.5 0xB0: 1.76/3.52 0xB1: 1.77/3.54 0xB2: 1.78/3.56 0xB3: 1.79/3.58 0xB4: 1.80/3.6 0xB5: 1.81/Reserved 0xB6: 1.82/Reserved 0xB7: 1.83/Reserved 0xB8: 1.84/Reserved 0xB9: 1.85/Reserved 0xBA: 1.86/Reserved 0xBB: 1.87/Reserved 0xBC: 1.88/Reserved 0xBD: 1.89/Reserved 0xBE: 1.9/Reserved 0xBF: 1.91/Reserved 0xC0: 1.92/Reserved	

Address	Register	Bit	Type	Function	Detail	Default
					0xC1: 1.93/Reserved 0xC2: 1.94/Reserved 0xC3: 1.95/Reserved 0xC4: 1.96/Reserved 0xC5: 1.97/Reserved 0xC6: 1.98/Reserved 0xC7: 1.99/Reserved 0xC8: 2/Reserved 0xC9: 2.01/Reserved 0xCA: 2.02/Reserved 0xCB: 2.03/Reserved 0xCC: 2.04/Reserved 0xCD: 2.05/Reserved 0xCE: 2.06/Reserved 0xCF: 2.07/Reserved 0xD0: 2.08/Reserved 0xD1: 2.09/Reserved 0xD2: 2.1/Reserved 0xD3: 2.11/Reserved 0xD4: 2.12/Reserved 0xD5: 2.13/Reserved 0xD6: 2.14/Reserved 0xD7: 2.15/Reserved 0xD8: 2.16/Reserved 0xD9: 2.17/Reserved 0xDA: 2.18/Reserved 0xDB: 2.19/Reserved 0xDC: 2.2/Reserved 0xDD: Reserved … 0xFF: Reserved	
0x12	PMC_CH4_VOUT	7	R/W	CH4_VOUT_INT	CH4 output voltage (V) Format is (without divider)/(with divider) **Value Description** 0x00: Reserved … 0x4F: Reserved 0x50: 0.80/1.60 0x51: 0.81/1.62 0x52: 0.82/1.64 0x53: 0.83/1.66 0x54: 0.84/1.68 0x55: 0.85/1.70 0x56: 0.86/1.72 0x57: 0.87/1.74 0x58: 0.88/1.76 0x59: 0.89/1.78 0x5A: 0.90/1.80	50b

Address	Register	Bit	Type	Function	Detail	Default
					0x5B: 0.91/1.82 0x5C: 0.92/1.84 0x5D: 0.93/1.86 0x5E: 0.94/1.88 0x5F: 0.95/1.90 0x60: 0.96/1.92 0x61: 0.97/1.94 0x62: 0.98/1.96 0x63: 0.99/1.98 0x64: 1.00/2.00 0x65: 1.01/2.02 0x66: 1.02/2.04 0x67: 1.03/2.06 0x68: 1.04/2.08 0x69: 1.05/2.10 0x6A: 1.06/2.12 0x6B: 1.07/2.14 0x6C: 1.08/2.16 0x6D: 1.09/2.18 0x6E: 1.10/2.20 0x6F: 1.11/2.22 0x70: 1.12/2.24 0x71: 1.13/2.26 0x72: 1.14/2.28 0x73: 1.15/2.30 0x74: 1.16/2.32 0x75: 1.17/2.34 0x76: 1.18/2.36 0x77: 1.19/2.38 0x78: 1.20/2.40 0x79: 1.21/2.42 0x7A: 1.22/2.44 0x7B: 1.23/2.46 0x7C: 1.24/2.48 0x7D: 1.25/2.50 0x7E: 1.26/2.52 0x7F: 1.27/2.54 0x80: 1.28/2.56 0x81: 1.29/2.58 0x82: 1.30/2.60 0x83: 1.31/2.62 0x84: 1.32/2.64 0x85: 1.33/2.66 0x86: 1.34/2.68 0x87: 1.35/2.70 0x88: 1.36/2.72 0x89: 1.37/2.74 0x8A: 1.38/2.76 0x8B: 1.39/2.78 0x8C: 1.40/2.8	

Address	Register	Bit	Type	Function	Detail	Default
					0x8D: 1.41/2.82 0x8E: 1.42/2.84 0x8F: 1.43/2.86 0x90: 1.44/2.88 0x91: 1.45/2.9 0x92: 1.46/2.92 0x93: 1.47/2.94 0x94: 1.48/2.96 0x95: 1.49/2.98 0x96: 1.50/3 0x97: 1.51/3.02 0x98: 1.52/3.04 0x99: 1.53/3.06 0x9A: 1.54/3.08 0x9B: 1.55/3.1 0x9C: 1.56/3.12 0x9D: 1.57/3.14 0x9E: 1.58/3.16 0x9F: 1.59/3.18 0xA0: 1.60/3.2 0xA1: 1.61/3.22 0xA2: 1.62/3.24 0xA3: 1.63/3.26 0xA4: 1.64/3.28 0xA5: 1.65/3.3 0xA6: 1.66/Reserved 0xA7: 1.67/Reserved 0xA8: 1.68/Reserved 0xA9: 1.69/Reserved 0xAA: 1.7/Reserved 0xAB: 1.71/Reserved 0xAC: 1.72/Reserved 0xAD: 1.73/Reserved 0xAE: 1.74/Reserved 0xAF: 1.75/Reserved 0xB0: 1.76/Reserved 0xB1: 1.77/Reserved 0xB2: 1.78/Reserved 0xB3: 1.79/Reserved 0xB4: 1.8/Reserved 0xB5: 1.81/Reserved 0xB6: 1.82/Reserved 0xB7: 1.83/Reserved 0xB8: 1.84/Reserved 0xB9: 1.85/Reserved 0xBA: 1.86/Reserved 0xBB: 1.87/Reserved 0xBC: 1.88/Reserved 0xBD: 1.89/Reserved 0xBE: 1.9/Reserved	

Address	Register	Bit	Type	Function	Detail	Default
					0xBF: 1.91/Reserved 0xC0: 1.92/Reserved 0xC1: 1.93/Reserved 0xC2: 1.94/Reserved 0xC3: 1.95/Reserved 0xC4: 1.96/Reserved 0xC5: 1.97/Reserved 0xC6: 1.98/Reserved 0xC7: 1.99/Reserved 0xC8: 2/Reserved 0xC9: 2.01/Reserved 0xCA: 2.02/Reserved 0xCB: 2.03/Reserved 0xCC: 2.04/Reserved 0xCD: 2.05/Reserved 0xCE: 2.06/Reserved 0xCF: 2.07/Reserved 0xD0: 2.08/Reserved 0xD1: 2.09/Reserved 0xD2: 2.1/Reserved 0xD3: 2.11/Reserved 0xD4: 2.12/Reserved 0xD5: 2.13/Reserved 0xD6: 2.14/Reserved 0xD7: 2.15/Reserved 0xD8: 2.16/Reserved 0xD9: 2.17/Reserved 0xDA: 2.18/Reserved 0xDB: 2.19/Reserved 0xDC: 2.2/Reserved 0xDD: Reserved … 0xFF: Reserved	
0x14	PMC_CONFIG_00	[7:1]	R/W	I2C_SLAVE_ADDR	I2C slave address	A2b
		0	R/W	I2C_FMP	I2C mode 0: Fast-mode or standard mode 1: Fast-mode-plus	0b
0x1F	PMC_CONFIG_0B	[7:4]	R/W	RESERVED	-	Eb
		3	R/W	SEQ_EN	0: Disable (channels not enabled) 1: Enable (SEQ runs to enable channels)	0b
		[2:0]	R/W	RESERVED	-	3b
0x41	OTP_VARIANT_ID	[7:4]	R	MRC	Silicon revision	0b
		[3:0]	R/W	VRC	0: ASIC 2: ASSP	0b

Address	Register	Bit	Type	Function	Detail	Default
0x42	OTP_CUSTOMER_ID	[7:0]	R/W	CUST_ID	OTP file version	0b
0x43	OTP_CONFIG_ID	[7:0]	R/W	CONFIG_REV	OTP variant	0b
0x4C	BUCK_BUCK_OPT_04	7	R/W	BUCK1_OPT_CTRL6	Enable resistive divider on FB to double VOUT: 0: Divider disable 1: Divider enable	0b
		[6:0]	R/W	RESERVED	-	20b
0x4D	BUCK_BUCK_OPT_05	7	R/W	BUCK2_OPT_CTRL6	Enable resistive divider on FB to double VOUT: 0: Divider disable 1: Divider enable	0b
		[6:0]	R/W	RESERVED	-	28b
0x4E	BUCK_BUCK_OPT_06	7	R/W	BUCK3_OPT_CTRL6	Enable resistive divider on FB to double VOUT: 0: Divider disable 1: Divider enable	0b
		[6:0]	R/W	RESERVED	-	28b
0x4F	BUCK_BUCK_OPT_07	7	R/W	BUCK4_OPT_CTRL6	Enable resistive divider on FB to double VOUT: 0: Divider disable 1: Divider enable	0b
		[6:0]	R/W	RESERVED	-	28b

7 Package Information

7.1 Package Outlines

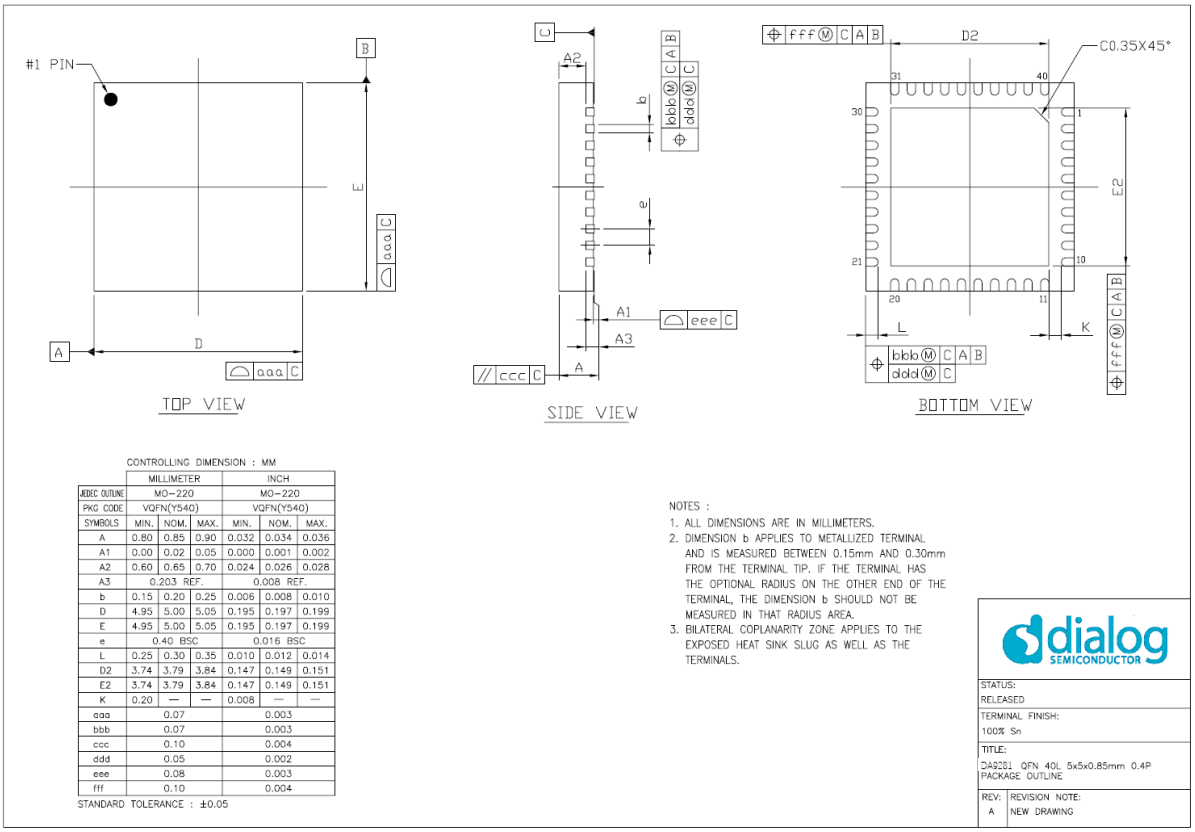


Figure 21: QFN40 Package Outline Drawing

7.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 19.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The QFN40 package is qualified for MSL 3.

Table 19: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

7.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

8 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 20: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9281-xxAT1	QFN-40	5 x 5 x 0.85	Waffle tray	490
DA9281-xxAT2	QFN-40	5 x 5 x 0.85	Tape and reel	5000

Part Number Legend:

DA9281-xxAT1

xx: OTP variant

9 Application Information

The following recommended components are references selected from requirements of a typical application.

9.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all V_{INx} and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 21: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tol. (%)	V-Rate	Type
V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4} input bypass	1x 22 µF	0805	X5R	±20	16 V	Murata GRM21BR61C226ME44L
V_{IN5}, V_{IN6}, V_{IN7}, V_{IN8} input bypass	1x 2.2 µF	0603	X7R	±10	10 V	TDK C1608X7R1A225K080AC
V_{OUT1} output bypass	5x 22 µF	0805	X5R	±20	16 V	Murata GRM21BR61C226ME44L
V_{OUT2}, V_{OUT3}, V_{OUT4}, output bypass	3x 22 µF	0805	X5R	±20	16 V	Murata GRM21BR61C226ME44L
V_{OUT5} output bypass	1x 10 µF	0603	X5R	±10	10 V	Murata GRM188R61A106KE69D
				±20		Murata GRM188R61A106ME69#
V_{OUT6}, V_{OUT7} output bypass	1x 4.7 µF	0603	X5R	±10	16 V	Murata GRM188R61C475KAAJD
						Murata GRM188R61C475KE11#
VOUT8 output bypass	1x 22 µF	0805	X5R	±20	16 V	Murata GRM21BR61C226ME44L
AVCC bypass	1x 10 µF	0603	X5R	±10	10 V	Murata GRM188R61A106KE69D

9.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current

  Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.

- DC resistance

  Critical for the converter efficiency and should therefore be minimized.

Fully shielded inductors are highly recommended to use. The typical recommended output inductances are 0.47 µH for CH1 and 1.0 µF for CH2, CH3 and CH4. Use of larger output inductance degrades the load transient performance of the buck converters.

Table 22: Recommended Inductor Types

Application	Value (µH)	Size (mm)	I_{MAX} (DC) (A)	I_{SAT} (A)	Tol. (%)	DC Resistance (mΩ)	Type
LX_1 output inductor	0.47	2.5 x 2.0 x 1.2	5.8	7.4	±20	17	Murata DFE252012F-R47M=P2
LX_2, LX_3, LX_4 output inductor	1.0	2.5 x 2.0 x 1.2	3.9	5.3	±20	33	Murata DFE252012F-1R0M=P2

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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