High Efficiency Dual Cell Switched Capacitor Divider

General Description

DA9313 is a high-voltage power converter with a maximum output current of 10 A, suitable for applications supplied from a dual (2S) Li-ion or Li-polymer stacked cell battery pack, or any input voltage between 5 V and 10.5 V. The converter operates with efficiency during conversion of up to 98 %. Master/slave operation is offered, where a pair of devices can combine to double the peak output current to 20 A.

Low profile external components and a minimum PCB footprint allow small circuit implementation in compact applications. The pass devices are fully integrated therefore no external FETs are needed.

DA9313 utilizes a programmable soft start to limit the inrush current from the input node and secure a slope controlled activation of the rails. It also implements integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components.

Enable, low power mode entry and exit, and power good signals are available at configurable ports flexibly supporting different applications and power-up or power-down scenarios.

Key Features

- 2S to 1S power voltage converter
- 5 V to 10.5 V input voltage (2S Li-ion stacked battery pack)
- 10 A total output current (standalone)
- 20 A total output current (master/slave)
- 1.0 mm max external components height
- Integrated power switches
- I^2C compatible interface
- $V_{OUT} = ½ V_{IN}$
- High and flat efficiency, up to 98 %
- Typical 55 µA quiescent current (standalone)
  - Typical 70 µA total quiescent current in master/slave configuration
- Package 43 WLCSP (RouteEasy™ equivalent to 0.65 mm pitch)

Applications

- Ultrabooks™
- Notebook computers
- Chromebooks™
- Tablets
- Smartphone direct charging
- DSLR and mirrorless cameras
- Camcorders
- Power banks
- 2S battery applications

Contents

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Tables

1 Terms and Definitions

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
HBM	Human Body Model
OTP	One Time Programmable
PCB	Printed Circuit Board
PG	Power Good
PMIC	Power Management Integrated Circuit
POR	Power On Reset
PVC	Power Voltage Converter
PWC	Power Cycle

2 References

[1] UM10204 I^2C Bus Specification and User Manual

3 Functional Block Diagrams

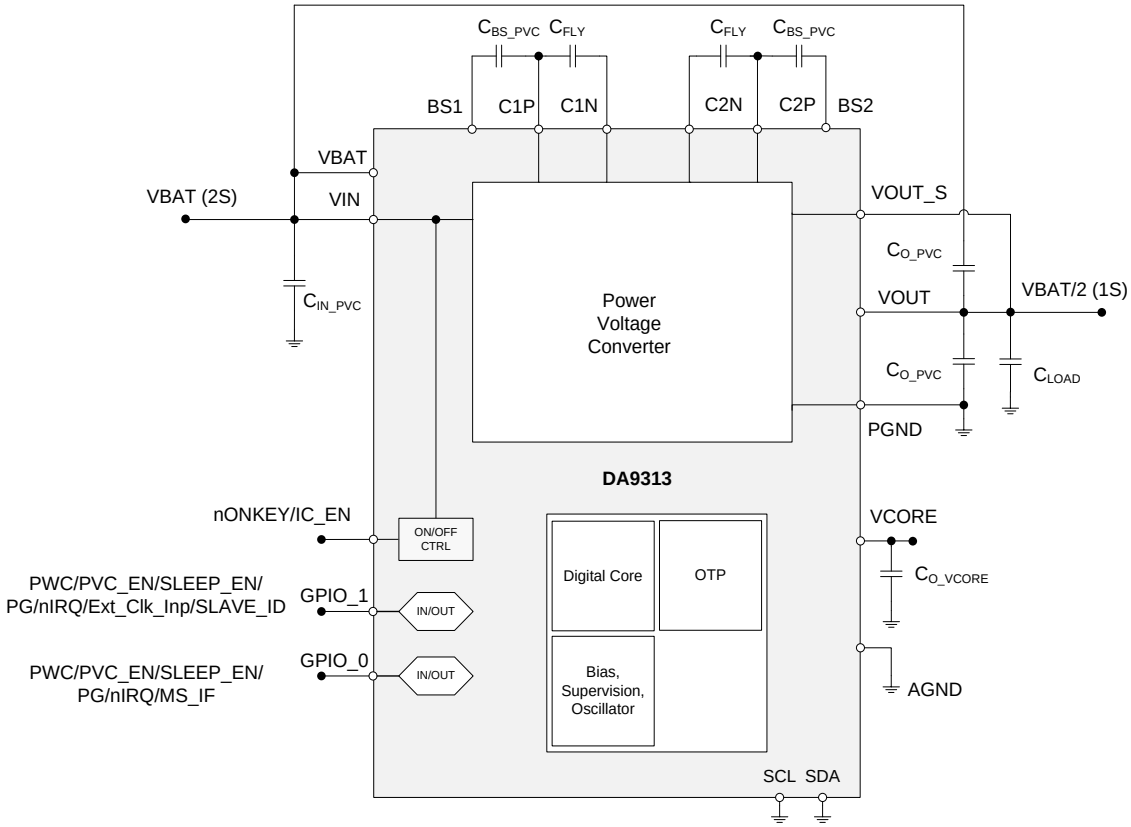


Figure 1: Functional Block Diagram Standalone (I^2C Not Connected)

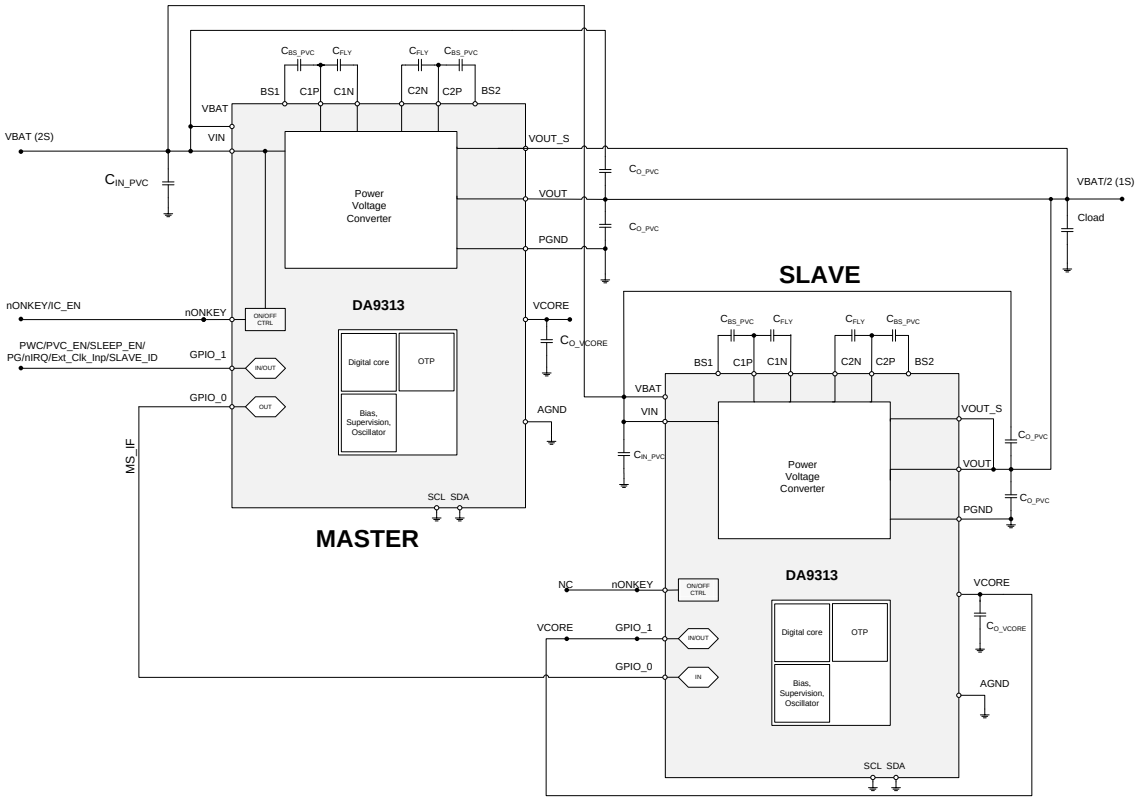


Figure 2: Functional Block Diagram Master/Slave Operation (I^2C Not Connected)

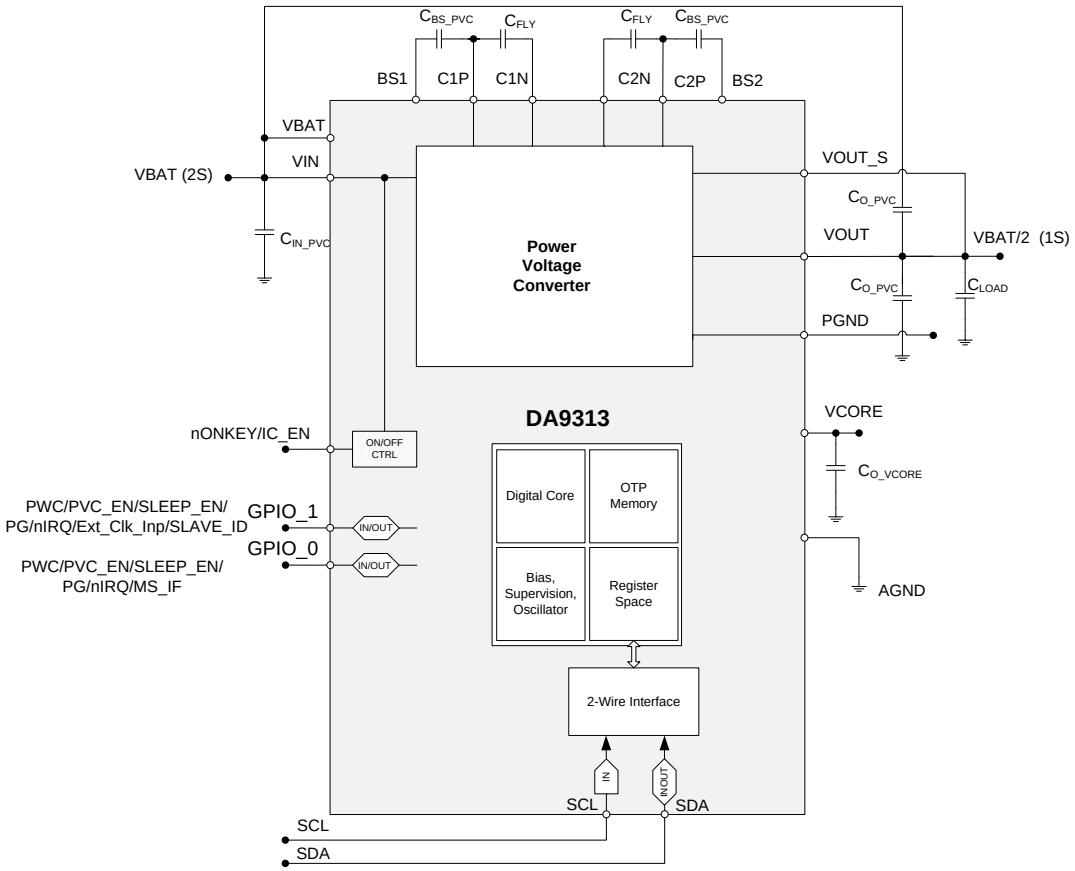


Figure 3: Functional Block Diagram Standalone (I^2C Connected)

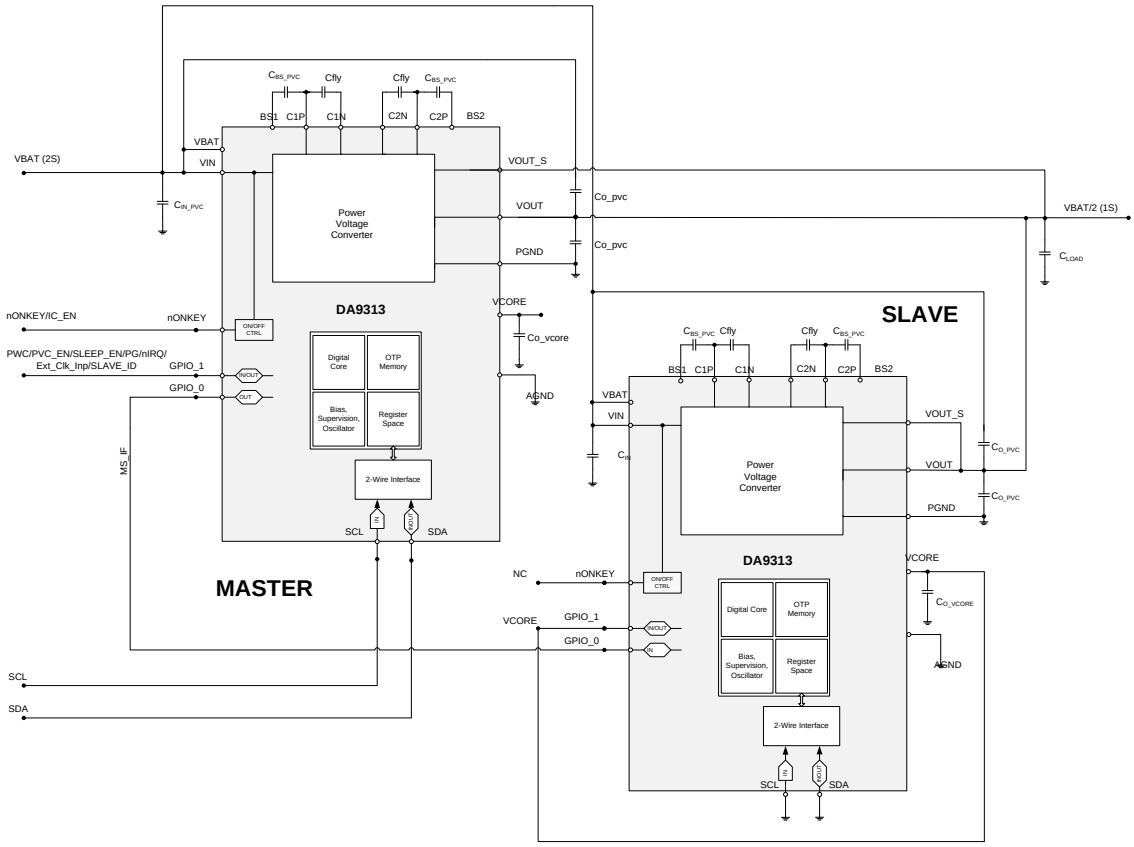


Figure 4: Functional Block Diagram Master/Slave Operation (I^2C Connected)

4 Pinout

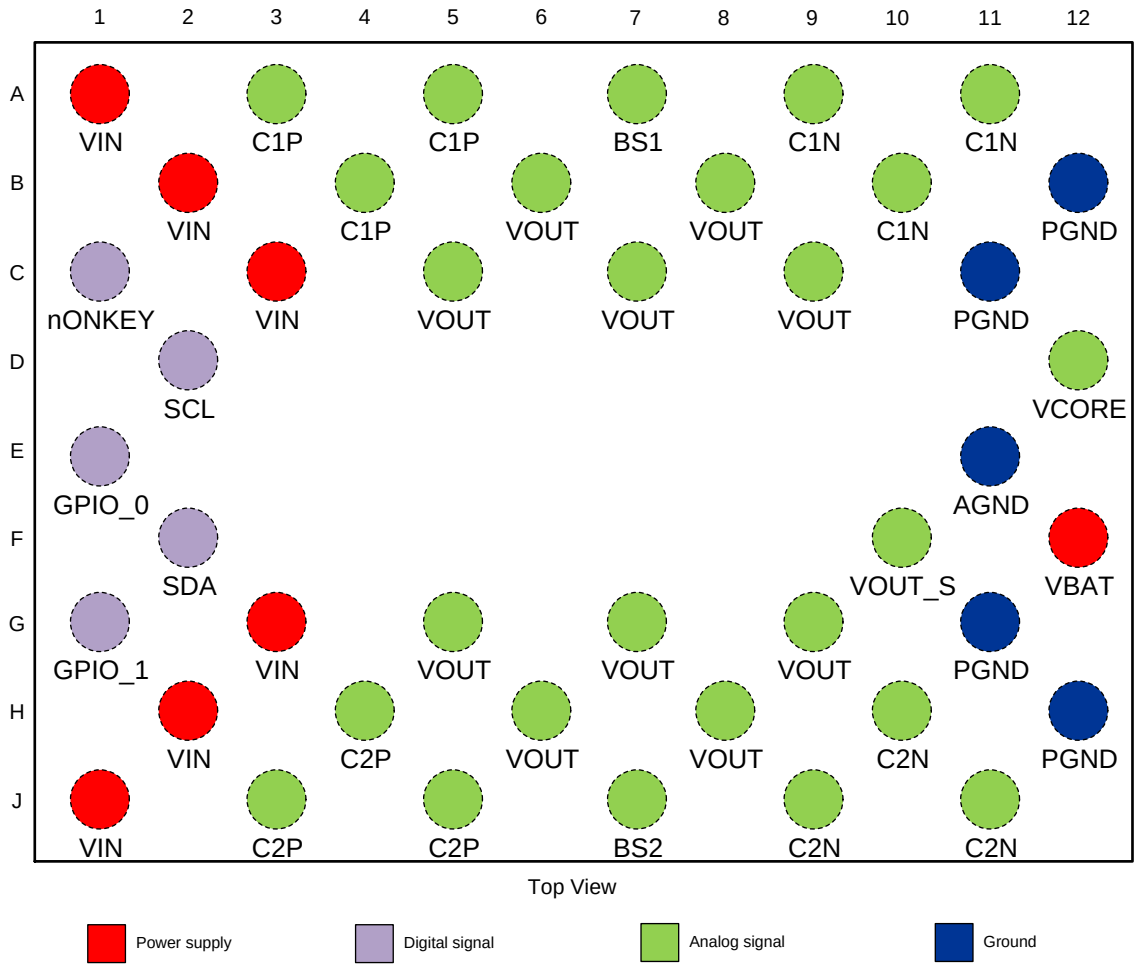


Figure 5: Connection Diagram

Table 1: Pin Description

Location	Pin Name	Pin Type (Table 2)	Description
F12	VBAT	AI/P	V_{BAT} input for voltage supervision and supply input voltage for power voltage converter controller
A1, B2, C3 J1, H2, G3	VIN	PWR	Supply input voltage for power path
A3, B4, A5	C1P	AIO	Flying capacitance 1 positive terminal
A9, B10, A11	C1N	AIO	Flying capacitance 1 negative terminal
A7	BS1	AIO	Boot strap capacitor positive terminal for power voltage converter
J3, H4, J5	C2P	AIO	Flying capacitance 2 positive terminal
J9, H10, J11	C2N	AIO	Flying capacitance 2 negative terminal
J7	BS2	AIO	Boot strap capacitor positive terminal for power voltage converter
B6, B8, C5, C7, C9, G5, G7,G9, H6, H8	VOUT	AO	Power voltage converter output voltage

Location	Pin Name	Pin Type (Table 2)	Description
F10	VOUT_S	AI	Power voltage converter output sense
D12	VCORE	AIO	Main internal supply
C1	nONKEY	AIO	On key signal (active low)
E1	GPIO_0	DIO	General purpose input/output
G1	GPIO_1	DIO	General purpose input/output
F2	SDA	DIO	I^2C data. Must be connected to GND if no I^2C interface
D2	SCL	DI	I^2C clock. Must be connected to GND if no I^2C interface
E11	AGND	GND	Analog quiet ground
B12, C11, G11, H12	PGND	GND	Power ground for power voltage converter

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
PWR	Power Supply	GND	Ground

5 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_{STG}	Storage temperature		-65	+165	°C
T_A	Operating temperature		-40	+85	°C
T_J	Junction temperature		-40	+125	°C
V_{DD_LIM}	Limiting supply voltage VBAT, VIN,	PVC_EN =0 and VBAT, VIN ramp < 1 V/µs	-0.3	20	V
V_{VOUT_LIM}	Limiting output voltage converter voltage		-0.3	5.5	V
V_{C1P_LIM}, V_{C2P_LIM}	Limiting flying cap positive pin voltage C1P, C2P	When the voltage converter is off $V_{C1P} = V_{C2P} = V_{VOUT} = 0$	-0.3	V_{O_PVC} + 5.5	V
V_{C1N_LIM}, V_{C2N_LIM}	Limiting flying cap negative pin voltage C1N, C2N		-0.3	+ 5.5	V
V_{BS1_LIM}, V_{BS2_LIM}	Limiting bootstrap voltage converter pin voltage BS1, BS2		-0.3	$V_{C1P/C2P}$ + 5.5	V
V_{CORE_LIM}	Limiting VCORE voltage		-0.3	5.5	V
V_{PIN_LIM}	Limiting voltage at all pins		-0.3	V_{O_VCORE} + 0.3	V
R_{TH}	Thermal resistance (junction to ambient θ_{JA})			36.8	ºC/W
V_{ESD_HBM}	Electrostatic discharge voltage	Human Body Model (HBM)		2	kV

Note 1 Stresses beyond those listed under absolute maximum ratings (Table 3) may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	$V_{DD} = V_{BAT}$	5	7.4	10.5	V
$I_{O\_MAX\_PVC\_DC}$	PVC maximum continuous output current		8.2			A

7 Electrical Characteristics

7.1 Power-On-Reset, Reference Generation and Supervision

Table 5: Power-on-Reset, Reference and Supervision Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{IN} = 5 V to 10.5 V for standalone/master device

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{DD_PD}	Quiescent current in POWER_DOWN mode			6		µA
I_{DD_ACT}	Quiescent current in ACTIVE/SLEEP mode (standalone)	PVC enabled in auto. frequency mode no load VDDIO disabled		55		µA
$I_{DD\_ACT\_MASTER}$	Quiescent current in ACTIVE mode (master)	PVC enabled in auto. frequency mode no load VDDIO disabled		60		µA
$I_{DD\_ACT\_SLAVE}$	Quiescent current (slave)	Master PVC in auto. frequency mode no load VDDIO disabled		10		µA
$V_{TH\_LO\_POR}$	Power on reset lower threshold	Measured @VCORE VDD decreasing	2.8			V
$V_{TH\_HI\_POR}$	Power on reset higher threshold	Measured @VCORE VDD increasing			3.7	V
$V_{TH\_UVLO\_VDD}$	Under voltage lockout threshold @ VDD	VDD decreasing Configurable in 50 mV steps (Note 1) (VBAT_UV_CRIT)	4.6	5.0	6.15	V
$V_{TH\_UVLO\_ACC}$	Under voltage lockout threshold accuracy		-2		+2	%
$V_{HYST\_UVLO\_VDD}$	Under voltage lockout hysteresis @ VDD	Configurable in 50 mV steps (VBAT_UV_HYS)	50	200	400	mV
V_{TH_WARN}	Under voltage warning threshold	V_{DD} decreasing Configurable in 200 mV steps (VBAT_UV_WARN)	5.2		6.6	V
$V_{TH\_WARN\_ACC}$	Under voltage warning threshold accuracy		-2		+2	%
$V_{TH\_PG\_PVC}$	Power voltage converter power good threshold	Configurable in 100 mV steps (PVC_PG_ADJ)	2.5	3.0	5.0	V
$V_{TH\_PG\_ACC}$	Power voltage converter power good threshold accuracy		-2		+2	%
$V_{HYST\_PG\_PVC}$	Power voltage converter power good hysteresis			100		mV
T_{TH_WARN} (Note 2)	Thermal warning threshold temperature		110	125	140	°C
T_{TH_CRIT} (Note 2)	Thermal critical threshold temperature		125	140	155	°C
t_{ACTIVE}	Time to ACTIVE from	NONKEY_MODE= 0	1.5		3.5	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
	OFF mode	AUTOBOOT = 1				
t_{EN}	Time to ACTIVE from POWER_DOWN mode	NONKEY_MODE= 1 after IC_EN asserted NONKEY_DEBOUNCE = 001			500	µs

Note 1 PVC requires 5.0 V minimum setting for correct operation.

Note 2 Thermal thresholds are non-overlapping.

7.2 Internal Oscillator

Table 6: Internal Oscillator Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{DD} = 5 V to 10.5 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OSC}	Internal oscillator frequency			6		MHz
f_{OSC_ACC}	Internal oscillator frequency accuracy	After trimming	-5		+5	%

7.3 Power Voltage Converter

Table 7: Power Voltage Converter Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{DD} = 5 V to 10.5 V and typical external components

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	V_{DD} = V_{BAT} (Note 1)	5.0		10.5	V
V_{O_PVC}	Power voltage converter output voltage	I_{OUT} = 0		50		%
$I_{O\_MAX\_PVC}$	Power voltage converter maximum output current				10	A
I_{LIM_PVC}	Power voltage converter current limit	Configurable in 450 mA steps (PVC_ILIM)	4.8		11.55	A
I_{LIM_ACC}	Power voltage converter current limit accuracy	I_O = I_{LIM_PVC} trimming range	-20		+20	%
		I_O = 10 A	-10		+10	
I_{ALARM}	Current alarm			80 % I_{LIM_PVC}		A
C_{FLY}	External flying capacitors	Nominal (Note 2)		2 * 47		µF
C_{O_PVC}	External output capacitors	Nominal		4.7		µF
C_{LOAD}	External load capacitor			47	470	µF
C_{BS_PVC}	External boot strap capacitors 1 and 2	Nominal		10		nF
C_{IN_PVC}	External decoupling capacitor	Nominal		2 * 4.7		µF

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{STUP_PVC}	Power voltage converter start-up current	Configurable in 500 mA steps (I_STUP_PVC)	500		2000	mA
f_{SW_PVC}	Power voltage converter switching frequency	Fixed frequency mode		500		kHz
η_{peak}	Power converter peak efficiency	V_{DD} = 7.4 V fixed frequency mode / auto. frequency mode		98		%
η_{PVC}	Power voltage converter efficiency	V_{DD} = 7.4 V I_{OUT} = 30 mA to 3 A, auto. frequency mode	97.5			%
η_{PVC}	Power voltage converter efficiency	V_{DD} = 7.4 V I_{OUT} = 500 mA to 8 A, fixed frequency mode I_{OUT} = 10 mA to 5.5 A auto. frequency mode		95		%
η_{PVCMS}	Power voltage converter efficiency (master/slave)	V_{DD} = 7.4 V I_{OUT} = 1 A to 15 A, fixed frequency mode I_{OUT} = 10 mA to 10 A auto. frequency mode		95		%
I_{Q_PVC}	PVC quiescent current	V_{DD} = 7.4 V no load auto. frequency mode		13		µA

Note 1 When PVC_EN = 1, the maximum allowed slew rate on V_{BAT} and V_{IN} is 0.2 V/µs

Note 2 Effective capacitance must be C_{FLY} ≥ 18 µF @ 5 V, I_{RMS} = 8 A

7.4 VCORE

Table 8: VCORE Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{DD} = 5 V to 10.5 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	V_{DD} = V_{BAT}	5.0		10.5	V
V_{O_VCORE}	Output voltage @ VCORE			4.0		V
I_{O_VCORE}	Max load on VCORE				20	mA
$V_{O\_VCORE\_ACC}$	Accuracy of output voltage at VCORE		-5		+5	%
C_{O_VCORE}	External output capacitance @ VCORE (Note 1)	Including voltage and temperature coefficient		2.2		µF

Note 1 Effective external capacitance should be min 0.5 µF, max 1.3 µF and is typically 1.0 µF.

7.5 VDDIO

Table 9: VDDIO Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{DD} = 5 V to 10.5 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DDIO}	Internal VDDIO voltage rail	Internally generated, no external capacitor Configurable via VDDIO_CONF	1.5	1.8	3.3	V
V_{DDIO_ACC}	Accuracy of internal VDDIO voltage rail		-5		+5	%

7.6 Digital I/O Characteristics

Table 10: Digital I/O Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC, V_{DD} = 5 V to 10.5 V, VDDIO enabled

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH_ONKEY}	HIGH level input voltage @ pin nONKEY		1.1			V
V_{IL_ONKEY}	LOW level input voltage @ pin nONKEY				0.4	V
V_{HYS_ONKEY}	Hysteresis voltage @ pin nONKEY			100		mV
$R_{O\_PU\_GPO}$	Pull-up resistor @ GPO			24		kΩ
$R_{I\_PD\_GPI}$	Pull-down resistor @ GPI			210		kΩ
$R_{I\_PU\_ONKEY}$	Pull-up resistor @ nONKEY	To VCORE		21		kΩ
V_{IH}	GPI_0-1, SCL, SDA, Input HIGH voltage		0.7*V_{DDIO}			V
V_{IL}	GPI_0-1, SCL, SDA, Input LOW voltage				0.3* V_{DDIO}	V
V_{OH}	GPO_0-1 Output HIGH voltage	Push-pull mode @1 mA	0.8* (V_{CORE} or V_{DDIO})			V
V_{OL1}	GPO_0-1, SDA, Output LOW voltage	@I_{OL} = 1 mA			0.1	V
V_{OL3}	SDA, Output LOW voltage	@I_{OL} = 3 mA			0.24	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL20}	SDA Output LOW voltage	@I_{OL} = 20 mA			0.4	V
C_{GPO_LOAD}	GPO_0-1 Maximum capacitive load				50	pF
C_{IN_I2C}	CLK, SDA Input capacitance			2.5	10	pF
t_{SP}	CLK, SDA Spike suppression pulse width	Fast-mode / Fast-mode Plus High-speed (Hs) mode	0 0		50 10	ns

8 I²C Control Bus

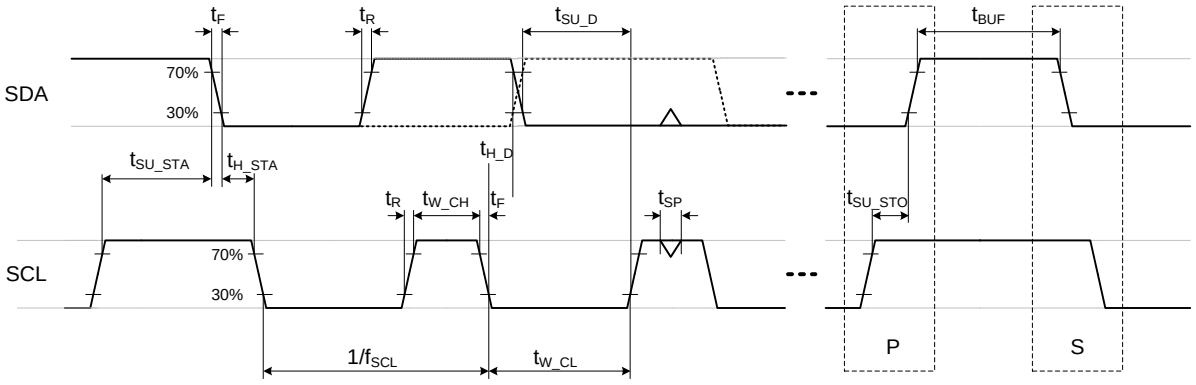


Figure 6: I²C Bus Timing

Table 11: I²C Control Bus Characteristics

Unless otherwise noted, the following is valid for T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Max	Unit
t_{BUF}	Bus free time from STOP to START condition		0.5		µs
C_b	Bus line capacitive load			150	pF
Standard-mode / Fast-mode / Fast-mode Plus					
f_{SCL}	Clock frequency @ pin SCL		0 (Note 1)	1000	kHz
t_{SU_STA}	START condition set-up time		0.26		µs
t_{H_STA}	START condition hold time		0.26		µs
t_{W_CL}	Clock LOW duration		0.5		µs
t_{W_CH}	Clock HIGH duration		0.26		µs
t_R	Rise time @ pin SCL and SDA	Input requirement		1000	ns
t_F	Fall time @ pin SCL and SDA	Input requirement		300	ns
t_{SU_D}	Data set-up time		50		ns
t_{H_D}	Data hold time		0		ns
High-Speed Mode					
f_{CLK_HS}	Clock frequency @ pin SCL		0 (Note 1)	3400	kHz
$t_{SU\_STA\_HS}$	START condition set-up time		160		ns
$t_{H\_STA\_HS}$	START condition hold time		160		ns
$t_{W\_CL\_HS}$	Clock LOW duration		160		ns
$t_{W\_CH\_HS}$	Clock HIGH duration		60		ns
t_{R_HS}	Rise time @ pin SCL and SDA	Input requirement		160	ns
t_{F_HS}	Fall time @ pin SCL and SDA	Input requirement		160	ns
$t_{SU\_D\_HS}$	Data set-up time		10		ns
$t_{H\_D\_HS}$	Data hold time		0		ns
$t_{SU\_STO\_HS}$	STOP condition set-up time		160		ns

Note 1 Maximum clock period is 38 ms if OTP control I2C_TO_EN is enabled.

9 Typical Characteristics

9.1 Standalone Operation

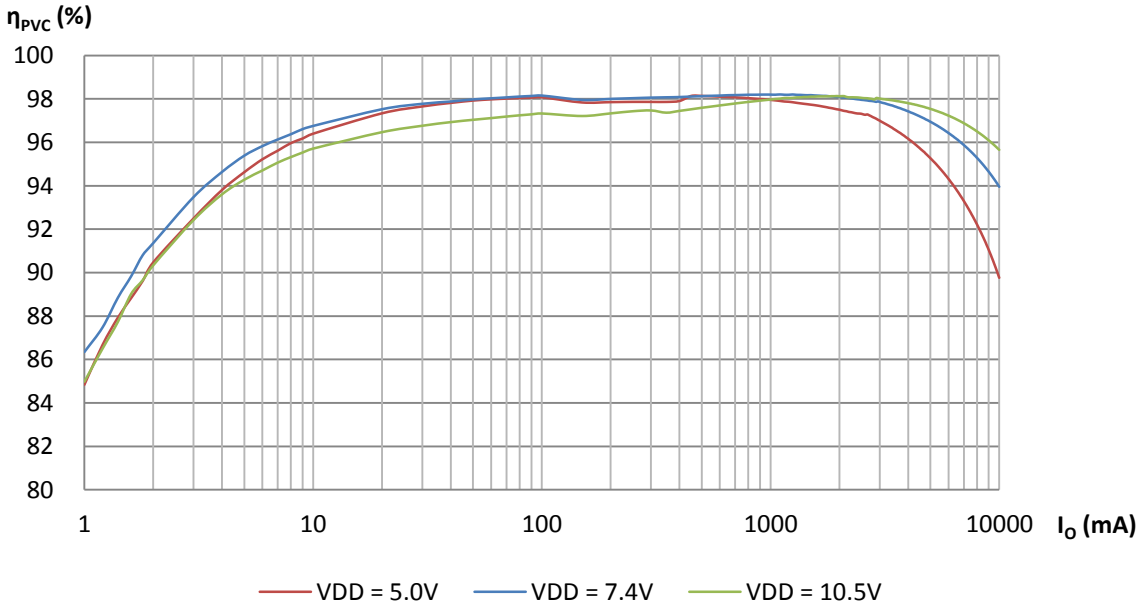


Figure 7: DA9313 Efficiency Automatic Mode Standalone

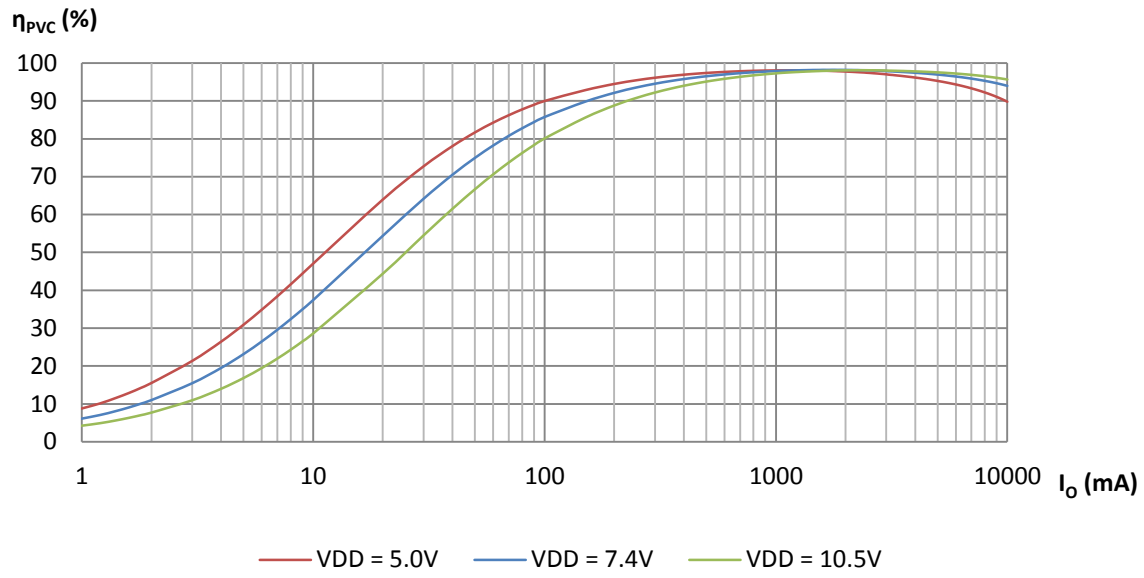


Figure 8: DA9313 Efficiency Fixed Frequency Mode Standalone

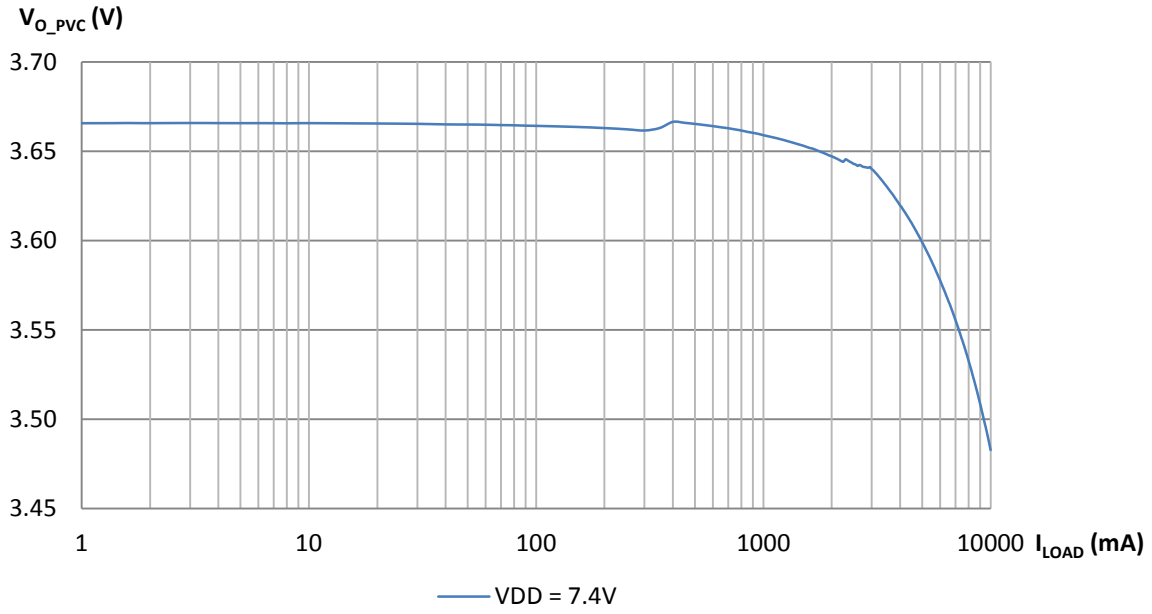


Figure 9: DA9313 Output Voltage Drop Automatic Mode Standalone

9.2 Master/Slave Operation

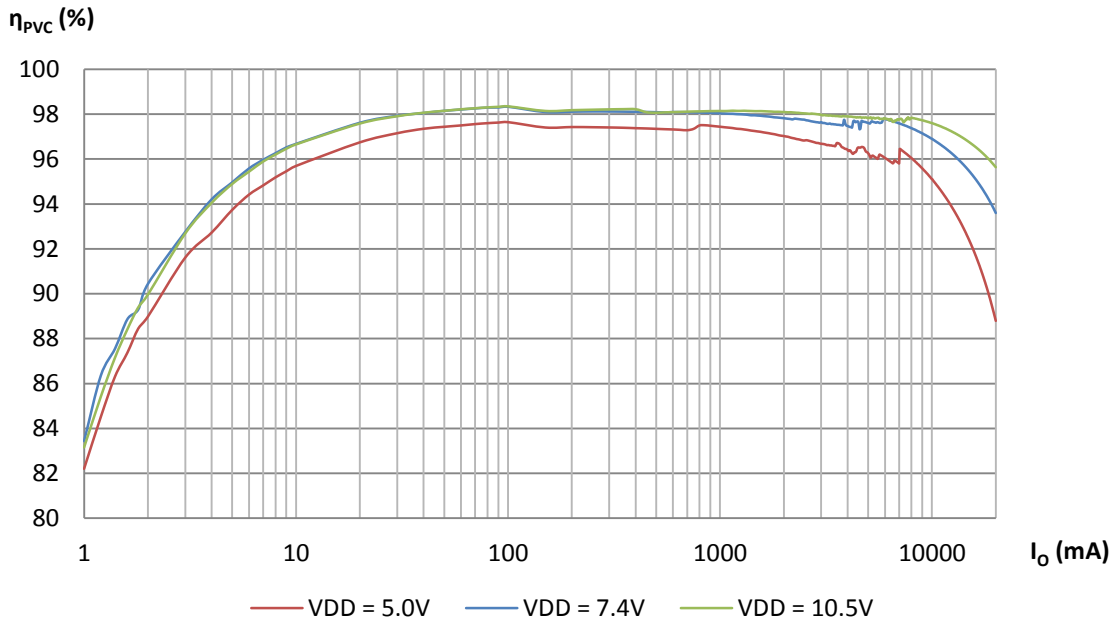


Figure 10: DA9313 Efficiency Automatic Mode Master/Slave

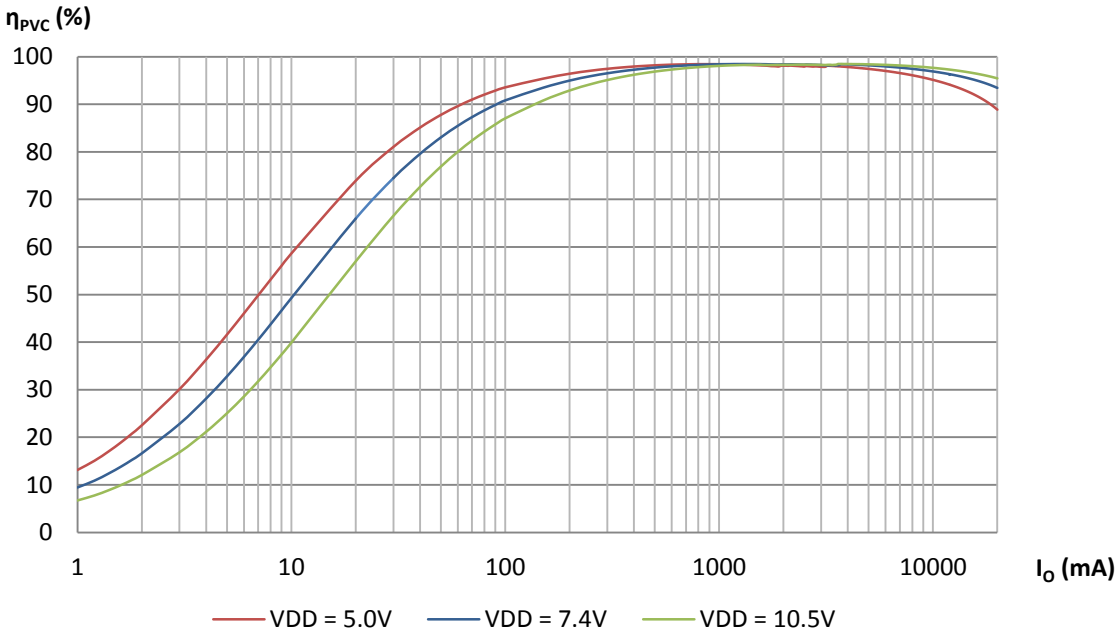


Figure 11: DA9313 Efficiency Fixed Frequency Mode Master/Slave

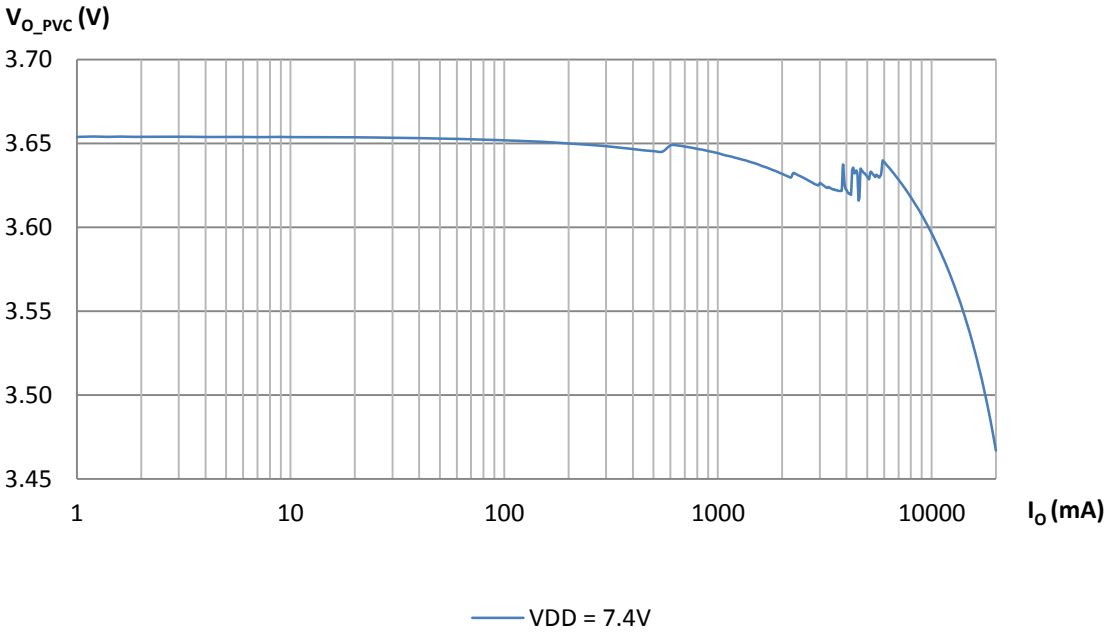


Figure 12: DA9313 Output Voltage Drop Automatic Mode Master/Slave

10 Functional Description

DA9313 is a 2S compliant high-voltage power converter that generates an unregulated 1S output voltage (V_{OUT}) of half of V_{IN} using a capacitive interleaved charge-pump divider. V_{OUT} is a 10 A peak current output in standalone configuration and 20 A peak current when driven from two DA9313 chips paired in master/slave configuration.

Host communication is not required for operation with OTP loading to configure DA9313 on start-up. However, an I^2C interface is available for host configuration of the register map if required. In addition, the GPIOs can be configured as nIRQ for fault signaling and recovery. An internal LDO can be enabled to supply VDDIO if required.

10.1 Start Up

DA9313 is OTP configured as a standalone or master/slave variant. The OTP variants are described in a separate document.

10.1.1 Standalone Operation

DA9313 starts as a standalone device as default, when master/slave operation is not enabled (MSTSLV_IF_EN bit is set to 0).

On battery insertion the full OTP content is loaded to the register map. DA9313 self-checks that the system is stable and then proceeds to ACTIVE Mode or POWER_DOWN Mode as configured by the AUTOBOOT bit.

POWER_DOWN mode is an ultra-low power state of the system implemented to extend the shelf life of applications with a battery connected during shipping and before first user boot. DA9313 can be brought from POWER_DOWN mode to ACTIVE mode via a user press of the nONKEY pin (the user, or external IC, activated power on/off button). Once in ACTIVE mode the system will perform as configured in either automatic or fixed frequency mode, see section 10.3.3.

To ensure minimal quiescent current requirements the oscillator is enabled only on demand, see section 11.8. If necessary, the system can safely transfer clocking from the internal oscillator to an external clock (within the specified operating frequency, see Table 6) via GPIO configuration, see section 10.2.1.4.

DA9313 responds to critical faults by power cycling the device to protect circuitry, see section 11.5.

10.1.2 Master/Slave Operation

DA9313 starts in master/slave mode when MSTSLV_IF_EN bit is set to 1. GPIO_0 operates as the master/slave interface (MS_IF) and is pulled down internally. On the master device, GPIO_1 should not be driven externally. To configure the device as slave, GPIO_1 should be tied to VCORE of the slave device, see Figure 2. DA9313 will remain in this state unless a cold boot is performed by removing the battery.

The master takes control over the slave in such a way that the slave always operates in POWER_DOWN Mode.

10.1.2.1 Master Operation

In master operation, GPIO_0 operates as the master slave interface (MS_IF) and provides the PVC phase and enable/disable sequencing controls from the master to the slave. The start-up time is extended to ensure that the slave device completes the cold boot to POWER_DOWN mode sequence. Once the slave device has entered POWER_DOWN Mode, the master device enters ACTIVE Mode and GPIO_0 is configured as a push-pull GPO for use as a master/slave interface (MS_IF).

After the master device has entered ACTIVE mode, the master PVC triggers the slave PVC over the MS_IF. GPIO_1 is functional in the master and can be configured via I^2C.

NOTE
All master IOs, GPIO_1 and I^2C, are supplied from VCORE in master mode not VDDIO. Thus I^2C communications are only possible if host I^2C IOs also run from a 4 V supply, or are externally level shifted.

10.1.2.2 Slave Operation

When the device is operating as slave, it goes directly to POWER_DOWN Mode. There is no communication to the slave (slave I^2C lines are grounded) and the master controls the slave PVC directly via MS_IF.

10.2 Interface Functions

DA9313 incorporates two general purpose input/output pins (GPIOs) and a dual mode onkey (nONKEY) pin. Functions are assigned to the GPIOs via GPIO_CTRL and GPIO_CTRL_2 registers and to nONKEY via NONKEY_MODE in the MODE_CTRL register.

Table 12: GPIO Configuration Overview

GPIO	Input Functionality	Output Functionality	Alternative Functionality
GPIO_1	GPI (Note 1) PVC_EN SLEEP_EN PWC	GPO (Note 1) PG nIRQ (Note 1)	Digital clock input (Ext_Clk_Inp) SLAVE_ID
GPIO_0	GPI (Note 1) PVC_EN SLEEP_EN PWC	GPO (Note 1) PG nIRQ (Note 1)	Master/slave control interface (MS_IF)

Note 1 Valid when I^2C is enabled

10.2.1 GPIOs

A power good (PG) indicator can be routed to either GPIO for host power up sequencing. The power voltage converter enable, disable, and status field, PVC_EN, can be controlled via I^2C or GPI. The system controller can also be moved to a configurable SLEEP mode via I^2C or GPI control.

NOTE
When DA9313 is in master/slave mode all GPI's must be referenced to VCORE.

10.2.1.1 PVC Enable

The PVC can be disabled by an external PMIC (supplied from a different rail to the DA9313 PVC output). This function is only provided in ACTIVE Mode and SLEEP Mode when VDDIO_EN bit is high.

Either GPIO_1 or GPIO_0 can be configured as a PVC_EN pin via the GPIO_CTRL register, GPIO_1_PIN and GPIO_0_PIN. The PVC_EN pin controls the PVC_EN bit in the PVC_CTRL

register, allowing read-back of the current setting. The PVC_EN bit can also be controlled over I²C when not set to be driven from GPIO_1 or GPIO_0.

10.2.1.2 SLEEP Enable

In order to reduce power consumption to a minimum, the host processor can send DA9313 into SLEEP Mode. SLEEP mode is a configurable mode with configuration via the SLEEP_CTRL register. This function is available in ACTIVE Mode and SLEEP mode when VDDIO_EN bit is high.

Any GPI pin can be configured as SLEEP_EN via the GPIO_1_PIN and GPIO_0_PIN bits. The SLEEP_EN pin controls the SLEEP status bit in the MODE_CTRL register allowing read-back of the current setting. The SLEEP bit can also be controlled over I²C when not set to be driven from GPI, see section 11.4.

10.2.1.3 Power Cycle

The power cycle (PWC) input allows the host to perform a power cycle of DA9313 with OTP reload. This function is provided in ACTIVE Mode and SLEEP Mode when VDDIO_EN bit is high.

Any GPI pin can be configured as PWC via the GPIO_1_PIN and GPIO_0_PIN bits. After PWC assertion DA9313 de-asserts the power good (PG) pin for 10 µs and then initiates a power cycle.

The GPI_RESET bit is set in the FAULT_LOG for host read-back following power cycle back to ACTIVE mode.

10.2.1.4 Clock Input

GPIO_1 supports the connection of an external oscillator delivering the target 6 MHz, see Table 6, to the system. This requires that GPIO_1 is selected for external clock input (Ext_Clk_Inp) via GPIO_1_PIN. The GPI does not generate any event in this case.

The switch over from the internal to external clock occurs on the falling edge of the clock. If the external clock is not present, a clock detect switches control to the internal clock. In this case, I²C communication is possible.

⚠ CAUTION
Removing an external clock without first reverting the internal clocking GPI setting may damage the device.

10.2.1.5 Output Ports

Output ports (GPOs) are supplied from the internal rail (VCORE or VDDIO) and can be configured to be open drain or push-pull (selected via GPIO_1_MODE or GPIO_0_MODE). If a GPO is used as a push-pull driver VDDIO has to be enabled. GPOs can also be supplied from an external rail by disabling the internal 20 kΩ pull-up resistor in open-drain mode.

If the output ports are defined as general purpose outputs (GPOs), the low/high level is defined in register bits GPIO_1_TYPE or GPIO_0_TYPE. If the output ports are associated to power good (PG), defined by GPIO_1_PIN and GPIO_0_PIN, the GPIO_1_TYPE or GPIO_0_TYPE fields indicates the active low/high characteristics.

NOTE
In master/slave mode, with GPIO_1 operating in open drain with an external pull-up, the pull-up resistor must be > 820 kΩ to prevent a false SLAVE_ID recognition.

10.2.1.6 Power Good Indication

Power good (PG) voltage monitoring at the PVC output can be enabled. The PG function monitors the VOUT rail and informs the host processor about a power cycle in advance of the power cycle occurring. PG indication is selected via GPIO_1_PIN or GPIO_0_PIN .

The voltage monitoring threshold can be configured between 2.5 V and 5 V in 100 mV steps via PVC_PG_ADJ. When the voltage drops below the VTH_PG_PVC threshold, the event E_PVC_PG is generated and the PG pin is de-asserted. Active level is configurable via GPIO_0_TYPE.

After an under voltage condition has been triggered, the indicator will return back to PG after the output voltage has recovered above VTH_PG_PVC + VHYS_PG_PVC, see Table 5.

When a power cycle is initiated the PG will be always be de-asserted for 10 µs in advance of the power cycle occurring before exiting ACTIVE or SLEEP mode.

10.2.1.7 nIRQ

GPIO_0 and GPIO_1 both support an nIRQ function that indicates that an interrupt causing event has occurred. The related event and status information, such as warnings about temperature and voltages, over-current fault conditions or status changes at GPI ports, is available in the EVENT and STATUS registers.

The nIRQ output is enabled via GPIO_1_PIN or GPIO_0_PIN.

nIRQ can be push-pull or open drain, selected via GPIO_1_TYPE or GPIO_0_TYPE, and can be active LOW or active HIGH.

The EVENT registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set the nIRQ signal is asserted, unless this interrupt is masked by the appropriate in MASK register.

The masked bits only mask the nIRQ assertion, and do not suppress the event generation. The nIRQ is not released until all event bits are cleared by writing a 1 to the appropriate EVENT register bits. New events which have occurred during the reading of the EVENT register are held until the register has been cleared; ensuring that host processor does not miss them.

10.2.2 nONKEY

The nONKEY pin can be configured via the NONKEY_MODE register. It can operate as a user power button or as a level sensitive IC_EN pin, which allows the DA9313 state to be controlled from the GPO of another device.

The nONKEY input port is always enabled to ensure that activities which should generate an application wake-up or power down are always captured. The level of the debounced signal is provided by the status flag nONKEY.

NOTE
The nONKEY port should be never externally overdriven to a voltage higher than VCORE.

10.2.2.1 Event Generation

In ACTIVE or SLEEP modes a press of nONKEY causes an IRQ assertion if not suppressed via the interrupt mask M_nONKEY.

The event can be generated from either the rising or the falling edge of the nONKEY pin via NONKEY_PIN setting:

0: An E_nONKEY event is generated when the debounced signal from port nONKEY goes low (asserting edge). If not masked, an interrupt is signaled to the host via nIRQ.

1: An E_nONKEY event is generated when the debounced signal from port nONKEY goes high (de asserting edge). If not masked, an interrupt is signaled to the host via nIRQ.

10.2.2.2 Press Detection

Host notification of button presses via a maskable interrupt is available from the STATUS register, field nONKEY. A configurable long press can be used to trigger a power cycle of the device as a blue-screen lock up escape.

10.2.2.3 Wake Up

When DA9313 is in POWER_DOWN mode a user press of the nONKEY, for longer than the configured debounce setting in NONKEY_DEBOUNCE, triggers a transition to ACTIVE mode.

NOTE
Subsequent de-asserting edges of the nONKEY following a wake-up from POWER_DOWN require a release of the external button and new assertion to generate subsequent events.

10.2.2.4 Long Press

When DA9313 is in ACTIVE mode, a user press of the nONKEY, for longer than the configured debounce setting in NONKEY_DEBOUNCE plus the KEY_DELAY and SHUT_DELAY settings, triggers a power cycle which results in the device entering ACTIVE or POWER_DOWN mode (depending on the settings in NONKEY_CYCLE). If a long press of nONKEY has been detected, DA9313 will power cycle in 1 s unless this bit is cleared by the host, see E_KEY_RESET.

10.2.2.5 External IC Enable

The operation of the pin as an external IC enable (IC_EN) is configured in OTP via NONKEY_MODE. In this mode, the pin must be driven externally to VCORE or pulled to ground. The level of the nONKEY port controls transitions between ACTIVE (IC_EN high) and POWER_DOWN (IC_EN low).

During cold boot it is the responsibility of the host processor and the external application to make sure that the level of IC_EN is correct. The port should be active high in this case, level sensitive and without the pull-up to VCORE. There should be external resistors, in the 100 kΩ range, defining the correct level when the port is not actively driven.

The FAULT_TIME system controller state is bypassed when moving from ACTIVE to POWER_DOWN due to IC_EN de assertion but is still enabled for fault handling.

NOTE
When NONKEY is set as IC_EN, SLEEP mode has a restricted usage. System behavior is only guaranteed if SLEEP mode is entered / exited via I^2C/GPI while IC_EN is high, using SL_nONKEY_CONT as SLEEP mode exit is invalid as this will bring chip to POWER_DOWN on the de-asserting edge of IC_EN

10.3 Power Voltage Converter

The high efficiency 2S to 1S power voltage converter (PVC) is capable of supplying multiple 1S voltage rails with up to 10 A output current. The dual phase interleaved operation ensures an almost constant input current, thereby highly improving the application design against noise.

10.3.1 PVC Output Voltage

The PVC can be configured via OTP or I^2C and outputs a non-regulated voltage which is nominally half of the input voltage, in the case where no load is applied. When a current (I_{OUT}) is drawn at the V_{OUT} node and the PVC is switching at frequency of f_{SW_PVC}, the output voltage is determined as:

$$V_{OUT} = \frac{V_{IN}}{2} - R_{EQ} \cdot I_{OUT}$$

Where:

- R_{EQ} is a function of the sum of all resistances in the input/output power path (including the power device's on-resistance and the PCB routing resistance) as well as the switching frequency, C_{FLY} and PCB parasitics.
- R_S is the sum of all resistances in the input/output power path (including the power devices on-resistance and the PCB routing resistance).
- The switching frequency of the PVC, f_{SW_PVC} = 500 kHz. This has been pre-selected for optimized and efficient operation.

The voltage ripple at V_{OUT} can be first order approximated as the voltage drop due to the discharge of the C_{FLY} capacitor in half of the period at an f_{SW_PVC} switching frequency, plus the discharge voltage of the output V_{OUT} capacitor during a typical 30 ns short dead time for phase switch. In addition, the PVC provides an optional hardware enable/disable via selectable GPI, configured via the PVC_EN register field, see section 10.2.1.1.

10.3.2 PVC Start-Up

The PVC can be OTP configured to enable on entry to ACTIVE mode and to run in automatic (mixed DCM and CCM based on load sensing) or in fixed frequency (CCM). Alternatively the PVC can be set to CCM in ACTIVE mode and to run in automatic in SLEEP mode. See section 10.3.3.

During PVC start-up, the PVC does not switch and the flying capacitors C_{FLY} are connected in parallel to the output capacitor C_{LOAD}. An internal current source charges the capacitors up to a voltage value close to the target average in normal operation. The internal current source can be configured from 500 mA to 2 A via I_STUP_PVC.

At the end of the start-up phase the normal switching operation of the PVC is restored.

NOTE

A start-up phase with an output load greater than I_STUP_PVC will not be successful. The PVC has a ramp-up timer which checks the ramp-up happens in approx. 20 ms. If the output voltage has not reached a value close to $V_{DD}/2$ at this time this indicates a failure condition and the regular switching is not started. This is reported as PVC_RAMPUP in FAULT_LOG.

CAUTION

To avoid damage to the device, the PVC output must reach $V_{DD}/2$ – 80 mV before a load greater than half of I_STUP_PVC can be applied to its output.

10.3.3 PVC Operating Modes

10.3.3.1 Standalone Mode

When the PVC is enabled, the operating mode is defined by the PVC_MODE register field. The PVC operates either in fixed frequency (PVC_MODE= 0) or in automatic frequency mode (PVC_MODE= 1).

In automatic frequency mode, the switching frequency is not always constant, see Figure 13. The PVC operates in continuous conduction mode (CCM) at high loads and moves to discontinuous conduction mode (DCM) as soon as the load becomes lower than a certain threshold.

- When the load decreases, the V_{OUT} voltage increases over the V_{PVC_DROP} threshold and the PVC moves from CCM to DCM.
- When the load increases again and the V_{OUT} voltage decreases by V_{PVC_HYST} below V_{PVC_DROP} and the PVC moves back from DCM to CCM.

Operating in automatic frequency mode extends the efficiency range to low levels of output loads, enabling the PVC to supply a low voltage PMIC in low power mode over a long period.

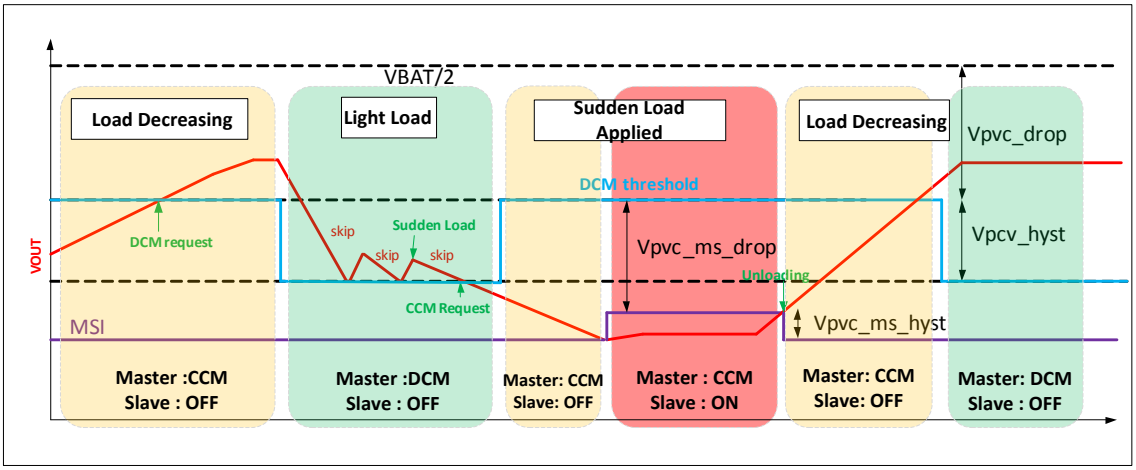


Figure 13: Master Slave Timing in Automatic Frequency Mode

10.3.3.2 Master/Slave Operation

The master device behaves in the same way as a standalone device, see section 10.3.3.1, with additional V_{OUT} monitoring at V_{MSI} level (see Note below). This monitoring is used to trigger the slave device via the master/slave interface (MS_IF). The level at which the master triggers the slave is defined in PVC_MS_DROP.

When the V_{OUT} voltage decreases beyond V_{MSI} due to progressive output loading, the master DA9313 enables the slave DA9313 over MS_IF.

When the V_{OUT} voltage increases above V_{MSI} + $V_{PVC\_MS\_HYST}$ (defined in PVC_MS_HYST), the master DA9313 disables the slave DA9313 over MS_IF.

Disabling the master PVC triggers a shutdown of the slave PVC over MS_IF.

NOTE
$V_{MSI} = V_{CCM} – V_{PVC\_MS\_DROP}$ Where: • $V_{CCM} = (V_{BAT}/2 - V_{PVC\_DROP} - V_{PVC\_HYSTMAX})$ • $V_{PVC\_HYSTMAX}$ is a constant value of 30 mV

10.3.4 PVC Power Down

During PVC power down, the PVC does not switch and the flying capacitors C_{FLY} are connected in parallel to the output capacitor C_{LOAD}. An internal pull-down is used to ensure the PVC is in a defined start condition. When the output voltage drops below the threshold of 1 V, the PVC can accept a re-start.

In master/slave configuration, power down is synchronized by the master/slave interface (MS_IF) in a way where both devices connect the flying capacitors (C_{FLY}) in parallel to the output capacitor (C_{LOAD}) at the same time. These capacitors are discharged by the master.

10.3.5 PVC Current Limit

The configurable integrated current limit is aimed to protect DA9313's power stages and the external components from excessive current.

When hitting the current limit I_{LIM_PVC} (configured in PVC_ILIM) DA9313 enters FAULT RECOVERY.

DA9313 provides an indication that the system current is approaching the critical limit, before hitting the current limit itself, allowing an active host processor to take some countermeasures.

When the warning threshold I_{ALARM} is reached the event E_PVC_OC_WARN is generated. The status of the over-current alarm comparator can be read back on FAULT_LOG via the I^2C control interface.

11 Operating Modes

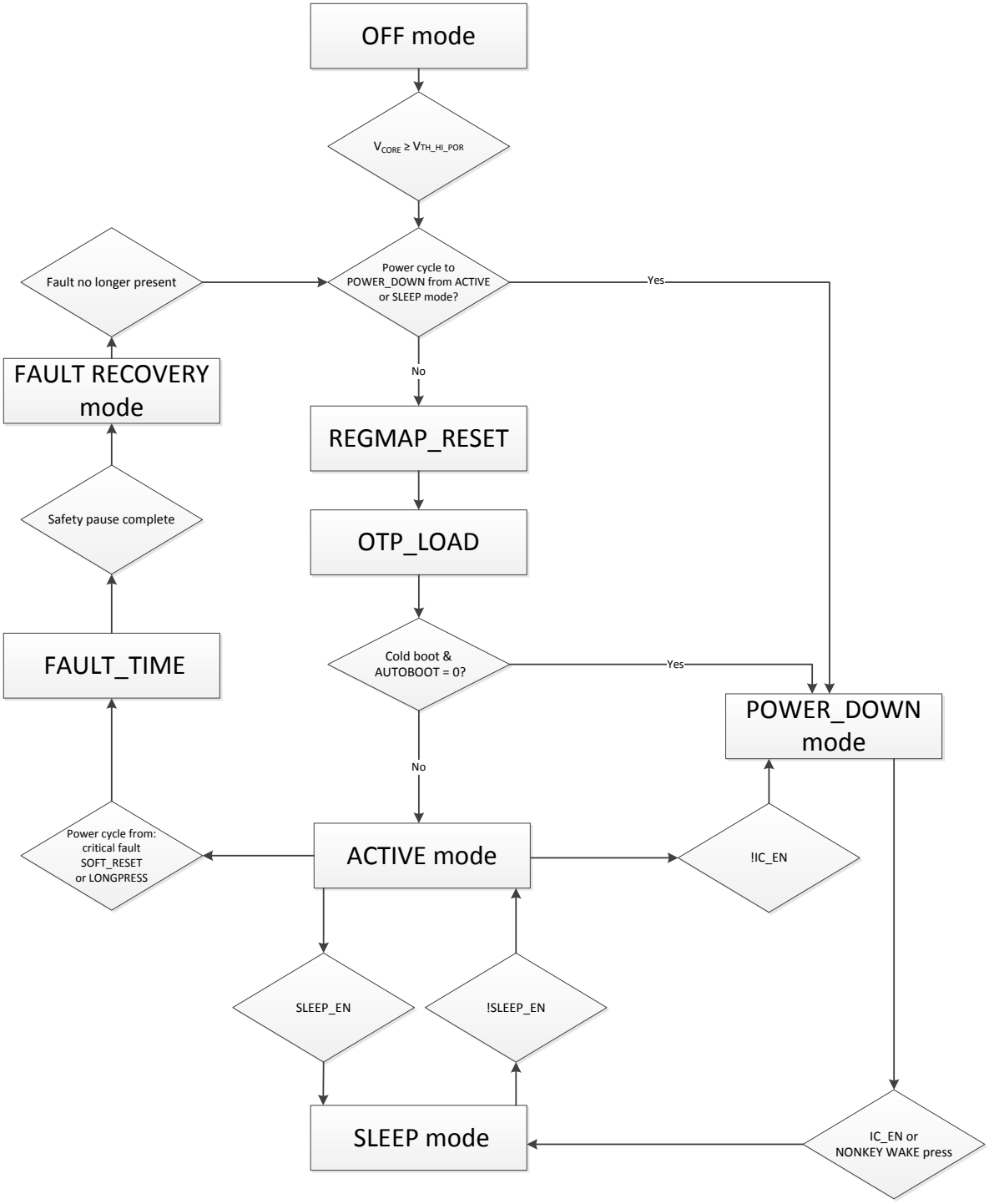


Figure 14: Operating Modes

11.1 OFF Mode (HARDRESET)

DA9313 is in OFF mode without being supplied or with a low supply, when $V_{O\_VCORE} \leq V_{TH\_LO\_POR}$. The only circuitry enabled is the VCORE regulator and its voltage supervision. The digital core is kept reset in OFF mode.

When $V_{O\_VCORE} \geq V_{TH\_HI\_POR}$ DA9313 transitions from OFF mode to ACTIVE mode or to POWER_DOWN mode, depending on the AUTOBOOT setting.

11.2 POWER_DOWN Mode

The POWER_DOWN mode is the lowest quiescent current operating mode with a valid input voltage. It can support a shelf mode for applications with integrated battery packs, which allows connecting pre-charged batteries before the user enables the device for the first time.

PVC, oscillator, and analog references are disabled, only the nONKEY sense circuit is left running on VCORE. A nONKEY wake press will transition the system to ACTIVE, see section 10.2.2.3.

11.3 ACTIVE Mode

ACTIVE mode is the main operating mode of DA9313 and is entered into after OTP load. The PVC is then automatically turned on and operates in the configured mode.

NOTE
The host processor should wait for DA9313 to reach the ACTIVE mode following a start-up from OFF or POWER_DOWN before starting the I^{2}C communication with DA9313, see Table 5 for timing details.

After the application starts up, the host processor should always read the FAULT_LOG register to determine which one of the following sequences occurred before ACTIVE mode was enabled:

- from a fault condition (dedicated fault bit)
- from OFF during cold boot (POR bit)
- from power cycle due to long press of nONKEY
- from power cycle initiated via SOFTRESET write
- from power cycle initiated by PWC

11.4 SLEEP Mode

SLEEP mode is used to support application low power modes with lower quiescent current. The mode can be entered into and exited from by register write or via GPI. An optional exit via nONKEY is also supported when VDDIO has been disabled in SLEEP mode.

SLEEP mode is configurable via the SLEEP_CTRL register, see Table 13 for configuration options.

- To enter SLEEP mode via I^{2}C, assert the SLEEP bit in the MODE_CTRL register.
- To enter SLEEP mode via GPI, configure GPIO_1_PIN or GPIO_0_PIN to SLEEP_EN. The level of the GPI controls entry into SLEEP mode and exit back to ACTIVE mode.

ACTIVE configuration settings are re-applied on exit of SLEEP mode.

Table 13: SLEEP_CTRL Register Configuration

Control bit	Block
PVC_SL	PVC operation in SLEEP mode: 0: no change 1: automatic frequency mode The PVC is changed to automatic frequency mode (variable frequency). PVC_MODE setting is overwritten (old value restored at the exit of SLEEP mode)

Control bit	Block
PVC_DIS_SL	PVC enable control, in SLEEP mode: 0: no change 1: PVC disabled The PVC is disabled PVC_EN setting is overwritten (old value restored at the exit of SLEEP mode)
VDDIO_DIS_SL	Control VDDIO supply enable, in SLEEP mode: 0: no change 1: VDDIO rail disabled. IOs supplied from VCORE

11.5 FAULT RECOVERY Mode

DA9313 responds to critical under-voltage, over-current, and over-temperature conditions and safely power cycles the device through FAULT RECOVERY mode. Fault events are captured in the FAULT_LOG register for host interrogation on reboot and warning levels generate maskable interrupt events.

FAULT RECOVERY is a temporary mode and is automatically entered and exited depending on fault condition presence. DA9313 enters FAULT RECOVERY mode from ACTIVE or SLEEP mode. In POWER_DOWN mode there is no supervision therefore FAULT RECOVERY mode cannot be entered.

The device waits for a configurable FAULT_TIME, when the PVC is disabled, to ensure discharge of all critical nodes in the application before any attempt to reboot. DA9313 automatically exits FAULT RECOVERY mode when the fault condition has expired.

The FAULT_LOG register can be reset by a register write of 1 to the appropriate register bit.

11.5.1 Input Under-Voltage

V_{BAT} voltage is continuously sensed, except in RESET and POWER_DOWN modes, by dedicated analog circuitry based on two configurable levels: a warning level, V_{TH_WARN} and a shutdown level, $V_{TH\_UVLO\_VDD}$.

The upper comparator triggers a warning if V_{BAT} drops below V_{TH_WARN}. The lower comparator triggers a fault condition if V_{BAT} drops below $V_{TH\_UVLO\_VDD}$.

The $V_{TH\_UVLO\_VDD}$ voltage threshold is configurable and can be set via VBAT_UV_CRIT_THRSH from 4.6 V to 6.15 V (5.0 V default) in steps of 50 mV.

The $V_{HYST\_UVLO\_VDD}$ hysteresis can be also be configured via VBAT_UV_HYS from 50 mV to 400 mV (200 mV default) in steps of 50 mV.

The V_{TH_WARN} voltage threshold is configurable and can be set via VBAT_UV_WARN from 5.2 V to 6.6 V in steps of 200 mV.

To reduce the current consumption of the block only the warning comparator is permanently on, the shutdown comparator is enabled on demand in the interval where V_{BAT} is below the warning threshold.

The critical under voltage threshold comparator is also debounced, this guarantees that short spikes do not trigger the application power-down.

When the warning comparator triggers, the status bit VBAT_WARN is asserted and the event E_VBAT_WARN is generated. If not masked via M_VBAT_WARN, the output port nIRQ is asserted (providing a GPIO is configured as nIRQ). The host processor is then informed that the input voltage level is close to critical and it can take action such as powering down the application.

If the input voltage keeps dropping and the shutdown comparator is triggered the PVC is disabled and the VBAT_UV_CRIT bit is asserted in FAULT_LOG. When the V_{BAT} voltage recovers over $V_{TH\_UVLO\_VDD} + V_{HYST\_UVLO\_VDD}$, DA9313 enters ACTIVE mode after having performed an OTP read.

11.5.2 Over-Temperature

FAULT RECOVERY mode is entered when $T_J \geq T_{TH\_CRIT}$ and is exited when $T_J < T_{TH\_CRIT}$. The TEMP_CRIT bit is asserted in FAULT_LOG.

11.5.3 PVC Current Limit

When the PVC hits the current limit, FAULT RECOVERY mode is entered and is immediately exited, because the root cause (current limit reached) is removed when the PVC is disabled. The PVC_OC_CRIT bit is asserted in FAULT_LOG.

11.5.4 PVC Start-Up Failure

FAULT RECOVERY mode is entered when the PVC has failed its start-up procedure. This occurs when the output voltage has not reached a voltage close to VDD/2 within approximately 20 ms. FAULT RECOVERY mode is immediately exited and a new power up is started. The PVC_RAMPUP bit is asserted in FAULT_LOG.

11.6 VCORE Voltage Regulator

The VCORE supply is a 4 V rail internally generated by DA9313 for the internal analog and digital supply. It is always enabled except in OFF mode.

The additional VDDIO rail is internally generated directly from VCORE. The slave has VDDIO disabled.

VCORE is the only regulator with an external bypass capacitor and can supply up to 20 mA to an external circuit.

11.7 VDDIO Generation

The VDDIO rail is internally generated by DA9313 from VCORE and is assigned to the I/O interfaces and to the GPIOs. The VDDIO is controlled via VDDIO_EN bit. The rail assignment determines the IO voltage levels and logical thresholds see section 7.5. A specific VDDIO voltage can be selected via VDDIO_CONF (1.5 V, 1.8 V, 2.8 V, or 3.3 V).

The VDDIO generation is off in OFF and POWER_DOWN modes, and always in the slave device. In SLEEP mode the VDDIO generation is disabled if VDDIO_SL is asserted.

The internally generated VDDIO is monitored for under voltage VTH_UVLO_IO. If VDDIO voltage is not in range, the I^2C interface is reset. All IOs are run from VCORE if VDDIO is disabled. All IOs are supplied on VCORE only when in master/slave mode (it is not possible to enable VDDIO in these modes).

11.8 Internal Oscillator

The internal high-speed oscillator generates a signal at f_{OSC}, the internal 6 MHz clock reference. The high-speed oscillator is enabled on demand.

It is possible to apply an external oscillator delivering the target 6 MHz, see Table 6, to the system. This requires that GPIO_1 is selected as Ext_Clk_Inp on GPIO_1_PIN. GPIO_1 does not generate any event in this case.

11.8.1 Internal Temperature Supervision

Due to the high power density and to protect DA9313 from damage due to excessive power dissipation the internal temperature is continuously monitored, except in DCM, OFF and POWER_DOWN modes.

There are two temperature thresholds, T_{TH_WARN} and T_{TH_CRIT}, respectively at typically 125 °C and 140 °C. To minimize the current consumption only the T_{TH_WARN} comparator is always on. The T_{TH_CRIT} comparators are enabled on demand at >125 °C when T_{TH_WARN} is reached.

When the junction temperature reaches the T_{TH_WARN} threshold, DA9313 will assert the bit TEMP_WARN and will generate the event E_TEMP_WARN. The status bit TEMP_WARN will remain asserted as long as the junction temperature is higher than T_{TH_WARN}.

When the junction temperature increases further over T_{TH_CRIT} DA9313 will immediately disable the PVC, will assert the status bit TEMP_CRIT and will progress to FAULT RECOVERY mode, see section 11.5.

The status bit TEMP_CRIT will remain asserted as long as the junction temperature is higher than T_{TH_CRIT}. DA9313 will remain in FAULT RECOVERY mode as long as the junction temperature is bigger than T_{TH_CRIT} and will not allow re-enabling of the supplies via I^2C port or register write.

Where the I^2C interface is not connected, providing DA9313 has been configured to boot to ACTIVE mode via AUTOBOOT, the PVC will shut down (power cycle) then restart and PG on GPIO will go down and then up again.

12 Control Interface

I²C is always enabled in ACTIVE/SLEEP and IOs run on either VDDIO or VCORE, see section 11.7.

DA9313 can be software controlled through an I²C serial control interface. Data are shifted into or out of DA9313 under the control of the host processor that also provides the serial clock. In a normal application case the interface is only configured once from OTP values, which are loaded during the initial start-up of DA9313. In this phase the I²C address is loaded from OTP.

The LOCK_REG register provides a software-controlled write protection (soft lock) of selected registers from 0xE0 to 0x2F, the registers remain readable. This feature prevents malicious or accidental writes to these critical registers from damaging the device. This soft lock is intended for control by the system driver during device configuration on power up.

NOTE
The soft lock will reassert during all power cycles.

12.1 I²C Communication

DA9313 has an OTP configurable device write address (default: 0xD0) and an OTP configurable device read address (default: 0xD1). The 4 MSB of the I²C device address can be OTP configured in the register field IF_BASE_ADDR1.

The SCL port functions as the I²C clock and the SDA port carries the bi-directional I²C data.

NOTE
SDA and SCL must be connected to GND if I²C is not being used. The slave SDA and SCL must always be connected to GND.

The I²C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ range). The devices connected to the I²C SDA can only drive the bus line low to ground. As a result two devices cannot conflict if they drive the bus simultaneously. In Standard/Fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9313 internal clock signals. DA9313 does not initiate any clock arbitration or slow down the clock. An automatic I²C reset can be triggered via control I2C_TO_EN if the clock signal stays low for more than 35 ms.

The interface supports an operation compatible to Standard, Fast, Fast-Plus and High Speed mode of the I²C-bus specification Rev 4 [1]. The operation in High Speed mode at 3.4 MHz requires mode changing in order to switch spike suppression and slope control characteristics compatible to the I²C-bus specification. The High Speed mode can be enabled on a transfer by transfer basis by sending the master code (0000 1XXX) at the begin of the transfer.DA9313 does not make use of clock stretching and delivers read data, without additional delay, up to 3.4 MHz.

Alternatively the interface can be configured to continuously use High Speed mode via PM_IF_HSM (OTP configurable), so that the master code is not required at the beginning of every transfer. This reduces the communication overhead on the bus but limits the attachable slaves to the bus to compatible devices.

The communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. The DA9313 will only operate as a slave.

The master or standalone device has stored the device address in register IF_BASE_ADDR1.

NOTE
When DA9313 is operating in master/slave mode, the I²C bus is referenced to 4 V.

12.2 I²C Control Bus Protocol

Data are transmitted over the I²C bus in groups of 8 bits. To send a bit the SDA line is driven to the intended state while the SCL is low (for example, a low on SDA indicates a zero bit). Once the SDA

has settled the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receivers shift register.

DA9313 uses a two byte serial protocol which contains one byte for the address and one byte for data. Data and address transfer is based on the MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master as long as the bus is in IDLE state (the bus is free). The START condition is defined as a high to low transition at the SDA line while the SCL is high. The STOP condition is defined as a low to high transition at the SDA line while the SCL is high.

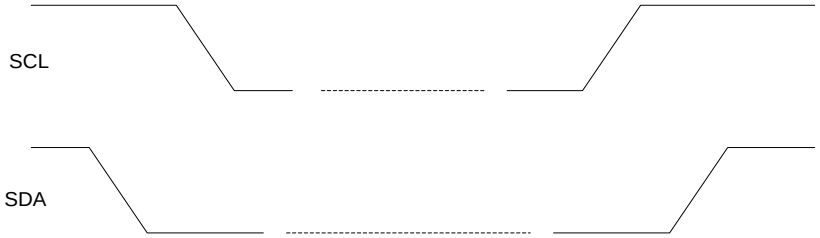


Figure 15: Timing of I²C START and STOP Condition

The I²C bus will be monitored by DA9313 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. This acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 16 to Figure 20).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded to by DA9313 with Acknowledge):

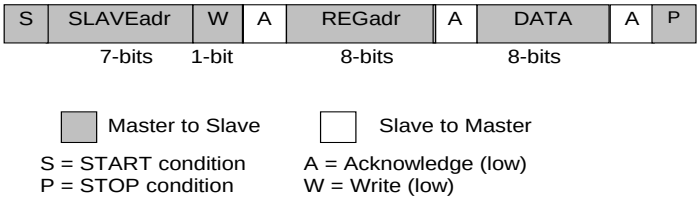


Figure 16: I²C Byte Write (SDA Line)

When the host reads data from a register it first has to write access DA9313 with the target register address and then read access DA9313 with a Repeated START or alternatively a second START condition. After receiving the data the host sends No Acknowledge and terminates the transmission with a STOP condition:

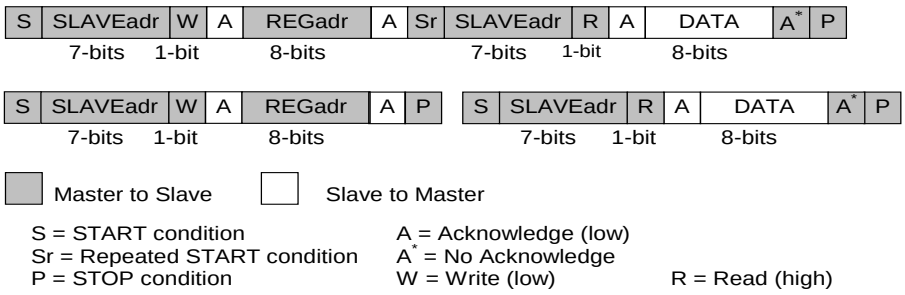


Figure 17: I²C Byte Read (SDA Line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of No Acknowledge after receipt of the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a No Acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent I²C address is read out then the DA9313 will return code zero:

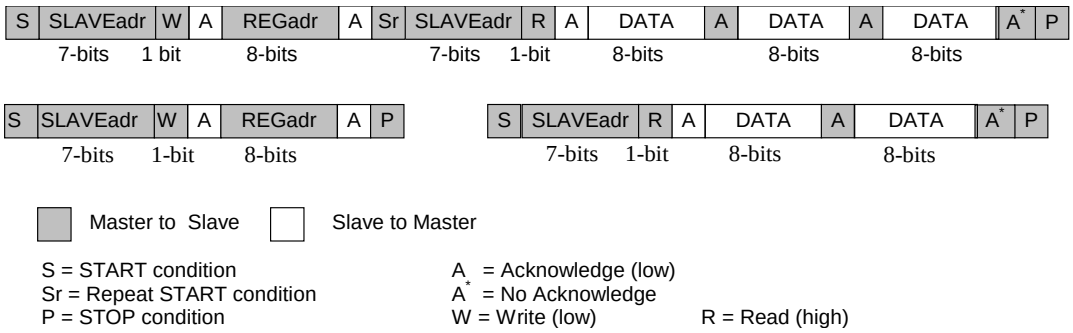


Figure 18: I²C Page Read (SDA Line)

NOTE
The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The I²C control block then increments the address pointer to the next I²C address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

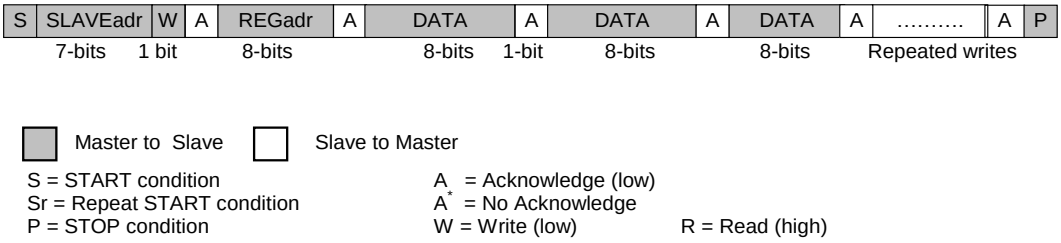


Figure 19: I²C Page Write (SDA Line)

An alternative write mode, alternating register address and data, can be configured via register bit WRITE_MODE. Register addresses and data are sent alternately, see Figure 20, to support host repeated write operations that access several non-consecutive registers. Data will be stored at the previously received register address.

An update of WRITE_MODE cannot be done without interruption within a transmission frame. Thus, if not previously selected or not set as OTP default, the activation of Repeated Write must be done with a regular write on WRITE_MODE followed by a STOP condition. The next frame after a START condition can be written in Repeated Write

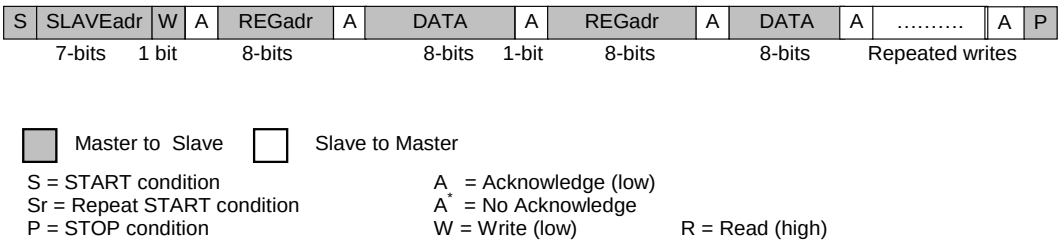


Figure 20: I²C Repeated Write (SDA Line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

13 Register Definitions

Table 14: Register Map

Address #	Name	7	6	5	4	3	2	1	0
Register Page 0									
0x01	VENDORID	VENDORID							
0x02	MODE_CTRL	Reserved	AUTOBOOT	RESET_CYCLE	nONKEY_CYCLE	MSTSLV_IF_EN	NONKEY_MODE	SOFTRESET	SLEEP
0x03	SLEEP_CTRL	Reserved				SL_nONKEY_CONT	PVC_DIS_SL	PVC_SL	VDDIO_DIS_SL
0x04	PVC_CTRL	Reserved						PVC_MODE	PVC_EN
0x05	GPIO_CTRL	Reserved	GPIO_1_PIN			Reserved	GPIO_0_PIN		
0x06	GPIO_CTRL_2	GPIO_1_PD	GPIO_1_PU	GPIO_1_MODE	GPIO_1_TYPE	GPIO_0_PD	GPIO_0_PU	GPIO_0_MODE	GPIO_0_TYPE
0x07	INTERFACE_CTRL	WRITE_MODE	PM_IF_HSM	PC_DONE	I2C_TO_EN	GPIO_0_DEGLITCH	GPI_DEBOUNCE		
0x08	NONKEY_CTRL	SHUT_DELAY		KEY_DELAY		NONKEY_PIN	NONKEY_DEBOUNCE		
0x09	MASK	Reserved	M_TEMP_WARN	M_VBAT_WARN	M_nONKEY	M_PVC_OC_WARN	M_PVC_PG	M_GPI_1	M_GPI_0
0x0A	STATUS	PVC_OC_WARN	TEMP_WARN	VBAT_WARN	Reserved	nONKEY	PVC_PG	GPI_1	GPI_0
0x0B	EVENT	E_KEY_RESET	E_TEMP_WARN	E_VBAT_WARN	E_nONKEY	E_PVC_OC_WARN	E_PVC_PG	E_GPI_1	E_GPI_0
0x0C	FAULT_LOG	PVC_RAMPUP	PD_RESET	GPI_RESET	NONKEY_RESET	VBAT_UV_CRIT	PVC_OC_CRIT	TEMP_CRIT	POR
0x0D	LOCK_REG	LOCK_REG							
0x0E	PVC_CONFIG_1	PVC_DROP		PVC_HYST		PVC_MS_DROP		PVC_MS_HYST	
0x0F	PVC_CONFIG_2	PVC_SLV_IF_PHASE		Reserved		PVC_ILIM			
0x10	PVC_CONFIG_3	PVC_PG_DIS	PVC_PG_ADJ					I_STUP_PVC	
0x11	CONFIG_A	VBAT_UV_HYS			VBAT_UV_CRIT_THRSH				
0x13	CONFIG_C	VDDIO_EN	FAULT_TIME		VDDIO_CONF		VBAT_UV_WARN		
0x14	CONFIG_D	Reserved				IF_BASE_ADDR1			
0x30	VARIANT_ID	MRC				VRC			
0x31	DEVICE_ID	DEVICE_ID							
0x32	CUSTOMER_ID	CUSTOMER_ID							
0x33	CONFIG_ID	CONFIG_REV							

Table 15: VENDORID 0x01

Bit	Mode	Symbol	Description	Reset
7:0	R/W	VENDORID	Specific vendor ID.	0x0

Table 16: MODE_CTRL 0x02

Bit	Mode	Symbol	Description	Reset
7	R/W	-	Reserved	0x0
6	R/W	AUTOBOOT	0: The cold boot from OFF stops in POWER_DOWN mode. An nONKEY press is needed to move to ACTIVE 1: The cold boot from OFF ends in ACTIVE	0x1
5	R/W	RESET_CYCLE	0: A power cycle initiated by SOFTRESET stops in POWER_DOWN mode. An nONKEY press is needed to move to ACTIVE 1: A power cycle initiated by SOFTRESET ends in ACTIVE	0x1
4	R/W	nONKEY_CYCLE	0: A power cycle initiated by long nONKEY press stops in POWER_DOWN mode. An nONKEY press is needed to move to ACTIVE 1: A power cycle initiated by long nONKEY press ends in ACTIVE	0x1
3	R/W	MSTSLV_IF_EN	0: Standalone; GPIO_0 as per GPIO_0_PIN configuration 1: GPIO_0 is dedicated master/slave interface; GPIO_0_PIN has no effect (Pad Deglitch settings as per GPIO_0_DEGLITCH) GPI0_0 == MstSlv_IF INPUT // Slave Chip else GPI0_0 == MstSlv_IF OUTPUT // Master chip or standalone	0x0
2	R/W	NONKEY_MODE	0: nONKEY button MODE (pin operates as edge sensitive, active low, user button) 1: nONKEY IC_EN MODE (operates as level driven IC enable, where nONKEY = VCORE puts chip in ACTIVE state, nONKEY = 0 V puts chip into POWER_DOWN state.	0x0
1	R/W	SOFTRESET	When asserted, triggers a power cycle and a reset of all internal registers, followed by an OTP read	0x0
0	R/W	SLEEP	Target and status of SLEEP Mode Controlled from OTP, I^2C interface or from GPI if configured via GPIO_X_PIN	0x0

Table 17: SLEEP_CTRL 0x03

Bit	Mode	Symbol	Description	Reset
7:4	R/W	-	Reserved	0x0
3	R/W	SL_nONKEY_CONT	Configuration of the exit from SLEEP Mode via nONKEY press 0: nONKEY press does not cause DA9313 to exit SLEEP Mode 1: nONKEY press causes DA9313 to exit SLEEP Mode	0x0
2	R/W	PVC_DIS_SL	PVC enable control in SLEEP Mode: 0: no change 1: PVC disabled	0x0

Bit	Mode	Symbol	Description	Reset
1	R/W	PVC_SL	PVC operation in SLEEP Mode: 0: no change 1: automatic mode	0x0
0	R/W	VDDIO_DIS_SL	Control VDDIO LDO enable in SLEEP Mode: 0: no change 1: VDDIO LDO disabled	0x0

Table 18: PVC_CTRL 0x04

Bit	Mode	Symbol	Description	Reset
7:2	R/W	-	Reserved	0x0
1	R/W	PVC_MODE	0: PVC operates in fixed frequency mode 1: PVC operates in automatic frequency mode (variable frequency)	0x1
0	R/W	PVC_EN	Current PVC ACTIVE configuration target and status, set via OTP load, controllable via I^2C or GPI via GPIO_X_PIN 0: PVC disabled 1: PVC enabled	0x0

Table 19: GPIO_CTRL 0x05

Bit	Mode	Symbol	Description	Reset
7	R/W	-	Reserved	0x0
6:4	R/W	GPIO_1_PIN	GPIO_1 PIN assigned to: 000: GPI 001: PVC_EN (Readback available in PVC_EN register field) 010: SLEEP_EN (Readback available in SLEEP register field) 011: Power Cycle 100: GPO 101: Power Good 110: IRQ 111: Digital clock input Note: GPIO_0 has priority over GPIO_1 for matching input function selections	0x0
3	R/W	-	Reserved	0x0

Bit	Mode	Symbol	Description	Reset
2:0	R/W	GPIO_0_PIN	GPIO_0 PIN assigned to: 000: GPI 001: PVC_EN (read-back available in PVC_EN register) 010: SLEEP_EN (read-back available in SLEEP register) 011: Power Cycle 100: GPO 101: Power Good 110: IRQ 111: N/A Note: GPIO_0 has priority over GPIO_1 for matching input function selections Note: Configuration of this register is ignored if MSTSLV_IF_EN is set	0x0

Table 20: GPIO_CTRL_2 0x06

Bit	Mode	Symbol	Description	Reset
7	R/W	GPIO_1_PD	0: GPI: pull-down resistor disabled No impact if defined as output port 1: GPI: pull-down resistor enabled No impact if defined as output port	0x1
6	R/W	GPIO_1_PU	0: GPI: pull-up resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-up resistor enabled GPO (open drain): pull-up resistor	0x0
5	R/W	GPIO_1_MODE	0: GPI: debouncing off GPO: open drain 1: GPI: debouncing on GPO: push-pull	0x1
4	R/W	GPIO_1_TYPE	0: GPI/PG/IRQ: active low GPO: low level 1: GPI/PG/IRQ: active high GPO: high level	0x1
3	R/W	GPIO_0_PD	0: GPI: pull-down resistor disabled No impact if defined as output port 1: GPI: pull-down resistor enabled No impact if defined as output port	0x1
2	R/W	GPIO_0_PU	0: GPI: pull-up resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-up resistor enabled GPO (open drain): pull-up resistor	0x0
1	R/W	GPIO_0_MODE	0: GPI: debouncing off GPO: open drain 1: GPI: debouncing on GPO: push-pull	0x1
0	R/W	GPIO_0_TYPE	0: GPI/PG/IRQ: active low GPO: low level 1: GPI/PG/IRQ: active high GPO: high level	0x1

Table 21: INTERFACE_CTRL 0x07

Bit	Mode	Symbol	Description	Reset
7	R/W	WRITE_MODE	I^2C write mode 0 = Page Write mode 1 = Repeated Write mode	0x0
6	R/W	PM_IF_HSM	Enables continuous High Speed mode on I^2C interface if asserted (no master code required)	0x0
5	R/W	PC_DONE	Asserted from Power Commander software after the emulated OTP read has finished, automatically cleared when leaving emulated OTP read	0x0
4	R/W	I2C_TO_EN	Enables automatic reset of I^2C interface when clock stays low for > 35 ms 0: Disabled 1: Enabled	0x1
3	R/W	GPIO_0_DEGLITCH	0: Pad Deglitching disabled 1: Pad rejects pulses < 50 ns in duration	0x0
2:0	R/W	GPI_DEBOUNCE	GPI signal debounce time: 000: no debounce 001: 0.125 ms 010: 1.0 ms 011: 10 ms (default) 100: 30 ms 101: 250 ms 110: 500 ms 111: 750 ms	0x3

Table 22: NONKEY_CTRL 0x08

Bit	Mode	Symbol	Description	Reset
7:6	R/W	SHUT_DELAY	Long press configuration at nONKEY for initiating a power cycle: 00: Long press function disabled 01: KEY_DELAY + 4 s 10: KEY_DELAY + 5 s 11: KEY_DELAY + 6 s	0x0
5:4	R/W	KEY_DELAY	KEY_DELAY threshold at nONKEY 00: 1 s 01: 1.5 s 10: 2 s 11: 7 s	0x2
3	R/W	NONKEY_PIN	0: An E_nONKEY event is generated when the debounced signal from port nONKEY goes low (asserting edge). If not masked, an interrupt is signaled to the host via nIRQ 1: An E_nONKEY event is generated when the debounced signal from port nONKEY goes high (de-asserting edge). If not masked, an interrupt is signaled to the host via nIRQ	0x0

Bit	Mode	Symbol	Description	Reset
2:0	R/W	NONKEY_DEBOUNCE	nONKEY signal debounce time: 000: no debounce 001: 0.125 ms 010: 1.0 ms 011: 10 ms 100: 30 ms 101: 250 ms 110: 500 ms 111: 750 ms	0x3

Table 23: MASK 0x09

Bit	Mode	Symbol	Description	Reset
7	R/W	-	Reserved	0x0
6	R/W	M_TEMP_WARN	Mask for thermal warning event TEMP_WARN	0x0
5	R/W	M_VBAT_WARN	Mask for under voltage warning event E_VBAT_WARN	0x0
4	R/W	M_nONKEY	Mask for nONKEY event E_nONKEY	0x0
3	R/W	M_PVC_OC_WARN	Mask for PVC current warning event E_PVC_OC_WARN	0x0
2	R/W	M_PVC_PG	Mask for power good loss at PVC event E_PVC_PG	0x0
1	R/W	M_GPI_1	Mask for GP1_1 event E_GPI_1	0x0
0	R/W	M_GPI_0	Mask for GP1_0 event E_GPI_0	0x0

Table 24: STATUS 0x0A

Bit	Mode	Symbol	Description	Reset
7	R	PVC_OC_WARN	Asserted as long as the PVC current reached the alarm threshold	0x0
6	R	TEMP_WARN	Asserted as long as the thermal warning threshold is reached	0x0
5	R	VBAT_WARN	Asserted as long as the battery under voltage warning is reached	0x0
4	R/W		Reserved	0x0
3	R	nONKEY	Asserted as long nONKEY is pressed (low level)	0x0
2	R	PVC_PG	Asserted as long as the PVC output voltage is in range	0x0
1	R	GPI_1	GPI_1 Level	0x0
0	R	GPI_0	GPI_0 Level	0x0

Table 25: EVENT 0x0B

Bit	Mode	Symbol	Description	Reset
7	RW1C	E_KEY_RESET	A long press of nONKEY has been detected. DA9313 will power cycle in 1 s unless this bit is cleared by the host	0x0
6	RW1C	E_TEMP_WARN	TEMP_WARN caused an event	0x0
5	RW1C	E_VBAT_WARN	VBAT_WARN caused an event	0x0
4	RW1C	E_nONKEY	nONKEY caused an event	0x0
3	RW1C	E_PVC_OC_WARN	PVC current alarm caused an event.	0x0
2	RW1C	E_PVC_PG	Power good loss at PVC caused an event	0x0
1	RW1C	E_GPI_1	GPI_1 event according to active state setting	0x0
0	RW1C	E_GPI_0	GPI_0 event according to active state setting	0x0

Table 26: FAULT_LOG 0x0C

Bit	Mode	Symbol	Description	Reset
7	R/W	PVC_RAMPUP	PVC has failed to ramp output voltage on start-up. Critical fault.	0x0
6	R/W	PD_RESET	Power cycle initiated via SOFTRESET write	0x0
5	R/W	GPI_RESET	Power cycle initiated by PWC GPI reset	0x0
4	R/W	NONKEY_RESET	Power cycle due to long press of nONKEY	0x0
3	R/W	VBAT_UV_CRIT	Input under voltage triggered a fault condition	0x0
2	R/W	PVC_OC_CRIT	PVC over-current triggered a fault condition	0x0
1	R/W	TEMP_CRIT	Junction over-temperature triggered a fault condition	0x0
0	R/W	POR	Power up from OFF (cold boot)	0x0

Table 27: LOCK_REG 0x0D

Bit	Mode	Symbol	Description	Reset
7:0	R/W	LOCK_REG	Soft lock for registers from 0x0E to 0x2F Writing to registers in this region while the region is LOCKED has no effect Region will default to LOCKED (LOCK_REG read-back value 0) Writing the key (documented as the reset value) will UNLOCK the region Writing any value other than the key will LOCK the region from 0x0E to 0x2F	0x4A

Table 28: PVC_CONFIG_1 0x0E

Bit	Mode	Symbol	Description	Reset
7:6	R/W	PVC_DROP	V_{DROP}: drop from $V_{BAT}/2$ at which V_{OUT}, when increasing and crossing ($V_{BAT}/2$-V_{DROP}) (so becoming greater), generates a transition to DCM 00: 20 mV 01: 30 mV 10: 40 mV (default) 11: 50 mV	0x2
5:4	R/W	PVC_HYST	VHYST: hysteresis on the V_{DROP} to go back to CCM. So when V_{OUT} is decreasing and crosses ($V_{BAT}/2$-V_{DROP}-V_{HYST}) (so becoming lower), it generates a transition back to DCM. 00: 0 V 01: 10 mV 10: 20 mV (default) 11: 30 mV.	0x2
3:2	R/W	PVC_MS_DROP	Definition of four levels at which the master triggers the slave request. VMSI referenced to VCCM, where VCCM = (VBAT/2-PVC_DROP-PVC_HYSTMAX): 00: 15 mV below VCCM 01: 30 mV below VCCM (default) 10: 45 mV below VCCM 11: 60 mV below VCCM Note HYSTMAX is a constant value of 30 mV.	0x1
1:0	R/W	PVC_MS_HYST	MSI comparator hysteresis 00: 0 mV above VMSI 01: 15 mV above VMSI (default) 10: 30 mV above VMSI 11: 45 mV above VMSI	0x1

Table 29: PVC_CONFIG_2 0x0F

Bit	Mode	Symbol	Description	Reset
7:6	R/W	PVC_SLV_IF_PHASE	In master/slave configuration a clock is generated to control the slave interface. This clock has a configurable phase offset to the PVC_CLOCK: 0: 0° 1: 90° 2: 180° 3: 270°	0x0
5:4	R/W	-	Reserved	0x1

Bit	Mode	Symbol	Description	Reset
3:0	R/W	PVC_ILIM	Note: PVC recommended max value is 10 A. PVC peak current limit. 0000: 4800 mA 0001: 5250 mA 0010: 5700 mA 0011: 6150 mA 0100: 6600 mA 0101: 7050 mA 0110: 7500 mA 0111: 7950 mA 1000: 8400 mA 1001: 8850 mA 1010: 9300 mA 1011: 9750 mA 1100: 10200 mA 1101: 10650 mA 1110: 11100 mA 1111: 11550 mA	0xC

Table 30: PVC_CONFIG_3 0X10

Bit	Mode	Symbol	Description	Reset
7	R/W	PVC_PG_DIS	0: PVC power good comparator enabled 1: PVC power good comparator disabled This setting must be static and cannot be reconfigured in the application.	0x0
6:2	R/W	PVC_PG_ADJ	00000: 2.50 V 00001: 2.60 V 00010: 2.70 V 00101: 3.00 V 11000: 4.90 V 11001: 5.00 V >11001: 5.00 V	0x5
1:0	R/W	I_STUP_PVC	PVC start up current 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA	0x3

Table 31: CONFIG_A 0x11

Bit	Mode	Symbol	Description	Reset
7:5	R/W	VBAT_UV_HYS	Programmable hysteresis for the critical undervoltage threshold: 000: 50 mV 001: 100 mV 010: 150 mV 011: 200 mV 100: 250 mV 101: 300 mV 110: 350 mV 111: 400 mV	0x3
4:0	R/W	VBAT_UV_CRIT_THRSH	Note: PVC design requires 5.0 V minimum setting for correct operation: 00000: 4.60 V 00001: 4.65 V 00010: 4.70 V 00011: 4.75 V 01000: 5.00 V 11100: 6.00 V 11101: 6.05 V 11110: 6.10 V 11111: 6.15 V	0x0

Table 32: CONFIG_C 0x13

Bit	Mode	Symbol	Description	Reset
7	R/W	VDDIO_EN	0: VDDIO LDO disabled, pads supplied from VCORE 1: VDDIO LDO enabled, pads supplied at level set via VDDIO_CONF Note: When VDDIO_EN == 0, open drain GPO configurations via GPIO_1_PIN or GPIO_0_PIN valid only	0x1
6:5	R/W	FAULT_TIME	System controller configurable, pause when power cycling to ensure discharge of all critical nodes in the application before any attempt to reboot. 00: 0 ms (wait disable) 01: 10 ms 10: 100 ms 11: 500 ms	0x2
4:3	R/W	VDDIO_CONF	Selects the internal generated VDDIO voltage: 00: 1.5 V 01: 1.8 V 10: 2.8 V 11: 3.3 V	0x3

Bit	Mode	Symbol	Description	Reset
2:0	R/W	VBAT_UV_WARN	000: 5.2 V 001: 5.4 V 010: 5.6 V 011: 5.8 V 100: 6.0 V 101: 6.2 V 110: 6.4 V 111: 6.6 V	0x1

Table 33: CONFIG_D 0x14

Bit	Mode	Symbol	Description	Reset
7:4	R/W	-	Reserved	0xC
3:0	R/W	IF_BASE_ADDR1	I^2C uses slave address as follows: IF_BASE_ADDR1 = 4 MSBs of 7 Bit I^2C slave address (XXXX000) Example: For code XXXX = 1101 110_1000: Slave address of I^2C interface = 0x68.	0xD

Table 34: VARIANT_ID 0x30

Bit	Mode	Symbol	Description	Reset
7:4	R/W	MRC	Read-back of mask revision code (MRC) -code 0 to AA die release	0x0
3:0	R/W	VRC	Read-back of package variant code (VRC) -indicates type of package option	0x0

Table 35: DEVICE_ID 0x31

Bit	Mode	Symbol	Description	Reset
7:0	R	DEVICE_ID	Device ID: 0x81	0x81

Table 36: CUSTOMER_ID 0x32

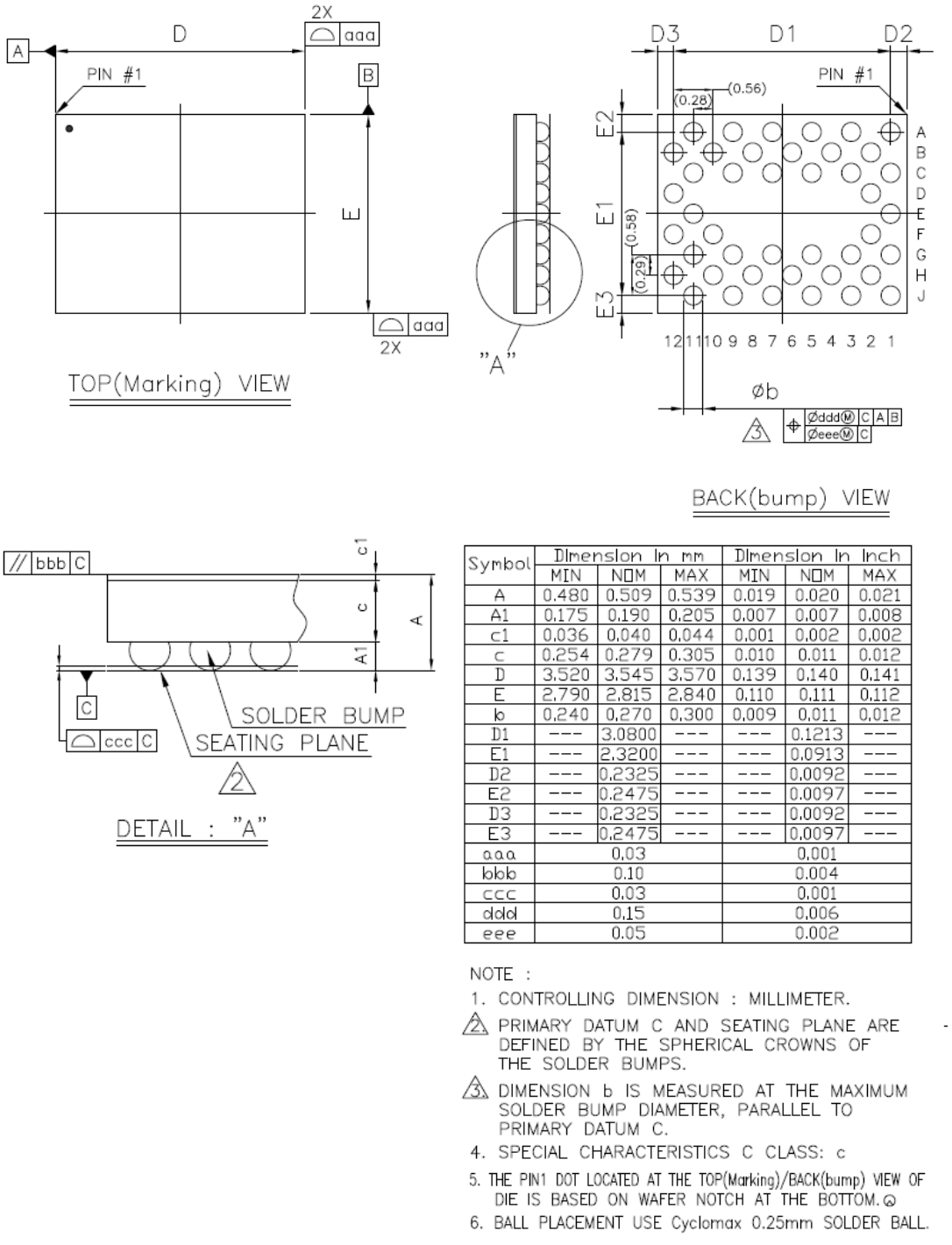
Bit	Mode	Symbol	Description	Reset
7:0	R/W	CUSTOMER_ID	ID for customer and target application platform, written during production of variant	0x0

Table 37: CONFIG_ID 0x33

Bit	Mode	Symbol	Description	Reset
7:0	R/W	CONFIG_REV	ID for revision of OTP settings, written during production of variant 00000000 - OTP unconfigured (reserved) >00000000 - OTP configuration revision xxx	0x0

14 Package Information

14.1 Package Outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.480	0.509	0.539	0.019	0.020	0.021
A1	0.175	0.190	0.205	0.007	0.007	0.008
c1	0.036	0.040	0.044	0.001	0.002	0.002
c	0.254	0.279	0.305	0.010	0.011	0.012
D	3.520	3.545	3.570	0.139	0.140	0.141
E	2.790	2.815	2.840	0.110	0.111	0.112
b	0.240	0.270	0.300	0.009	0.011	0.012
D1	---	3.0800	---	---	0.1213	---
E1	---	2.3200	---	---	0.0913	---
D2	---	0.2325	---	---	0.0092	---
E2	---	0.2475	---	---	0.0097	---
D3	---	0.2325	---	---	0.0092	---
E3	---	0.2475	---	---	0.0097	---
aaa	0.03			0.001		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.15			0.006		
eee	0.05			0.002		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: c
5. THE PIN1 DOT LOCATED AT THE TOP(Marking)/BACK(bump) VIEW OF DIE IS BASED ON WAFER NOTCH AT THE BOTTOM.
6. BALL PLACEMENT USE Cyclomax 0.25mm SOLDER BALL.

Figure 21: 43 WLCSP Package Outline Drawing

14.2 Suggested PCB Layout

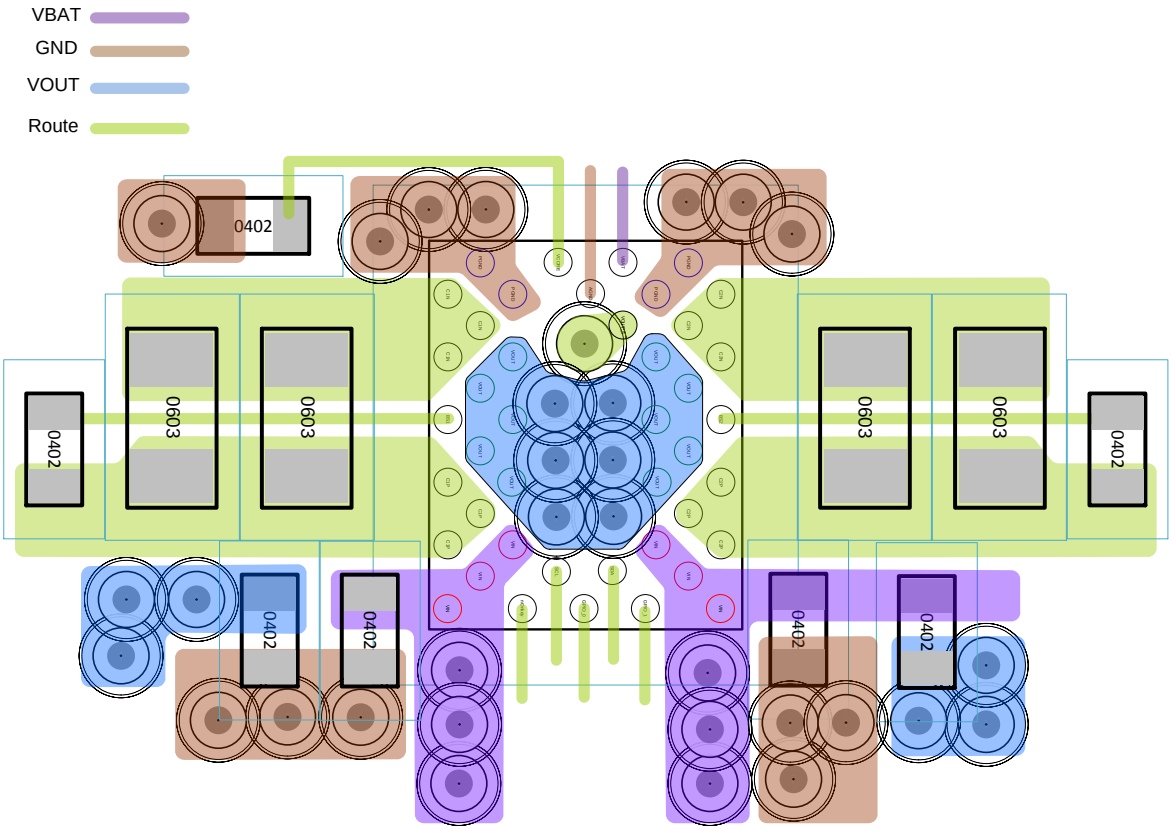


Figure 22: Suggested PCB Layout

The concept of PCB layout is presented in Figure 22. All drawn layers are top layer. Standard PTH VIAs connect the top layer to underlying VBAT, VOUT and GND plane(s).

14.3 RouteEasyTM Technology Chart

BGA ball diameter: 0.27 mm (10 mil)

BGA land size: 0.25 mm (10 mil)

Via hole size (finished): ≤ 0.2 to 0.25 mm (8 to 10 mil)

Via pad size: ≤ 0.55 mm (22 mil)

Anti-pad size: ≤ 0.75 mm (30 mil)

Trace width: 0.1 mm (4 mil)

Trace/trace space: 0.1 mm (4 mil)

Trace/pad/land space: ≥ 0.075 mm (3 mil)

15 Application Information

The following recommended components are examples selected from requirements of a typical application.

15.1 Recommended Capacitors

Ceramic capacitors are used as bypass capacitors at input and output rails as well as flying capacitors for the PVC. When selecting a capacitor the DC bias characteristic has to be taken into account. For the flying capacitors the temperature rise from maximum ripple current must be considered.

Table 38: Recommended Capacitor Types

Application	Value	Size	Temp Char	Tol (%)	Rated V	Type
PVC flying CFLY	4x 47 µF	0603	X5R ± 15 %	± 20	6.3 V	Murata GRM188R603476ME15
	4x 47 µF	0805	X5R ± 15 %	± 20	6.3 V	Murata GRM219R603476ME44#
PVC bypass CO_PVC and CIN_PVC	2x 4.7 µF	0402	X5R ± 15 %	± 20	10 V	Murata GRM155R61A475MEAA
PVC bootstrap CBS_PVC	2x 10 nF	0402	X7R ± 15 %	± 10	16 V	Murata GRM15XR71C103KA86#
	2x 10 nF	0201	X7R ± 15 %	± 10	10 V	Murata GRM033R71A103KA01#
VCORE output bypass CO_VCORE	1x 2.2 µF	0402	X5R ± 15 %	± 20	6.3 V	Murata GRM155R60J225ME95
PVC input decoupling CIN_PVC	2x 4.7 µF	0402	X5R ± 15 %	± 20	16 V	Murata GRM155R61C475ME15

16 Ordering Information

The order number consists of the part number followed by a suffix indicating the packing method. For details, please consult the customer portal on our web site or your local sales representative.

Table 39: Ordering Information

Part Number (Note 1)	Package Name	Package Description	Package Outline
DA9313-xxVK2	43 WLCSP	Tape and reel (2000 pcs)	Figure 21
DA9313-xxVK6	43 WLCSP	Waffle tray	Figure 21

Note 1 xx is the OTP variant

Revision History

Revision	Date	Description
1.0	04-Apr-2016	Initial release
1.1	04-May-2016	Addition of package drawing details and register maps
1.2	07-Jun-2016	Internal release
1.3	08-Jul-2016	Added functional description
1.4	11-Jul-2016	Corrected error in Section 10.1.2, GPIO_0 operates as the master/slave interface (MS_IF) and is pulled down internally, not GPIO_1
1.5	01-Aug-2016	Minor changes
1.6	22-Aug-2016	Added note to PVC Characteristics table regarding maximum allowed slew rate Minor rewording change to SLEEP mode enable in section 11.4
2.0	18-Oct-2016	Changes made post evaluation phase: Recommended Operating Conditions ● VPP removed ● IO_DC_PVC added DC Characteristics ● VTH_HI_POR max increased to 4.7 V VCORE Characteristics ● IO_VCORE added PVC Characteristics ● Efficiency changed from typ 95 % to min 97 % ● ILIM_ACC range tightened Addition to Note in section 10.3.2 Redesign of Pin Configuration Diagram (no pin placement changes)
2.1	09-Dec-2016	Added to Ordering Information.
2.2	24-Feb-2017	Updated Applications section Updated Ordering Information Updated RI_PD_GPI, RO_PU_GPO and RO_PU_GPI typical values Change to definition of REQ in section 9.3.1 PVC Ouput Voltage
3.0	07-Apr-2017	Final production release No changes to descriptions or parameters.

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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