Multimode Switched Capacitive Divider

General Description

The DA9389 is a bi-directional switched capacitor converter capable of up to 6A output current and targeting 2S or 3S battery-powered applications. When a mobile device is connected to any USB input voltage between 4 V and 13.5 V, the DA9389 can be used in current multiplier (voltage divider) mode to half the voltage applied to the V2X pin and double the available current to the system. It can also be configured to forward BYPASS and supply the V2X pin voltage directly to the system.

In capacitive voltage multiplier (current divider) mode, the input voltage range (V1X pin) supports a 1S Li-Ion or Li-Polymer battery pack, or any input voltage between 2.5 V and 6.5 V and provides twice the voltage on the output of the V2X pin at half the available input current. It can also be configured to reversed BYPASS and supply the V1X pin voltage directly to the system.

The power voltage converter (PVC) stage operates with conversion efficiency up to 98%. Low profile external components and a minimum PCB footprint allow small circuit implementation in compact applications. Since the switching devices are fully integrated, no external power FETs are needed.

The feature-rich DA9389 integrates a watchdog timer and supports voltage detection with autonomous wake-up and soft-start to limit inrush current from the power node. Additionally, Enable / ON-key supervision and power good signals are available for shelf-mode and different power up or power cycle scenarios. It also implements integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components.

The DA9389 is available in a 2.455 mm x 2.808 mm, 40-ball WLCSP package and all external components required are less than 1mm height.

Key Features

- Input voltage V_{V2X} (Divide mode)
  4 V to 13.5 V
- Input voltage V_{V1X} (Multiply mode)
  2.5 V to 6.5 V
- Output voltage
  V_{V1X} = 0.5 * V_{V2X} (Divide mode)
- Output voltage
  V_{V2X} = 2 * V_{V1X} (Multiply mode)
- 6 A Output current (Divide mode)
- 3 A Output current (Multiply mode)
- 4 A Output current (BYPASS mode)
- Typical 8 µA quiescent current
- Watchdog timer
- Spread spectrum frequency modulation
- Autonomous soft-start
- ON-key with long press power cycle
- Application Shelf-mode
- Voltage, current, and temperature supervision
- -40 ºC to +125 ºC junction temperature range
- 40 ball WLCSP 2.455 mm x 2.808 mm
  (0.4 mm pitch)
- 1 mm max. external components' height

Applications

- Notebook computers
- Tablet PCs
- Smartphones
- DSLR and mirrorless cameras
- Power banks
- Game consoles
- Drones
- Other 1S or 2S battery powered applications

System Diagram

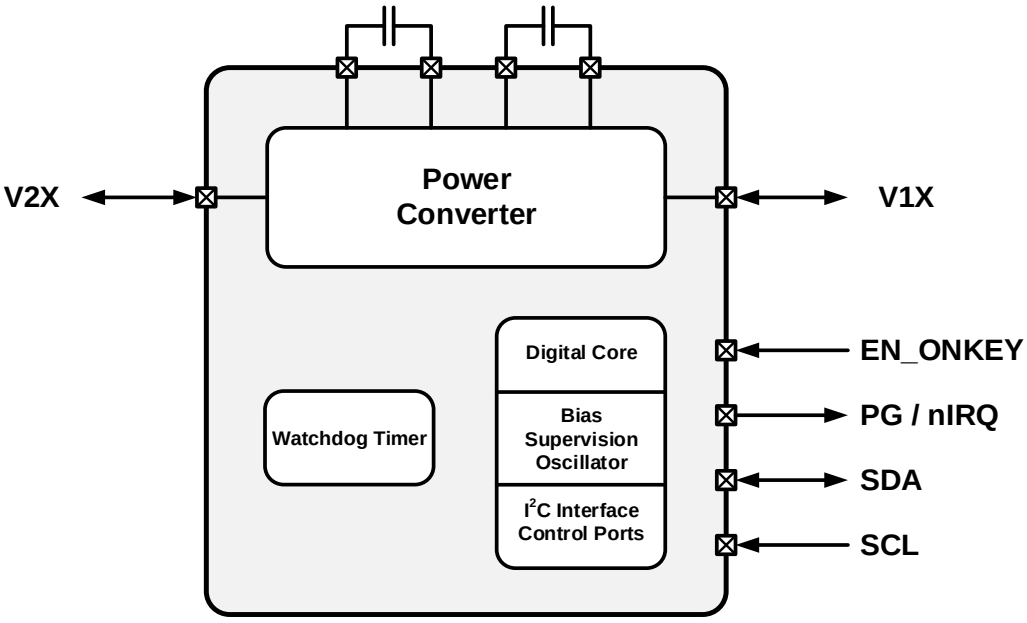

Figure 1: System Diagram

Contents

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1 Terms and Definitions

CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
HBM	Human body model
Li-Ion	Lithium-ion
nIRQ	Active low interrupt request
OTP	One-time programmable memory
PCB	Printed circuit board
PG	Power Good
PMIC	Power management integrated chip
POR	Power on reset
PVC	Power voltage converter
SCL	Serial clock
SDA	Serial data
SMBus	System management bus
USB	Universal serial bus

2 References

[1] NXP Semiconductors N.V., UM10204 I^2C-Bus Specification and User Manual, Revision 6, 2014.

3 Block Diagram

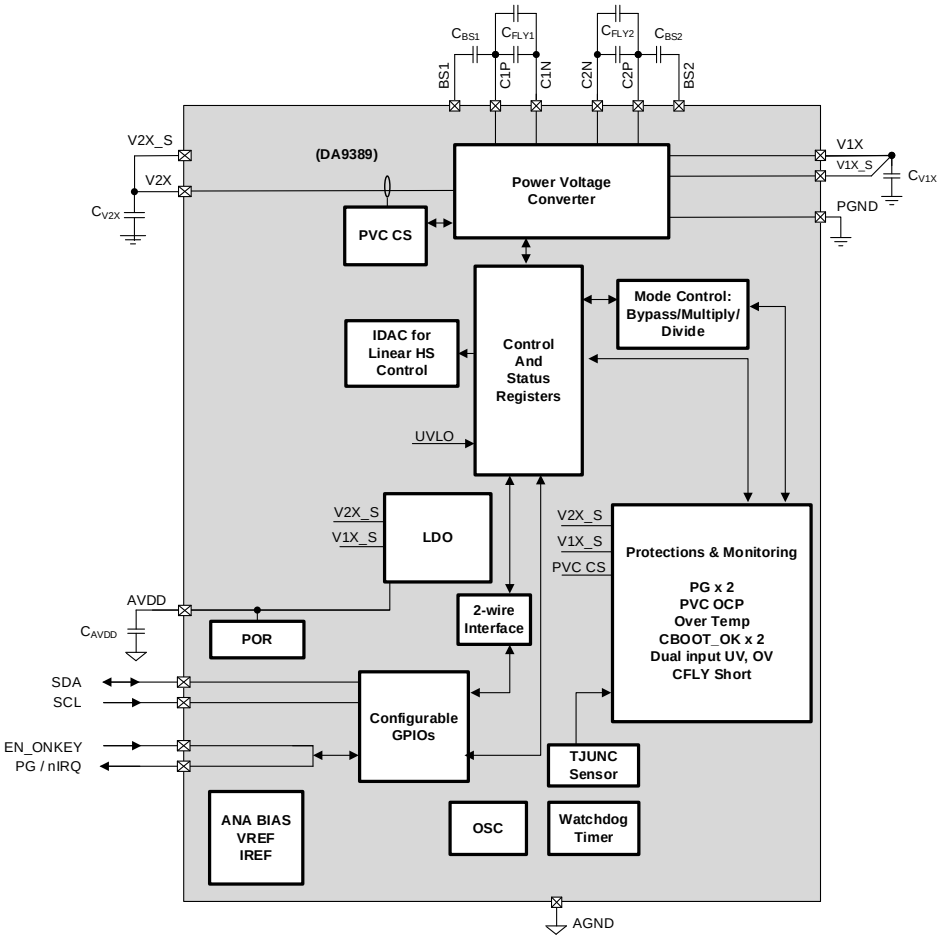


Figure 2: Block Diagram

4 Pinout

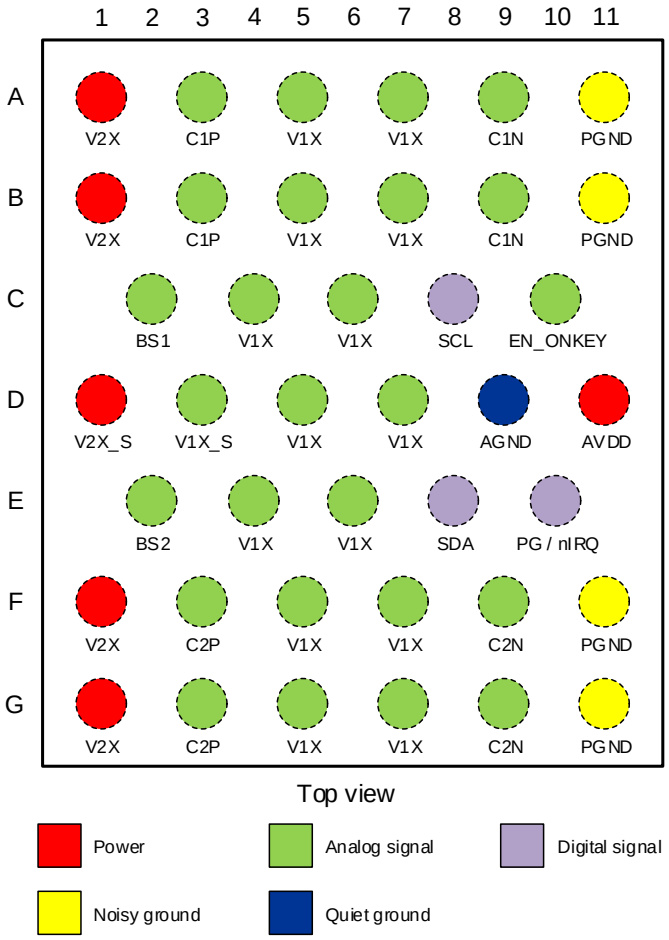


Figure 3: WLCSP Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Description
A1, B1, F1, G1	V2X	PWR	Power supply / output voltage
A3, B3	C1P	AIO	Flying capacitor #1 positive terminal
A5, A7, B5, B7, C4, C6, D5, D7, E4, E6, F5, F7, G5, G7	V1X	PWR	Output voltage / power supply
A9, B9	C1N	AIO	Flying capacitor #1 negative terminal
C2	BS1	AIO	Boot-strap capacitor #1 positive terminal
C8	SCL	DI	I^2C clock.
C10	EN_ONKEY	AIO	nON-key signal (active low) or IC_EN (active high)
D1	V2X_S	AI	Power supply / output voltage sense
D3	V1X_S	AI	Output voltage / power supply sense
D9	AGND	GND	Analog quiet ground

Pin #	Pin Name	Type (Table 2)	Description
D11	AVDD	AIO	Power supply for internal logic and control
E2	BS2	AIO	Boot-strap capacitor #2 positive terminal
E8	SDA	DIO	I^2C data
E10	PG / nIRQ	DO	Power good flag (open drain output, active high) / nIRQ interrupt GPO
F3, G3	C2P	AIO	Flying capacitor #2 positive terminal
F9, G9	C2N	AIO	Flying capacitor #2 negative terminal
A11, B11, F11, G11	PGND	GND	Power ground

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AIO	Analog input/output
DIO	Digital input/output	PWR	Power
GND	Ground		

5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-65	150	°C
T_J	Junction temperature		-40	150	°C
V_{V2X_LIM}	Limiting voltage V2X	V_{V2X} = 0 V to 22 V, ramp < 5 V/µs V_{V2X} = 0 V to 10 V, ramp < 20 V/µs	-0.3	22	V
V_{V1X_LIM}	Limiting voltage V1X	V_{V1X} = 0 V to 7 V, ramp < 20 V/µs	-0.3	7	V
V_{BS_LIM}	Limiting bootstrap voltage BS1, BS2		-0.3	7	V
V_{AVDD_LIM}	Limiting core voltage AVDD		-0.3	5.5	V
V_{PIN}	Limiting voltage on all pins except above		-0.3	V_{AVDD} + 0.3	V

5.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Junction temperature		-40		+125	°C
T_A	Ambient temperature		-40		+85	°C
V_{V2X_HI}	Input supply voltage range for the higher voltage rail	V2X in SWITCHING (Divide mode)	4		13.5	V
		V2X in BYPASS (Forward mode)	4		6.5	V
V_{V1X_LO}	Input supply voltage range for the lower voltage rail	V1X in SWITCHING (Multiply mode with a 1S Li-Ion or Li-Polymer battery pack (VBAT_MIN = 4.5 V) connected to V2X)	2.5		6.5	V
		V1X in SWITCHING (Multiply mode with no battery pack connected to V2X)	3.5		6.5	V
		V1X in BYPASS (Reverse mode)	3.5		6.5	V
$I_{V2X\_MAX\_BYP}$	Maximum continuous current on V2X	BYPASS (Forward and Reverse modes)			4	A
$I_{V2X\_MAX\_SW}$	Maximum continuous current on V2X	SWITCHING (Multiply and Divide modes)			3	A
$I_{V1X\_MAX\_BYP}$	Maximum continuous current on V1X	BYPASS (Forward and Reverse modes)			4	A
$I_{V1X\_MAX\_SW}$	Maximum continuous current on V1X	SWITCHING (Multiply and Divide modes)			6	A

5.3 Thermal Characteristics

5.3.1 Thermal Ratings

Table 5: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{TH_JA}	Package thermal resistance	Junction to ambient		26.08		ºC/W

5.3.2 Power Dissipation

Table 6: Power Dissipation

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_D	Power dissipation	R_{TH_JA} = 26.08 ºC/W T_A = 85 °C Note 1		1		W

Note 1 Obtained from package thermal simulation, board dimension 76 mm x 114 mm x 1.6 mm (JEDEC), 6-layer board, 35 µm thick copper top/bottom layers, 17 µm thick copper inside layers, natural convection (still air).

5.4 ESD Characteristics

Table 7: ESD Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	1.5			kV
V_{ESD_CDM}	Electrostatic discharge protection	Charged device model (CDM)	0.5			kV

5.5 Current Consumption

Table 8: Current Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$I_{Q\_PWR\_DWN}$	Current consumption POWERDOWN state	Pin EN_ONKEY = 0 V ONKEY_MODE = 0x1 $V_{AVDD} > V_{THR\_UP}$ $V_{V2X} < 5$ V $V_{V1X} = 0$ V T_A = 25 ºC		8		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_ACT}	Current consumption ACTIVE state	Pin EN_ONKEY = AVDD ONKEY_MODE = 0x1 Auto mode operation No load $V_{AVDD} > V_{THR\_UP}$ V2X > 6 V T_A = 25 ºC		20		µA
I_{Q_BYP}	Quiescent current in BYPASS state	Pin EN_ONKEY = AVDD ONKEY_MODE = 0x1 PVC_EN = 0x1 $V_{V2X} = V_{V1X}$ = 5 V T_A = 25 ºC		2		mA
I_{Q_RBYP}	Quiescent current in BYPASS state (Reverse mode)	Pin EN_ONKEY = AVDD ONKEY_MODE = 0x1 PVC_EN = 0x1 $V_{V1X} = V_{V2X}$ = 5 V T_A = 25 ºC		2		mA

5.6 Electrical Characteristics

Unless otherwise noted, the following is valid for T_A = -40 °C to +85 ºC and V_{V2X} = 8 V (SWITCHING state) or V_{V2X} = 4 V (BYPASS state)

5.6.1 Power Voltage Converter

Table 9: Power Voltage Converter

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{V2X_SW}	Input supply voltage range for the higher supply voltage rail	V2X in SWITCHING (Divide mode)	4		13.5	V
V_{V1X_SW}	Input supply voltage range for the lower supply voltage rail	V1X in SWITCHING (Multiply mode) Note 1	2.5		6.5	V
V_{V2X_BYP}	Input supply voltage range for the higher supply voltage rail	V2X in BYPASS (Forward mode)	4		6.5	V
V_{V1X_RBYP}	Input supply voltage range for the lower supply voltage rail	V1X in BYPASS (Reverse mode)	3.5		6.5	V
$I_{V1X\_SW\_MAX}$	Maximum continuous current on V1X	SWITCHING (Divide mode)	6			A
$I_{V2X\_SW\_MAX}$	Maximum continuous current on V2X	SWITCHING (Multiply mode)			-3	A
I_{FBYP_MAX}	Maximum current on V1X	Forward BYPASS mode	4			A
I_{RBYP_MAX}	Maximum current on V2X	Reverse BYPASS mode			-4	A
f_{SW}	PVC switching frequency	Fixed frequency mode	200		1000	kHz
f_{SW_EMI}	Spread spectrum modulation frequency range	Configurable via SPREAD_WIDTH (±2, ±4, ±8 or ±16)	-16		16	%
f_{SW_USONIC}	Ultrasonic switching frequency Note 2	EN_DCM_ULTRASONIC_VAL = 0x1	20			kHz
η_{PK_DIV}	Peak efficiency in SWITCHING (Divide mode)	2x 47 µF 0603 per phase V_{V2X} = 8 V I_{V1X} ~ 2 A f_{SW} = 300 kHz		98		%
η_{CCM_DIV}	High current efficiency in SWITCHING (Divide mode)	2x 47 µF 0603 per phase V_{V2X} = 8 V I_{V1X} = 5 A f_{SW} = 300 kHz		97		%

Parameter	Description	Conditions	Min	Typ	Max	Unit
η_{DCM_DIV}	Light load efficiency in SWITCHING (Divide mode)	2x 47 µF 0603 per phase V_{V2X} = 8 V I_{V1X} = 10 mA to 1000 mA f_{SW} = 300 kHz		96.5		%
η_{PK_MUL}	Peak efficiency in SWITCHING (Multiply mode)	2x 47 µF 0603 per phase V_{V1X} = 4 V I_{V2X} = ~ 1.5 A f_{SW} = 300 kHz		98		%
η_{CCM_MUL}	High current efficiency in SWITCHING (Multiply mode)	2x 47 µF 0603 per phase V_{V1X} = 4 V I_{V2X} = 2.5 A f_{SW} = 300 kHz		97		%

Note 1 2.5 V Min with a 1S Li-Ion or Li-Polymer battery pack (VBAT_MIN = 4.5 V) connected to V2X. 3.5 V Min without a battery connected to V2X.

Note 2 Limiting the frequency to 20 kHz can increase I_{Q_ACT}.

5.6.2 AVDD Regulator

Table 10: AVDD Regulator

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{V2X}	Supply voltage	High voltage power rail	4		13.5	V
V_{V1X}	Supply voltage	Low voltage power rail	2.5		6.5	V
V_{AVDD}	Internal analog supply voltage			4		V
C_{AVDD}	Effective capacitance @ AVDD	Including voltage and temperature coefficient	0.5	1	2	µF

5.6.3 Internal Oscillator

Table 11: Internal Oscillator

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
f_{OSC}	Internal oscillator frequency			6		MHz
f_{ACC}	Internal oscillator frequency accuracy	After trimming	-5		5	%

5.6.4 Power-on-Reset and Current Supervision

Table 12: Power-on-Reset and Current Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{THR_DWN}	Power-on-reset lower threshold	Measured @ AVDD V_{V2X} / V_{V1X} decreasing	2.1			V
V_{THR_UP}	Power-on-reset upper threshold	Measured @ AVDD V_{V2X} / V_{V1X} increasing			2.5	V
V_{POR_HYS}	Power-on-reset hysteresis			55		mV
$I_{V2X\_POS\_OCP\_SW}$	Positive peak current protection programmable range in SWITCHING (Divide mode)	Maximum current on V2X programmable via SEL_OCP (3.25, 3.5, 3.75, 4.0, 4.25, 4.5, 4.75, 5.0) A	3.25		5	A
$I_{V2X\_POS\_OCP\_BYP}$	Positive peak current protection programmable range in BYPASS (Forward mode)	Maximum current on V2X programmable via SEL_OCP_BYPASS (3.25, 3.5, 3.75, 4.0, 4.25, 4.5, 4.75, 5.0) A	3.25		5	A
$I_{V2X\_NEG\_OCP\_SW}$	Negative peak current protection programmable range in SWITCHING (Multiply mode) Note 1	Maximum current on V2X programmable via SEL_OCP (-3.25, -3.5, -3.75, -4.0, -4.25, -4.5, -4.75, -5.0) A	-5		-3.25	A
$I_{V2X\_NEG\_OCP\_BYP}$	Negative peak current protection programmable range in BYPASS (Reverse mode) Note 1	Maximum current on V2X programmable via SEL_OCP_BYPASS (-3.25, -3.5, -3.75, -4.0, -4.25, -4.5, -4.75, -5.0) A	-5		-3.25	A
$I_{V2X\_OCP\_ACC}$	Accuracy of current protection	Protection on V2X	-20		20	%

Note 1 The PVC turns off but the current is not stopped (no RCP).

5.6.5 Timers

Table 13: Timers

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{D_FLT}	Minimum latch-off delay from fault		0		500	ms
t_{DEB}	EN_ONKEY de-bounce time		0		750	ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{D_KEY}	EN_ONKEY minimum press timer		1		7	s
t_{D_SHDN}	EN_ONKEY forced power cycle delay timer		4		6	s
t_{WD}	Watchdog period	Controlled by writting a timeout value to WD_TIMER_SEL	5		33	s

5.6.6 Input Voltage Supervision

Table 14: Input Voltage Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{IN\_OV\_DIV}$	V_{IN} over-voltage programmable range on V2X in Divide mode	2-bit programmble via SEL_OVP (12, 13, 14, 15) V	12		15	V
$V_{IN\_OV\_BYP}$	V_{IN} over-voltage programmable range on V2X in Forward BYPASS mode and on V1X in Reverse BYPASS mode	2-bit programmble via SEL_OVP (6.0, 6.5, 7.0, 7.5) V	6		7.5	V
$V_{IN\_OV\_MUL}$	V_{IN} over-voltage programmable range on V1X in Multiply mode	2-bit programmble via SEL_OVP_MUL (6.0, 6.5, 7.0, 7.5) V	6		7.5	V
$V_{IN\_OV\_DIV\_HYS}$	Input over-voltage hysteresis on V2X in SWITCHING (Divide mode)	Falling hysteresis		600		mV
$V_{IN\_OV\_FBYP\_HYS}$	Input over-voltage hysteresis on V2X in Forward BYPASS mode	Falling hysteresis		300		mV
$V_{IN\_OV\_MUL\_RBYP\_HYS}$	Input over-voltage hysteresis on V1X in SWITCHING (Multiply mode) and BYPASS (Reverse mode)	Falling hysteresis		300		mV
$V_{IN\_OV\_ACC}$	Input over-voltage accuracy		-2		2	%
$V_{IN\_UV\_MUL}$	VIN under-voltage on V1X in SWITCHING (Multiply mode)	2-bit programmble via SEL_UVP (2.4, 2.7, 3.0, 3.3) V	2.4		3.3	V
$V_{IN\_UV\_RBYP}$	VIN under-voltage on V1X in BYPASS (Reverse mode)			3.3		V
$V_{IN\_UV\_DIV\_BYP}$	VIN under-voltage on V2X in SWITCHING (Divide mode) and BYPASS (Forward mode)	2-bit programmable via SEL_UVP (3.8, 4.0, 4.2, 4.4) V	3.8		4.4	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IN\_UV\_HYS}$	Input under-voltage hysteresis	Falling hysteresis 2-bit programmable via SEL_UVP_HYS (50, 100, 150, 200) mV		50		mV
$V_{IN\_UV\_ACC}$	Input under-voltage accuracy		-4		4	%

5.6.7 Junction Temperature Supervision

Table 15: Junction Temperature Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
T_{THR_CRIT}	Critical temperature threshold	Note 1	140	145	150	°C
T_{THR_EN}	Temperature threshold for re-enabling regulation	Note 1	130	135	140	°C

Note 1 Thermal thresholds are non-overlapping.

5.6.8 Digital I/O Characteristics

Table 16: Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
EN_ONKEY Pin						
$V_{IH\_EN\_ONKEY}$	Input high voltage EN_ONKEY		1.2			V
$V_{IL\_EN\_ONKEY}$	Input low voltage EN_ONKEY				0.4	V
$V_{HYS\_EN\_ONKEY}$	Hysteresis for EN_ONKEY	Falling EN_ONKEY	-100			mV
$R_{PU\_EN\_ONKEY}$	Pull-up resistance for EN_ONKEY	Tied to AVDD ONKEY_PU = 0x1		22		kΩ
$R_{PD\_EN\_ONKEY}$	Pull-down resistance for EN_ONKEY	IC_EN_PULLDOWN = 0x1 ONKEY_MODE = 0x1 (IC_EN mode) POWERDOWN state		100		kΩ
SDA Pin						
V_{IH_SDA}	Input high voltage SDA	Note 1	1.2			V
V_{IL_SDA}	Input low voltage SDA	Note 1			0.4	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL_SDA}	Output low voltage SDA	Open drain I_{OUT_SDA} = 3 mA			0.24	V
PG / nIRQ Pin						
V_{OL_PG}	Output low voltage PG	Open drain, Active high PG_PIN_EN = 0x1			0.24	V
R_{PU_PG}	External pull-up resistor	PG_PIN_EN = 0x1		22		kΩ
V_{OL_nIRQ}	Output low voltge nIRQ	External pull-up resistor = 22 kΩ PG_PIN_EN = 0x0			0.24	V
SCL Pin						
V_{IH_SCL}	Input high voltage SCL	Note 1	1.2			V
V_{IL_SCL}	Input low voltage SCL	Note 1			0.4	V

Note 1 Input range compatible with 1.8 V and 3.3 V logic.

5.6.8.1 I²C Timing Characteristics

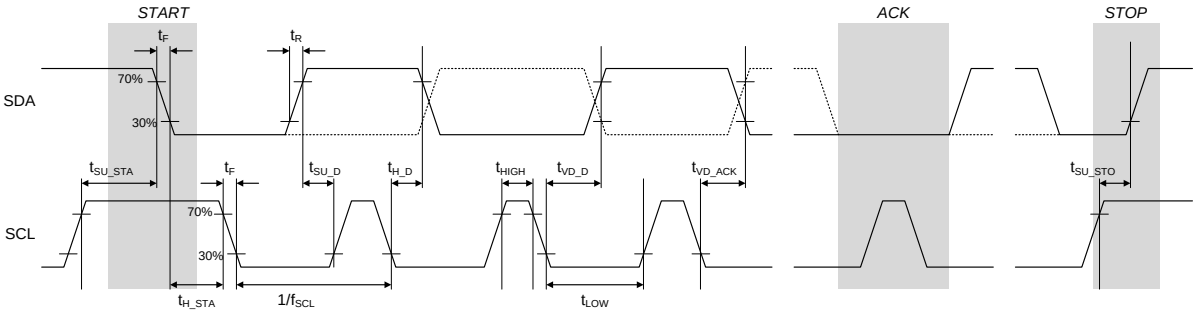


Figure 4: Interface Timing

Table 17: I2C Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{BUF}	Bus free time STOP to START		0.5			µs
C_{BUS}	Bus line capacitive load				150	pF
f_{SCL}		Note 1	0		1000	kHz
t_{SETUP_START}	Start condition set-up time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE}	I²C SCL and SDA rise time	(input requirement)			300	ns
t_{FALL}	I²C SCL and SDA fall time	(input requirement)			300	ns
t_{SETUP_DATA}	Data set-up time		50			ns
t_{HOLD_DATA}	Data hold time		0			ns
t_{VAL_DATA}	Data valid time				0.45	µs
$t_{VAL\_DATA\_ACK}$	Data valid time acknowledge				0.45	µs
t_{SETUP_STOP}	Stop condition set-up time		0.26			µs

Note 1 Maximum clock period is 35 ms if OTP control I2C_TIMEOUT_EN is enabled.

6 Functional Description

The DA9389 is a power voltage converter (PVC) that generates an unregulated output voltage of approximately half the input voltage in Divide mode (or twice the input voltage in Multiply mode) using a capacitive interleaved current doubler.

Host communication is not required for operation with OTP loading to configure DA9389 on start up. However, an I^2C interface is available for host configuration of the register map if required.

In addition, the PG / nIRQ pin can be configured as nIRQ for fault signaling and recovery or PG to detect when the input-to-output voltage is within a safe operating range.

6.1 Power Voltage Converter

The high efficiency 2S to 1S PVC is capable of supplying 1S voltage rails with up to 6 A output current, see Figure 5. The dual phase interleaved operation ensures an almost constant input current, resulting in improved immunity to noise.

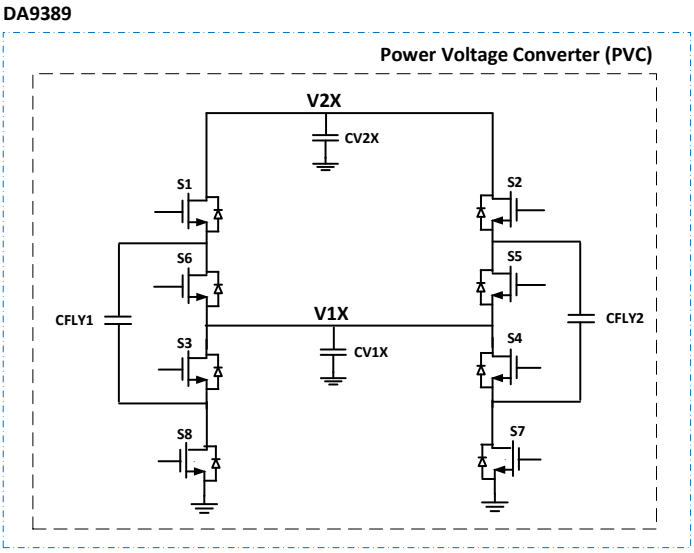


Figure 5: Power Voltage Converter Diagram

6.1.1 PVC Output Voltage

The PVC operates with a fixed duty cycle. Under no-load condition, the output voltage is half of the input voltage. When a current, I_{V1X}, is drawn at the low voltage pin (V1X) and the PVC is switching at frequency of f_{SW}, the output voltage is determined as:

$$V_{V1X} = \frac{V_{V2X}}{2} - R_{EQ} \cdot I_{V1X}$$

Where:

- R_{EQ} is a function of the sum of all resistances in the input/output power path (including the power device's on-resistance and the PCB routing resistance) as well as the switching frequency, C_{FLY}, and PCB parasitics

The voltage ripple at V1X can be first order approximated as the voltage drop due to the discharge of the C_{FLY} capacitor in half of the period at an f_{SW} switching frequency, plus the discharge voltage of the output capacitor during a typical 20 ns short dead time for phase switch.

6.1.2 PVC Start Up

DA9389 supports a PVC start up into the pre-biased output rail (input and output). The PVC operation starts in current limited switching until the voltage between the high voltage pin (V2X) and the low voltage pin (V1X) is considered safe by the PVC's state machine, based on the power good (PG) comparators. The duration of the PVC start up depends on the total effective capacitance connected to the PVC (flying capacitors and capacitance connected to the high and low voltage power pins) and the initial voltage deviation from the target ratio of 2:1, 1:1 or 1:2. During PVC start up the PVC does not switch and the flying capacitors, C_{FLY}, are connected in parallel to the output capacitor, C_{V1X}.

NOTE
A start up phase with a large load will not be successful. The PVC has a ramp-up timer which checks the ramp-up happens in approximately 20 ms. If the output voltage has not reached a value close to $V_{V2X}/2$ (or $2*V_{V1X}$) at this time this indicates a failure condition and the regular switching is not started.

NOTE
To avoid overheating with thermal power cycling during the PVC start up it is the responsibility of the external application to limit load current from any of the power pins until the assertion of PG. At the end of the start up phase the normal operation (BYPASS or SWITCHING) of the PVC is restored.

6.1.3 PVC Operation Modes

Following start up the PVC operates in fixed frequency or in automatic frequency mode by writing into bit MODE. For minimum input and output voltage ripple / EMI the PVC ensures nearly constant input current using two separate PVC phases (flying capacitance C_{FLY1} and C_{FLY2}) with interleaved switching.

The PVC switching frequency f_{SW} is derived from f_{OSC}. Spread spectrum can be selected in OTP for reduced EMI. To avoid audible noise a minimum switching frequency of f_{SW_USONIC} can be forced during automatic frequency mode.

In automatic frequency mode, the PVC operates in continuous conduction mode (CCM) at high loads and moves to discontinuous conduction mode (DCM) as soon as the load drops below a certain threshold.

In Multiply mode, the PVC solely operates in CCM regardless of the MODE setting.

Operating in automatic frequency mode extends the high efficiency range to low levels of output loads.

6.2 PVC Operation States

DA9389 operates in five different states (OFF, STANDBY, ACTIVE (SWITCHING or BYPASS), POWERDOWN, or FAULT). At low input supply voltages ($V_{AVDD} < V_{THR\_DWN}$) DA9389 goes into OFF state, waiting for input power to recover. FAULT is typically triggered from a fault condition like supply voltage being outside the operating range or high junction temperature.

Figure 6 shows DA9389 operational states as well as the conditions that make DA9389 transition from one state to another.

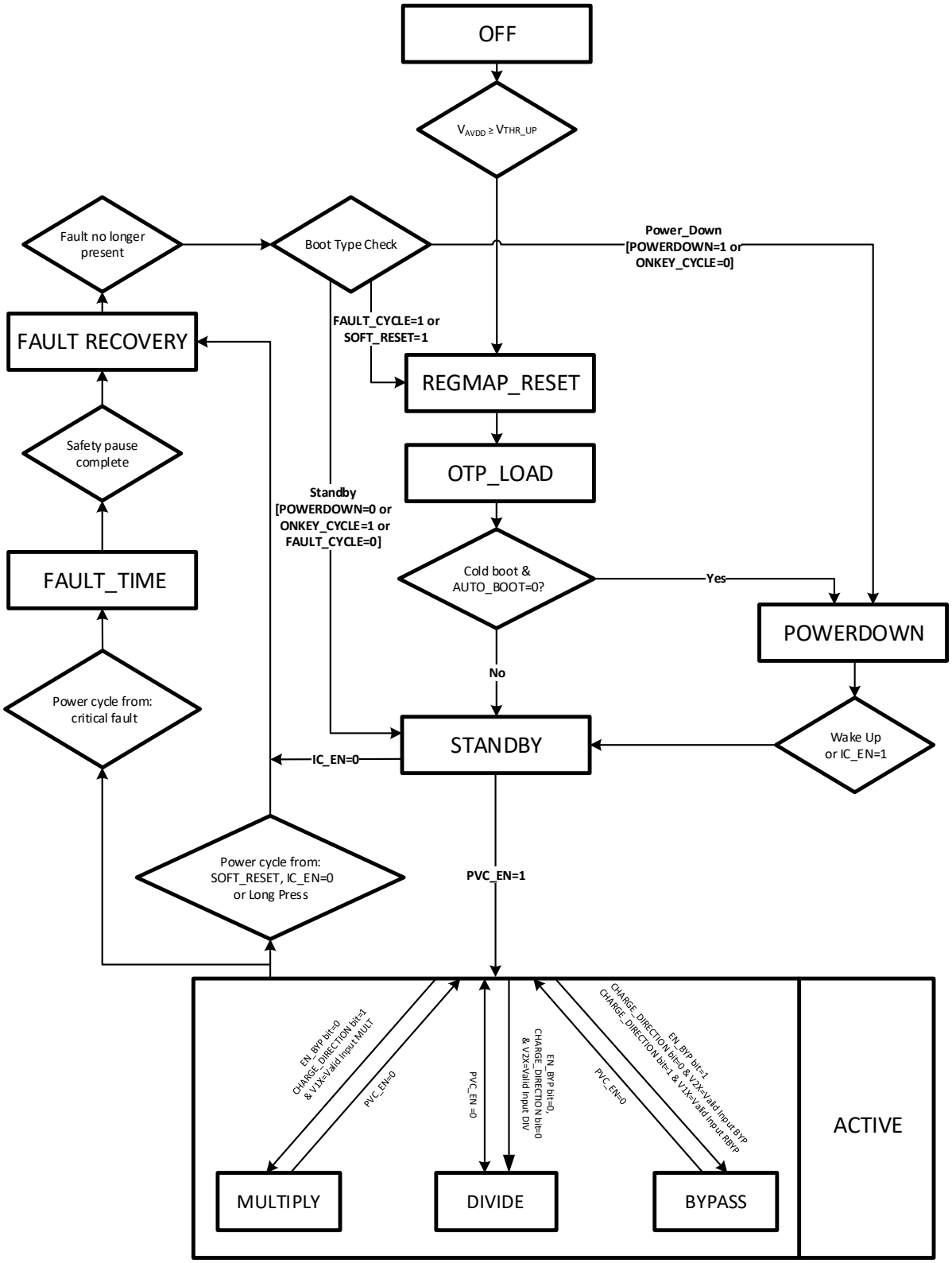


Figure 6: DA9389 Power States

Note 1 Valid input SWITCHING (Divide mode) = $V_{IN\_UV\_DIV\_BYP} < V2X < V_{IN\_OV\_DIV}$
Valid input BYPASS (Forward mode) = $V_{IN\_UV\_DIV\_BYP} < V2X < V_{IN\_OV\_BYP\_MUL}$
Valid input SWITCHING (Multiply mode) = $V_{IN\_UV\_MUL\_BYP} < V1X < V_{IN\_OV\_BYP\_MUL}$
Valid input BYPASS (Reverse mode) = Same conditions as SWITCHING (Multiply mode)

6.2.1 OFF State

During OFF state the supply voltage is too low for the operation of DA9389 and the Power-on Reset (POR) circuitry waits for sufficient input power. With sufficient supply voltage ($V_{AVDD} > V_{THR\_UP}$) DA9389 progresses from OFF state into OTP load followed by POWERDOWN, STANDBY or ACTIVE state depending on the configuration of ONKEY_MODE and PVC_EN.

6.2.2 POWERDOWN State

In POWERDOWN state the only active circuitry is the internal AVDD regulator and the EN_ONKEY pin supervision. The PVC stops switching and the flying capacitors are disconnected from pin V1X.

DA9389 transitions from POWERDOWN to ACTIVE/STANDBY state from a button press at pin EN_ONKEY (push-button mode) or the voltage level at EN_ONKEY changing from 0 V to V_{AVDD} (IC_EN mode).

6.2.3 STANDBY State

In STANDBY state the PVC is off and other blocks are operational. The 6 MHz main oscillator can be on during this state and I^2C is functional. Other circuitry available includes OV and UV protection comparators on V2X and V1X, nIRQ, and event handler.

STANDBY is also used to support application low power modes with lower quiescent current. This state can be entered and exited with PVC_EN register write.

6.2.4 FAULT State

Whenever one of the internal supervision and protection circuits flags an error, DA9389 transitions into FAULT state.

FAULT state can also be forced via an unconditional application power cycle (re-boot) from a long press of the push button connected to pin EN_ONKEY. Table 18 summarizes the triggers for FAULT state .

Table 18: Triggers for FAULT State

Fault Name	Trigger
Thermal shutdown	T_J rising above T_{THR_CRIT}
Input over-voltage protection	V_{IN} rising above OVP threshold
Input under-voltage protection	V_{IN} falling below UVP threshold
CBOOT voltage protection	< 3 V is developed across the bootstrap capacitor
PVC transition state timer monitor	State timer expired
Internal power good monitor	Input-to-output voltage is outside a safe operating range
CFLY short protection	A CFLY capacitor is shorted
Watchdog timer monitor	Watchdog timer expired
PVC latch-off	PVC latched-off due to an over-current condition

DA9389 remains in FAULT state for a minimum duration of t_{D_FLT}. It will stay in FAULT state until no supervision circuitry is flagging a fault. It will then perform an OTP read and progresses to POWERDOWN or ACTIVE/STANDBY state depending on the OTP settings.

6.2.5 ACTIVE State

ACTIVE is the main operating state of DA9389 and is entered after OTP load. The PVC is then automatically turned on and operates in the configured SWITCHING Divide / Multiply mode or BYPASS Forward / Reverse mode.

ACTIVE state exits towards FAULT state due to the faults mentioned in Table 18.

6.2.5.1 SWITCHING State - Divide or Multiply Mode

During SWITCHING, any two of the PVC switches in one branch are turned fully on (for example S1 and S3) while the other two switches (in this case S6 and S8) are off, see Figure 5. This configuration occurs during one phase cycle of the PVC. In the second phase, the polarity of these switches is reversed.

The PVC is switching between these two phases to place the flying capacitor in series or parallel to the V1X capacitor. The act of charging the capacitor in one phase and redistributing the charge to the V1X capacitor in the other phase enables the doubling or halving operation.

This is dependent on the direction of the configured PVC and input voltage applied (V2X or V1X). The PVC operates with two branches interleaved to reduce switching ripple and improve efficiency performance.

There are two modes of operation in SWITCHING (Divide or Multiply). The configuration of either of these modes is dependent on a valid input supply being applied (V1X) and the settings of the EN_BYP and CHARGE_DIRECTION register bits, see Table 19.

6.2.5.2 BYPASS State - Forward or Reverse Mode

In BYPASS, the PVC turns on the four switches (S1, S2, S5, and S6) on the high side, see Figure 5. V1X ≈ V2X and both PG comparators are set to high.

The PVC will remain in Forward mode if the EN_BYP bit is asserted and the CHARGE_DIRECTION bit is deasserted, see Table 19.

To operate in Reverse mode (when input voltage supply is applied on V1X), set EN_BYP and CHARGE_DIRECTION bits high.

Table 19: PVC Operation Modes

Input Voltage Supply	EN_BYP Bit	CHARGE_DIRECTION Bit	Operating Modes
V2X	0	0	SWITCHING (Divide mode)
V1X	0	1	SWITCHING (Multiply mode)
V2X	1	0	BYPASS (Forward mode)
V1X	1	1	BYPASS (Reverse mode)

NOTE
Automatic mode transition between Forward (Divide or BYPASS) and Reverse (Multiply or BYPASS) under a large load is not supported. The load current must be reduced < 100 mA before changing mode.

6.3 Monitoring and Protections

Monitoring and Protections is a matrix of comparators for protecting the circuit from functioning in hazardous conditions and for controlling the state transitions.

6.3.1 Input Voltage Protection

Input voltage protection is used for detecting the presence of an input supply, V_{IN} (on V2X or V1X), and for disabling the PVC when V_{IN} rises too high. The PVC is only operational when V_{IN} is within the range defined by ($V_{IN\_UV\_DIV\_BYP}$ or $V_{IN\_UV\_MUL\_BYP}$) and ($V_{IN\_OV\_DIV}$ or $V_{IN\_OV\_BYP\_MUL}$).

V_{IN} over-voltage debounce conditions will disable the PVC and will trigger OV_FAULT_EVENT. Resuming normal operation is allowed after all fault conditions are gone.

Similarly, under-voltage conditions will disable the PVC and will trigger UV_FAULT_EVENT. Resuming normal operation is allowed after all fault conditions are gone.

Multimode Switched Capacitive Divider

In DA9389, the feedback for the under-voltage and over-voltage comparators depends on the state and functional mode setting (CHARGE_DIRECTION and EN_BYP register bits) of the PVC. The feedback may be input to either the V2X_S or V1X_S pins. Configuration for the feedback of these protection comparators is shown in Table 20.

Table 20: Input Selection for Under-Voltage and Over-Voltage Protection Comparators

CHARGE_DIRECTION Bit	EN_BYP Bit	UV and OV Input	UV and OV Settings
0	1	V2X_S	BYPASS (Forward mode)
0	0	V2X_S	SWITCHING (Divide mode)
1	X	V1X_S	BYPASS (Reverse mode) / SWITCHING (Multiply mode)

Note 1 If PVC is on, any change in CHARGE_DIRECTION or EN_BYP bits will not be registered until PVC turns off.

6.3.2 Power Good Protection and Fault Generation

The purpose of the power good (PG) protection is to detect when the input-to-output voltage is within a safe operating range, defined by V_{PG_POS} and V_{PG_NEG} thresholds, see conditions for PG comparators ($V_{PG\_POS\_SW}$,$V_{PG\_NEG\_SW}$, $V_{PG\_POS\_BYP}$, $V_{PG\_NEG\_BYP}$), Section 5.6.6.

DA9389 has two sets of PG comparators:

- PG_POS with V2X_S positive input and V1X_S negative input
- PG_NEG with V1X_S positive input and V2X_S negative input

Both comparators are used to detect a PG fault or to assist with start up during the state transitions. Each comparator has OTP configuration settings and trimming capabilities.

The PG1 and PG2 comparators output a 1 if the operating conditions on V2X_S and V1X_S are considered within safe limits for the PVC (indicating that the ratio is less than the PG comparator threshold).

A PG fault is generated if at least one of the comparators outputs a 0 while the PVC is in BYPASS or SWITCHING state.

6.3.3 Over-Current Protection and Latch-Off

DA9389 features bi-directional current protection for protection from over-current conditions in both forward and reverse direction. If the sensed current exceeds the set threshold the OCP comparator will trigger a fault condition.

The OCP comparator has 3-bit programmability for over-current threshold selection during SWITCHING state and another 3-bit setting for operation in BYPASS state, see SEL_OCP and SEL_OCP_BYPASS settings.

When the current through **one** of the switching PVC phases is increasing above the set OCP thresholds the DA9389 latches off from over-current, causing all PVC switches to become Hi-Z, and enters FAULT state.

6.3.4 CFLY Short Protection

In addition to over-current protection, the PVC has a safety feature to protect the flying capacitors from being shorted. This generates a PG fault or OC fault.

6.3.5 CBOOT_OK Monitoring

During certain states (such as BYPASS) of the PVC's field state machine (FSM), the bootstrap capacitors are being charged using an internal charge pump. The CBOOT_OK comparators (1 and 2) are monitoring the voltage on the bootstrap capacitor. If enough voltage (≥ 3 V) is developed

across the bootstrap capacitor, the comparator will set CBOOT_OK = 1. The CBOOT_OK signal ensures that high-side power FETs are turned on with enough voltage gate drive.

A CBOOT_OK fault is generated if CBOOT_OK = 0 for longer than the TCP_OK_FALL_DEB debounce setting, while the PVC is in BYPASS state. CBOOT_OK fault will not be generated in any other PVC state, regardless of the CBOOT_OK output.

6.3.6 Over-Temperature Supervision

DA9389 is protected from damage due to excessive power dissipation by thermal shutdown.

There are two thresholds concerning thermal protection, thermal critical (T_{THR_CRIT}) and thermal re-enable (T_{THR_EN}). When $T_J > T_{THR\_CRIT}$ DA9389 enters FAULT state until $T_J < T_{THR\_EN}$.

Due to the slow changing nature of T_J, a single comparator with an input hysteresis of T_{THR_CRIT} - T_{THR_EN} is included. To reduce current consumption, the comparator is turned off during NO POWER and POWERDOWN states.

6.3.7 PVC Timer Fault

This is a fault generated by the PVC's state machine whenever a transitional state timer expires before the condition to exit from that state. This will force the PVC to turn off instead of proceeding to the next state.

6.3.8 Watchdog Timer

DA9389 features a watchdog timer which monitors the host during its operation and disables the PVC if a timeout event occurs.

The watchdog timer is enabled, via I^2C, through WD_TIMER_EN. If enabled, the timer is active in ACTIVE.

When enabled, the watchdog timer is loaded with a pre-programmed timeout period and starts decrementing. The timeout period value is selected, via I^2C, in WD_TIMER_SEL.

When the watchdog timer is on, the host is expected to issue an I^2C transaction to DA9389 before the end of the timeout period. The I^2C transaction re-starts the watchdog timer by over-writing a new value to WD_TIMER_SEL.

However, if the host does not issue the transaction within the timeout period, and DISABLE_WD_TO_EVENT is not set:

A timeout event occurs.

WD_TO_EVENT is asserted, unless masked by MASK_WD_TO_EVENT.

If the system is in ACTIVE state, the PVC is disabled.

A watchdog timer fault is indicated by the WD_TO_STATUS bit.

NOTE
The register fields WD_TIMER_SEL and WD_TIMER_EN are password protected. I^2C access is required to unlock those bits. Write 0x3D to address 0xB541.

6.3.9 nIRQ Fault

Pin nIRQ (PG / nIRQ) is an active low, open drain output signal that indicates that an interrupt causing event has occurred. The related event and status information, such as warnings about temperature and voltages, over-current fault conditions or status is available in the EVENT and STATUS registers. The nIRQ output is enabled via bit PG_PIN_EN.

The EVENT registers hold information about the events that have occurred. The conditions that are triggering the events are described in the individual event bit descriptions within the EVENT register tables, see Table 39 and Table 40. When an event bit is set the nIRQ signal is asserted, unless this event is masked by the appropriate MASK register.

The masked bits only mask the nIRQ assertion, they do not suppress the event generation. The nIRQ is not released until all event bits are cleared by writing a 1 to the appropriate EVENT register bits.

The assertion of the following conditions results in an nIRQ generation:

- OV_FAULT_EVENT
- UV_FAULT_EVENT
- OT_FAULT_EVENT
- OC_FAULT_EVENT
- WD_TO_EVENT
- PG_FAULT_EVENT
- CBOOT_OK_FAULT_EVENT
- CFLY_SHORT_FAULT_EVENT
- PVC_TIMER_FAULT_EVENT

The following status or events prevent the PVC from turning on:

- OV_FAULT_STATUS
- UV_FAULT_STATUS
- OT_FAULT_STATUS
- WD_TO_STATUS
- OV_FAULT_EVENT
- UV_FAULT_EVENT
- OT_FAULT_EVENT

The following faults disable the PVC:

- OV_FAULT_STATUS
- UV_FAULT_STATUS
- OT_FAULT_STATUS
- OC_FAULT_STATUS
- WD_TO_STATUS
- PG_FAULT_STATUS
- CBOOT_FAULT_STATUS
- CFLY_SHORT_FAULT_STATUS
- PVC_TIMER_FAULT_STATUS

6.3.10 AVDD Voltage Regulator

The 4 V power supply for internal analog / digital logic and control is generated from an internal regulator at pin AVDD. It is always enabled. Both V2X and V1X voltage power pins of the DA9389 are possible supplies. For voltages lower than $V_{THR\_SEL\_HI}$ the pin with the higher voltage is selected. For voltages rising above $V_{THR\_SEL\_HI}$ DA9389 switches its supply to the rail with the lower voltage and continues to use that supply until a voltage of $V_{THR\_SEL\_LO}$ or less is required. Providing the highest available supply voltage does not cause the AVDD regulator output, V_{AVDD}, to reach a voltage > V_{THR_UP}, DA9389 remains in OFF state. If $V_{AVDD} < V_{THR\_DWN}$, DA9389 enters OFF mode.

6.3.11 Internal Oscillator

The internal high-speed oscillator generates a signal at f_{OSC}, the internal clock reference. The high-speed oscillator is only enabled on demand.

6.4 EN_ONKEY

The EN_ONKEY pin is configured from OTP via the ONKEY_MODE bit. It can operate as a user power button or as a level sensitive IC_EN pin, which allows the DA9389 operation to be controlled from another device. Unless DA9389 is in OFF state, the EN_ONKEY input pin is always enabled to ensure that activities which should generate an application wake up or power down are always captured.

6.4.1.1 Onkey Power Button

When configured as a push button, the OTP setting of ONKEY_PU determines if pin EN_ONKEY is internally pulled to AVDD via resistance $R_{PU\_EN\_ONKEY}$. If enabled, the connected circuitry has to

withstand 4 V. A reduced control voltage with a high level down to $V_{IH\_EN\_ONKEY}$ may be implemented with external logic instead.

Wake Up

When DA9389 is in POWERDOWN state, a press of the EN_ONKEY pin triggers a transition to ACTIVE state. Subsequent de-asserting edges of EN_ONKEY following a wake up from POWERDOWN require a release of the external button and new assertion to generate a subsequent wake up.

Long Press

When DA9389 is in ACTIVE state, a long press of the EN_ONKEY triggers a power cycle, which results in the device entering ACTIVE or POWERDOWN state.

6.4.1.2 External IC Enable

The operation of the EN_ONKEY pin as an external IC enable (IC_EN) is configured in OTP via ONKEY_MODE. In this mode, the pin must be driven to AVDD or pulled to ground. If ONKEY_MODE is set to button mode, an automatic pull-up to AVDD can be enabled via ONKEY_PU. The level of the EN_ONKEY pin controls transitions between ACTIVE (EN_ONKEY = V_{AVDD}) and POWERDOWN (EN_ONKEY = 0 V) state. If ONKEY_MODE is set to IC_EN, an automatic pull-down can be enabled via IC_EN_PULLDOWN.

NOTE
During cold boot it is the responsibility of the external application to make sure that the level of EN_ONKEY is correct.

7 I²C Control Interface

The I²C interface is always enabled in ACTIVE and IOs are voltage compatible with 1.8 V and 3.3 V logic.

The I²C interface provides access to multiple control registers. The interface supports operations compatible to the Standard and Fast modes of the I²C-Bus Specification Rev. 6, [1].

Communication on the I²C bus is always between two devices; one acting as the master and the other as the slave.

7.1 I²C Communication

DA9389 has an OTP configurable 7-bit I²C slave address (default: 0x70) which can be configured in the register field I2C_SLAVE_ADDR.

Pin SCL transmits I²C clock data and SDA transmits the bidirectional data.

The I²C interface is open-drain supporting multiple devices on one line. The bus lines have to be pulled high by an external pull-up resistor (typically 20 kΩ). The attached devices drive the bus lines low by connecting them to ground. As a result, two devices can drive the bus simultaneously without conflict. The highest frequency of the bus is 1000 kHz. With asserted control I2C_TIMEOUT_EN an automatic interface RESET can be triggered when the clock signal ceases to toggle for > 35 ms (compatible with SMBus $t_{TIMEOUT}$).

When the SDA line is stuck (because of missing clock edges), the bus can be cleared by sending additional clock pulses. The PMIC does not use clock stretching and delivers read data without delay.

7.2 I²C Control Bus Protocol

All data is transmitted across the I²C bus in 8-bit groups. To send a bit, the SDA line is driven at the intended state while the SCL line is low. Once the SDA line has settled, the SCL line is brought high and then low. This pulse on the SCL lineclocks the SDA bit into the receiver's shift register.

DA9389 uses a 3-byte serial protocol which contains two bytes for the address and one byte for data. Data and address transfer transmits the MSB first for both read and write operations. All transmissions begin with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in high state. The START and STOP conditions are illustrated in Figure 7.

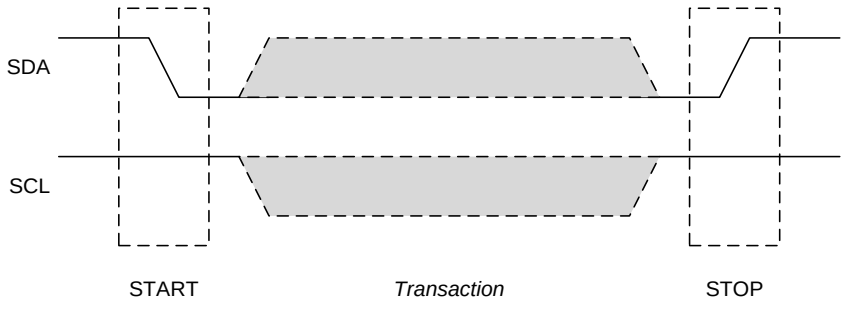


Figure 7: Timing of the START and STOP Conditions

The DA9389 monitors the I²C bus for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. The PMIC responds to all bytes with an ACK. A register write operation is illustrated in Figure 8.

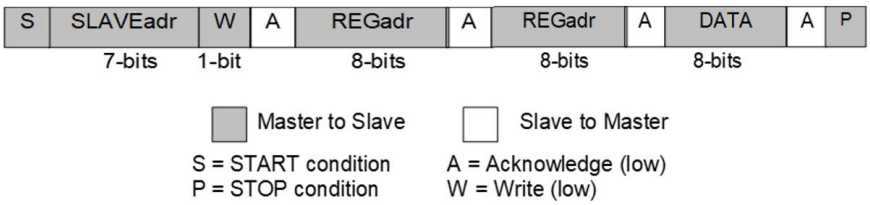


Figure 8: Byte Write Operation

When the host reads register data the slave has to access the target register address with write access and then with read access and a repeated START, or alternatively a second START, condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition, see Figure 9.

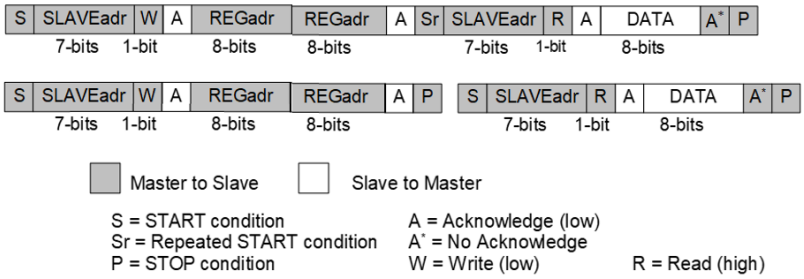


Figure 9: Examples of Byte Read Operations

8 Register Definitions

NOTE

The following register fields are password protected. I²C access is required to unlock those bits. Write 0x3D to address 0xB541. To lock those register fields, write any value to address 0xB541.

- PVC_CONFIG.CHARGE_DIRECTION
- PVC_CONFIG.FSW
- I2C_SLAVE_ADDR.I2C_SLAVE_ADDR
- I2C_SLAVE_ADDR.I2C_TIMEOUT_EN
- SYS_CONFIG_1.DIS_TIMER_RAMPUP_CFLY_CTL
- DCM_CTRL.EN_DCM_PSH
- DCM_CTRL.EN_DCM_DCM
- DCM_CTRL.EN_DCM_ULTRASONIC_VAL
- DCM_CTRL.DCM_SHYST_CONFIG_VAL
- DCM_CTRL.DCM_SKIP_PSK_CTL
- DCM_CTRL.EN_DCM_SPREAD_SPECTRUM
- PVC_CTRL.V1X_DISCH_OVR_VALUE
- PVC_CTRL.V1X_DISCH_OVR_EN
- CONFIG_ID.CONFIG_ID
- CONFIG_ID.VARIANT_ID

8.1 Register Map

Table 21: Register Map

Address	Register	Description
0x0002	STATUS_B	FSM and HW/SW modes
0x0003	REV_ID	Revision Code
0x0004	VENDOR_ID	Specific Vendor ID
0x0005	CONFIG_ID	Target application ID
0x000B	ONKEY_CONFIG_1	Onkey configuration byte 1
0x000C	ONKEY_CONFIG_2	Onkey configuration byte 2
0x000D	SYS_CONFIG_1	System configuration byte 1
0x000E	SYS_CONFIG_2	System configuration byte 2
0x000F	SYS_CONFIG_3	System configuration byte 3
0x0013	MASK_FAULT_CONFIG	Fault masking configuration 1
0x0014	MASK_FAULT_CONFIG_B	Fault masking configuration 2
0x0015	DISABLE_FAULT_CONFIG	Fault disable configuration 1
0x0016	DISABLE_FAULT_CONFIG_B	Fault disable configuration 2
0x0017	PVC_CONFIG	PVC configuration
0x0018	SYS_CTRL_1	POWERDOWN and SOFT_RESET assertion
0x001C	DCM_CTRL	PVC DCM configuration
0x001D	PVC_CTRL	PVC configuration 2
0x0022	PVC_EVENT	PVC events 1
0x0023	PVC_EVENT_B	PVC events 2
0x0024	PVC_STATUS	PVC status 1

Address	Register	Description
0x0025	PVC_STATUS_B	PVC status 2
0x0026	PVC_STATUS_C	PVC status 3
0x0027	EVENT_LOG	Event logger
0x0039	I2C_SLAVE_ADDR	I²C reset and slave address
0x003A	I2C_DEGLITCH	I²C pin deglitch selection and enable
0x0113	ANABIAS4	Comparator threshold settings 1
0x0114	ANABIAS5	Comparator threshold settings 2
0x0210	PROTECTION1	Power good comparator thresholds
0x0311	PROTECTION10	UV comparator thresholds
0x0312	PROTECTION11	OV comparator thresholds

8.2 Register Descriptions

Table 22: STATUS_B (0x0002)

Bit	Mode	Symbol	Description	Reset
5:2	RO	SYS_CTRL_STATE_READBACK	Readback Sys Ctrl FSM states 0x0: POWERDOWN 0x1: ACTIVE 0x2: FAULT_TIME 0x3: FAULT_RECOVERY 0x4-0x5: RESERVED 0x6: STANDBY 0x7-0x15: RESERVED	0x0

Table 23: REV_ID (0x0003)

Bit	Mode	Symbol	Description	Reset
7:4	RO	MAJREV	Major revision code	0xA
3:0	RO	MINREV	Minor revision code	0xD

Table 24: VENDOR_ID (0x0004)

Bit	Mode	Symbol	Description	Reset
7:0	RO OTP	VENDOR_ID	Specific vendor ID	0x0

Table 25: CONFIG_ID (0x0005)

Bit	Mode	Symbol	Description	Reset
7:2	R/W OTP	CONFIG_ID	ID for customer and target application platform, written during production of variant	0x0
1:0	R/W OTP	VARIANT_ID	Variant ID (part number)	0x0

Table 26: ONKEY_CONFIG_1 (0x000B)

Bit	Mode	Symbol	Description	Reset
6	R/W OTP	AUTO_FAULT_RECOVERY	This bit determines the auto start of the PVC in case of previous faults. 0x0: The host needs to clear all asserted events to allow the device to go back into ACTIVE state 0x1: No host intervention is required. The device will re-enable itself if the faults go away. The events are still held.	0x1
5	R/W OTP	FAULT_CYCLE	This bit determines the behaviour of the device after a fault caused the device to go out of ACTIVE state. 0x0: No OTP re-download triggered. After fault handling sequence, system proceeds to STANDBY 0x1: After fault handling sequence, a soft reset is triggered to the system. Registers will reset and OTP will download before system goes to STANDBY state	0x1
4	R/W OTP	AUTO_BOOT	AUTO_BOOT selection 0x0: The cold boot from OFF stops in POWERDOWN state. An EN_ONKEY press is needed to move to ACTIVE state 0x1: The cold boot from OFF ends in ACTIVE state	0x1
3	R/W OTP	IC_EN_PULLDOWN	IC_EN pull-down enable 0x0: No internal pull-down for pin IC_EN (EN_ONKEY) 0x1: Automatic pull-down enabled for pin IC_EN (EN_ONKEY)	0x0
2	R/W OTP	ONKEY_MODE	nONKEY mode 0x0: Button mode (pin operates as edge sensitive, active low, user button and follows corresponding time values) 0x1: IC_EN mode (operates as level driven IC Enable, where EN_ONKEY = AVDD puts chip in ACTIVE state, EN_ONKEY = 0 V puts chip into POWERDOWN state)	0x0
1	R/W OTP	ONKEY_PU	nONKEY pull-up enable 0x0: No internal pull-up for pin EN_ONKEY 0x1: Internal pull-up of pin EN_ONKEY to AVDD	0x1
0	R/W OTP	ONKEY_CYCLE	nONKEY power cycle 0x0: A power cycle initiated by long EN_ONKEY press stops in POWERDOWN state. An EN_ONKEY press is needed to move to ACTIVE state 0x1: A power cycle initiated by long EN_ONKEY press ends in ACTIVE state	0x1

Table 27: ONKEY_CONFIG_2 (0x000C)

Bit	Mode	Symbol	Description	Reset
6:4	R/W OTP	ONKEY_DEB	nONKEY debounce selection 0x0: no debounce 0x1: 0.125 ms 0x2: 1 ms 0x3: 10 ms 0x4: 30 ms 0x5: 250 ms 0x6: 500 ms 0x7: 750 ms	0x3
3:2	R/W OTP	ONKEY_KEY_DEL	nONKEY delay selection 0x0: 1 s 0x1: 1.5 s 0x2: 2 s 0x3: 7 s	0x0
1:0	R/W OTP	ONKEY_SHUT_DEL	nONKEY long press delay selection 0x0: Long press function disabled 0x1: ONKEY_KEY_DELAY + 4 s 0x2: ONKEY_KEY_DELAY + 5 s 0x3: ONKEY_KEY_DELAY + 6 s	0x0

Table 28: SYS_CONFIG_1 (0x000D)

Bit	Mode	Symbol	Description	Reset
4	R/W OTP	MODE	Switching mode 0x0: Auto mode 0x1: Fixed frequency switching mode	0x0
3	R/W OTP	EN_BYP	Enable control of BYPASS mode 0x0: Disabled 0x1: Enabled	0x0
2	R/W OTP	DIS_TIMER_RAMPUP_CFLY_CTL	Disable control of the ramp-up timer 0x0: Enable 0x1: Disable	0x0
0	R/W OTP	PG_PIN_EN	Enable control of power good indicator 0x0: nIRQ function 0x1: Power good indicator	0x0

Table 29: SYS_CONFIG_2 (0x000E)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	SPREAD_WIDTH	Spreading of oscillator frequency during spread spectrum 0x0: ±2 % 0x1: ±4 % 0x2: ±8 % 0x3: ±16 %	0x3

Bit	Mode	Symbol	Description	Reset
5	R/W OTP	SPREAD_EN	Spread spectrum enable 0x0: Disable 0x1: Enable	0x0
2:1	R/W OTP	WD_TIMER_SEL	Watchdog timeout selection 0x0: 5 s 0x1: 9 s 0x2: 17 s 0x3: 33 s	0x3
0	R/W OTP	WD_TIMER_EN	Watchdog timer enable in ACTIVE 0x0: Disabled 0x1: Enabled	0x0

Table 30: SYS_CONFIG_3 (0x000F)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	FAULT_TIME	FAULT_TIME selection 0x0: 0 ms 0x1: 10 ms 0x2: 100 ms 0x3: 500 ms	0x3

Table 31: MASK_FAULT_CONFIG (0x0013)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	MASK_OV_FAULT	Mask the over-voltage fault 0x0: Mask disabled 0x1: Mask enabled	0x0
6	R/W OTP	MASK_UV_FAULT	Mask the under-voltage fault 0x0: Mask disabled 0x1: Mask OV fault enabled	0x0
5	R/W OTP	MASK_OT_FAULT	Mask the over-temperature fault 0x0: Mask disabled 0x1: Mask OT fault enabled	0x0
4	R/W OTP	MASK_OC_FAULT	Mask the over-current fault 0x0: Mask disabled 0x1: Mask OC fault enabled	0x0
3	R/W OTP	MASK_CBOOT_FAULT	Mask the CBOOT fault 0x0: Mask disabled 0x1: Mask CBOOT fault enabled	0x0

Table 32: MASK_FAULT_CONFIG_B (0x0014)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	MASK_WD_TO_EVENT	Mask watchdog timeout event 0x0: Mask disabled 0x1: Mask watchdog timeout fault enabled	0x0

Bit	Mode	Symbol	Description	Reset
6	R/W OTP	MASK_SYS_RESET_EVENT	Mask SYS_RESET event 0x0: Mask disabled 0x1: Mask SYS RESET fault enabled	0x0
2	R/W OTP	MASK_PVC_TIMER_FAULT	Mask PVC TIMER fault 0x0: Mask disabled 0x1: Mask PVC TIMER fault enabled	0x0
1	R/W OTP	MASK_CFLY_SHORT_FAULT	Mask CFLY SHORT fault 0x0: Mask disabled 0x1: Mask CFLY SHORT fault enabled	0x0
0	R/W OTP	MASK_PG_FAULT	Mask PG fault 0x0: Mask disabled 0x1: Mask PG fault enabled	0x0

Table 33: DISABLE_FAULT_CONFIG (0x0015)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	DISABLE_OV_FAULT	Disable OV fault 0x0: Enable 0x1: Disable	0x0
6	R/W OTP	DISABLE_UV_FAULT	Disable UV fault 0x0: Enable 0x1: Disable	0x0
5	R/W OTP	DISABLE_OT_FAULT	Disable OT fault 0x0: Enable 0x1: Disable	0x0
4	R/W OTP	DISABLE_OC_FAULT	Disable OC fault 0x0: Enable 0x1: Disable	0x0
3	R/W OTP	DISABLE_CBOOT_FAULT	Disable CBOOT fault 0x0: Enable 0x1: Disable	0x0

Table 34: DISABLE_FAULT_CONFIG_B (0x0016)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	DISABLE_WD_TO_EVENT	Watchdog timeout fault disable 0x0: Enabled 0x1: Disabled	0x0
2	R/W OTP	DISABLE_CP_TIMER_FAULT	Disable PVC timer fault 0x0: Enable 0x1: Disable	0x0
1	R/W OTP	DISABLE_CFLY_SHORT_FAULT	Disable CFLY_SHORT fault 0x0: Enable 0x1: Disable	0x1
0	R/W OTP	DISABLE_PG_FAULT	Disable PG fault 0x0: Enable 0x1: Disable	0x0

Table 35: PVC_CONFIG (0x0017)

Bit	Mode	Symbol	Description	Reset
4	R/W OTP	PVC_EN	PVC enable 0x0: Disabled 0x1: Enabled	0x0
3:1	R/W OTP	FSW	PVC switching frequency 0x0: RESERVED 0x1: 200 kHz 0x2: 300 kHz 0x3: 375 kHz 0x4: 500 kHz 0x5: 600 kHz 0x6: 750 kHz 0x7: 1 MHz	0x2
0	R/W OTP	CHARGE DIRECTION	Charge direction 0x0: Divide/Forward mode 0x1: Multiply/Reverse mode	0x0

Table 36: SYS_CTRL_1 (0x0018)

Bit	Mode	Symbol	Description	Reset
5	R/W	POWERDOWN	Force POWERDOWN state when asserted from I^2C write. Automatically cleared from wake-up 0x0: POWERDOWN enabled 0x1: POWERDOWN not enabled	0x0
0	R/W	SOFT_RESET	When asserted, triggers a power cycle and a reset of all internal registers, followed by an OTP download 0x0: Not enabled 0x1: Enabled	0x0

Table 37: DCM_CTRL (0x001C)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	EN_DCM_PSH	Phase shedding enable 0x0: Disable 0x1: Enable	0x0
6	R/W OTP	EN_DCM_DCM	DCM function enable 0x0: Disable 0x1: Enable	0x1
5	R/W OTP	EN_DCM_ULTRASONIC_VAL	Ultrasonic mode enable 0x0: Disable 0x1: Enable	0x0
4	R/W OTP	DCM_SHYST_CONFIG_VAL	DCM hysteresis section 0x0: 50 mA 0x1: 150 mA	0x0

Bit	Mode	Symbol	Description	Reset
3	R/W OTP	DCM_SKIP_PSK_CTL	DCM behavior control 0x0: Pulse extend mode 0x1 Pulse skip mode	0x0
1	R/W OTP	EN_DCM_SPREAD_SPECTRUM	DCM spread spectrum enable 0x0: Disable 0x1: Enable	0x0

Table 38: PVC_CTRL (0x001D)

Bit	Mode	Symbol	Description	Reset
1	R/W OTP	V1X_DISCH_OVR_EN	V1X discharge override enable 0x0: Disabled 0x1: Enabled	0x0
0	R/W OTP	V1X_DISCH_OVR_VALUE	V1X discharge override value. This bit is active when bit [0] is high 0x0: Disabled 0x1: Enabled	0x0

Table 39: PVC_EVENT (0x0022)

Bit	Mode	Symbol	Description	Reset
7	RW1C	OV_FAULT_EVENT	Over-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
6	RW1C	UV_FAULT_EVENT	Under-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
5	RW1C	OT_FAULT_EVENT	Over-temperature event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
4	RW1C	OC_FAULT_EVENT	Over-current event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
3	RW1C	CBOOT_FAULT_EVENT	V_{CBSx} voltage is not high enough to drive power FET gate 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0

Table 40: PVC_EVENT_B (0x0023)

Bit	Mode	Symbol	Description	Reset
7	RW1C	WD_TO_EVENT	Event to indicate that the watchdog timer has expired. 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
6	RW1C	SYS_RESET_EVENT	Event to indicate that the system has undergone a reset (POR or I2C triggered). This is not a fault. 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0

Bit	Mode	Symbol	Description	Reset
2	RW1C	PVC_TIMER _FAULT_EVENT	Indicates a PVC timer fault event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
1	RW1C	CFLY_SHORT_FAULT_EVENT	Indicates a PVC CFLY short fault event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
0	RW1C	PG_FAULT_EVENT	Power good signal fault in SWITCHING state (Multiply and Divide modes) or BYPASS state (Forward and Reverse modes). 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear.	0x0

Table 41: PVC_STATUS (0x0024)

Bit	Mode	Symbol	Description	Reset
7	RO	OC_FAULT_STATUS	OC fault status 0x0: No fault 0x1: Indicates an over-current condition	0x0
6	RO	OV_FAULT_STATUS	OV fault status 0x0: No fault 0x1: Indicates an over-voltage condition	0x0
5	RO	UV_FAULT_STATUS	UV fault status 0x0: No fault 0x1: Indicates an under-voltage condition	0x0
4	RO	OT_FAULT_STATUS	OT fault status 0x0: No fault 0x1: Indicates an over-temperature condition	0x0
3	RO	CBOOT_FAULT_STATUS	CBOOT fault status 0x0: No fault 0x1: Indicates CBOOT fault is active	0x0

Table 42: PVC_STATUS_B (0x0025)

Bit	Mode	Symbol	Description	Reset
7	RO	WD_TO_STATUS	Indicates a watchdog timeout fault 0x0: No fault 0x1: Fault	0x0
2	RO	PVC_TIMER_FAULT_STATUS	Indicates a PVC timeout fault 0x0: No fault 0x1: Fault	0x0
0	RO	PG_FAULT_STATUS	Indicates a fault when the PVC is in SWITCHING state or in BYPASS state and at least one of the comparators is de-asserted. 0x0: No fault 0x1: Fault	0x0

Table 43: PVC_STATUS_C (0x0026)

Bit	Mode	Symbol	Description	Reset
7	RO	NIRQ	Reflects the status of the PG / nIRQ pin 0x0: NIRQ 0x1: PG	0x0
6	RO	CHARGING_STATUS	Indicates the Multiply mode state 0x0: Multiply is off 0x1: Multiply in on	0x0
5	RO	PVC_EN_STATUS	PVC enable (final control going to PVC) 0x0: PVC not enabled 0x1: PVC enabled	0x0
4	RO	SWITCHING_STATUS	Indicates if PVC is in SWITCHING or BYPASS state 0x0: BYPASS state (Forward or Reverse) 0x1: SWITCHING state (Divide or Multiply)	0x0
3	RO	DIRECTION_STATUS	Indicates the direction of operation 0x0: Forward mode 0x1: Reverse mode	0x0

Table 44: EVENT_LOG (0x0027)

Bit	Mode	Symbol	Description	Reset
7:4	RO	RESERVED		0x0
3:0	RO	FIRST_EVENT_LOG	First event logger 0x0: RESERVED 0x1: PVC_TIMER_EVENT 0x2: CFLY_SHORT_EVENT 0x3: OT_FAULT_EVENT 0x4: UV_FAULT_EVENT 0x5: OV_FAULT_EVENT 0x6: OC_FAULT_EVENT 0x7: CBOOT_OK_FAULT_EVENT 0x8: PG_FAULT_EVENT 0x9-0x13: RESERVED 0x14: WD_TIMEOUT_FAULT_EVENT 0x15: RESERVED	0x0

Table 45: I2C_SLAVE_ADDR (0x0039)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	I2C_TIMEOUT_EN	Enable automatic reset of I^2C interface (if BYP / SCL pin stays low for greater than 35 ms) 0x0: I^2C timeout disabled 0x1: I^2C timeout enabled	0x0
6:0	R/W OTP	I2C_SLAVE_ADDR	7-bit I^2C Slave address. Default is 7'h70. If user wants to change I^2C Slave ID, overwrite the I^2C Slave ID as last register to program before OTP program, so that other register writes will not be affected.	0x70

Table 46: I2C_DEGLITCH (0x003A)

Bit	Mode	Symbol	Description	Reset
1	R/W OTP	I2C_DEGLITCH_EN	Enable deglitch on I^2C pins 0x0: Disabled 0x1: Enabled	0x1
0	R/W OTP	I2C_DEGLITCH_SEL	Deglitch time for I^2C pins 0x0: 50 ns 0x1: 10 ns	0x1

Table 47: ANABIAS4 (0x0113)

Bit	Mode	Symbol	Description	Reset
7:5	R/W OTP	SEL_OCP	V2X over-current protection comparator threshold (per phase) in Divide mode 0x0: 3250 mA 0x1: 3500 mA 0x2: 3750 mA 0x3: 4000 mA 0x4: 4250 mA 0x5: 4500 mA 0x6: 4750 mA 0x7: 5000 mA	0x2
4:0	R/W OTP	RESERVED		0x1B

Table 48: ANABIAS5 (0x0114)

Bit	Mode	Symbol	Description	Reset
2:0	R/W OTP	SEL_OCP_BYPASS	V2X over-current protection comparator threshold in BYPASS state 0x0: 3250 mA 0x1: 3500 mA 0x2: 3750 mA 0x3: 4000 mA 0x4: 4250 mA 0x5: 4500 mA 0x6: 4750 mA 0x7: 5000 mA	0x7

Table 49: PROTECTION1 (0x0210)

Bit	Mode	Symbol	Description	Reset
7:5	R/W OTP	SEL_PG_POS (SELPG1)	Threshold selection in Divide mode to progress from current-limited start up to normal PVC operation 0x0: 100 mV 0x1: 150 mV 0x2: 200 mV 0x3: 250 mV 0x4: 300 mV 0x5: 350 mV 0x6: 400 mV 0x7: 450 mV	0x5
4:2	R/W OTP	SEL_PG_NEG (SELPG2)	Threshold selection in Multiply mode to progress from current-limited start up to normal PVC operation 0x0: 100 mV 0x1: 150 mV 0x2: 200 mV 0x3: 250 mV 0x4: 300 mV 0x5: 350 mV 0x6: 400 mV 0x7: 450 mV	0x5

Table 50: PROTECTION10 (0x0311)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	SEL_UVP	UV threshold selection 0x0: V2X_UVP = 3.8 V, V1X_UVP = 2.4 V, FBYP_UVP = 3.8 V, RBYP_UVP = 3.3 V 0x1: V2X_UVP = 4.0 V, V1X_UVP = 2.7 V, FBYP_UVP = 4.0 V, RBYP_UVP = 3.3 V 0x2: V2X_UVP = 4.2 V, V1X_UVP = 3.0 V, FBYP_UVP = 4.2 V, RBYP_UVP = 3.3 V 0x3: V2X_UVP = 4.4 V, V1X_UVP = 3.3 V, FBYP_UVP = 4.4 V, RBYP_UVP = 3.3 V	0x0
5:0	R/W OTP	SEL_UVP_HYS	UV hysteresis selection 0x0: 50 mV 0x1: 100 mV 0x2: 150 mV 0x3: 200 mV	0x0

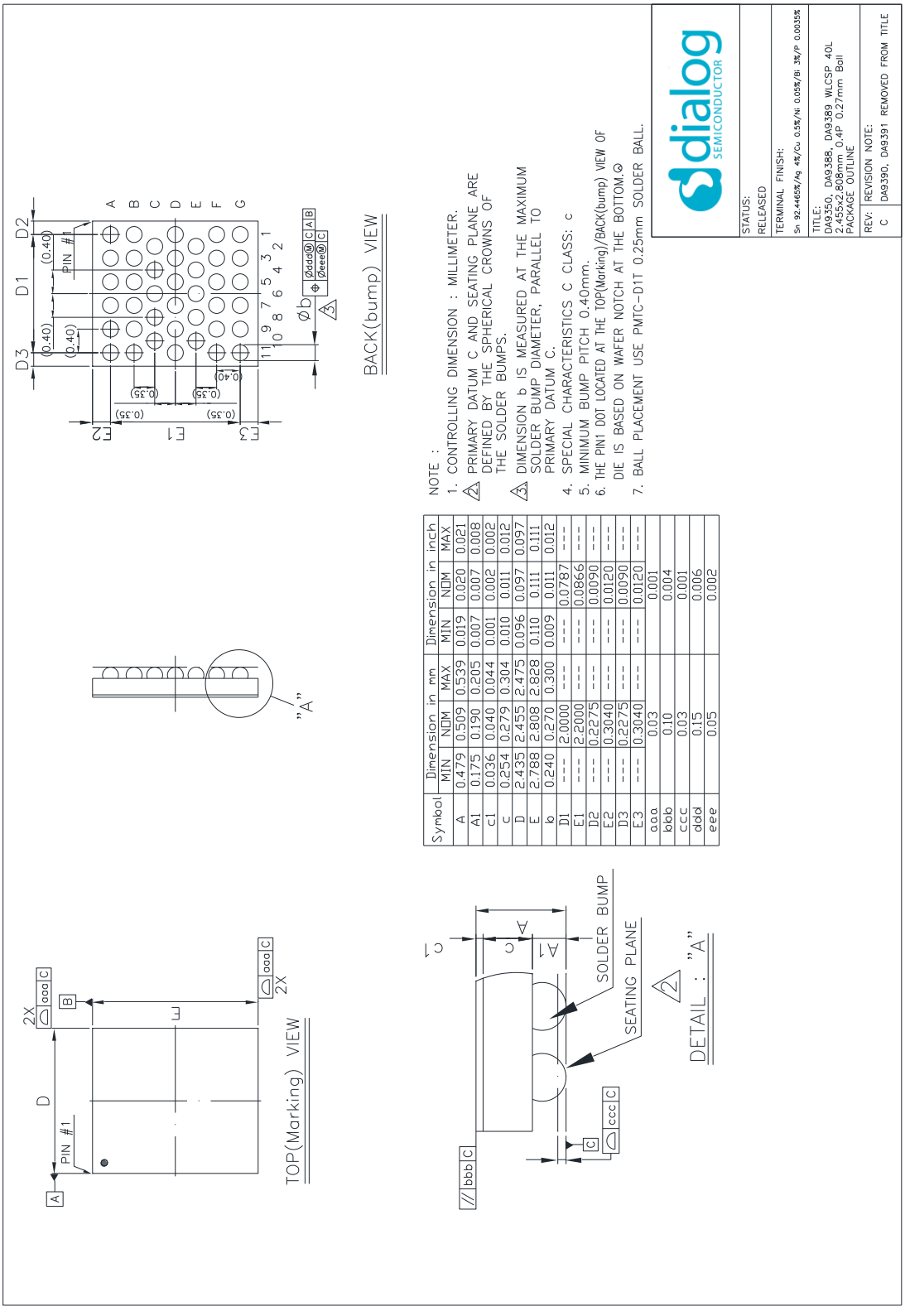
Table 51: PROTECTION11 (0x0312)

Bit	Mode	Symbol	Description	Reset
2	R/W OTP	EN_DCM_OVP	OVP enable in DCM mode 0x0: Disable 0x1: Enable	0x1

Bit	Mode	Symbol	Description	Reset
6:5	R/W OTP	SEL_OVP_MUL	OV threshold selection Multiply mode 0x0: V1X OVP = 6 V 0x1: V1X OVP = 6.5 V 0x2: V1X OVP = 7 V 0x3: V1X OVP = 7.5 V	0x3
4:3	R/W OTP	SEL_OVP	OV threshold selection in Forward mode (Divide and BYPASS) and Reverse BYPASS mode 0x0: V2X OVP = 12 V, FBYP V2X OVP = 6 V, RBYP V1X OVP = 6 V 0x1: V2X OVP = 13 V, FBYP V2X OVP = 6.5 V, RBYP V1X OVP = 6.5 V 0x2: V2X OVP = 14 V, FBYP V2X OVP = 7 V, RBYP V1X OVP = 7 V 0x3: V2X OVP = 15 V, FBYP V2X OVP = 7.5 V, RBYP V1X OVP = 7.5 V	0x3

9 Package Information

9.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.479	0.509	0.539	0.019	0.020	0.021
A1	0.175	0.190	0.205	0.007	0.007	0.008
c1	0.036	0.040	0.044	0.001	0.002	0.002
c	0.254	0.279	0.304	0.010	0.011	0.012
D	2.435	2.455	2.475	0.096	0.097	0.097
E	2.788	2.808	2.828	0.110	0.111	0.111
b	0.240	0.270	0.300	0.009	0.011	0.012
D1	---	2.0000	---	---	0.0787	---
E1	---	2.2000	---	---	0.0866	---
D2	---	0.2275	---	---	0.0090	---
E2	---	0.3040	---	---	0.0120	---
D3	---	0.2275	---	---	0.0090	---
E3	---	0.3040	---	---	0.0120	---
aaa		0.03			0.001	
bbb		0.10			0.004	
ccc		0.03			0.001	
ddd		0.15			0.006	
eee		0.05			0.002	

Figure 10: WLSCP Package Outline Drawing

9.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 52.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The WLCSP package is qualified for MSL 1.

Table 52: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

9.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

9.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

10 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 53: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9389-xxOQ2	WLCSP40	2.455 x 2.808 x 0.509	Tape and reel	7500
DA9389-xxOQ6	WLCSP40	2.455 x 2.808 x 0.509	Waffle tray	TBD

Part Number Legend:

DA9389-xxOQ2

xx: OTP variant

11 Application Information

11.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all input and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 54: Recommended Capacitor Types

Application	Value	Size	Temp Char	Tol (%)	Rated (V)	Type
C_{FLY1} / C_{FLY2}	47 µF	0603	X5R ±15 %	±20	6.3	Murata GRM188R60J476ME15
	2x 47 µF	0603	X5R ±15 %	±20	6.3	Murata GRM188R60J476ME15
	22 µF	0603	X5R ±15 %	±20	10	Murata GRM187R61A226ME15#
	2x 22 µF	0603	X5R ±15 %	±20	10	Murata GRM187R61A226ME15#
C_{V1X}	4.7 µF	0402	X5R ±15 %	±20	10	Murata GRM155R61A475MEAA
C_{V2X}	4.7 µF	0402	X5R ±15 %	±20	16	Murata GRM155R61C475ME15
C_{BS1}, C_{BS2}	100 nF	0201	X5R ±15 %	±20	16	Murata GRM033R61C104ME18
C_{AVDD}	2.2 µF	0402	X5R ±15 %	±20	6.3	Murata GRM155R60J225ME95

11.2 PCB Layout

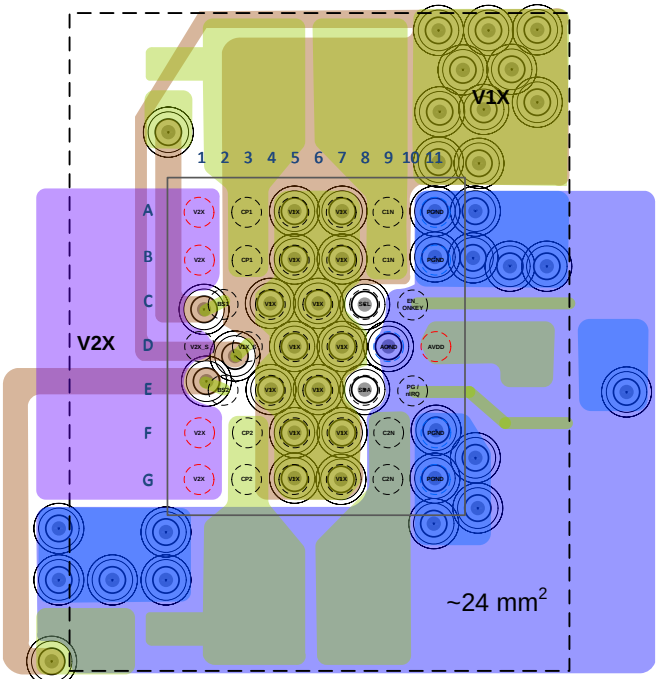


Figure 11: PCB Solution Size

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via http://www.renesas.com/.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Important Notice and Disclaimer

(Rev.1.0 Mar 2020)

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https://www.renesas.com/contact/