DAC-10
10-Bit High Speed Multiplying D/A Converter

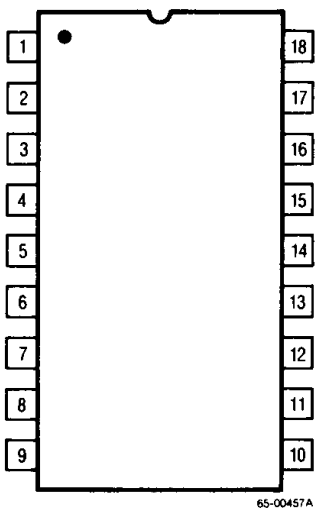
Features
- Nonlinearity to 0.05% max over temperature range
- Low full scale drift — 10ppm/°C
- Wide range multiplying capability — 1.0MHz bandwidth
- Wide power supply range — +5.0V/-7.5V to ±18V
- Two quadrant multiplying
- High output compliance
- High speed — 85nS

Applications
- A/D converters
- Servo controls
- Waveform generators
- Programmable power supplies
- High Speed Modems

Description
The DAC-10 is a high speed, 10-bit, monolithic, multiplying Digital-to-Analog Converter. Settling times of 85nS are achieved with low power consumption and minimal output glitches. Full scale (10-bit) accuracy is achieved. The DAC-10 can be operated from almost any logic level input due to its adjustable (V_{LC}) threshold. Monotonicity is guaranteed to 10 bits and nonlinearities of ±0.05% are guaranteed over the full operating temperature range. Power consumption can be reduced to 85mW by lowering supply voltages to +5.0V to -7.5V. Operation at supply voltages up to ±18V does not appreciably affect device performance. Zener-Zap trimming is performed at wafer probe to optimize the converter's accuracy.

Connection Information

18-Lead Hermetic Dual In-Line
(Top View)



Pin	Function
1	V_{LC} Trim
2	$\overline{I_O}$
3	$-V_S$
4	I_O
5	MSB B1
6	B2
7	B3
8	B4
9	B5
10	B6
11	B7
12	B8
13	B9
14	B10 LSB
15	$+V_S$
16	$V_{REF(+)}$
17	$V_{REF(-)}$
18	Comp

Absolute Maximum Ratings

Operating Temperature Range
- DAC-10BD, CD ..... -55°C to +125°C
- DAC-10FD, GD ..... 0°C to +70°C

Storage Temperature Range ..... -65°C to +150°C

Lead Soldering Temperature (60 Sec) ..... +300°C

Supply Voltage ($+V_S$ to $-V_S$) ..... +36V

Logic Inputs ..... $-V_S$ to $-V_S$ plus 36V

V_{LC} ..... $-V_S$ to $+V_S$

Analog Current Outputs ..... $-V_S$ to $+V_S$

Reference Inputs (V_{16} to V_{17}) ..... $-V_S$ to $+V_S$

Reference Input Differential Voltage (V_{16} to V_{17}) ..... ±18V

Reference Input Current (I_{16}) 2.5mA

Ordering Information

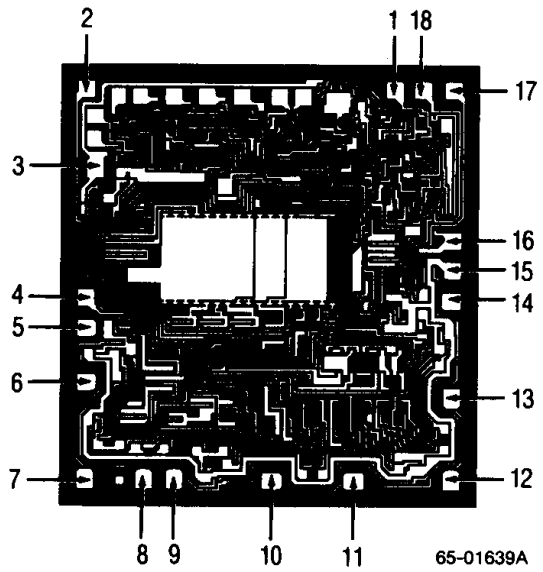
Part Number	Package	Operating Temperature Range	Non-linearity
DAC-10FD	D	0°C to +70°C	±0.05%
DAC-10GD	D	0°C to +70°C	±0.01%
DAC-10BD	D	-55°C to +125°C	±0.05%
DAC-08BD/883B	D	-55°C to +125°C	±0.05%
DAC-08CD	D	-55°C to +125°C	±0.05%
DAC-08CD/883B	D	-55°C to +125°C	±0.05%

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D =18-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	18-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θJA	120°C/W
For T_A >50°C Derate at	8.38 mW/°C

Mask Pattern



Die Size: 94 x 100 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-10B, DAC-10C, $0°C \leq T_A \leq +70°C$ for DAC-10F, DAC-10G. Output characteristics apply to both I_O and $\overline{I_O}$ unless otherwise specified.)

Parameters	Test Conditions	DAC-10B/F			DAC-10C/G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB		-5.5 +10			-5.5 +10		V
Gain Temperature Coefficient	See Note		±10	±25		±10	±50	ppm/°C
Full Scale Current	$V_{REF} = 10.000V$ $R_{16} = R_{17} = 5.000k\Omega$	3.968	3.996	4.024	3.936	3.996	4.056	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		1.0	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Reference Input Slew Rate	$R_{EQ} = 200\Omega$, $C_C = 0$		6.0			6.0		mA/μS
Power Supply Sensitivity Positive	$+4.5V \leq +V_S \leq +18V$		0.001	0.01		0.001	0.01	$\%\Delta_{FS}/\%\Delta V$
Negative	$-18V \leq -V_S \leq -10V$		0.0012	0.01		0.0012	0.01	
Supply Current Positive	$V_S = \pm 15V$		2.3	4.0		2.3	4.0	mA
Negative	$I_{REF} = 2.0mA$		9.0	15		9.0	15	
Positive	$V_S = +5.0V/-7.5V$;		1.8	4.0		1.8	4.0	
Negative	$I_{REF} = 1.0mA$		5.9	9.0		5.9	9.0	
Power Consumption	$V_S = \pm 15V$ $I_{REF} = 2.0mA$		231	276		231	276	mW
	$V_S = +5.0V/-7.5V$; $I_{REF} = 1.0mA$		85	107		85	107	
Logic Input Levels Low	$V_{LC} = 0$			0.8			0.8	V
High		2.0			2.0			
Logic Input Currents Low	$V_{LC} = 0$; $-5.0V \leq V_{IN} \leq +0.8V$	-10	-5.0		-10	-5.0		μA
High	$+2.0V \leq V_{IN} \leq +18V$		0.001	10		0.001	10	

Note: Guaranteed by Design.

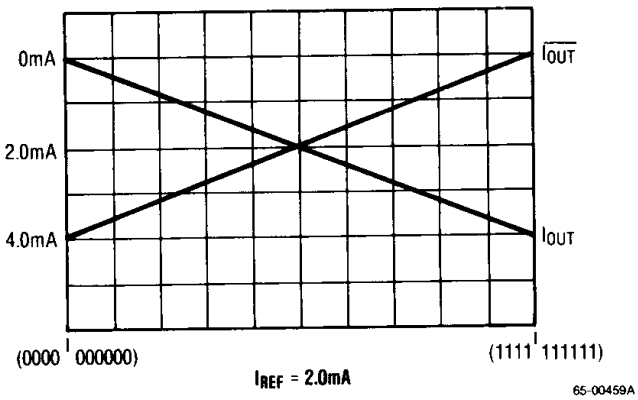
Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$; $T_A = +25°C$, unless otherwise noted. Output characteristics apply to both I_O and $\overline{I_O}$.)

Parameters	Test Conditions	DAC-10B/C/F			DAC-10G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB	-5.0	-6/+18	+10	-5.0	-6/+15	+10	V
Full Scale Current	V_{REF} = 10.000V, $R_{16} = R_{17}$ = 5.000kΩ	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		0.1	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Settling Time	All Bits Switched ON or OFF Settle to 0.05% of FS See Note		85	135		85	150	nS
Output Capacitance			18			18		pF
Propagation Delay	R_L = 5.0kΩ		50			50		nS

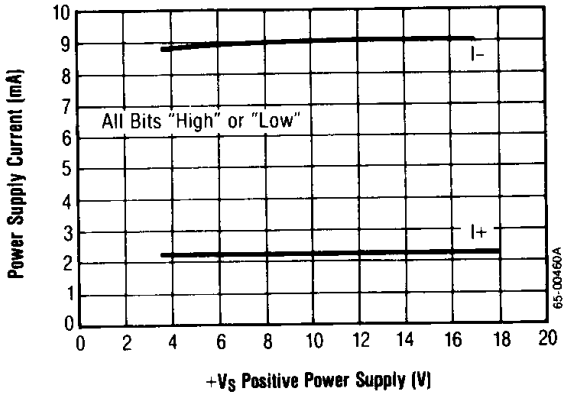
Note: Guaranteed by Design

Typical Performance Characteristics

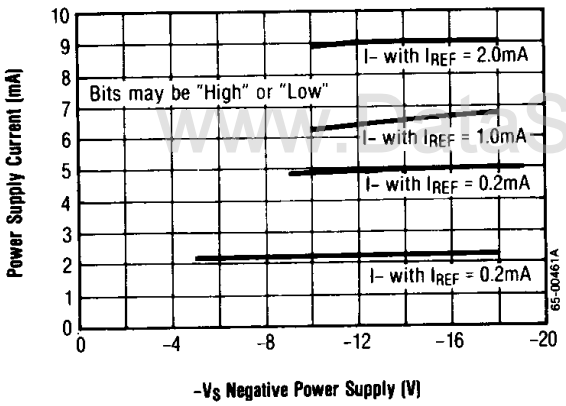
True and Complementary Output Operations



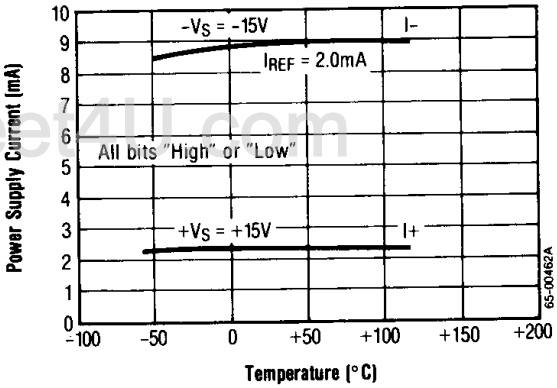
Power Supply Current vs. $+V_S$



Power Supply Current vs. $-V_S$



Power Supply Current vs. Temperature



Propagation and Settling Time

Propagation delays from logic input to analog outputs are typically less than 35nS. Settling times and propagation delays are relatively insensitive to logic input amplitude, power supply voltage or reference current. However, larger reference currents allow for the use of smaller output resistors. This reduces the degradation of speed that occurs due to the DACs output capacitance.

The settling time circuit (Figure 1) yields the optimal settling time that can achieved (85nS). However, in real applications the settling time will be somewhat degraded from ideal. The following applications indicate circuits and settling times for commonly used applications.

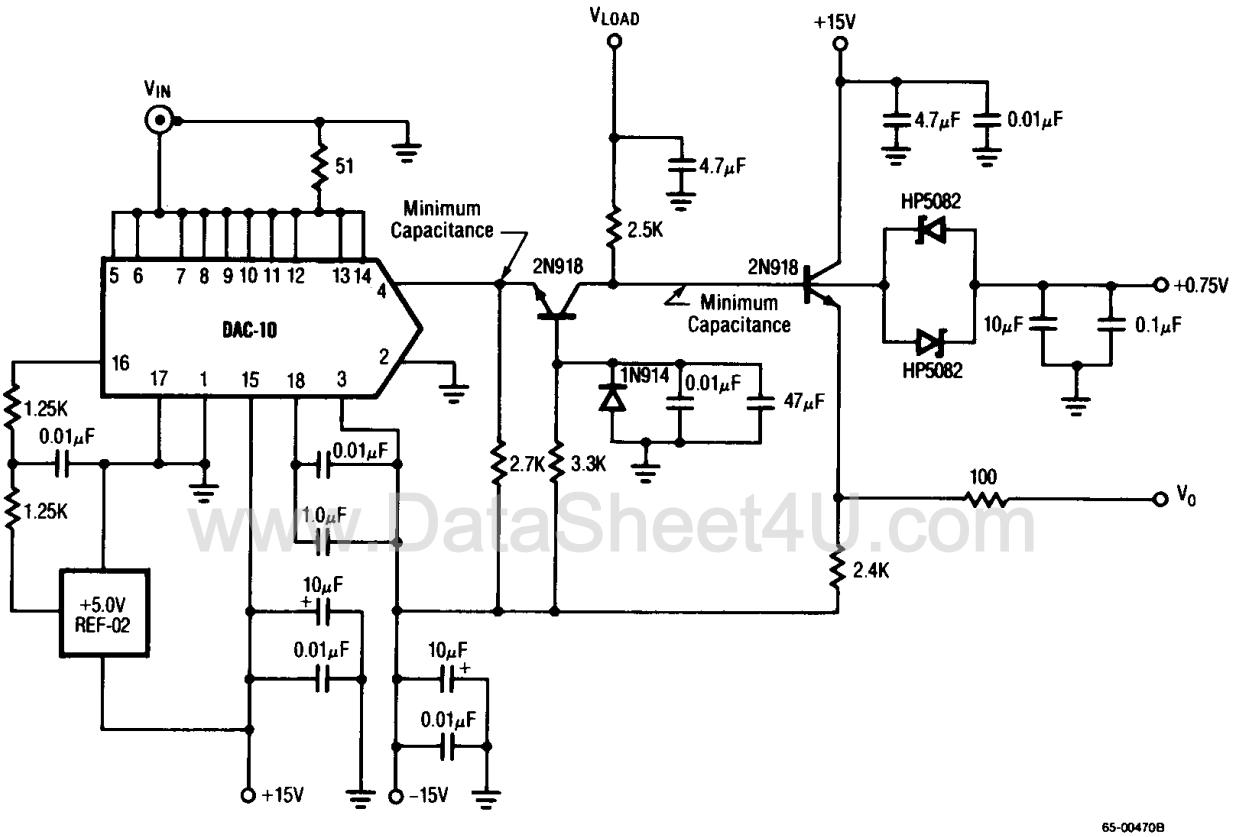


Figure 1. Settling Time Test Fixture

Applications

Output Currents

The analog output currents consist of both true and complemented output sink currents. The sum of the true and complemented currents is always equal to the full scale output current. Full scale output current (I_{FS}) is related to the input reference current by the equation:

$$I_{FS} = 1023/1024 \times 2I_{REF}$$

Input coding of either positive true binary or complementary binary is allowed. The difference of the two output currents is a linear function of the binary input. This feature results in some useful DAC applications where differential outputs are desired, such as differential line driving or digital offset nulling of op amps.

Input Reference

The output current of the DAC-10 is the product of the binary input and the input reference current. The output current is twice the input reference current, defined by the equation:

$$I_O = D/1024 \times 2I_{REF}$$

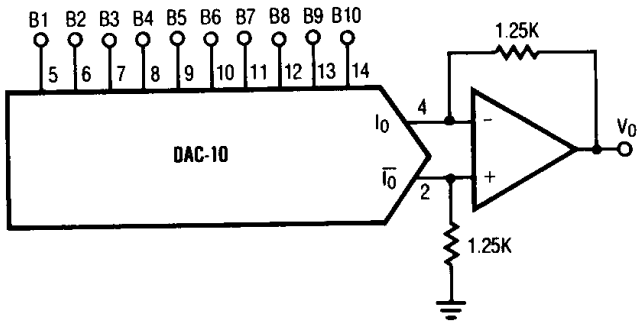
Where I_{REF} is the input reference current into pin 16 and D represents the value of the binary input.

The voltage reference may either be postive or negative. A positive reference is used to force current into pin 16 through bias resistor R16. A negative reference is used to force the voltage at pin 17 negative. The high gain reference amplifier will cause pin 16 to follow pin 17 and again force current into pin 16. The bias resistor is always the resistor in series with pin 16 even when a negative reference is used. Either pin 16 or pin 17 may be offset to accommodate bipolar references.

Noise from the reference supply is reflected into the output. Since the noise output of a reference is directly proportional to bandwidth, the bandwidth must be restricted. A center tapped bias resistor serves as a simple one pole roll-off filter to minimize the effects of wideband noise. A +5V regulated voltage is recommended, with the bias resistor to pin 16 split into two equal resistors having the junction bypassed to ground with a 0.25μF capacitor. A typical +5V bandgap reference (REF-02) puts out a wideband noise voltage of 1 to $2mV_{p-p}$ at the full 10MHz bandwidth. For a multiplying DAC this voltage is transmitted directly to the output such that, for a +5V output system (LSB = 5.0mV) this amount of noise is significant. The simple filter suggested here restricts the noise bandwidth to 1/4RC. For a bias resistor of 1.25kΩ and a bypass capacitor of 0.25μF the noise bandwidth can be reduced to 800Hz and the noise voltage reduced to approximately $80\mu V_{p-p}$, a significant reduction. The +5V TTL supply should **never** be used for a DAC reference.

High Speed Multiplying Applications

For high speed multiplying applications the transient behavior of the input reference amplifier deserves special consideration. The reference amplifier is compensated with a capacitor from pin 18 to the negative supply. The size of this



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	+4.995
Pos Full Scale -LSB	1 1 1 1 1 1 1 1 1 0	+4.985
(+) Zero Scale	1 0 0 0 0 0 0 0 0 0	+0.005
(-) Zero Scale	0 1 1 1 1 1 1 1 1 1	-0.005
Neg Full Scale +LSB	0 0 0 0 0 0 0 0 0 1	-4.985
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	-4.995

65-00463A

Figure 2. Bipolar Operation

capacitor is a function of the equivalent driving impedance to pin 16. The larger the driving impedance, the larger the capacitor that is required to maintain an adequate phase margin. Although exact mathematical models of the compensated reference amplifier are somewhat involved, it has been established empirically that the compensating capacitor should never be smaller than 15pF per kΩ of driving impedance.

Finally, for a driving point impedance less than 800Ω the compensating capacitor is no longer required. The Pulsed Reference Operation panel shows how to compute driving point impedance R_{EQ}. In general the smaller R_{EQ} the faster the response. The output current will slew at 6.0mA per μS when no compensation capacitor is required.

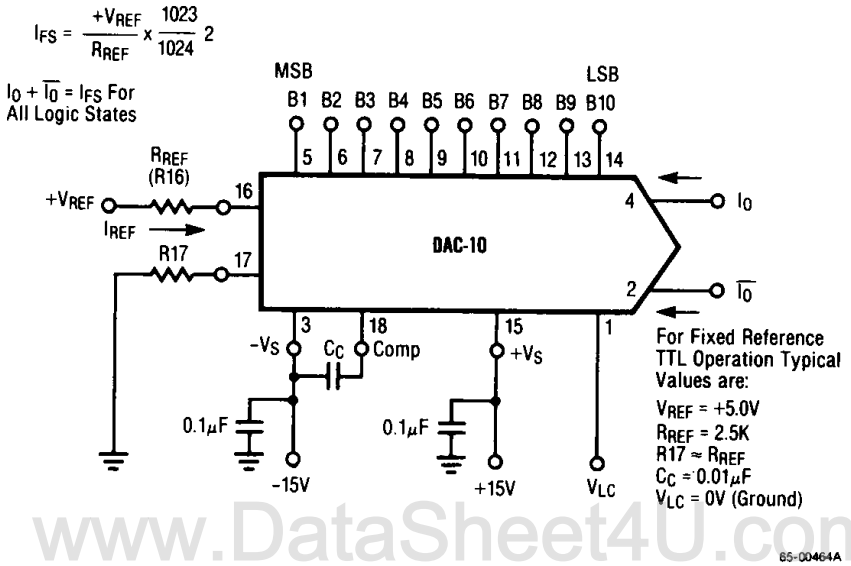


Figure 3. Positive Reference Operation

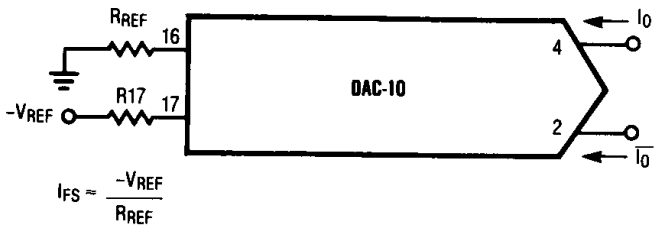


Figure 4. Negative Reference Operation

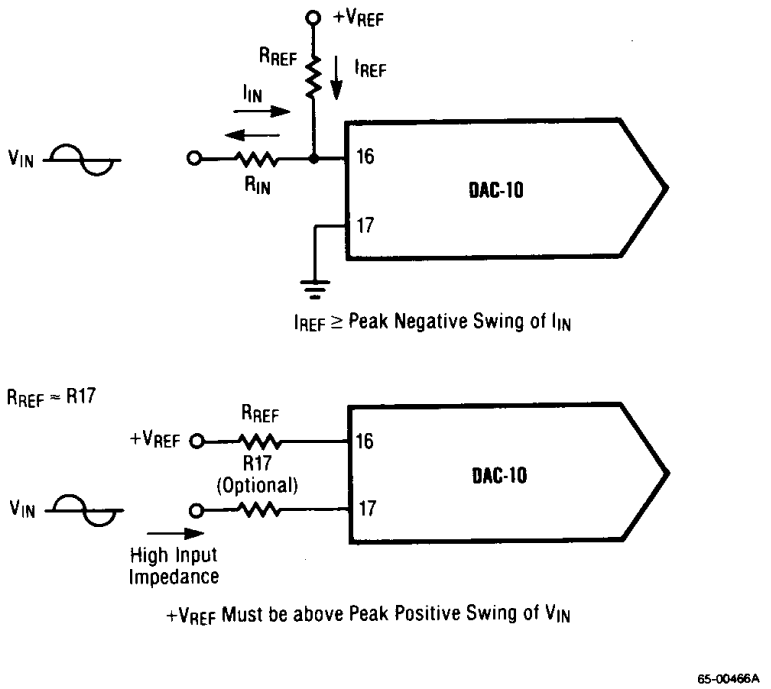


Figure 5. Providing Offsets to Accommodate Bipolar References

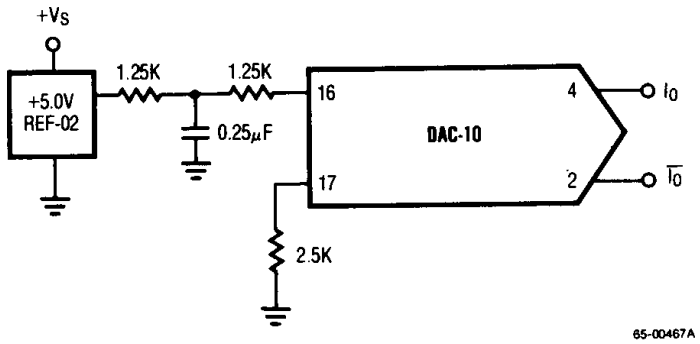


Figure 6. Input Reference Noise Limiting Filter

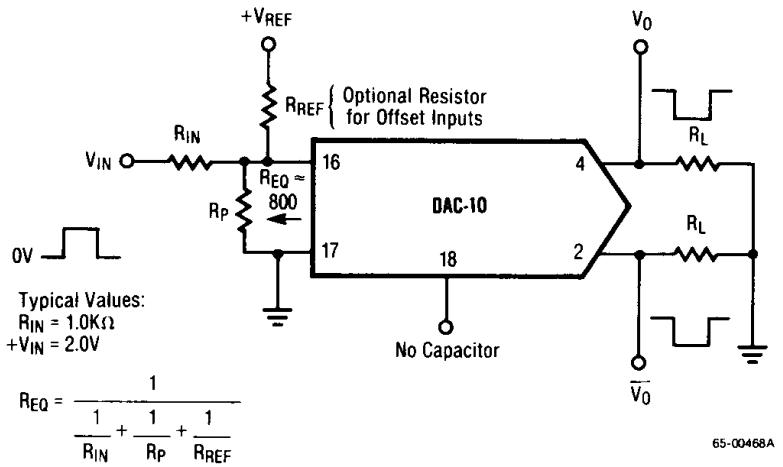


Figure 7. Pulsed Reference Operation

Analog-to-Digital Conversion

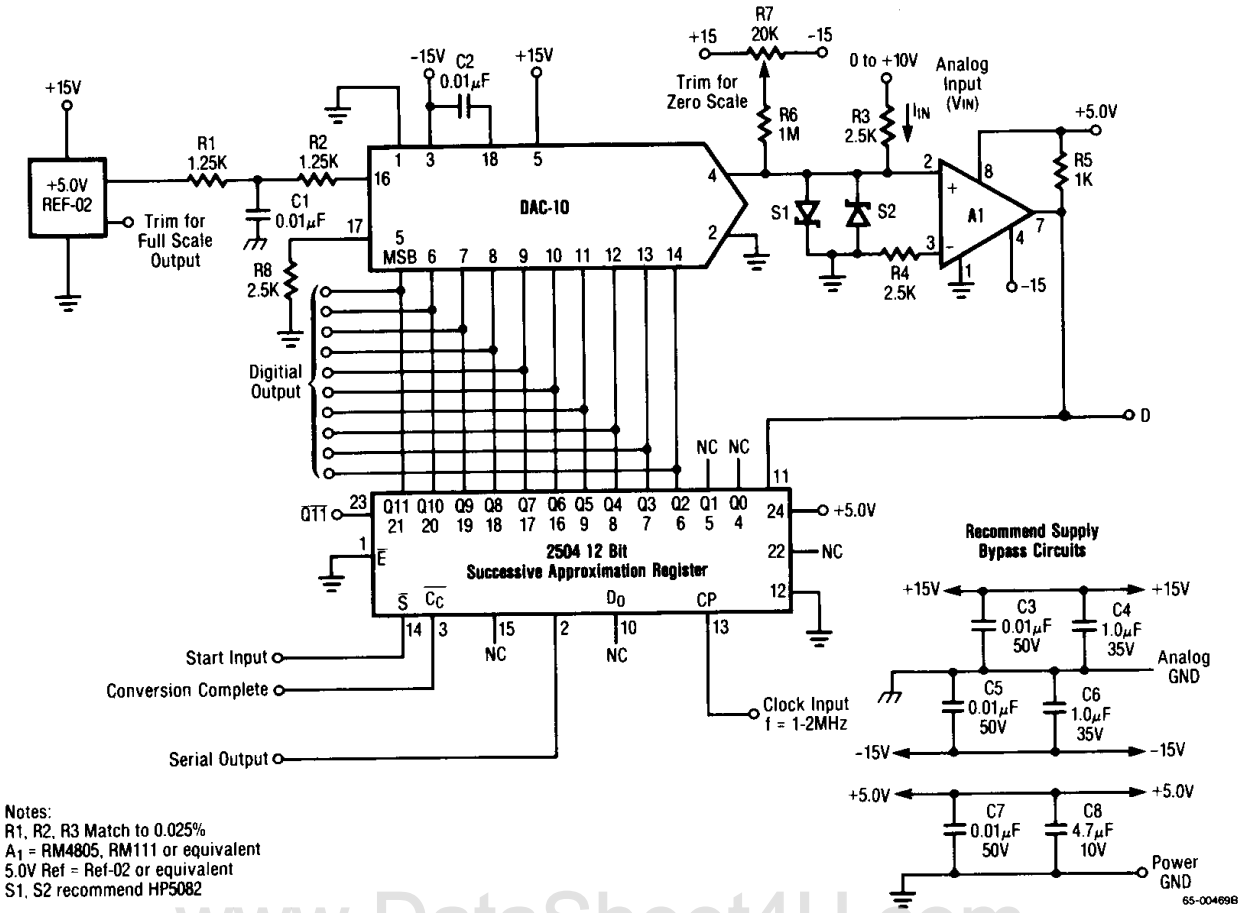
Successive approximation is a logical method of measuring an analog quantity using binary weighted approximation. For example, to measure an unknown weight using a balance scale, the weight is placed on one side of the balance and counterweights are placed on the other side until the scale is balanced. The number of "trials" is made equal to the number of counterweights by starting with the heaviest counterweight first, and either retaining it or rejecting it based on a comparison with the unknown weight. This process is repeated for each weight from heaviest to lightest until all weights have been tried.

By interfacing the DAC-10 with a commercially available successive approximation register (SAR) such as the DM2504 (Figure 8), an analog-to-digital converter (ADC) can be built. The DM2504 register operates as follows.

The register is reset by holding the $\overline{S}$ (Start) input low during a clock (CP) low-to-high transition. After $\overline{S}$ is brought back high, the MSB output (Q11) will be set low and all the remaining register outputs (Q10 - Q12) will be set high, providing a trial binary number for the DAC. This binary number (0111111111) causes the DAC to generate an output current (I_O) which is one half of the full scale output.

I_O is constantly being compared to a current I_{IN}. I_{IN} is generated by the analog input voltage ($I_{IN} = V_{IN}/R_3$). If the first trial number generates an I_O greater than I_{IN}, then the comparator sends a logical zero signal to the SAR. On the next clock low-to-high transition the logical zero is latched into the MSB (Q11) output of the SAR. If the first trial number generates an I_O less than I_{IN}, then the comparator output will be high, and a logical one will be latched into the MSB output. This is a decision making process where the circuit determines, bit by bit, whether the code present on the SAR digital outputs is proportional to the input voltage. After the MSB is latched, the circuit will go through the same decision making process for the next most significant bit, deciding whether it should be latched high or low. The process is repeated successively for each bit until the least significant bit is latched. At this time control logic in the SAR will stop the conversion and signal completion by bringing the QCC output low. The circuit will then stay in its latched output state until conversion is again initiated by the start input.

Since a bit is decided for each clock low to high transition the maximum time needed for a complete conversion will be equal to twelve clock cycles. As each bit is generated it is also latched into the D_O output so that D_O can be used as a serial output. The last two bits will be invalid data because this system uses a 12 bit SAR and a 10 bit DAC.



Notes:
R1, R2, R3 Match to 0.025%
A_1 = RM4805, RM111 or equivalent
5.0V Ref = Ref-02 or equivalent
S1, S2 recommend HP5082

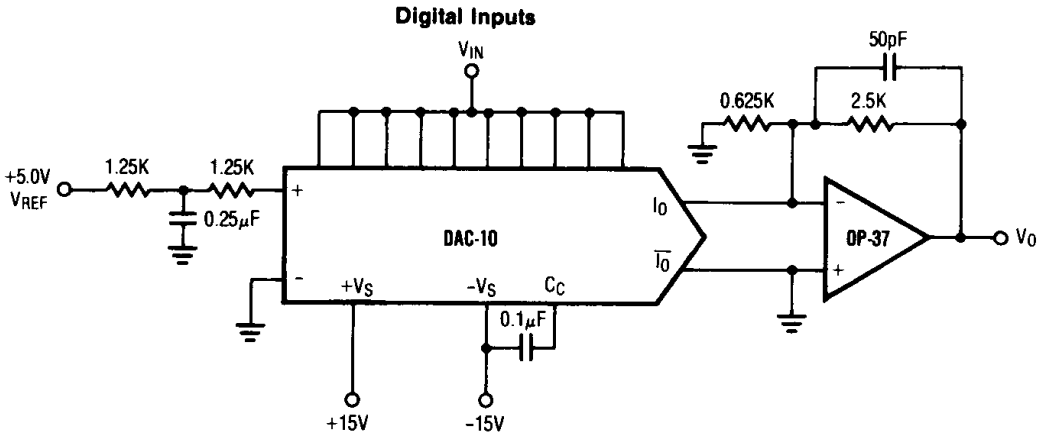
Figure 8. 10-Bit Successive Approximation A/D Converter

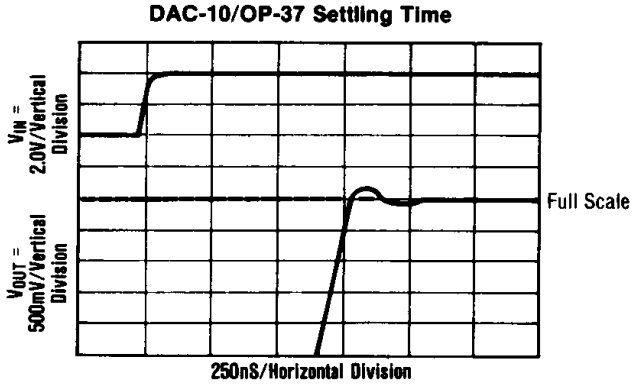
Output Voltage Compliance

The DAC-10 will operate over a wide range of supply voltages. However, the minimum negative output voltage is a direct function of the full scale output current and the negative supply voltage. Output voltage compliance range is the maximum voltage change from which the $\overline{I_O}$ and I_O can sink current. The minimum negative output voltage (V_S-) can be computed by the equation:

$$V_{OC}- \leq (-V_S) + 0.5I_{FS} + 2.6V$$

where V_{OC}- is in volts and full scale current I_{FS} is in milliamps. For instance V_{OC}- will be equal to -10.4V when $-V_S$ = -15V and I_{FS} = 4mA. V_{OC} (positive or negative) does not vary significantly over temperature. The maximum positive output voltage (V_{OC}+) has no theoretical limitations except for device breakdown phenomena. For $-V_S$ = -15V, I_{FS} = 4mA, V_{OC} is ±10V. The full scale current will typically change less than 1 LSB over this output range.

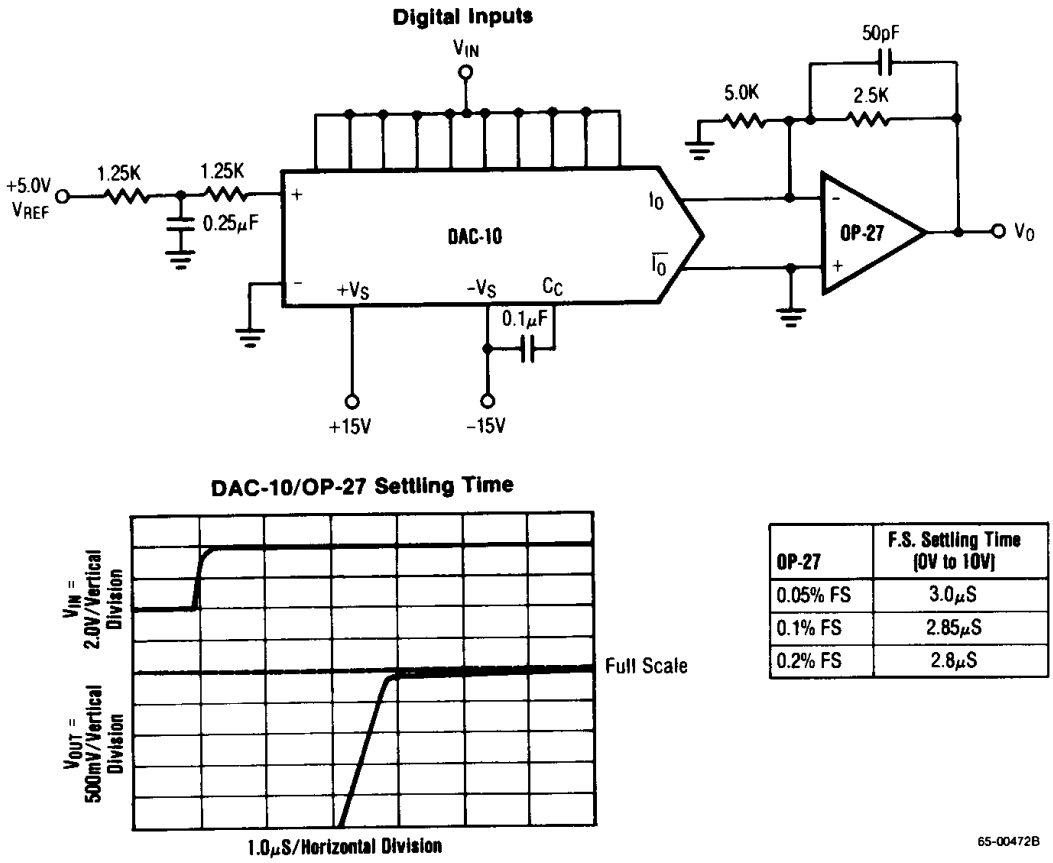




OP-37	F.S. Settling Time (0V to 10V)
0.05% FS	1080nS
0.1% FS	1000nS
0.2% FS	920nS

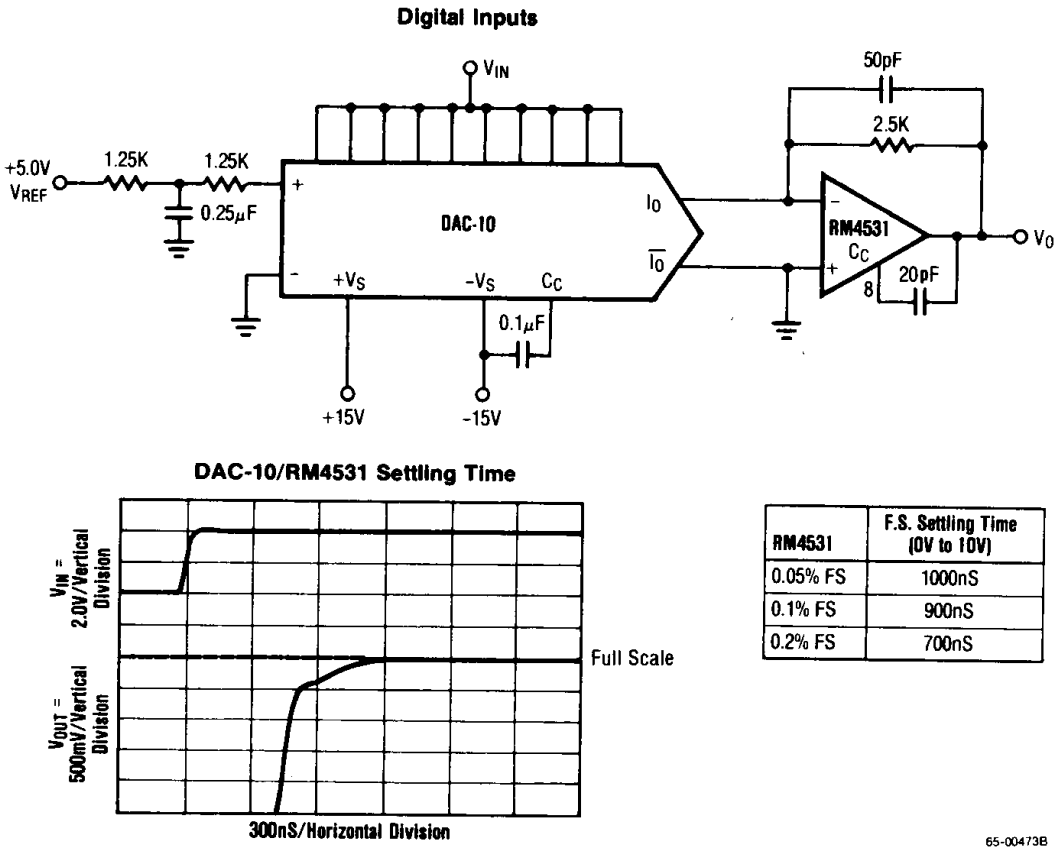
65-00471B

Figure 9. Settling Time Using OP-37



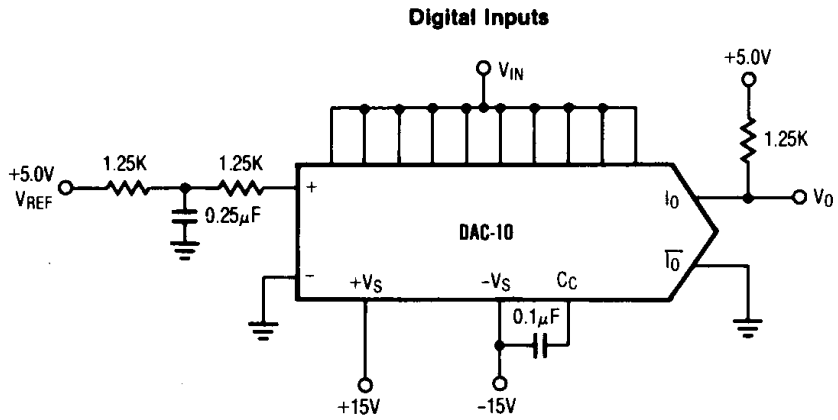
OP-27	F.S. Settling Time (0V to 10V)
0.05% FS	3.0μS
0.1% FS	2.85μS
0.2% FS	2.8μS

Figure 10. Settling Time Using OP-27

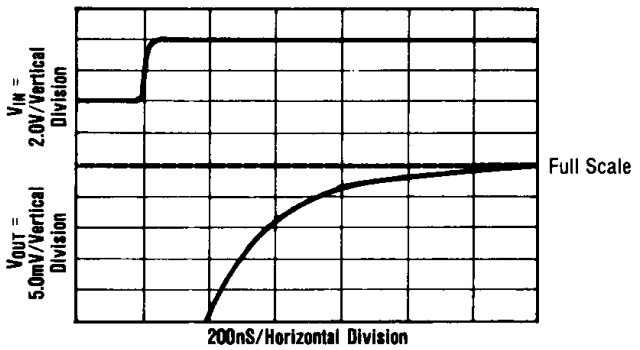


RM4531	F.S. Settling Time (0V to 10V)
0.05% FS	1000nS
0.1% FS	900nS
0.2% FS	700nS

Figure 11. Settling Time Using RM4531



DAC-10 with 1.25KΩ Resistive Output Settling Time



1.25KΩ Resistor	F.S. Settling Time (5.0V to 5.0mV)
0.05% FS	450nS
0.1% FS	320nS
0.2% FS	240nS

65-00474B

Figure 11. Settling Time Using 1.25kΩ Resistor Output

Logic Inputs

By programming the V_{LC} pin the DAC-10 can be made to interface with most logic families. The logic threshold voltage is approximately +1.4V above V_{LC}. Thus when V_{LC} = 0 the DAC-10 will interface with TTL logic; for other logic families V_{LC} must be programmed accordingly. Note that V_{LC} must be obtained from a low impedance source. Low impedance can be provided by a 0.1μF capacitor bypass (see Figure 12).

Output Glitches

The DAC-10 is designed for minimal output glitches. However, a further reduction of output glitches is possible, at a slight sacrifice in settling time, by installing small capacitors at the $I_O/\overline{I_O}$ outputs.

Full Scale Adjustment

Full scale trimming is sometimes required to compensate for resistor or voltage reference tolerances. If a potentiometer is used in series with pin 16 the performance of the DAC may be degraded by the temperature coefficient of the potentiometer. A preferred method of trimming is to use the potentiometer as a voltage divider to bias pin 17. With this method the temperature coefficient of the potentiometer has little effect on the circuit since I_{REF} expands on the tracking of the two resistor halves rather than the absolute value (see Figure 13).

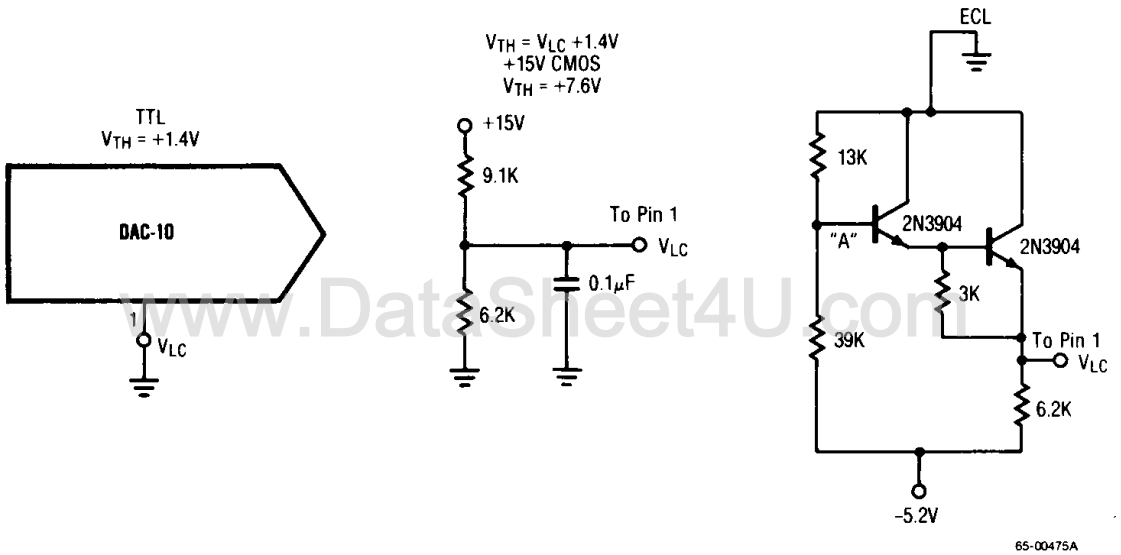


Figure 12. Interfacing With Various Logic Families

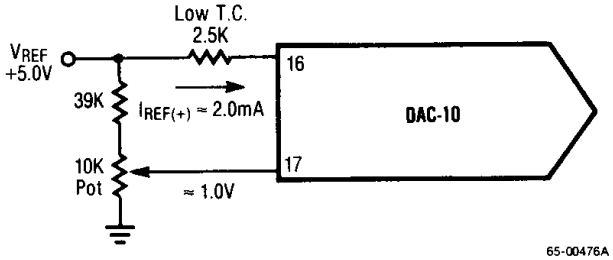
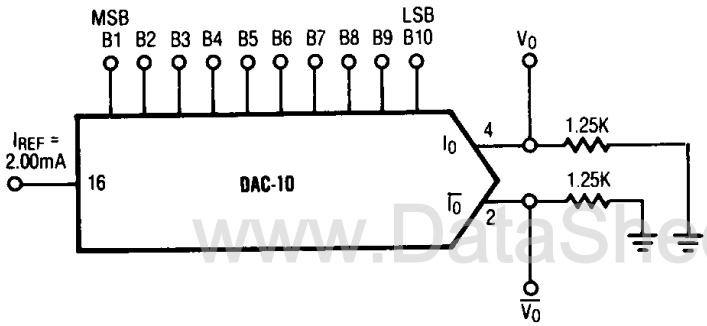


Figure 13. Recommended Full Scale Adjustment Circuit

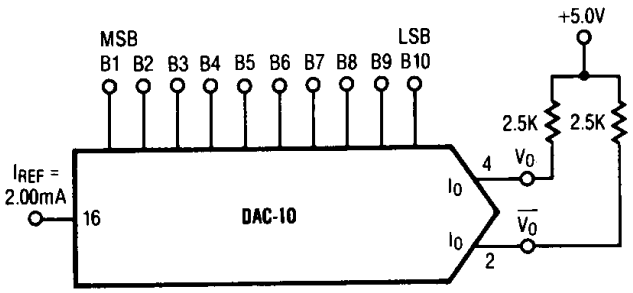
Basic Operation

Resistive terminations can be used to demonstrate basic operation of the DAC-10.



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	I_OmA	$\overline{I_O}$mA	V_O	$\overline{V_O}$
Full Scale	1 1 1 1 1 1 1 1 1 1	3.996	0.000	-4.995	-0.000
Half Scale +LSB	1 0 0 0 0 0 0 0 0 1	2.004	1.992	-2.505	-2.490
Half Scale	1 0 0 0 0 0 0 0 0 0	2.000	1.996	-2.500	-2.495
Half Scale -LSB	0 1 1 1 1 1 1 1 1 1	1.996	2.000	-2.495	-2.500
Zero Scale +LSB	0 0 0 0 0 0 0 0 0 1	0.004	3.992	-0.005	-4.990
Zero Scale	0 0 0 0 0 0 0 0 0 0	0.000	3.996	-0.000	-4.995

Figure 14. Basic Unipolar Negative Operation

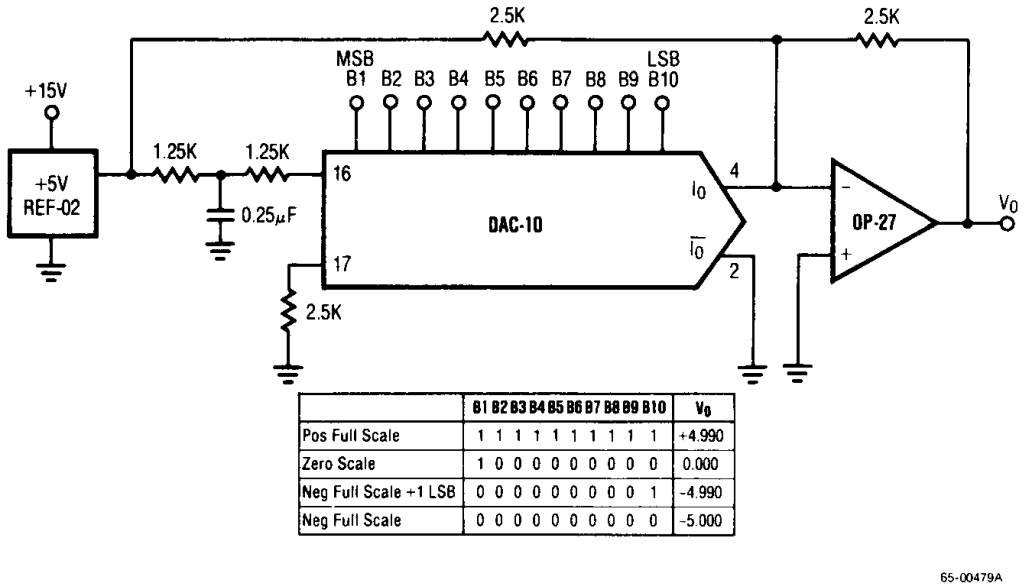


	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O	$\overline{V_O}$
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	-4.990	+5.000
Pos Full Scale -LSB	1 1 1 1 1 1 1 1 1 0	-4.980	+4.990
Zero Scale +LSB	1 0 0 0 0 0 0 0 0 1	-0.010	+0.020
Zero Scale	1 0 0 0 0 0 0 0 0 0	0.000	+0.010
Zero Scale -LSB	0 1 1 1 1 1 1 1 1 1	+0.010	0.000
Neg Full Scale +LSB	0 0 0 0 0 0 0 0 0 1	+4.990	-4.980
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	+5.000	-4.990

Figure 15. Basic Bipolar Output Operation

Offset Binary Operation

By feeding the inverting terminal of the output op amp a current equal to I_{REF} offset binary operation may be implemented.



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	+4.990
Zero Scale	1 0 0 0 0 0 0 0 0 0	0.000
Neg Full Scale +1 LSB	0 0 0 0 0 0 0 0 0 1	-4.990
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	-5.000

65-00479A

Figure 16. Offset Binary Operation

Simplified Schematic Diagram