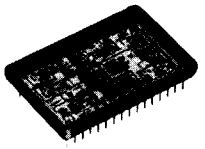
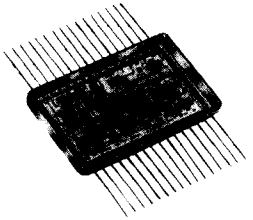
DAC-02310® AND DAC-02311®

14 BIT DEGLITCHED D/A CONVERTER
10MHz Update Rate; Voltage Output



DAC-02310



DAC-02311

DESCRIPTION:

The DAC-02310 is a 14 bit, 10 MHz update rate, deglitched hybrid D/A converter with a low impedance voltage output. Its input registers, precision DC voltage reference and track/hold deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 32 pin TDIP hybrid, the DAC-02310 operates over the full -55°C to +125°C temperature range and is available with military processing.

DAC-02310 is available in linearity grades of 13 bits (±0.006%) and 12 bits (±0.012%). It can be pin programmed for 5 different output voltage ranges; and offset, gain, and pedestal errors can be trimmed to zero with external potentiometers.

With its 14 bit resolution, low glitch voltage output and small hermetic package, the DAC-02310 is ideal for the most demanding low noise DAC requirements. It is particularly well suited for applications such as vector-stroke CRT displays, waveform generators and automatic test equipment.

FEATURES

- *FULL FUNCTION: INCLUDES INPUT REGISTERS AND TRACK/HOLD DEGLITCHER OUTPUT*
- *HIGH SPEED: 10MHz UPDATE RATE FOR SMALL STEP CHANGES*
- *LOW GLITCH: 10mVpp GLITCH VOLTAGE*
- *SMALL SIZE: 32 PIN TDIP HYBRID*
- *WIDE OPERATING TEMPERATURE: -55°C to +125°C*

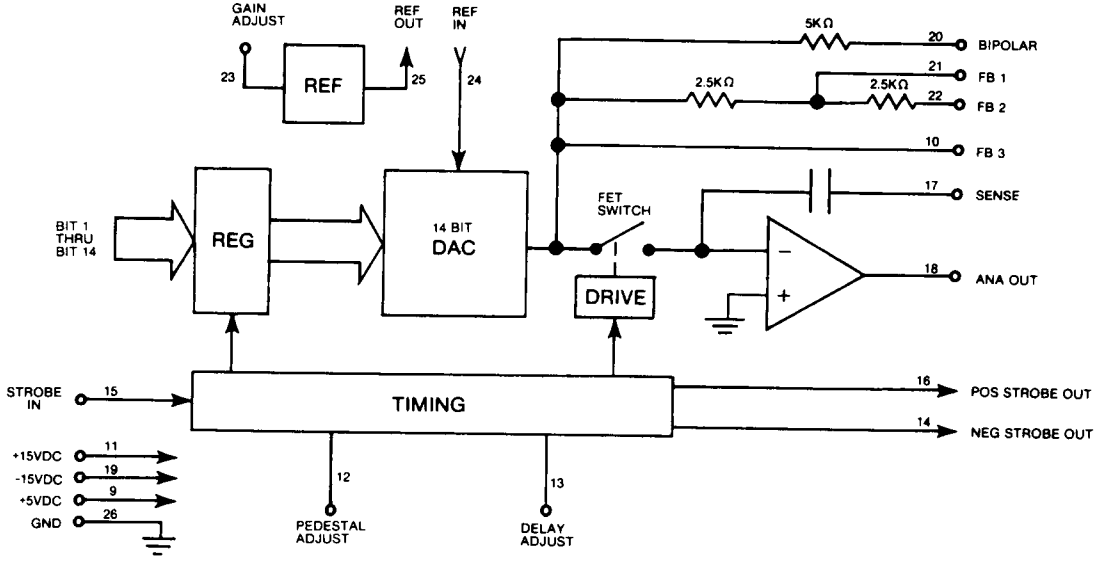


FIGURE 1. DAC-02310 BLOCK DIAGRAM

TABLE 1. DAC-02310 AND DAC-02311 SPECIFICATIONS
Typical values at +25° and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUE	
		13 BIT LIN	12 BIT LIN
RESOLUTION	**Bits**	**14**	**14**
ACCURACY			
Linearity Error	% FSR	±0.006 max	±0.012 max
Linearity Tempco	ppm/°C	±1 max	±2 max
Gain Error (1)	% FSR	±0.1	±0.2
Gain Tempco	ppm/°C	±25 max	±25 max
Offset Error (1)	mV	±10	±20
Offset Tempco	ppmFSR/°C	20 max	20 max
Pedestal Error (1)	mV	±10	±20
Pedestal Tempco (2)	ppmFSR/°C	10	10
Monotonicity	Bits	13	12
DYNAMIC CHARACTERISTICS			
Settling Time to ±½0.01% FSR			
±10V Full Scale Change	µsec	1.8 max	
±5V Full Scale Change	µsec	1.1 max	
±2.5V Full Scale Change	µsec	0.6 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/usec	20 typ 15 min	
Glitch (3)			
Voltage	mVpp	10 typ 30 max	
Energy (7)	mV•nsec	250 typ 750 max	
DIGITAL INPUTS			
Logic Compability		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar) Binary (Unipolar)	
Strobe Input (4)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to +0.8	
Loading		2 standard S TTL loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges (5)	V	±10, ±5, ±2.5, 0 to -10, 0 to -5	
Current Load	mA	±5 max	
Impedance	Ω	0.1 max	
REFERENCE			
Output Voltage	V	-10 ±0.1	
Output Current (6)	mA	±1 max	
Input Voltage	V	0 to -10	
Input Impedance	Ω	3.3K	
POWER SUPPLIES			
+15V Supply			
Tolerance	%	±5	
Max Voltage	V	+18 max	
Current Drain	mA	40 typ 50 max	
-15V Supply			
Tolerance	%	±5	
Max Voltage	V	-18 max	
Current Drain	mA	25 typ 35 max	
+5V Supply			
Tolerance	%	±5	
Max Voltage	V	+5.5 max	
Current Drain	mA	30 typ 45 max	
TEMPERATURE RANGE			
Operating (Case)			
-1 option	°C	-55 to +125	
-3 option	°C	0 to +70	
Storage	°C	-65 to +150	

TABLE 1. DAC-02310 AND DAC-02311 SPECIFICATIONS (CONT'D)

PARAMETER	UNITS	VALUE	
RESOLUTION	**Bits**	**14**	**14**
PHYSICAL CHARACTERISTICS			
Package		32 pin TDIP	
Size	in (mm)	1.15×1.75×0.21 (29×44×5)	
Weight	oz (g)	0.67 (19)	

NOTES: (1) Gain, offset, and pedestal errors are trimmable to zero.
(2) Pedestal tempco is with no delay adjust capacitor pin 13 to pin 14.
(3) Glitch is at 1 MHz update rate with a 5MHz filter.
(4) Strobe input is a positive pulse. Data transferred on rising edge.
(5) Output voltage ranges are pin programmable.
(6) Measured with REFIN, REFOUT and BIPOLAR pins connected together.
(7) Max Energy valid for 5V power supply ±2% Energy increases at 150mV/%5V power supply.

TECHNICAL DESCRIPTION

GENERAL

DAC-02310 is a completely self-contained deglitched D/A converter. As shown in the block diagram of Figure 1, it contains a 14 bit DAC, input registers, a precision DC reference, a track/hold deglitcher output and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon application of a STROBE IN signal the input registers are updated and the DAC-02310 output is held constant. As shown in Figure 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a POS STROBE OUT pulse which is used to open the FET switch at the op amp summing point. The output remains constant since the op amp feedback capacitor is charged. During this hold mode interval of approximately 40 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval, POS STROBE OUT returns to is original track mode level and the FET switch closes. The DAC-02310 then smoothly changes to its new output level. The track/hold has effectively "masked out" the DAC glitch. POS STROBE OUT (pin 16) and NEG STROBE OUT (pin 14) should not be loaded with external circuitry.

DELAY ADJUST

The hold time interval is internally set to approximate 40 nanoseconds. For applications, such as CRT displays, which may require matched delays, an external DELAY ADJUST pin is provided. By adding a capacitor from pin 13 to pin 14, the hold time interval is made longer. This effectively increases the delay of the DAC-02310. Figure 3 illustrates the effect on hold time of adding capacitance to pin 13.

EXTERNAL TRIMS

Factory adjustment of DAC-02310 offset, gain and pedestal errors result in performance that is adequate for most applications. For more critical applications, DAC-02310 provides pins for externally trimming offset, gain and pedestal errors to zero. Figure 4 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

DAC-02310 can be programmed for 5 different output voltage ranges by external jumpers between pins. Figure 6 illustrates the jumper connections required to yield ±10V, ±5V, ±2.5V, 0 to -10V, and 0 to -5V output voltage ranges.

OUTPUT CURRENT

The DAC-02310 can drive a load of ±5mA. For applications with higher current loads, the DAC-02310 can be used with a current booster. Figure 5 shows the interconnection of the DAC-02310 and DDC model HCD-13 hybrid cable driver; this allows the use of ±200mA loads.

INTERNAL REFERENCE

DAC-02310 contains a precision -10 volt internal reference which is made available for external use. For normal operation, REF OUT (Pin 25) must be jumpered to REF IN (Pin 24). Under these conditions, a maximum output current of 1 milliamp will be provided by the internal reference, while maintaining rated performance.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02310 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be kept to a minimum, and a large area ground plane must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output must be kept as close to the D/A converter package as possible. Circuit connections to the external adjustment (offset, gain and pedestal) pins must be kept as short as possible, and must be kept separated from digital lines to minimize noise coupling.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each power supply for minimum noise operation. Each of the power supplies should have a 1 microfarad or larger tantalum capacitor in parallel with a 0.01 microfarad ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

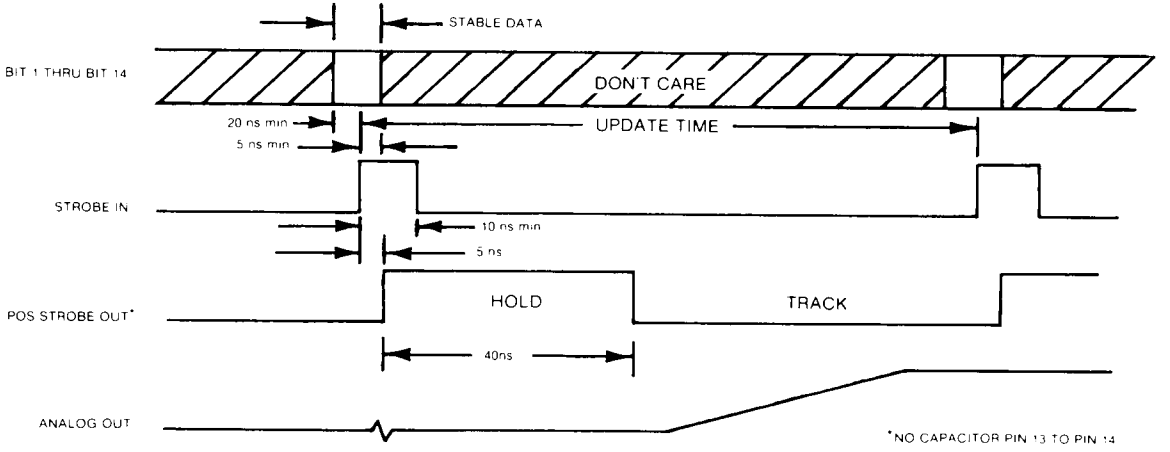


FIGURE 2. TIMING DIAGRAM

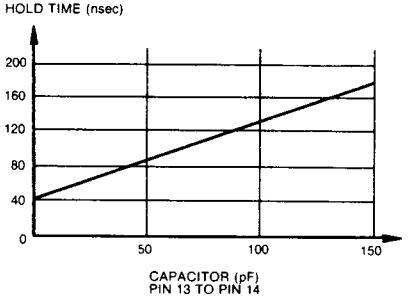


FIGURE 3. DELAY (HOLD) TIME ADJUST

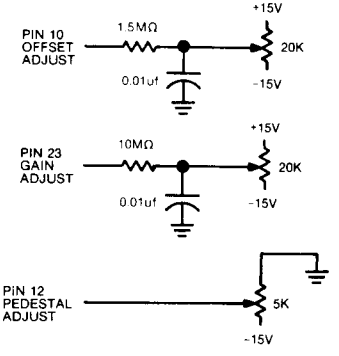


FIGURE 4.
EXTERNAL TRIM CIRCUITS

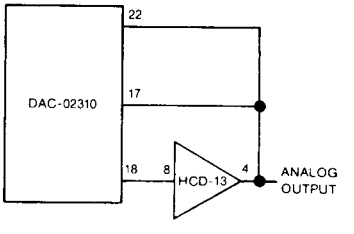


FIGURE 5. DAC-02310 AND CURRENT BOOSTER INTERCONNECTION

Voltage Range	JUMPER CONNECTIONS				
	Pin 22 to	Pin 21 to	Pin 20 to	Pin 17 to	Pin 24 to
±10V	Pin 18	—	Pin 25	Pin 18	Pin 25
±5V	Pin 18	Pin 22	Pin 25	Pin 18	Pin 25
±2.5V	Pin 10	Pin 18	Pin 25	Pin 18	Pin 25
0 to -10V	Pin 18	Pin 22	—	Pin 18	Pin 25
0 to -5V	Pin 10	Pin 18	—	Pin 18	Pin 25

FIGURE 6. OUTPUT VOLTAGE PROGRAMMING

INPUT DATA	OUTPUT VOLTAGE*	
	BIPOLAR	UNIPOLAR
00 0000 0000 0000	+5.0000V	0
01 1111 1111 1111	+0.0006V	−4.9994V
10 0000 0000 0000	0	-5.0000V
11 1111 1111 1111	-4.9994V	-9.9994V

*10 Volt Full Scale Range

FIGURE 7. INPUT DATA CODING

TABLE 2. PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION
1	Bit 8	17	Sense
2	Bit 7	18	Analog Out
3	Bit 6	19	-15 Volts
4	Bit 5	20	Bipolar
5	Bit 4	21	Feedback 1
6	Bit 3	22	Feedback 2
7	Bit 2	23	Gain Adjust
8	Bit 1 (MSB)	24	Reference In
9	+5 volts	25	Reference Out
10	Feedback 3	26	Ground
11	+15 Volts	27	Bit 14 (LSB)
12	Pedestal Adjust	28	Bit 13
13	Delay Adjust	29	Bit 12
14	Neg. Strobe Out	30	Bit 11
15	Strobe In	31	Bit 10
16	Pos. Strobe Out	32	Bit 9

ORDERING INFORMATION

DAC-02310-103

- Linearity Grade:
  - 3 = 13 bit
  - 2 = 12 bit
- Reliability Grade:
  - 0 = Standard DDC procedures
  - 1 = Military processing available.*
  - 2 = Military processing available but without QCI testing.*
- Operating Temperature Range (case):
  - 1 = -55°C to +125°C
  - 3 = 0°C to +70°C
- Packaging:
  - 0 = 32 pin TDIP
  - 1 = 32 pin flatpack

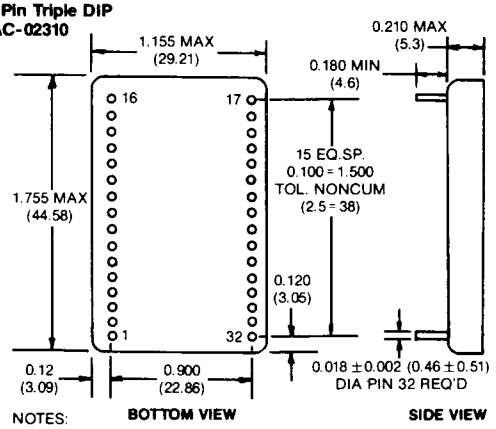
*Consult factory for details.

For current booster order HCD-13.

MECHANICAL OUTLINE

32 Pin Triple DIP

DAC-02310



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead spacing dimensions apply at seating plane (TDIPs only).
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

MECHANICAL OUTLINE

32 Pin Flatpack

DAC-02311