DAC1003D160

Dual 10 bits DAC, up to 160 MHz, 2 x interpolation

Rev. 03 — 2 July 2012 | Product data sheet

1. General description

The DAC1003D160 is optimized to reduce architecture complexity and overall system cost. The Digital-to-Analog Converter (DAC) leads dynamic performance in multi-carrier support because of its direct IF conversion capabilities. With an internal sampling rate up to 160 MHz, the DAC1003D160 is an extremely competitive solution for broadband wireless systems transmitters, as well as a wide range of applications.

2. Features

- Dual 10-bit resolution
- Spurious Free Dynamic Range (SFDR) = 80 dBc at 2.5 MHz
- Input data rate up to 80 MHz
- 2 × interpolation filter
- Output data rate up to 160 Mhz
- Single 3.3 V power supply
- Low noise capacitor free integrated Phase-Locked Loop (PLL)
- Low power dissipation
- HTQFP80 package
- Ambient temperature from –40 °C to +85 °C

3. Applications

- Broadband wireless systems
- Digital radio links
- Cellular base stations
- Instrumentation
- Cable modems
- Cable Modem Termination System (CMTS)/Data Over Cable Service Interface Specification (DOCSIS)

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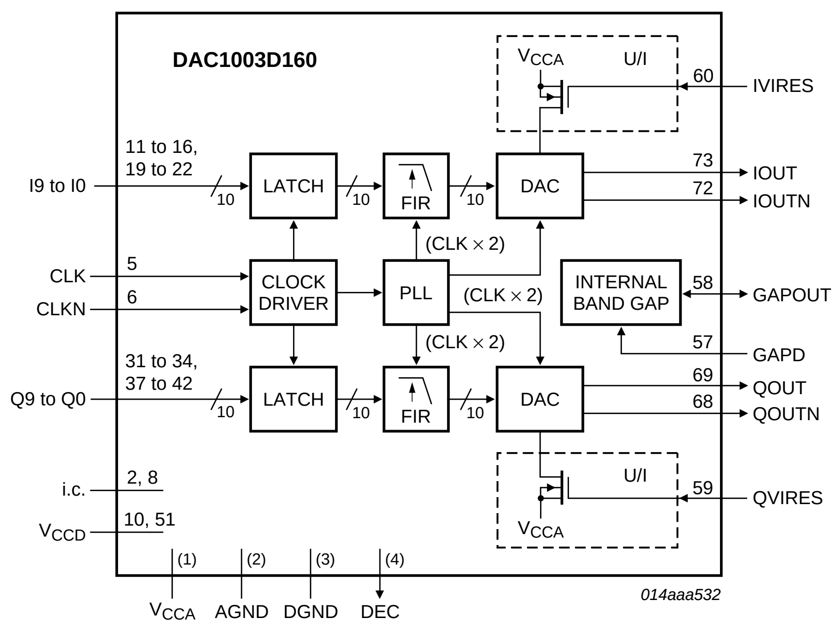
4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
DAC1003D160HW	HTQFP80	plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad	SOT841-1

5. Block diagram



(1) Pins 1, 3, 61, 65, 76 and 80.

(2) Pins 4, 7, 62, 64, 66, 67, 70, 71, 74, 75, 77 and 79.

(3) Pins 9, 17, 25, 29, 30, 35, 44, 49, 50, 52, 53, 54, 55 and 56.

(4) Pins 18, 26, 36, 43, 63 and 78.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

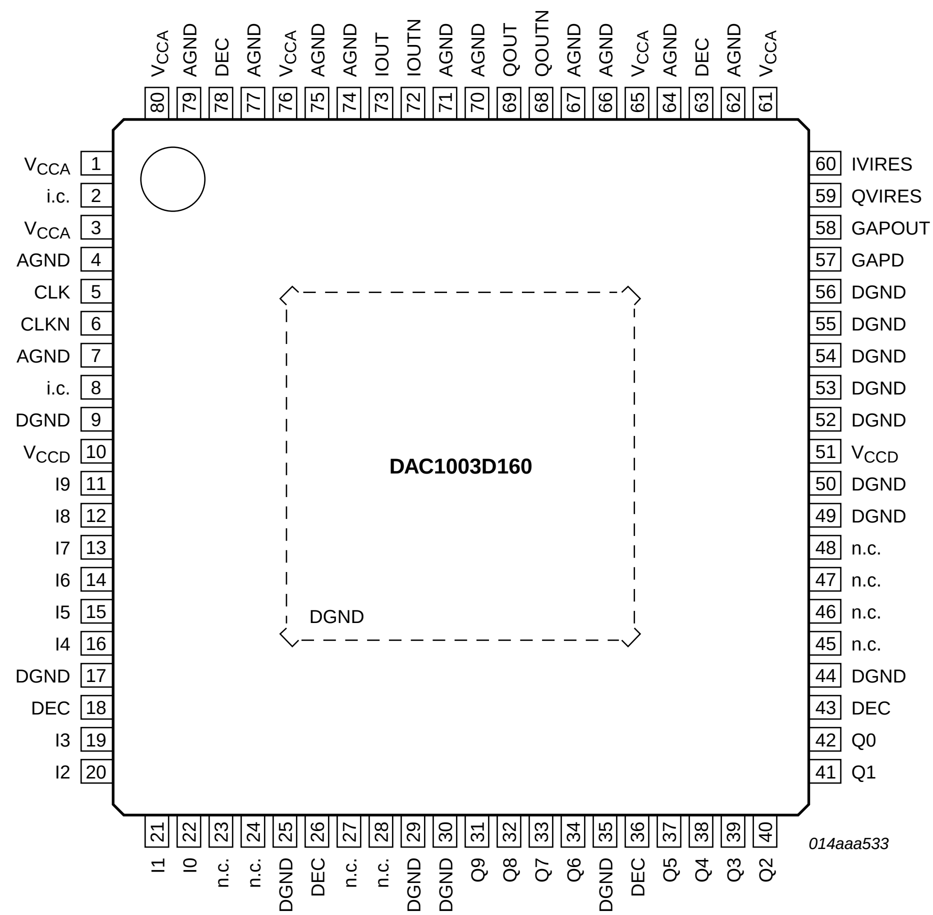


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
V_{CCA}	1	S	analog supply voltage
i.c.	2	I/O	internally connected; leave open
V_{CCA}	3	S	analog supply voltage
AGND	4	G	analog ground
CLK	5	I	clock input
CLKN	6	I	complementary clock input
AGND	7	G	analog ground
i.c.	8	O	internally connected; leave open
DGND	9	G	digital ground

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
V_{CCD}	10	S	digital supply voltage
I9	11	I	I data input bit 9 (Most Significant Bit (MSB))
I8	12	I	I data input bit 8
I7	13	I	I data input bit 7
I6	14	I	I data input bit 6
I5	15	I	I data input bit 5
I4	16	I	I data input bit 4
DGND	17	G	digital ground
DEC	18	O	decoupling node
I3	19	I	I data input bit 3
I2	20	I	I data input bit 2
I1	21	I	I data input bit 1
I0	22	I	I data input bit 0 (Least Significant Bit (LSB))
n.c.	23	I	not connected
n.c.	23	I	not connected
DGND	25	G	digital ground
DEC	26	O	decoupling node
n.c.	27	I	not connected
n.c.	28	I	not connected
DGND	29	G	digital ground
DGND	30	G	digital ground
Q9	31	I	Q data input bit 9 (MSB)
Q8	32	I	Q data input bit 8
Q7	33	I	Q data input bit 7
Q6	34	I	Q data input bit 6
DGND	35	G	digital ground
DEC	36	O	decoupling node
Q5	37	I	Q data input bit 5
Q4	38	I	Q data input bit 4
Q3	39	I	Q data input bit 3
Q2	40	I	Q data input bit 2
Q1	41	I	Q data input bit 1
Q0	42	I	Q data input bit 0 (LSB)
DEC	43	O	decoupling node
DGND	44	G	digital ground
n.c.	45	I	not connected
n.c.	46	I	not connected
n.c.	47	I	not connected
n.c.	48	I	not connected
DGND	49	G	digital ground
DGND	50	G	digital ground

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
V_{CCD}	51	S	digital supply voltage
DGND	52	G	digital ground
DGND	53	G	digital ground
DGND	54	G	digital ground
DGND	55	G	digital ground
DGND	56	G	digital ground
GAPD	57	I	internal band gap power disable input
GAPOUT	58	I/O	band gap output voltage
QVIRES	59	I	Q DAC biasing resistor
IVIRES	60	I	I DAC biasing resistor
V_{CCA}	61	S	analog supply voltage
AGND	62	G	analog ground
DEC	63	O	decoupling node
AGND	64	G	analog ground
V_{CCA}	65	S	analog supply voltage
AGND	66	G	analog ground
AGND	67	G	analog ground
QOUTN	68	O	complementary Q DAC output current
QOUT	69	O	Q DAC output current
AGND	70	G	analog ground
AGND	71	G	analog ground
IOUTN	72	O	complementary I DAC output current
IOUT	73	O	I DAC output current
AGND	74	G	analog ground
AGND	75	G	analog ground
V_{CCA}	76	S	analog supply voltage
AGND	77	G	analog ground
DEC	78	O	decoupling node
AGND	79	G	analog ground
V_{CCA}	80	S	analog supply voltage

[1] Type description: S: Supply; G: Ground; I: Input; O: Output.

7. Functional description

The DAC1003D160 is a segmented architecture composed of a 7-bit thermometer sub-DAC and the remaining 3-bit in a binary weighted sub-DAC.

The device produces two complementary current outputs on both channels, respectively pins IOUT/IOUTN and QOUT/QOUTN which need to be connected via a load resistor to the ground.

Figure 3 shows the equivalent analog output circuit of one DAC, which consists of a parallel combination of PMOS current sources and associated switches for each segment.

The cascade source configuration enables the increase of the output impedance of the source and the improvement of the dynamic performance of the DAC by introducing less distortion.

Figure 4 shows the internal reference configuration. In this case the bias current is given by the output of the internal regulator connected to the inverting input of the internal operational amplifiers, while external resistors R_I and R_Q are connected respectively to pins IVIRES and QVIRES. Thus the output current of the two DACs is typically fixed to 20 mA with an appropriate choice of these resistors. This configuration is optimal for temperature drift compensation because the band gap can be matched with the voltage on the feedback resistors.

The relation between full-scale output current $I_{O(fs)}$ and the R_I (R_Q) is:

$$R_I = \frac{2048 \times V_{GAPOUT}}{82 \times I_{O(FS)}} \Omega$$

The output current can also be adjusted by imposing an external reference voltage to the inverting input pin GAPOUT and disabling the internal band gap with pin GAPD set to HIGH. At a voltage lower than 1.2 V the current can be set at values lower than 20 mA. The input references at pins IVIRES and QVIRES may also be driven by separate reference voltages to adjust independently the two DAC currents.

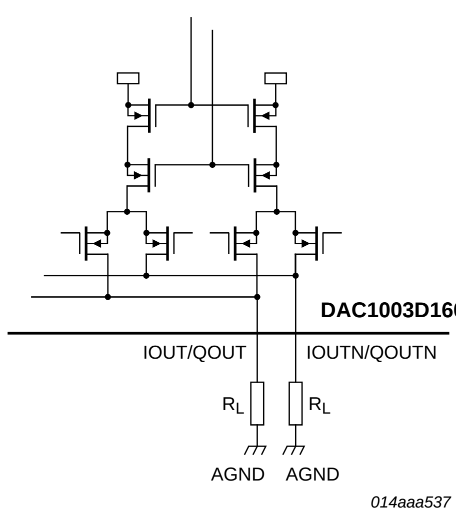


Fig 3. Equivalent analog output circuit

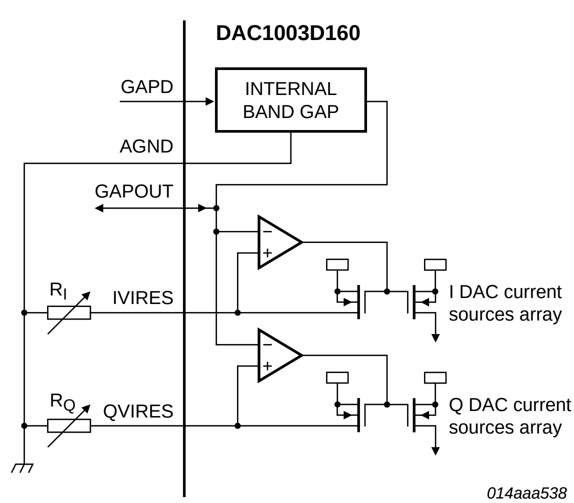


Fig 4. Internal reference configuration

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCD}	digital supply voltage		[1]	–0.3	+3.9	V
V_{CCA}	analog supply voltage		[1]	–0.3	+3.9	V
ΔV_{CC}	supply voltage difference	between the analog and digital supply voltages		–150	+150	mV
V_I	input voltage	pins Qn and In referenced to DGND		–0.3	V_{CCD} + 0.3	V
		pins IVIRES, QVIRES, GAPD, CLK and CLKN referenced to AGND		–0.3	V_{CCA} + 0.3	V
V_O	output voltage	pins IOUT, IOUTN, QOUT and QOUTN referenced to DAGND		–0.3	V_{CCA} + 0.3	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	125	°C

[1] All supplies are connected together.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	27.1	K/W
$R_{th(c-a)}$	thermal resistance from case to ambient	in free air	11.8	K/W

10. Characteristics

Table 5. Characteristics

V_{CCD} = V_{CCA} = 3.0 V to 3.6 V; AGND and DGND connected together; T_{amb} = –40 °C to +85 °C; typical values measured at V_{CCD} = V_{CCA} = 3.3 V, $I_{O(fs)}$ = 20 mA and T_{amb} = 25 °C; dynamic parameters measured using output schematic given in Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{CCD}	digital supply voltage		3.0	3.3	3.6	V
V_{CCA}	analog supply voltage		3.0	3.3	3.6	V
I_{CCD}	digital supply current		-	55	65	mA

Table 5. Characteristics *…continued*
V_{CCD} = V_{CCA} = 3.0 V to 3.6 V; AGND and DGND connected together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCD} = V_{CCA} = 3.3 V, $I_{O(fs)}$ = 20 mA and T_{amb} = 25 °C; dynamic parameters measured using output schematic given in Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CCA}	analog supply current			-	73	85	mA
P_{tot}	total power dissipation	f_{clk} = 80 MHz; f_{IOUT} = f_{QOUT} = 5 MHz		-	422	540	mW
Clock inputs (CLK and CLKN)							
$V_{I(cm)}$	common-mode input voltage			-	1.65	-	V
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage			-	1.0	-	V
Analog outputs (IOUT, IOUTN, QOUT and QOUTN)							
$I_{O(fs)}$	full-scale output current	differential outputs		4	-	20	mA
R_o	output resistance		[1]	-	150	-	kΩ
C_o	output capacitance		[1]	-	3	-	pF
Digital inputs (I0 to I9, Q0 to Q9 and GAPD)							
V_{IL}	LOW-level input voltage			DGND	-	0.3 V_{CCD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{CCD}	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.3 V_{CCD}		-	5	-	μA
I_{IH}	HIGH-level input current	V_{IH} = 0.7 V_{CCD}		-	5	-	μA
Reference voltage output (GAPOUT)							
V_{GAPOUT}	voltage on pin GAPOUT			-	1.31	-	V
I_{GAPOUT}	current on pin GAPOUT	external voltage		-	1	-	μA
ΔV_{GAPOUT}	voltage variation on pin GAPOUT			-	±133	-	ppm/°C
Clock timing inputs (CLK and CLKN)							
f_{clk}	clock frequency				-	80	MHz
$t_{w(clk)H}$	HIGH clock pulse width			5	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width			5	-	-	ns
Input timing (I0 to I9 and Q0 to Q9); see Figure 5							
$t_{h(i)}$	input hold time			1.1	-	3.4	ns
$t_{su(i)}$	input set-up time			−1.5	-	+0.7	ns
Output timing (IOUT, IOUTN, QOUT, QOUTN)							
t_s	settling time	$t_{o\pm}$ 0.5 LSB	[1]	-	16	-	ns
Digital filter specification (FIR); order N = 42 see Figure 6 and 7 and Table 7							
f_{data}	data rate			-	-	80	MHz
$\alpha_{ripple(pb)}$	pass-band ripple	f_{data}/f_{clk}; 0.005 dB attenuation		-	0.405	-	
B_p	power bandwidth	f_{data}/f_{clk}; 3 dB attenuation		-	0.479	-	
α_{stpb}	stop-band attenuation	f_{data}/f_{clk} = 0.6 dB to 1 dB		-	69	-	dB
$t_{d(grp)}$	group delay time			-	11 T_{clk}	-	ns
Analog signal processing							
INL	integral non-linearity			-	±0.2	-	LSB
DNL	differential non-linearity			-	±0.1	-	LSB

Table 5. Characteristics *...continued*

V_{CCD} = V_{CCA} = 3.0 V to 3.6 V; AGND and DGND connected together; T_{amb} = −40 °C to +85 °C; typical values measured at V_{CCD} = V_{CCA} = 3.3 V, $I_{O(fs)}$ = 20 mA and T_{amb} = 25 °C; dynamic parameters measured using output schematic given in Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{n(o)}$	output noise current		-	120	-	pA/√Hz
E_{offset}	offset error	relative to full-scale	-	−0.3	-	%
E_G	gain error	relative to full-scale	−5.4	-	+5.4	%
ΔG_{IQ}	IQ gain mismatch	between I and Q, relative to full-scale	-	±0.2	-	%
SFDR	spurious free dynamic range	f_{clk} = 80 MHz; B = Nyquist				
		f_o = 2.5 MHz at 0 dBFS	-	80	-	dBc
		f_o = 5 MHz at 0 dBFS	-	72	-	dBc
		f_o = 13 MHz at 0 dBFS	-	64	-	dBc
α_{2H}	second harmonic level	f_o = 5 MHz	-	73	-	dBc
		f_o = 13 MHz	-	65	-	dBc
α_{3H}	third harmonic level	f_o = 5 MHz	-	88	-	dBc
		f_o = 13 MHz	-	86	-	dBc
IMD2	second-order intermodulation distortion	f_{clk} = 80 MHZ; f_o 1 = 10 MHz; f_o 2 = 12 MHz; B = Nyquist	-	65	-	dBc
IMD3	third-order intermodulation distortion	f_{clk} = 80 MHz; f_o 1 = 10 MHz; f_o 2 = 12 MHz	-	84	-	dBc
THD	total harmonic distortion	f_{clk} = 80 MHz; B = Nyquist; T_{amb} = 25 °C				
		f_o = 2.5 MHz	-	75	-	dBc
		f_o = 5 MHz	68	71	-	dBc
NSD	noise spectral density	f_{clk} = 80 MHz				
		f_o = 2.5 MHz	-	−155	-	dBm/Hz
		f_o = 5 MHz	-	−155	-	dBm/Hz
		f_o = 19 MHz	-	−153	-	dBm/Hz
S/N	signal-to-noise ratio	f_{clk} = 80 Msample/s; B = Nyquist				
		f_o = 2.5 MHz	-	80	-	dBc
		f_o = 5 MHz	70	80	-	dBc
		f_o = 19 MHz	-	78	-	dBc
ACPR	adjacent channel power ratio	baseband; 5 MHz channel spacing; B = 3.84 MHz				
		f_o = 2.5 MHz	-	60	-	dBc
		f_o = 20 MHz	-	61	-	dBc

[1] Guaranteed by design.

Table 6. Band gap

Band gap disable (GAPD)	Band gap input/output (GAPOUT)	Internal band gap
LOW	output (V_{GAPOUT} = 1.2 V)	enable
HIGH	input	disable

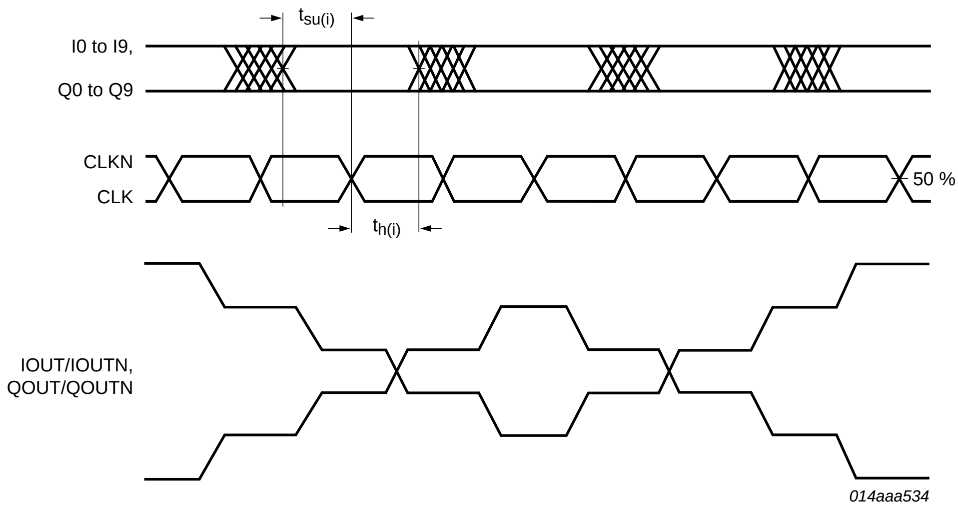


Fig 5. Input timing diagram

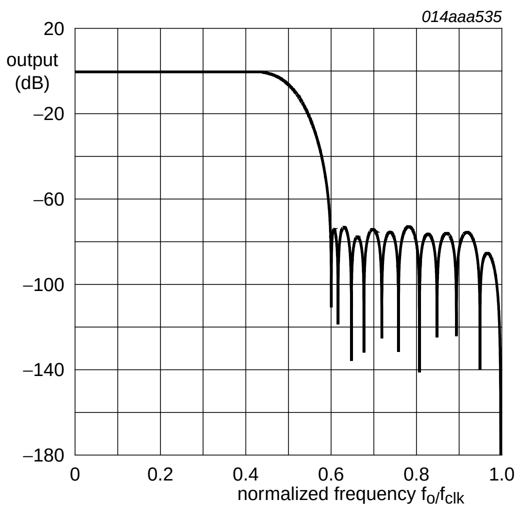


Fig 6. FIR filter frequency response

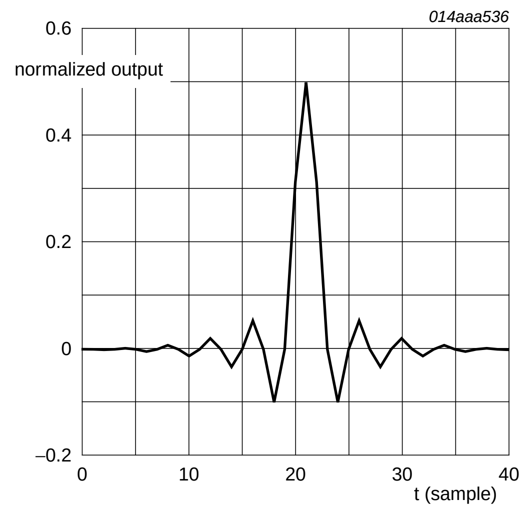


Fig 7. FIR filter impulse response

Table 7. Interpolation FIR filter coefficient

Coefficient	Coefficient	Value
H(1)	H(43)	10
H(2)	H(42)	0
H(3)	H(41)	−31
H(4)	H(40)	0
H(5)	H(39)	69
H(6)	H(38)	0
H(7)	H(37)	−138
H(8)	H(36)	0
H(9)	H(35)	248
H(10)	H(34)	0
H(11)	H(33)	−419
H(12)	H(32)	0
H(13)	H(31)	678
H(14)	H(30)	0
H(15)	H(29)	−1083
H(16)	H(28)	0
H(17)	H(27)	1776
H(18)	H(26)	0
H(19)	H(25)	−3282
H(20)	H(24)	0
H(21)	H(23)	10364
H(22)	-	16384

11. Application information

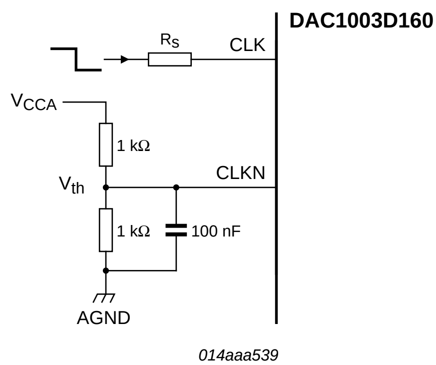


Fig 8. Single-ended clock schematic

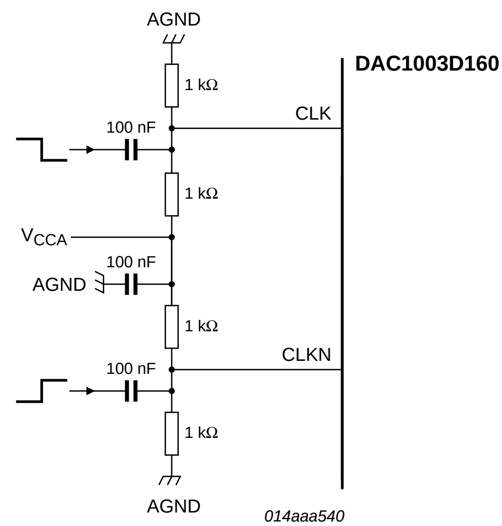
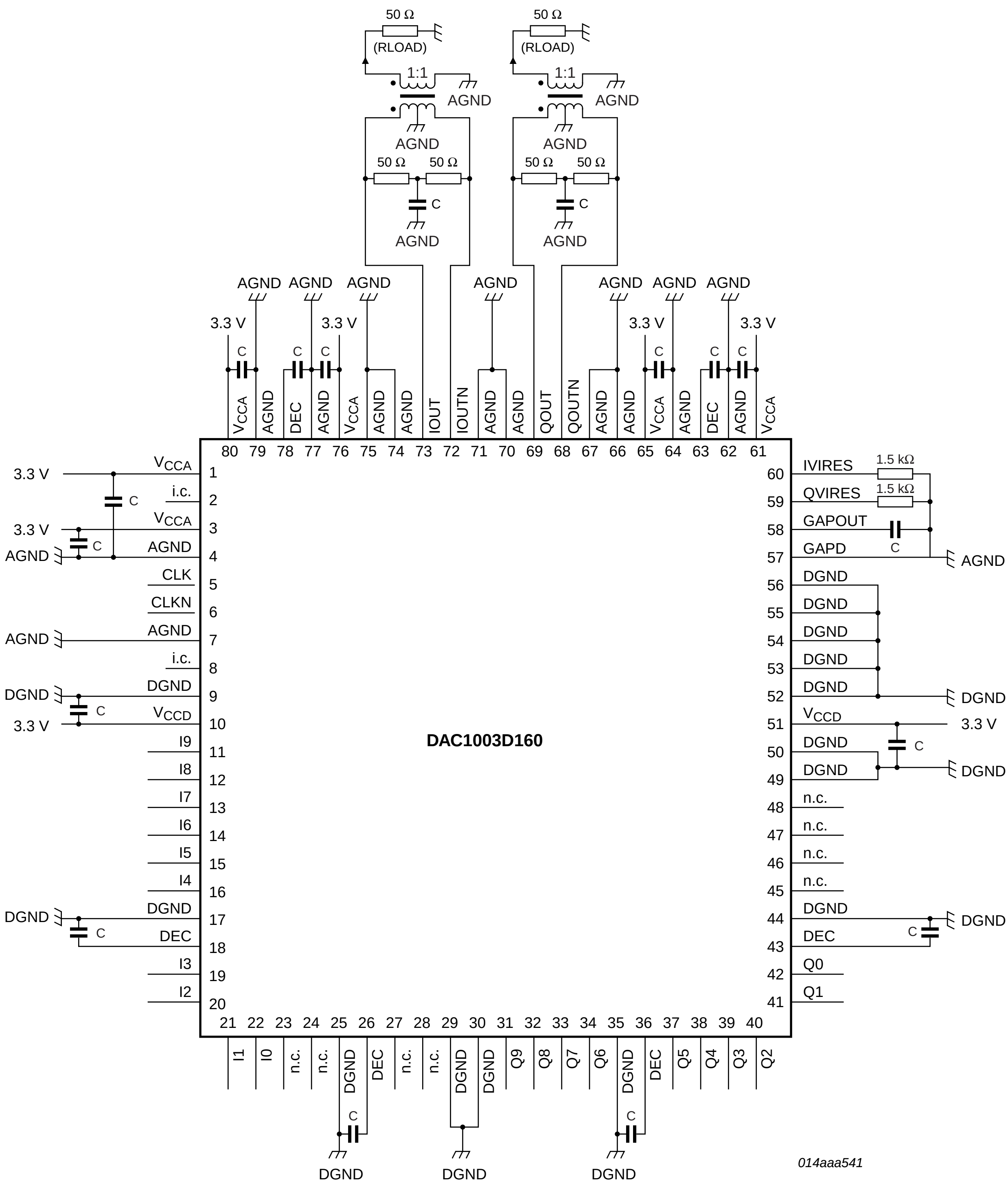


Fig 9. Differential clock schematic



All resistors are 1 % precision resistors.

C = 100 nF.

Fig 10. Application diagram

11.1 Alternative parts

The following alternative parts are also available:

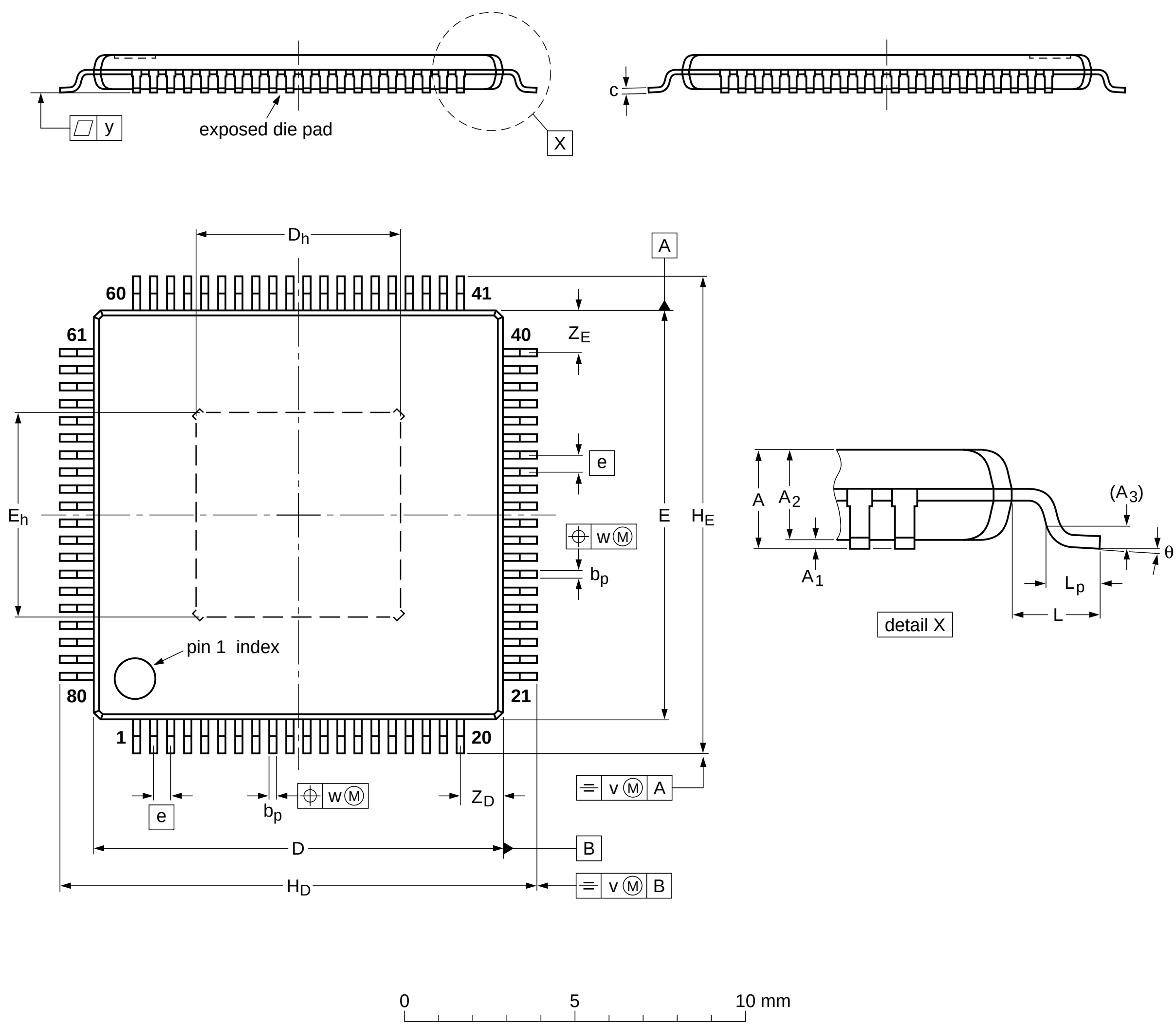
Table 8. Alternative parts

Type number	Description		Sampling frequency
DAC1403D160	Dual 14 bits DAC, with 2 × interpolating	[1]	160 MHz
DAC1203D160	Dual 12 bits DAC, with 2 × interpolating	[1]	160 MHz

[1] Pin to pin compatible

12. Package outline

HTQFP80: plastic thermal enhanced thin quad flat package; 80 leads; body 12 x 12 x 1 mm; exposed die pad **SOT841-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	A_3	b_p	c	D(1)	D_h	E(1)	E_h	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	12.1 11.9	6.05 5.95	12.1 11.9	6.05 5.95	0.5	14.15 13.85	14.15 13.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT841-1		MS-026				04-01-15

Fig 11. Package outline SOT841-1 (HTQFP80)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
FIR	Finite Impulse Response
IF	Intermediate Frequency
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-Locked Loop
PMOS	Positive-Metal Oxide Semiconductor

14. Glossary

14.1 Static parameters

DNL — Differential Non-Linearity. The difference between the ideal and the measured output value between successive DAC codes.

INL — Integral Non-Linearity. The deviation of the transfer function from a best-fit straight line (linear regression computation).

14.2 Dynamic parameters

IMD2 — Second-order intermodulation distortion. From a dual-tone digital input sine wave (these two frequencies are close together), the intermodulation distortion product IMD2 is the ratio of the RMS value of either tone and the RMS value of the worst 2nd-order intermodulation product.

IMD3 — Third-order intermodulation distortion. From a dual-tone digital input sine wave (these two frequencies are close together), the intermodulation distortion product IMD3 is the ratio of the RMS value of either tone and the RMS value of the worst 3rd-order intermodulation product.

SFDR — Spurious Free Dynamic Range. The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

S/N — Signal-to-Noise ratio. The ratio of the RMS value of the reconstructed output sine wave to the RMS value of the noise excluding the harmonics and the DC component.

THD — Total Harmonic Distortion. The ratio of the RMS value of the harmonics of the output frequency to the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DAC1003D160_3	20120702	Product data sheet	-	DAC1003D160_2
DAC1003D160_2	20080813	Product data sheet	-	DAC1003D160_1
Modifications:	• Added condition to t_s in Table 5. • Correction to Figure 10.			
DAC1003D160_1	20080612	Product data sheet	-	-

16. Contact information

For more information or sales office addresses, please visit: **http://www.idt.com**

17. Contents