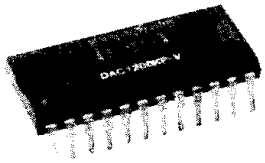
BURR-BROWN®

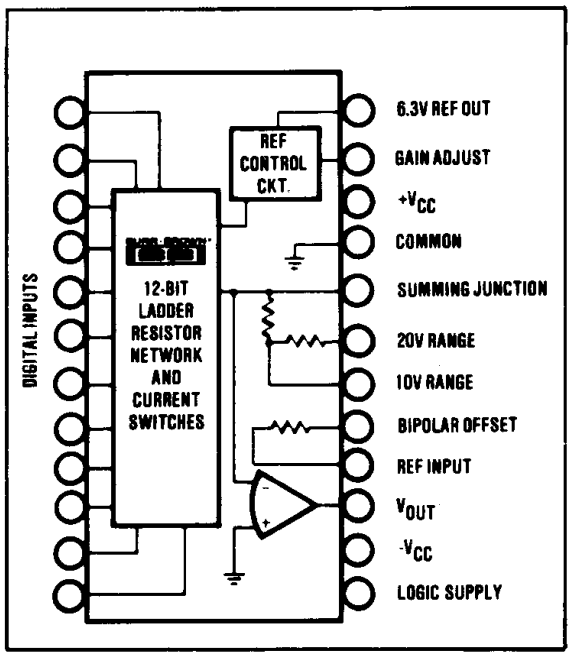
DAC1200KP-V



Integrated Circuit
12-Bit Resolution
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- ±1/2LSB LINEARITY ERROR
- MONOTONICITY GUARANTEED 0°C TO +70°C
- SETTLING TIME 7μs, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 24-PIN MOLDED PLASTIC DIP
- LOWEST COST 12-BIT DAC



DESCRIPTION

The low price of DAC1200KP-V makes this 12-bit resolution D/A converter the best value available for commercial applications.

The DAC1200 offers TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μsec maximum. It comes complete with internal reference and output operational amplifier.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1200 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use a 12-bit D/A converter for new applications in communications systems, control systems, medical systems, electronic games and personal computer peripherals.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1200KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	CSB, COB	
Resolution	12	Bits
Digital Logic Inputs[2]:		
V_{IH}, min to max	+2.4 to +V_{DD}	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2.7V, max	+20	μA
I_{IL}, V_I = +0.4V, max	−400	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0.018	% of FSR[4]
Differential Linearity Error, max	±0.024	% of FSR
Gain Error, max[5][6]	±0.3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
+V_{CC} and −V_{CC}	±0.003	% of FSR/%V_{CC}
V_{DD}	±0.0002	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Offset	±8	ppm of FSR/°C
SETTLING TIME to ±0.012% of FSR[10]		
20V Step and 2kΩ Load, max	7	μsec
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min	±2.5, ±5, ±10, +5, +10	V
Current, min[11][12]	±5	mA
Impedance	0.05	Ω
REFERENCE OUTPUT		
Voltage[13]	+6.3	V_{DD}
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
+V_{CC}/−V_{CC}[14]	+15/−15	V
V_{DD}[15]	+5	V
CURRENT (no load), max[16]		
+V_{CC}/−V_{CC}	+12/−25	mA
V_{DD}	+10	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

NOTES: (1) CSB = Complementary Straight Binary (unipolar), COB = Complementary Offset Binary (bipolar). (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to +V_{CC}. Digital input specs are guaranteed over 0°C to +70°C. These specs are tested at 25°C only. (3) ±0.018% of FSR is 3/4LSB at 12 bits. (4) FSR means Full Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation. (7) Error at input code FFF_H for unipolar operation (output at 0V). (8) Error at input code FFF_H for bipolar operation (output at minus full scale, −FS). (9) Guaranteed. Tested at 25°C only. (10) Guaranteed. Not tested. (11) For operation with supply voltages of less than ±13V, load current must be limited to 1mA. (12) Output may be indefinitely shorted to Common without damage. (13) Tolerance is ±5%. (14) Range of operation is ±11.4V to ±16.5V. (15) V_{DD} may be operated up to +V_{CC}. Digital input logic threshold remains at +1.4V over the V_{DD} range. (16) Typical power supply currents are about 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

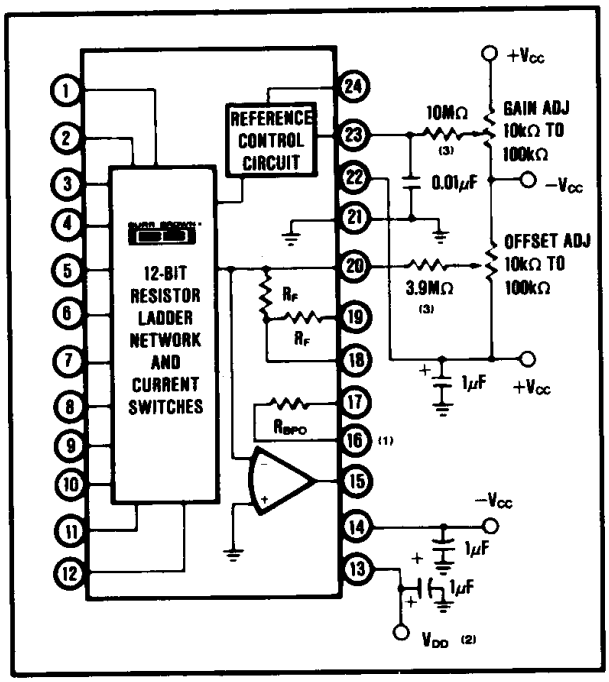
+V_{CC} to Common	0 to +18V
−V_{CC} to Common	0 to −18V
V_{DD} to Common	0 to +7V
Digital Inputs (pins 1—12) to Common	−0.4V to +18V
External Voltage Applied to Range Resistors	±12V
REF OUT	Indefinite short to Common
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0 to +70°C
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

Pin	Description	Pin	Description
1	Bit 1 (MSB)	13	Logic Supply, V_{DD}
2	Bit 2	14	−V_{CC}
3	Bit 3	15	V_{OUT}
4	Bit 4	16	Reference Input
5	Bit 5	17	Bipolar Offset
6	Bit 6	18	10V Range
7	Bit 7	19	20V Range
8	Bit 8	20	Summing Junction
9	Bit 9	21	Common
10	Bit 10	22	+V_{CC}
11	Bit 11	23	Gain Adjust
12	Bit 12 (LSB)	24	6.3V Reference Out

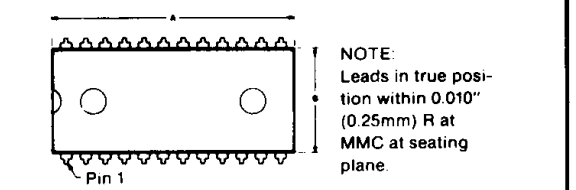
CONNECTION DIAGRAM

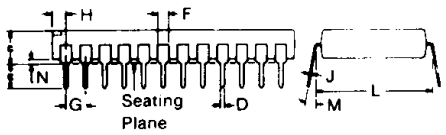


	Output Voltage Range Connections				
Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB	19	20	15	24
±5	COB	18	20	NC	24
±2.5V	COB	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

NOTES: (1) Pin 16 is used only to connect the bipolar offset resistor. An external reference voltage may not be used. (2) If connected to +V_{CC}, which is permissible, power dissipation increases 75mW typ, 100mW max. (3) Values shown are for ±15V supplies. For supplies below ±13.5V use 2.7MΩ in place of 3.9MΩ and 7.5MΩ in place of 10MΩ.

MECHANICAL





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.233	1.283	31.32	32.59
B	.538	.575	13.67	14.61
C	.169	.224	4.29	5.69
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.132	2.54	3.35
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56

CASE: Plastic
MATING CONNECTOR: 0245MC
WEIGHT: 3.7 grams (0.13 oz.)

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF to 10μF tantalum) should be located close to the DAC1200.

±12V OPERATION

The DAC1200 is fully specified for operation on ±12V power supplies. However, to use the ±10V and 0 to +10V ranges of the voltage output models, the power supplies must be ±13V or greater. All other voltage output ranges and all current output ranges provide satisfactory operation with ±11.4V supplies. The supplies should be balanced to obtain optimum performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC1200 to prevent noise pick-up. For operation with supplies of less than ±13.5V, use 2.7MΩ and 7.5MΩ resistors in place of the 3.9MΩ and 10MΩ resistors, respectively. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 1, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pick-up. Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

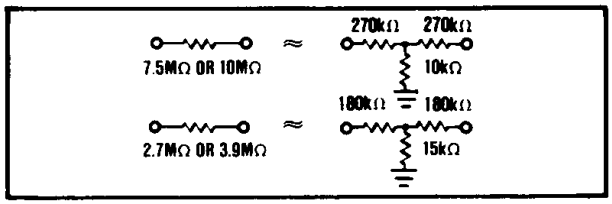


FIGURE 1. Equivalent Resistances.

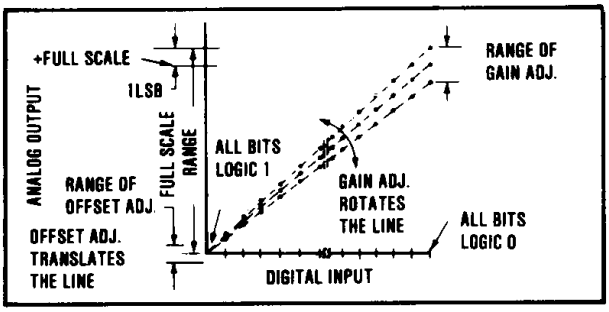


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

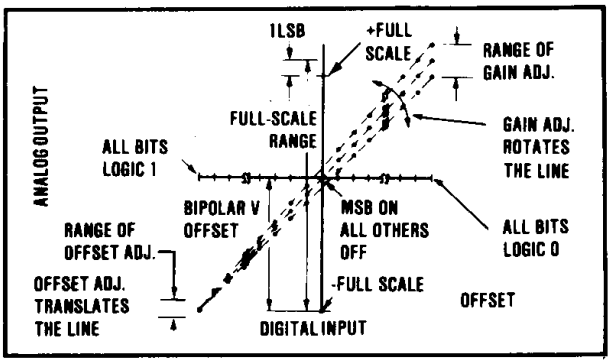


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is −10V. See Table I for corresponding codes. Offset should be adjusted before gain.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the

maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table I for positive full-scale voltages.

TABLE I. Digital Input/Analog Output.

Digital Input	Analog Output	
MSB LSB	0 to + 10V	±10V
000000000000	+9.9976V	+9.9951V
011111111111	+5.0000V	0.0000V
100000000000	+4.9976V	−0.0049V
111111111111	0.0000V	−10.0000V
One LSB	2.44mV	4.88mV

To obtain values for other ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.