National Semiconductor

PRELIMINARY

DAC1242/DAC1243 Process Control DACs

General Description

The DAC1242/1243 are 12-bit digital-to-analog converters with 4-20mA current loop output. The DAC1242 is a current-sinking device, while the DAC1243 provides true current sourcing into a ground referenced load. The digital input registers are similar to an INS8255, allowing direct TTL interfacing to a variety of 8-bit microprocessors (8080, 8085, 8048, 8070, 8073, NSC800, Z80, et al). Interfacing to other microprocessor families or larger computers requires only 1 or 2 TTL packages. The device occupies 4 contiguous bytes of I/O or address space.

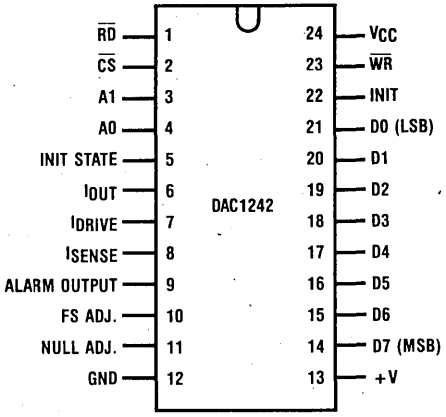
The converters produce a 4-20mA output current proportional to the digital input word with 12-bit resolution, guaranteed monotonicity, and <½LSB non- linearity; a 10-bit guaranteed part is also available. Null and span are internally calibrated to allow use of an external 100Ω, 1% current-sensing resistor with guaranteed null <4mA and full scale >20mA. Null and full-scale may be externally trimmed by the user.

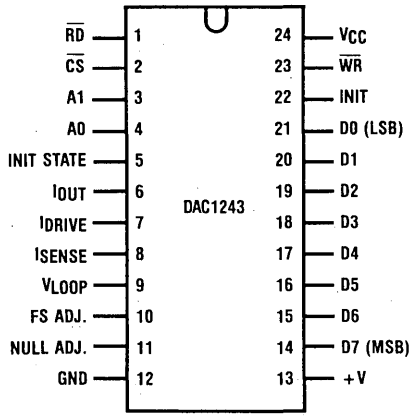
The devices are fully self-contained except for one external current sense resistor (some applications will utilize an external transistor for improved power dissipation). The package is a standard 24-pin ceramic DIP.

Features

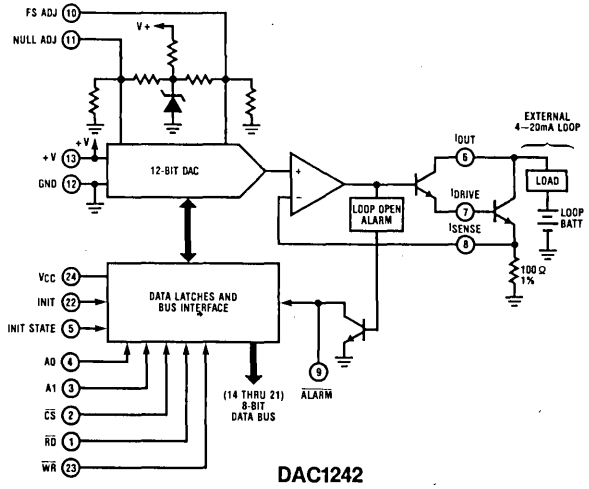
- 4-20mA current-loop output
- 12-bit resolution
- Monotonicity guaranteed
- Open loop alarm
- Data readback capability
- Initialize to zero or full-scale
- Internal reference
- Simple microprocessor interface
- Internal calibration
- No negative supply needed
- Standard 24-pin DIP
- Current sinking output (DAC1242)
- 12 to 60V loop supply (DAC1242)
- Open loop alarm available at pin (DAC1242)
- Simple 1-5V voltage output (DAC1243)
- Current sourcing output (DAC1243)
- 12 to 44V loop supply (DAC1243)

Connection Diagrams—Top Views

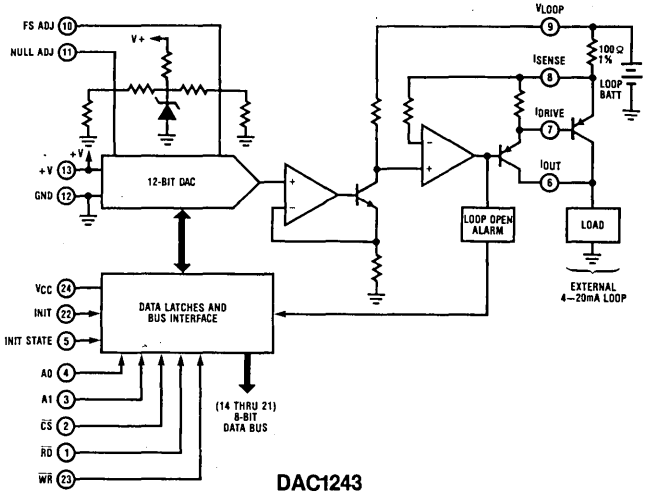




Equivalent Circuits



DAC1242



DAC1243

Command/Data Information

							DATA*							
							MSB							LSB
	INIT	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Initialize	1	X	X	X	X	X	X	X	X	X	X	X	X	X
Write Control Word	0	0	1	0	1	1	1	0	0	0	1	0	0	1
Write Low Data Byte	0	0	1	0	0	0	D	D	D	D	X	X	X	X
Write High Data Byte	0	0	1	0	0	1	D	D	D	D	D	D	D	D
Read Low Data Byte	0	0	0	1	0	0	F	F	F	F	X	X	X	X
Read High Data Byte	0	0	0	1	0	1	F	F	F	F	F	F	F	F
Read Loop-Open Alarm	0	0	0	1	1	0	F	X	X	X	X	X	X	X
Chip De-Select	0	1	X	X	X	X	X	X	X	X	X	X	X	X
	0	X	1	1	X	X	X	X	X	X	X	X	X	X

*Positive Logic, e.g., 0 = Low, 1 = High; X = Don't Care; D = Data to DAC; F = Data from DAC