DAPDNA-2

Dynamically Reconfigurable Processor

■ DAPDNA® Architecture

The **DAPDNA Dynamically Reconfigurable Processor** is configurable during run-time to instantly (in one clock) provide the optimal hardware circuitry for application in demand.

The DAPDNA has a dual-core architecture, comprised of a RISC core (the DAP) and a dynamically reconfigurable matrix (the DNA).
This platform provides the processing performance of hardware with the flexibility of software.

DAP (Digital Application Processor)
- High-performance RISC processor
- Controls the dynamic reconfiguration of the DNA

DNA (Distributed Network Architecture)
- Dynamically reconfigurable
- Two-dimensional array of 376 Processing Elements (PEs)
- Allows arbitrary configuration of the degree of parallelism and pipeline depth

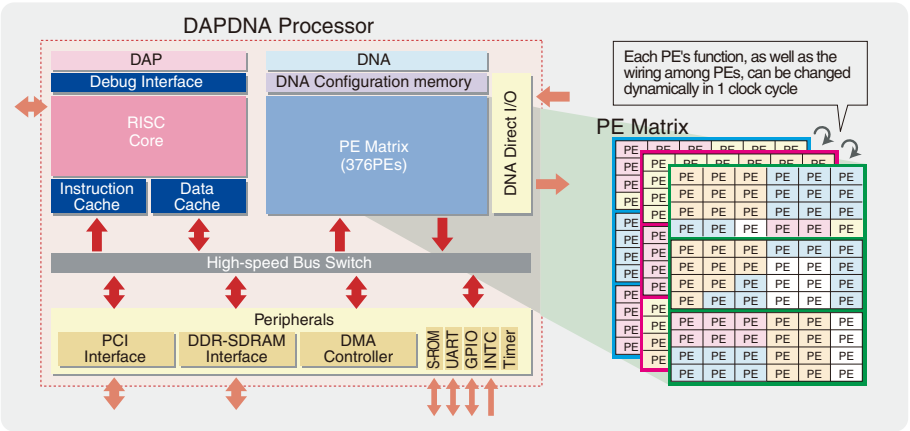

Fig.1 DAPDNA Architecture

■ Dynamic Reconfiguration

The DAPDNA-2's dynamic reconfiguration enables three beneficial usage models.

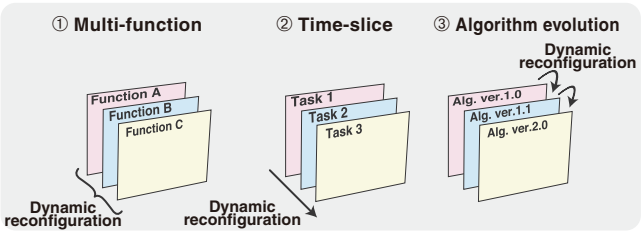

Fig.2 Dynamic Reconfiguration usage

① Multi-function
- Function can be selected and executed according to changes in operating conditions (e.g.different encoding methods in incoming data)

② Time-slice
- Algorithms can be partitioned in time
- As soon as one processing task is completed, the hardware immediately moves on to the next task

③ Algorithm evolution
- As algorithm evolves with time (as in the case of virus definition for firewall), change is incorporated dynamically into hardware

■ DNA Direct I/O

The DAPDNA-2 has six channels of DNA Direct I/O,which provides the interface for transfering data directly onto or out of the PE Matrix.

Each channel of DNA Direct I/O is 32-bit wide and operates at the maximum DAPDNA-2 system clock frequency of 166 MHz, reaching 32 Gbps. The DNA Direct I/O can operate synchronously on the system clock, or can be controlled by an external clock at a different frequency.

Multiple DAPDNA-2 processors can be connected through the DNA Direct I/O and integrated into a single system at 16 Gbps throughput.

The DNA Direct I/O can be also used to communicate directly with external devices, bringing data in for processing on the PE Matrix, bypassing the Bus Switch and memory interface.

■ Guaranteed Clock Speed

The DAPDNA-2's unique architecture guarantees clock speed regardless of resource usage. Simulation result matches hardware performance accurately, eliminating the time-consuming process of design iteration. This feature reduces the system development time considerably.

■ Large On-chip RAM

Large on-chip memory reduces the need to access off-chip memory, a process which often becomes a performance bottleneck. This feature allows the PE Matrix to provide the maximum possible parallel processing performance.

DAPDNA-2 Processing Elements (PEs)

PE	Quantity	Function
EXE	168	32-bit, 2 input 1 output execution Includes 56 multipliers (16-bit input, 32-bit output)
RAM	32	Internal memory, 16KB each, total 512KB
DLE	136	32-bit, 2 input 2 output delay Configurable delay length
CxE	24	Address generation Generic counter
LDx	8	Data input into DNA
STx	8	Data output from DNA
Total	376	

DAPDNA-2 Specification

DAP		32-bit RISC processor
		8 KB instruction cache, 8 KB data cache
DNA		Two-dimensional array of dynamically reconfigurable PEs (376PEs)
	Number of configurations	Four banks (one foreground bank, three background banks, Background banks can be loaded from external memory for unlimited number of configurations to be used.)
External interfaces	DNA Direct I/O	166 MHz maximum (can be synchronized to external clock) 32-bit width 6 I/O channels : up to 32 Gbps bandwidth (Can be used to connect multiple DAPDNA-2 processors)
	DDR-SDRAM	166 MHz, 64 bit DDR-SDRAM interface Supports up to 512 MB
	PCI	33 MHz, 32-bit PCI interface (3.3 V tolerant)
	ROM	SPI serial ROM interface for boot or program storage
	External interrupts	8
	Others	2 UART channels 16 GPIO channels 1 synchronous serial (master) channel
Operating frequency		166MHz
Power supply		2.5 V (I/O) 1.2 V (core)
Package		1156-pin FC-BGA

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