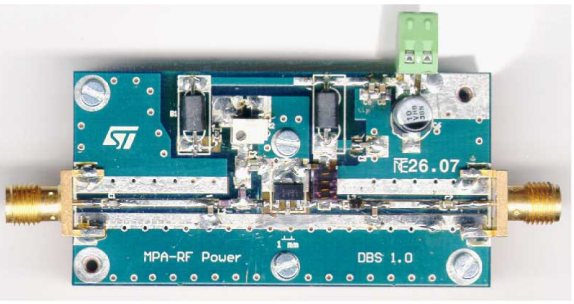
DB-499D-470

RF power amplifier using 1 x START499D NPN RF silicon transistor

Preliminary Data

Features

- Excellent thermal stability
- Frequency: 430 - 470 MHz
- Supply voltage: 3.6 V
- Output power: 29 dBm
- Power gain: 19 dB
- Efficiency: 52 %
- BeO free amplifier



AM02116v1

Mechanical specification:
L = 60 mm, W = 30 mm

Description

The DB-499D-470 is a NPN silicon RF power amplifier designed for UHF 2-way radio applications

Table 1. Device summary

Order codes
DB-499D-470

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = +25 °C)

Symbol	Parameter	Value	Unit
V_{CEO}	Collector - emitter voltage	4.5	V
V_{EBO}	Emitter - base voltage	1.5	V
I_C	Collector - current	1.0	A
P_{DISS}	Power dissipation	1.7	W
T_J	Max. operating junction temperature	150	°C
T_{STG}	Storage temperature	-65 to +150	°C

2 Electrical characteristics

T_A = +25 °C, V_{CC} = 3.6 V, I_{cq} = 400 mA, unless otherwise specified

Table 3. RF data

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
f	Frequency range		430		470	MHz
P_{out}	Output power	P_{IN} = 10 dBm		29		dBm
G_p	Power gain	P_{OUT} = 29 dBm		19		dB
N_D	Efficiency	P_{OUT} = 29 dBm		51 - 54		%
H2	2nd harmonic	P_{IN} = 10 dBm		-30		dBc
H3	3rd harmonic	P_{IN} = 10 dBm		-50		dBc

3 Typical performance

3.1 V_{CC} = 3.6, I_{CQ} = 400 mA

Figure 1. Gain vs output power

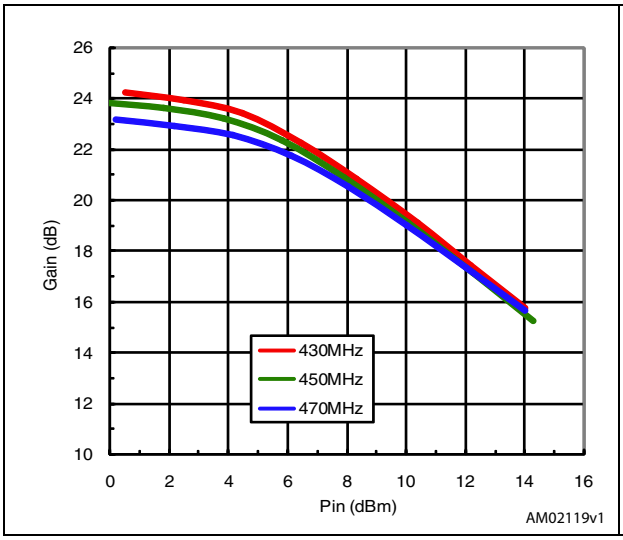


Figure 2. Efficiency vs Pout

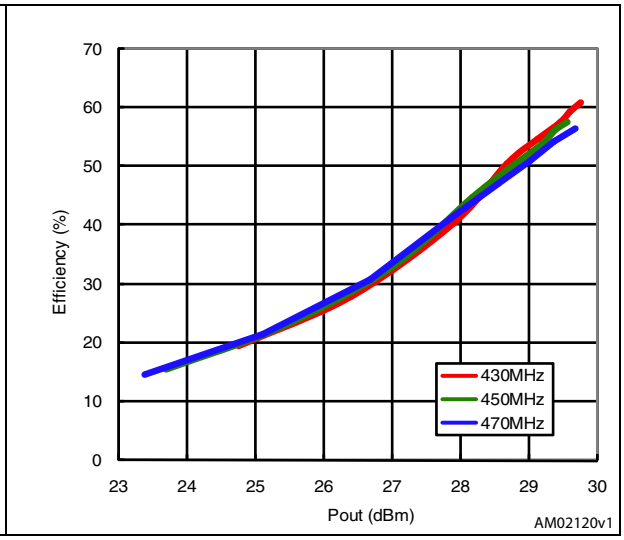
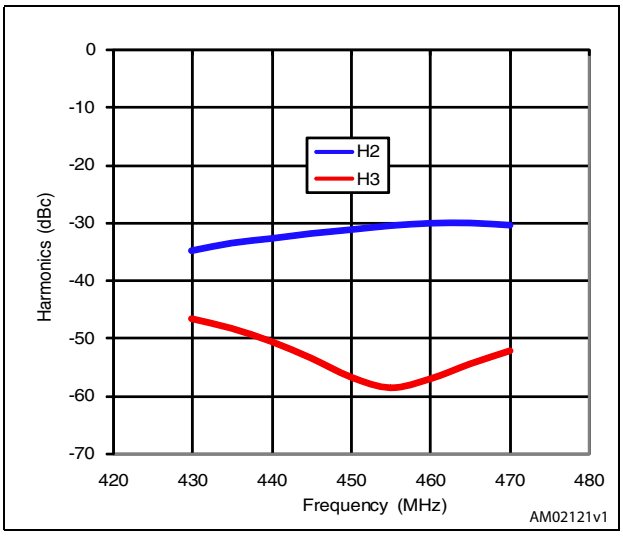


Figure 3. Harmonics



4 Test circuit

Table 4. Test circuit schematic

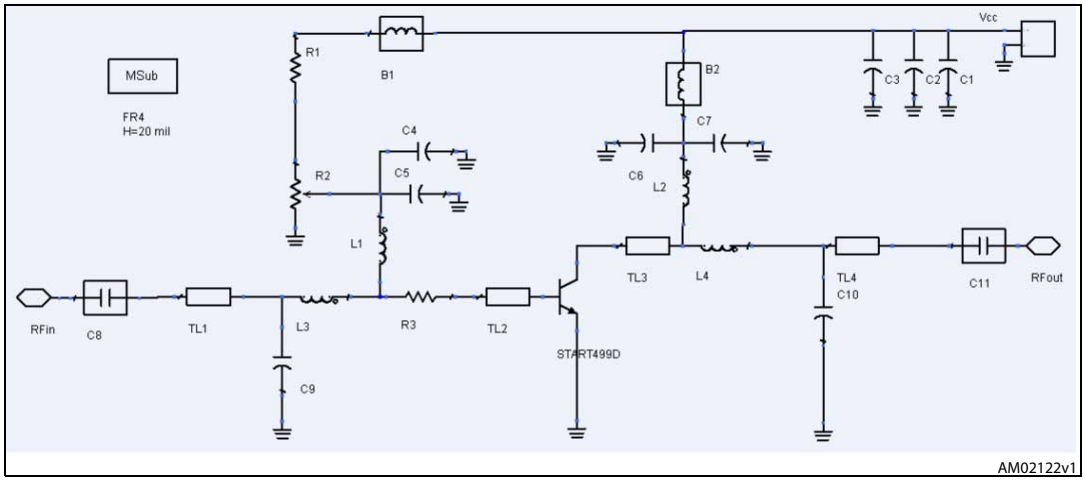


Table 5. Components part list for DB-499D-470

Component ID	Description	Value	Case size	Manufacturer	Part code
C1	Capacitor	10 µF	0603	MURATA	GRM188R60J106ME47
C2	Capacitor	10 nF	0603	MURATA	GRM188R71H103KA01
C3	Capacitor	100 nF	0603	MURATA	GRM188R71H104KA01
C5, C7	Capacitor	1000 pF	0603	MURATA	GRM188R71H102KA01
C4,C6,C8,C11	Capacitor	100 pF	0603	MURATA	GRM1885C1H101JA01
C9	Capacitor	12 pF	0603	MURATA	GRM1885C1H120JA01
C10	Capacitor	15 pF	0603	MURATA	GRM1885C1H150JA01
L1	Inductor	47 nH	0603	Coilcraft	0603HP-47NXJL
L2	Inductor	22 nH	1812	Coilcraft	1812SMS-22NJLB
L3	Inductor	8.2 nH	0603	Coilcraft	0603HP-8N2XJL
L4	Inductor	2.55 nH	0906	Coilcraft	0906-3JLB
B1, B2	Ferrite Bead		0603	PANASONIC	EXCELDRC35C
R1	Resister	470 Ω	0603		
R2	Potentiometer	10 kΩ		Bourns electronics	3214W-1-103E
R3	Resister	4.7 Ω	0603		
TL1	Transmission line	L = 14 mm	W=0.9 mm		
TL2		L = 2 mm	W=0.9 mm		
TL3		L = 3.6 mm	W=0.9 mm		
TL4		L = 12.5 mm	W=0.9 mm		
BJT1	BJT			STMicroelectronics	START499D
Board	FR4 Er=4.5 THk = 0.020" 1 OZ Cu both sides				

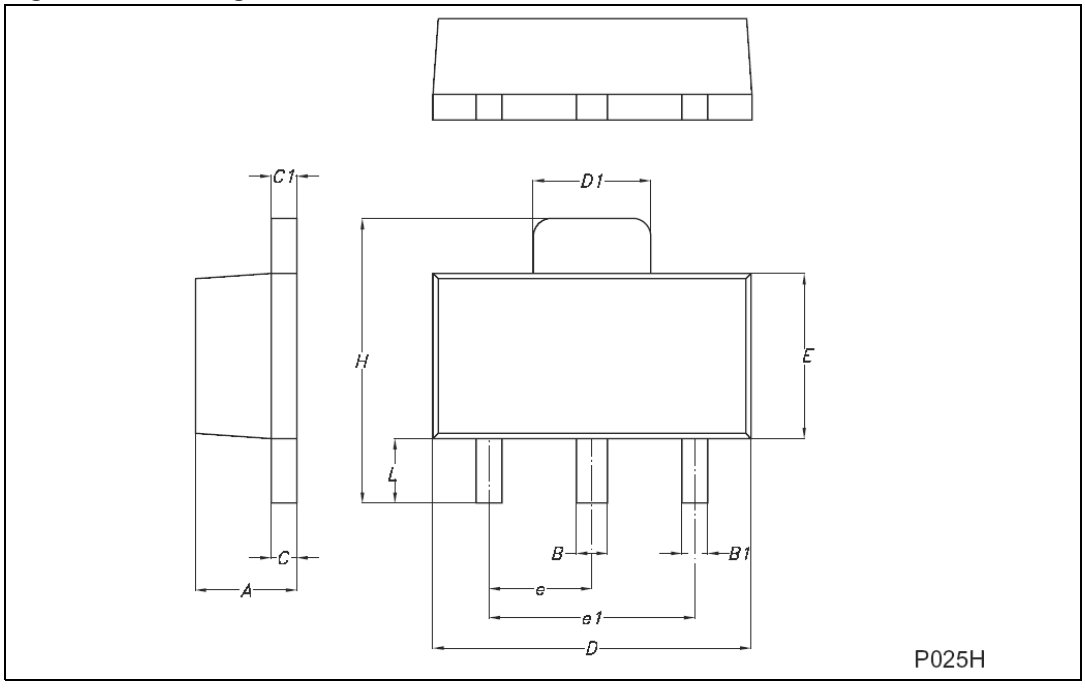
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 6. SOT-89 mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	1.4		1.6	55.1		63.0
B	0.44		0.56	17.3		22.0
B1	0.36		0.48	14.2		18.9
C	0.35		0.44	13.8		17.3
C1	0.35		0.44	13.8		17.3
D	4.4		4.6	173.2		181.1
D1	1.62		1.83	63.8		72.0
E	2.29		2.6	90.2		102.4
e	1.42		1.57	55.9		61.8
e1	2.92		3.07	115.0		120.9
H	3.94		4.25	155.1		167.3
L	0.89		1.2	35.0		47.2

Figure 4. Package dimensions

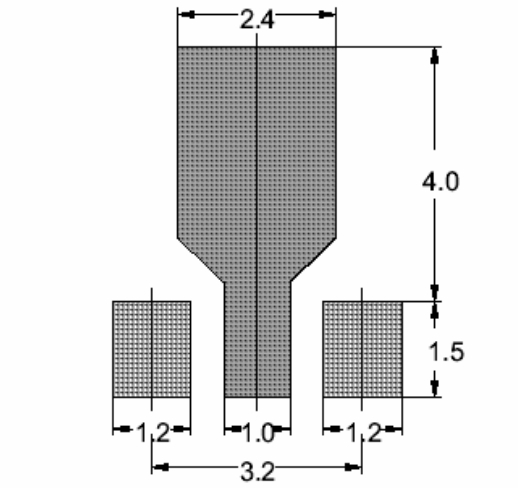


5.1 Thermal pad and via design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 5. Pad layout details



SOT-89 pattern.
Minimum Pad Size (dimensions in mm)

5.2 Soldering profile

Figure 6 shows the recommended solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

Figure 6. Recommended solder profile

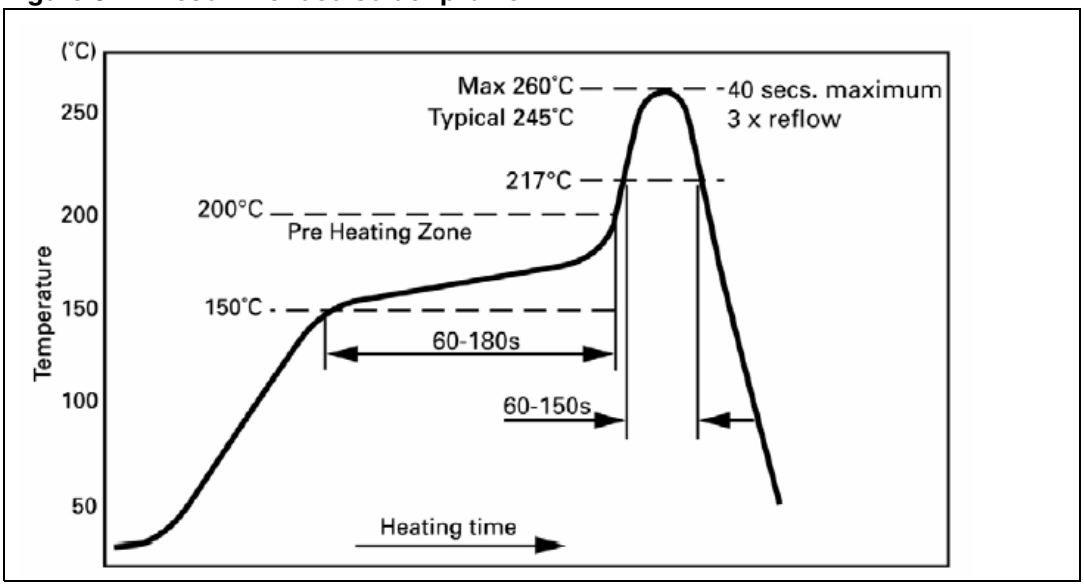


Figure 7 shows the recommended solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 7. Recommended solder profile for leaded devices

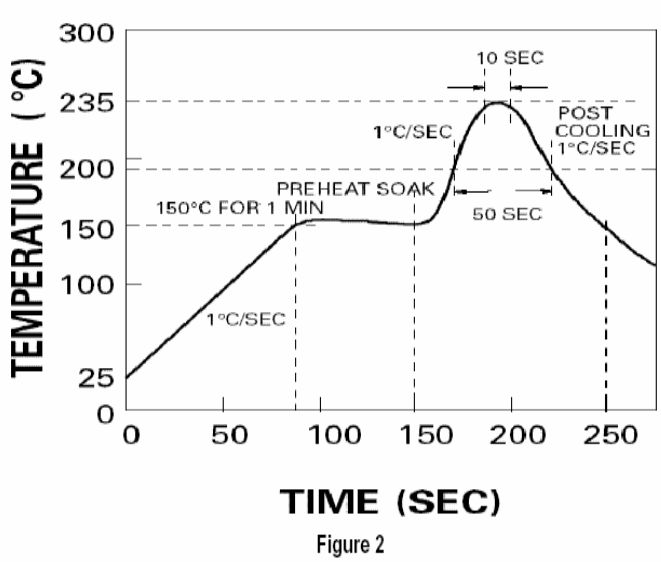
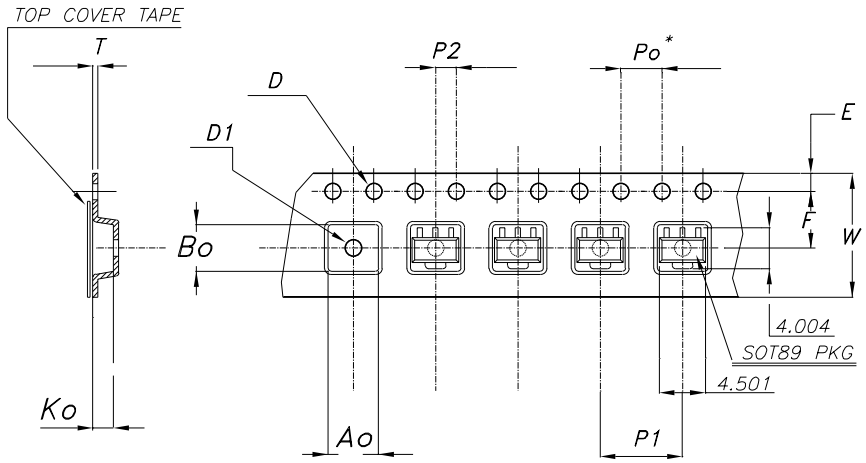


Figure 8. Reel information



Ao	4.91	±0.10
Bo	4.52	±0.10
Ko	1.90	±0.10
F	5.50	±0.10
E	1.75	±0.10
W	12	±0.30
P2	2	±0.10
Po	4	±0.10
P1	8	±0.10
T	0.30	±0.10
D	ø1.55	±0.05
D1	ø1.60	±0.10

NOTES :

– ACCEPTANCE SPEC. Nr. 0031932

* – CUMULATIVE TOLERANCE OF 10 SPROCKET HOLES IS ±0.20

– UNLESS OTHERWISE SPECIFIED TOLERANCE: ±0.10

– MATERIAL CODE : 3CP90069

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
23-Feb-2009	1	First release

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