

DBL 2036

PAL / SECAM DETECTOR FOR A VTR

The DBL 2036 is a monolithic integrated circuit designed for use the PAL / SECAM Signal Detector.

FUNCTION

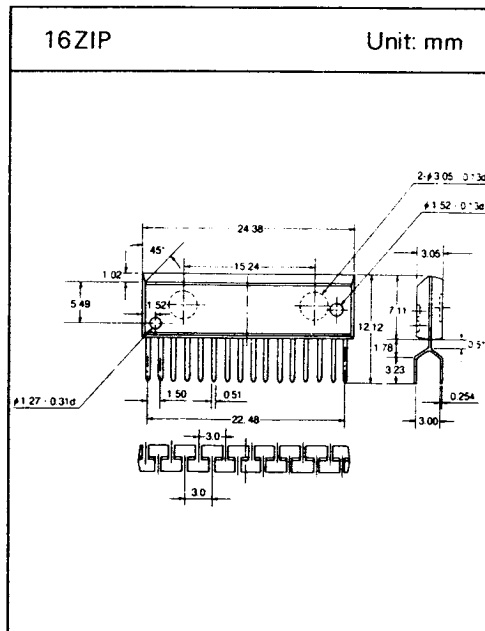
- Burst Gate and Limit Amp.
- F-V Converter
- Master-Slave F/F
- Level Shifter and Peak detector
- Diff Amp and Comparator

FEATURES

- Possible to detect high sensitivity for variation of noise and burst input level
- Very few external Components
- built-in display LED driver.
- Possible to use burst Gate Pulse of positive or negative charge
- Operating Supply voltage Range($V_{CC}=4.5V \sim 6.0V$)

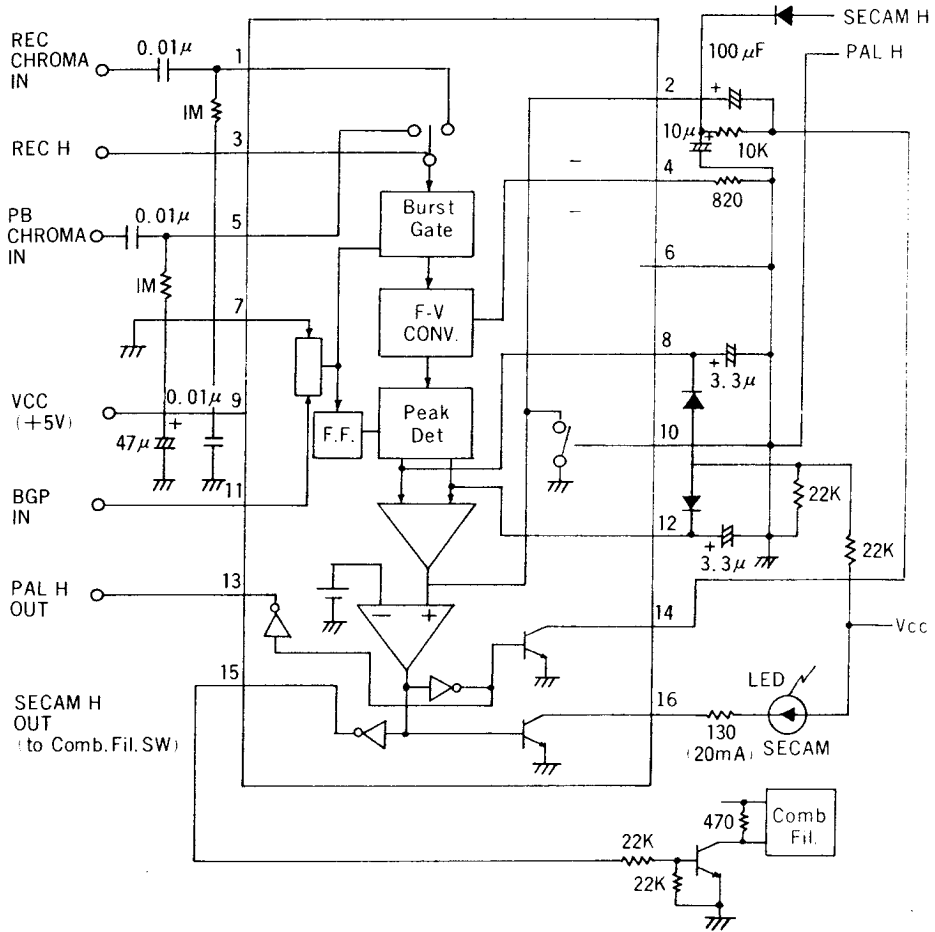
MAXIMUM RATINGS($T_a=25^{\circ}C$)

Characteristic	Symbol	Rating	Limit
Maximum Supply Voltage	$V_{CC}(\max)$	7.0	V
Allowable Power Dissipation	$P_d(\max)$	130	mW
Operating Temperature	T_{OPR}	$-10 \sim +70$	$^{\circ}C$
Storage Temperature	T_{STG}	$-55 \sim +150$	$^{\circ}C$



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□ BLOCK DIAGRAM AND APPLICATION CIRCUIT



note 1 : Pin 7 → input, pin 11 → V_{CC} When BGP is Positive charge.

note 2 : Pin 10 open When pin 10 is not use.

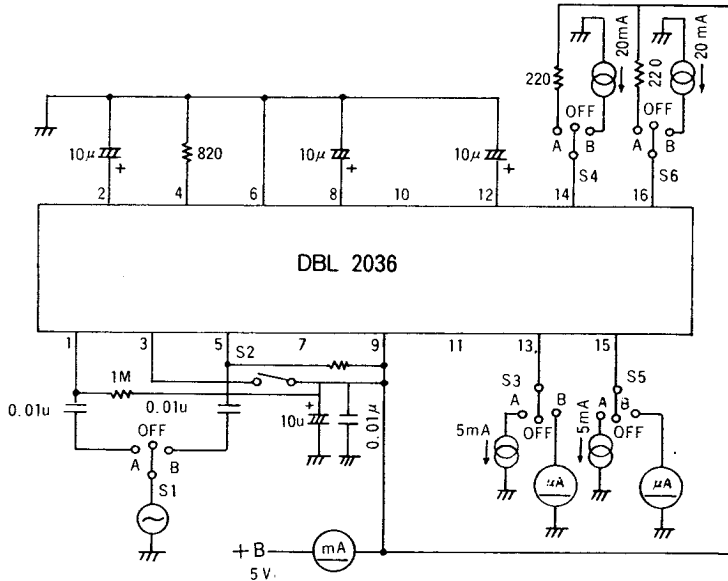
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ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vcc = 5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Dissipation Current	I_{CC}		6.7	9.6	12.4	mA
F-V Variable Gain(PB)	ΔV_P	Difference between 4.4MHz and 4.25MHz	75	105	135	mV
F-V Variable Gain(REC)	ΔV_R	"	75	105	135	mV
PAL→SECAM Difference of inverter voltage	V_{S12}		35	50	65	mV
R/P Convert Threshold Voltage	V_{TH}		2.0	2.35	2.7	V
BG Threshold Voltage I	V_{TH1}		1.5	1.7	1.9	V
" II	V_{TH2}		3.2	3.4	3.6	V
Forced PAL Threshold Voltage	V_{TH3}		1.3	1.7	2.2	V
Forced SECAM Threshold Voltage	V_{TH4}		1.7	2.0	2.3	V
Detector Output Voltage I	V_{D1}	ID = 5mA	4.0	4.2	4.4	V
" II	V_{D2}	ID = 5mA	4.0	4.2	4.4	V
Detector output Leak Current I	$I_{L1}(\text{Leak})$		—	0	5	μA
" II	$I_{L2}(\text{Leak})$		—	0	5	μA
Pin 12 DC Voltage	V_{12}	4.43MHz 100mV p-p input	2.1	2.6	3.1	V
Input Burst Level	V_{IN}		60	100	200	mVp-p
Drive Saturation Voltage I	V_{D1}	ID = 20mA	—	170	400	mV
" II	V_{D2}	ID = 20mA	—	170	400	mV

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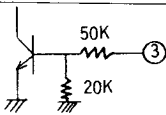

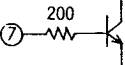
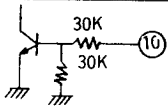
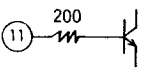
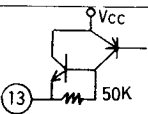

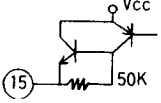

TEST CIRCUIT



	S1	S2	S3	S4	S5	S6	Condition
I_{CC}	off	off	off	off	off	off	$V_9 = 5V$
V_P	B	↓	↓	↓	↓	↓	Input : 100mVp-p, 4.4MHz and 4.25MHz, Measure Voltage Difference of V_8 (or V_{12})
V_R	A	on	↓	↓	↓	↓	the same as above
V_{8-12}	off	off	↓	A	↓	↓	$V_7 = 0V, V_{11} = 5V, V_8 = 1.9V, V_{12} = 1.9V + \alpha, V_{14} > 4V, \alpha (0V \uparrow)$
V_{3TH}	↓	↓	↓	off	↓	↓	$V_1 = V_7 = V_{11} = 0V, V_8 < 0.1V, \text{Measure } V_3 (0V \uparrow)$
V_{7TH}	↓	↓	↓	↓	↓	↓	$V_{11} = 5V, V_8 > 1.0V, \text{Measure } V_7 (0V \uparrow)$
V_{11TH}	↓	↓	↓	↓	↓	↓	$V_7 = 0V, V_8 > 1.0V, \text{Measure } V_{11} (5V \downarrow)$
V_{10TH}	↓	↓	↓	↓	↓	A	$V_7 = V_{11} = 0V, V_{16} > 4V, \text{Measure } V_{10} (0V \uparrow)$
V_{2TH}	↓	↓	↓	A	↓	off	$V_8 = V_{12} = 3V, V_{14} > 4V, \text{Measure } V_2 (0V \uparrow)$
V_{13}	↓	↓	A	off	↓	↓	Pin13 Voltage of $V_2 = 0V, \text{Drive Current } 5mA$
V_{15}	↓	↓	off	↓	A	↓	Pin15 Voltage of $V_2 = 3V, \text{Drive Current } 5mA$
$I_{13}(\text{leak})$	↓	↓	B	↓	off	↓	Drive Current when $V_2 = 3V, \text{Pin } 13 = GND$
$I_{15}(\text{leak})$	↓	↓	off	↓	B	↓	Drive Current when $V_2 = 0V, \text{Pin } 15 = GND$
$V_{14}(\text{sat})$	↓	↓	↓	B	off	↓	$V_2 = 0V, \text{Measure Pin14 Voltage, Drive Current } 20mA$
$V_{16}(\text{sat})$	↓	↓	↓	off	↓	B	$V_2 = 3V, \text{Measure Pin16 Voltage, Drive Current } 20mA$

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I/O FUNCTION

Pin	Function	I/O Impedance		DC voltage	Comment
1	REC Chroma in	10Kohm		4.1V	
2	SECAM Holder				SECAM > 2.0V
3	R/P Control			0V (PB)	REC > 2.4V
4	Current Source	Open Emitter		410mV	
5	PB Chroma In	10Kohm		4.1V	
6	GND			0V	
7	BGP In	Pulse			Burst Gate > 1.7V
8	Peak Filter 1	Emitter follower			
9	V _{cc}			5V	
10	PAL high In			0V	Forced PAL > 1.7V
11	BGP In	Pulse			Burst Gate > 3.4V
12	Peak Filter 2	Emitter follower			
13	PAL high out			4.1V (PAL)	Until 5mA
14	PAL Drive	NPN Open Collector			Until 25mA
15	SECAM high out			4.1V (SECAM)	Until 5mA
16	SECAM Drive	NPN Open Collector			Until 25mA