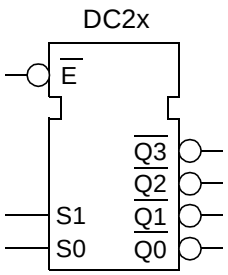
Description

DC2x is a family of two-to-four line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

HDL Syntax

Verilog ..... DC2x *inst_name* (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

VHDL..... *inst_name*: DC2x port map (Q0N, Q1N, Q2N, Q3N, EN, S0, S1);

Pin Loading

Pin Name	Equivalent Loads	
	DC21	DC22
S0	3.2	3.2
S1	3.2	3.2
EN	1.0	4.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC21	8.0	TBD	17.8
DC22	10.0	TBD	20.7

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	6	8 (max)
DC21	From: Sx To: QN	t_{PLH} t_{PHL}	0.26 0.35	0.30 0.42	0.35 0.55	0.41 0.69	0.46 0.82
	From: EN To: QN	t_{PLH} t_{PHL}	0.38 0.47	0.41 0.54	0.48 0.68	0.53 0.80	0.59 0.93
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
DC22	From: Sx To: QN	t_{PLH} t_{PHL}	0.23 0.42	0.33 0.57	0.45 0.73	0.60 0.90	0.71 1.02
	From: EN To: QN	t_{PLH} t_{PHL}	0.27 0.52	0.37 0.67	0.50 0.82	0.64 0.99	0.76 1.11

Delay will vary with input conditions. See page 2-17 for interconnect estimates.