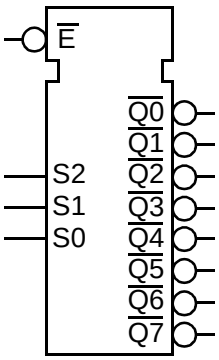
Description

DC3x is a family of three-to-eight line decoder/demultiplexers with active low enable.

Logic Symbol



Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Core Logic

HDL Syntax

Verilog ..... DC3x *inst_name* (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

VHDL..... *inst_name* DC3x port map (Q0N, Q1N, Q2N, Q3N, Q4N, Q5N, Q6N, Q7N, EN, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads	
	DC31	DC32
S0	5.8	5.7
S1	5.4	5.7
S2	5.3	5.3
EN	1.0	1.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DC31	20.0	TBD	39.8
DC32	29.0	TBD	61.2

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	2	4	5	7 (max)
DC31	From: Sx To: QN	t_{PLH} t_{PHL}	0.33 0.50	0.36 0.59	0.42 0.76	0.44 0.84	0.49 1.00
	From: EN To: QN	t_{PLH} t_{PHL}	0.51 0.70	0.55 0.77	0.63 0.94	0.67 1.03	0.73 1.20
	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
DC32	From: Sx To: QN	t_{PLH} t_{PHL}	0.23 0.43	0.33 0.60	0.44 0.78	0.57 0.97	0.68 1.12
	From: EN To: QN	t_{PLH} t_{PHL}	0.80 1.09	0.90 1.22	1.02 1.38	1.15 1.58	1.25 1.74

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic