DCP0606Y

Datasheet

Automotive 6 V - 6 A step-down converter

Maturity status link
DCP0606Y

Features

- AEC-Q100 Grade 1 qualified
  - Operating junction temperature range: -40 °C to +150 °C
- Designed for 3.3 V and 5 V power rails
- 6 A continuous output current
  - 6 A typical efficiency = 93% @ fsw = 2.25 MHz, Vin = 5 V, Vout = 3.3 V
- Integrated 11 mΩ MOSFETs for high efficiency
- Adjustable output voltage down to 0.6 V
- 1.5% Output voltage accuracy
- Fixed output voltage option on request
- Selectable switching frequency from 1.8 to 4 MHz with dithering
- Pulse skip mode to optimize light load efficiency
- OV / OC / OT auto-recovery protections
- Power Good output
- Output voltage tracking
- External synchronization with programmable phase shift
- DCP0606Y in QFN 2x3 mm package with wettable flanks

Applications

- High current low voltage post regulation
- Telematics, HUD, Infotainment, Multimedia and Camera Digital Core power supply
- ADAS power supply

Description

The DCP0606Y is a high efficiency monolithic step-down synchronous switching regulator designed to deliver up to 6 A continuous current. The IC operates from 2.9 V to 6 V input voltage.

The DCP0606Y features low-resistance integrated N-channel MOSFETs and diode emulation working mode for optimum efficiency over all the loading range.

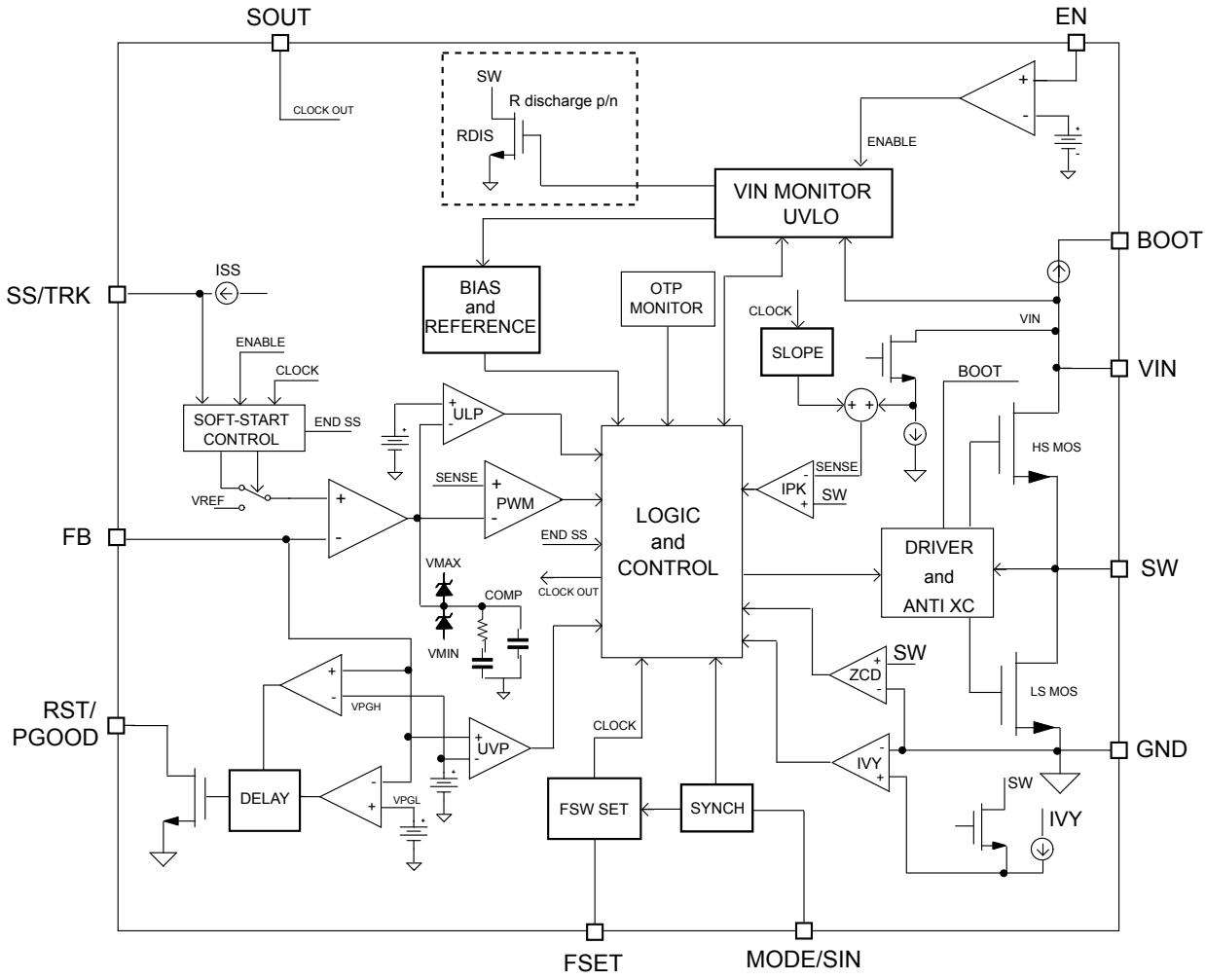
The integrated 0.6 V reference allows the regulation of output voltages with ± 1.5% accuracy over temperature variations. The switching frequency is externally adjustable between 1.8 MHz and 4 MHz.

The soft-start duration can be adjusted with an external capacitor or the same SS/TRK pin can be used for output voltage sequencing while the RST/PGOOD pin provides real-time information on the output voltage.

DCP0606Y is available in QFN 2 x 3 mm with 11 leads with wettable flanks.

1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin connection (top view)**

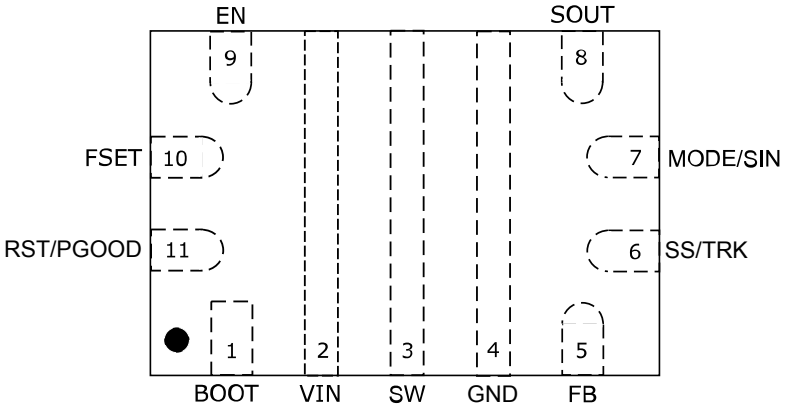


Table 1. **Pin description**

Pin #	Symbol	Function
1	BOOT	Bootstrap pin for integrated n-channel HS MOS driving. A 100 nF ceramic capacitor must be placed between BOOT and SW pin.
2	VIN	Power input voltage and device internal logic supply. Bypass VIN pin to GND pin close to the IC package with high quality MLCC capacitors (22 µF min. suggested).
3	SW	Output inductor connection. The pin is internally connected to the embedded MOSFETs (high-side source and low-side drain). Connect directly to the inductor.
4	GND	Signal and Power ground connection.
5	FB	Control loop voltage feedback. FB pin is output voltage sensing through an external voltage divider.
6	SS/TRK	Soft-Start / Tracking pin. A capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing. A maximum 47nF capacitor is expected on this pin.
7	MODE/SIN	Dynamic pin selection between Low Consumption Mode (LCM, active low) and Low Noise Mode operation (LNM, active high). This pin is also used for synchronization with an external clock (clock-in function).
8	SOUT	Clock out pin for synchronization with a slave device. The out-of-phase delay can be selected by the proper resistor mounted between SOUT and GND. If no shifted clock is required, SOUT must be shorted to GND to optimize light load efficiency.
9	EN	Enable pin. Pull down/up to disable/enable the device. Do not leave floating.
10	FSET	Connect an external resistor to program the oscillator frequency.
11	RST/PGOOD	Reset/Power good pin. The RST/PGOOD open collector output is driven low when the output voltage is out of regulation and it is released after a fixed 2 ms typ. delay once the output voltage is inside the PGOOD window. Pull up to a voltage lower than VIN; if not used, it can be left floating.

3 Typical application circuit

Figure 3. **Typical application**

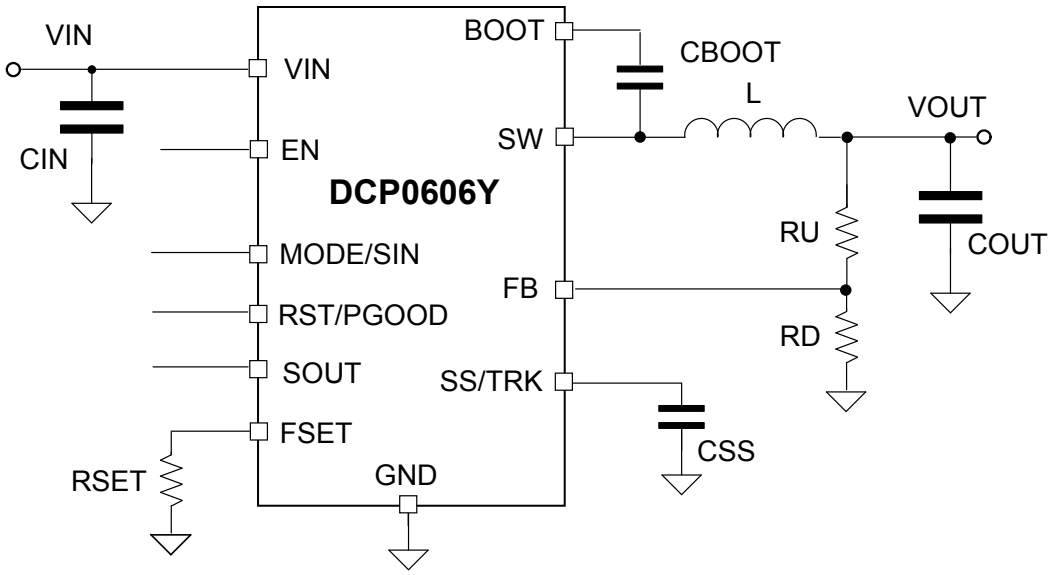


Table 2. **Typical application components – 3.3 Vout**

Symbol	Value	Description	Note
C_{IN}	2x 22 µF	Input capacitor	
L	470 nH	Inductor	
R_U	68 kΩ	Up resistor	External divider for VOUT programming
R_D	15 kΩ	Down resistor	
R_{SET}	27 kΩ	2.25 MHz / Mid COUT	See Frequency selection table
C_{BOOT}	100 nF	Bootstrap Capacitor	
C_{SS}	10 nF	Soft-start capacitor – Tss = 3 ms	See Section 6.4
C_{OUT}	3x 22 µF	Output capacitor	

Table 3. **Typical application components – 1.2 Vout**

Symbol	Value	Description	Note
C_{IN}	2x 22 µF	Input capacitor	
L	130 nH	Inductor	
R_U	15 kΩ	Up resistor	External divider for VOUT programming
R_L	15 kΩ	Down resistor	
R_{SET}	15 kΩ	4 MHz / MID COUT	See Frequency selection table
C_{BOOT}	100 nF	Bootstrap Capacitor	
C_{SS}	10 nF	Soft-start capacitor – Tss = 3 ms	See Section 6.4
C_{OUT}	3x 47 µF	Output capacitor	

4 Maximum ratings

Stressing the device above the ratings listed in may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VIN	Maximum pin voltage referred to GND pin	-0.3	6.5	V
EN, MODE/SIN, FSET	Maximum pin voltage referred to GND pin	-0.3	VIN + 0.3	V
SW (1)	Maximum pin voltage referred to GND pin	-0.3	VIN + 0.3	V
		-3 for 10 ns	7.5 for 10 ns	V
VBOOT	Maximum pin voltage referred to GND pin	-0.3	VSW + 5.5	V
RST/PGOOD	Maximum pin voltage referred to GND pin	-0.3	VIN + 0.3	V
SOUT	Maximum pin voltage referred to GND pin	-0.3	3.6	V
SS/TRK	Maximum pin voltage referred to GND pin	-0.3	VIN + 0.3	V
FB	Maximum pin voltage referred to GND pin	-0.3	5.5	V
IHS, ILS	High-side/low-side switch RMS current		6	A
T_J	Junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	- 65	150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C

1. *Peak voltage during switching activities caused by parasitic layout elements.*

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction-ambient measured in the evaluation board	42	°C/W

Table 6. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection voltage	HBM	2	kV
		CDM non-corner pins	500	V
		CDM corner pins	750	V

Table 7. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{IN}	Operating input voltage range	2.9 to 6	V
T_J	Operating junction temperature range	-40 to 150	°C

5 Electrical characteristics

V_{IN} = 5 V, T_J = -40 °C to +150 °C, typical values are at T_J = 25 °C unless otherwise specified.

Table 8. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN-UVLO}$	V_{IN} undervoltage lockout	Rising input voltage	2.55	2.70	2.85	V
		Falling input voltage	2.45	2.60	2.75	V
		Hysteresis		100		mV
I_Q	Quiescent current	V_{EN} = 5 V; SOUT=GND, MODE = 0 V, V_{FB} = 0.65 V, SW = GND, BOOT = 4.5 V, not switching, T_J = 25 °C (1) (2)		10	25	µA
		V_{EN} = 5 V; SOUT = GND, MODE = 0 V, V_{FB} = 0.65 V, SW = GND, BOOT = 4.5 V, not switching (1) (2)		10	60	µA
I_{OFF}	Shutdown current	V_{EN} = GND, SW = GND, T_J = 25 °C		3	4.5	µA
		V_{EN} = GND, SW = GND		3	30	µA
$R_{DS(ON)-H}$	High side MOSFET ON resistance	V_{IN} = 5 V, I_{SW} = 1 A		11	20	mΩ
		V_{IN} = 3.3 V, I_{SW} = 1 A		13	25	mΩ
$R_{DS(ON)-L}$	Low side MOSFET ON resistance	V_{IN} = 5 V, I_{SW} = 1 A		11	20	mΩ
		V_{IN} = 3.3 V, I_{SW} = 1 A		13	25	mΩ
I_{PK}	Peak current limit HS MOS sensing	(3)	8.1	9.0	9.9	A
I_{vy}	Valley current limit LS MOS sensing	(3)	6.7	8.0	9.2	A
I_{NEG}	Negative current limit LS MOS sensing	LNM sinking or LCM V_{OUT} overvoltage (3)		-3		A
T_{ON_MIN}	Minimum On Time	MODE/SIN = V_{IN}		50	75	ns
T_{OFF_MIN}	Minimum Off Time	BOOT-SW < 2.3 V (Forced when BOOT recharge requested)		60		ns
F_{SW}	Switching frequency	Refer to F_{SET} selection table	1.62	1.8	1.98	MHz
			2.025	2.25	2.475	MHz
			3.15	3.5	3.85	MHz
			3.6	4	4.4	MHz
R_{DIS}	Output discharge resistance	V_{IN} > = 2.2 V, EN = 0 – dedicated p/n		50		Ω
V_{FB}	Feedback voltage			0.600		V
	Accuracy	T_J = 25 °C	-1		+1	%
		T_J = -40 °C to 150 °C	-1.5		+1.5	%
I_{FB_LKG}	FB leakage current	V_{FB} = 0.68 V			150	nA
Synchronization and MODE/SIN						
V_{SOUTH}	Clock-out high-level	R_{SOUT} = 75 k		2.6	V_{IN}	V
V_{SOUTL}	Clock-out low-level			0		V
f_{CLKIN}	Synchronization range	R_{FSET} = 100 k or 33 k or 10 k	1.62			MHz

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{CLKIN}	Synchronization range	R_{FSET} = 47 k or 15 k or 4.7 k, Tj = 25 °C			4.40	MHz
		R_{FSET} = 47 k or 15 k or 4.7 k			4.20	MHz
$PHASE_{SOUT}$	Clock-out phase shift on S_{OUT} pin	2.25 MHz clock-in on MODE/SIN, R_{SOUT} = 75 k		90°		
		2.25 MHz clock-in on MODE/SIN, R_{SOUT} = 100 k		120°		
		2.25 MHz clock-in on MODE/SIN, R_{SOUT} = N.M.		180°		
$T_{CLKINMIN}$	Allowed pulses width on MODE/SIN pin for synchronization		30			ns
$V_{MODE/SINH}$	MODE input high voltage		1.2			V
$V_{MODE/SINL}$	MODE input low voltage				0.35	V
Overvoltage Protections						
V_{OVP}	Overvoltage trip (V_{OVP}/V_{FB})	V_{FB} rising	115	120	125	%
V_{OVP_HYST}	Overvoltage Hysteresis			3		%
Enable and Reset / Power Good						
V_{ENH}	EN input high voltage threshold	EN rising	1.1	1.2	1.3	V
V_{ENL}	EN input low voltage threshold	EN falling	0.9	1.0	1.1	V
V_{PGL}	RST/PGOOD low to high threshold voltage (V_{TH}/V_{FB})	V_{FB} increasing	90	92	94	%
V_{PGH_HYST}		Hysteresis		2		
V_{PGH}	RST/PGOOD high to low threshold voltage (V_{TH}/V_{FB})	V_{FB} increasing	115	120	125	%
V_{PGL_HYST}		Hysteresis		3		%
T_{DELAY}	Delay from VPGH threshold detection and RST/PGOOD release			2		ms
V_{PGLOW}	RST/PGOOD output (open drain)	V_{OUT}/V_{FB} = 80%, 4 mA sinking current			0.4	V
		2 < V_{IN} < V_{INH}, 4 mA sinking current			0.8	
I_{PGLKG}	RST/PGOOD leakage current	V_{RST}/P_{GOOD} = 6 V, V_{OUT}/V_{FB} = 105%			0.1	µA
Soft-start and tracking						
I_{SS}	Soft-start current	SS from 0 V to 0.6 V	1.5	2	2.5	µA
$V_{SSOFFSET}$	Offset voltage between FB and SS/TRK	$V_{SS/TRK}$ = 0.4 V		0		mV
R_{SSPD}	SS/TRK discharge resistor	Before soft-start begin		0.7		kΩ
Thermal shutdown						
T_{SHDWN}	Thermal shutdown temperature	(4)		170		°C
T_{HYS}	Thermal shutdown hysteresis	(4)		20		°C

1. *LCM enables SLEEP mode at light load.*
2. *To be reviewed after safe launch.*
3. *Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.*
4. *Not tested in production.*

6 Functional description

6.1 Overview

The DCP0606Y is a high efficiency synchronous step-down monolithic switching regulator designed to deliver up to 6 A continuous output current.

Due to 0.6 V internal reference voltage and close to 100% duty cycle capability, the DCP0606Y can precisely regulate output voltages ranging from 0.6 V to almost V_{IN} (limited only by minimum TOFF time). The output voltage accuracy is better than ± 1.5% over line, load, and temperature.

The DCP0606Y embeds low $R_{DS(on)}$ (11 mΩ typ.) N-channel MOSFETs for both HS (high-side) and LS (low-side) to maximize the full load efficiency. Nevertheless, the high efficiency over all the load range is guaranteed when the Low Consumption Mode (LCM) is selected. The frequency dithering is always implemented to improve the EMI performance.

The peak current mode control loop with integrated compensation enables fast response to load transient, and thanks to loop adjustment achieved by selecting the proper FSET resistor, a wide range of output filter configurations are supported.

The high-switching frequency selectable in the range 1.8 MHz ÷ 4 MHz and the small QFN 3x2 mm package allow very compact VR solutions.

The DCP0606Y features a full set of auto recovery protections and output voltage monitoring:

- Precise and accurate peak overcurrent protection (internally compensated vs temperature variations) with HS and LS current sensing, to avoid inductor current runaway.
- Overvoltage protection, with sinking current capability
- Overtemperature protection, with 20 °C typ. hysteresis
- Undervoltage lockout on V_{IN} rail
- The Power-Good open drain output easily provides real-time information about the output voltage and it can be exploited to program a RESET function.

A single resistor connected from FSET pin to ground selects the switching frequency and output capacitance range.

The MODE/SIN pin, when forced to GND, enables the Low Consumption Mode (LCM) to skip switching pulses and implement diode emulation at light load. When the MODE/SIN pin is forced high, the Low Noise Mode (LNM) is enabled, and the constant frequency operation is implemented.

Dynamic transition between LCM – LNM is allowed during the regulator operation.

An external clock can be provided on MODE/SIN pin to synchronize the DCP0606Y to an external clock in the range 1.8 MHz ÷ 4.0 MHz.

The DCP0606Y clock-out feature with programmable delay, implemented on SOUT pin, allows to synchronize up to 4 regulators with strong input current RMS reduction.

The dedicated enable pin (EN) offers easy control on the power sequencing. In case of the EN pin forced low, the device enters shutdown state. In this case, the total bias current from V_{IN} is lower than 3 µA (typ.).

6.2 Power section

The DCP0606Y high-side and low-side power switches are N-channel MOSFETs optimized for fast switching transition and high efficiency over the entire load range. The power stage is designed to deliver a continuous output current up to 6 A, depending on application conditions.

The HS MOSFET drain is connected to the V_{IN} pin, the LS MOSFET source is connected to the GND pin (ground). The HS MOSFET source and LS MOSFET drain are connected, providing the SW pin (see Figure 2).

The DCP0606Y embodies an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and consequently reduce power losses:

- When the voltage at the LX pin drops (to check high-side MOSFET turn-off), the LS MOSFET is suddenly switched on;
- When the gate driving voltage of LS drops (to check low-side MOSFET turn-off), the HS MOSFET is suddenly switched on.

If the current flowing in the inductor is negative, the voltage on the LX pin never drops. A watchdog controller is implemented to allow the LS MOSFET to turn on even in this case, allowing the negative current of the inductor to flow to the ground. This mechanism allows the system to regulate even if the current is negative (if LNM mode is enabled).

The high-side MOSFET is properly turned on thanks to the integrated bootstrap network, that only requires an external capacitor between BOOT and LX pin (100 nF typical). The bootstrap capacitor is recharged during low-side MOSFET on time, with a minimum impact on the maximum achievable duty cycle.

In case of input voltage drop close to or below the programmed output voltage, the DCP0606Y can increase the duty cycle up to 100% for up to 24 consecutive clock pulses. Then a minimum off time is implemented (TOFF, MIN) to guarantee the proper recharge of BOOT capacitor.

6.3 Output discharge

The output discharge feature is intended to smoothly discharge the output capacitor and keep V_{OUT} close to GND as long as the DCP0606Y is not enabled (i.e. EN forced low).

This feature is implemented by a controlled resistance connected between SW and GND, and it is available only in dedicated part numbers (refer to Figure 1 and Table 11 for details).

This resistor is active as long as EN is kept low and V_{IN} > 2 V.

6.4 Enable and soft-start

When the EN pin is kept low, the input current is limited to about 3 µA only.

In dedicated p/n (DCP0606Dzz) an optional discharge resistor, connected between SW and GND is integrated with R_{DIS} typical value (refer to Section 6.3 for details).

When EN is asserted high and V_{IN} voltage is higher than $V_{INH,}$ the DCP0606Y is powered-on.

After loading the device configuration (internal fuses and pin-strapping pins), the switching activity is allowed.

Before starting the switching activity, the SS pin is forced low by a pull-down (R_{SSPD} = 0.7 kΩ typ.) for T_{PD} = 200 µs to discharge the SS capacitor.

The same sequence is performed in case of overtemperature fault detection.

The voltage reference is increased with the timing programmed through the SS capacitor, given the following equation, considering I_{SS} = 2 µA and V_{REF} = V_{FB} = 0.6 V:

$$C_{SS} = \frac{T_{SS} \cdot I_{SS}}{V_{REF}}$$

Until the SS pin is kept lower than V_{FB} (0.6 V typ.), the tracking function is enabled. This feature can be exploited to program a proportional power-up and ramp-up sequence. As soon as the SS voltage is higher than 0.6 V, the control loop reference switches to the internal voltage reference, and the SS capacitor is slowly discharged.

The maximum allowed soft-start capacitor value is C_{SSMAX} = 47 nF to guarantee the complete discharge in the above described T_{PD} interval.

If no CSS capacitor is mounted, a minimum 150 µs typ. soft-start is nevertheless implemented.

During the soft-start interval, the DCP0606Y is not allowed to sink current from the output, even if LNM operation is selected (MODE/SIN forced HIGH) or a clock-in is provided on MODE/SIN. This feature is intended to guarantee the proper power-up also in case of output voltage pre-bias condition.

6.5 RESET / POWERGOOD

At the end of the soft-start interval, if the output voltage (sensed through FB pin) is detected higher than V_{PGL} threshold, the RST/PGOOD pin is released with T_{DELAY} delay.

During the operation, in case the output voltage is detected outside the power-good window, the RST/PGOOD pin is asserted low. When VFB is detected inside the power-good window again, the RST/PGOOD pin is released, after TDELAY interval as described above.

In case of overvoltage detection (OVP), the RST/PGOOD pin is asserted low. A VOVP_HYST hysteresis is required before releasing RST/PGOOD.

To summarize, the RST/PGOOD pin is pulled low when:

1. The FB pin voltage is lower than 90% (typ.) of the internal reference
2. The FB pin voltage is higher than 120% (typ.) of the internal reference
3. During the soft-start procedure, also with pre-charged VOUT
4. If a thermal shutdown event occurs
5. If a UVLO event occurs

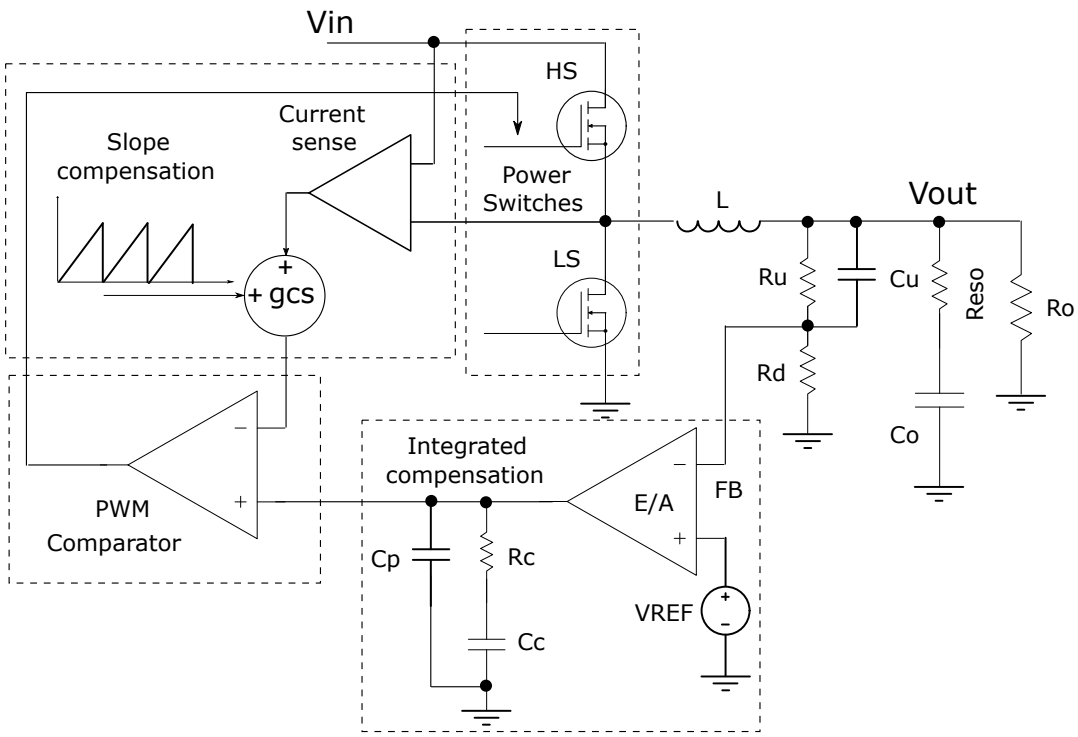
The RST/PGOOD pin is VIN compatible.

6.6 Control loop and voltage programming

The DCP0606Y is based on a constant frequency peak current mode architecture.

Thanks to the integrated compensation network and slope generation, no additional external components are necessary for loop stabilization.

Figure 4. Control loop block diagram



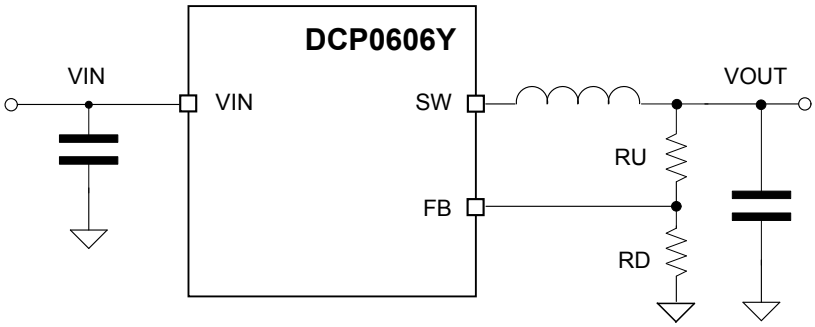
The output voltage can be programmed through an external resistor divider, from 0.6 V up to almost VIN.

The design equation is:

$$VOUT = 0.6 \cdot \left(1 + \frac{R_U}{R_D}\right)$$

Refer to the following figure for output voltage programming.

Figure 5. **Output voltage programming**

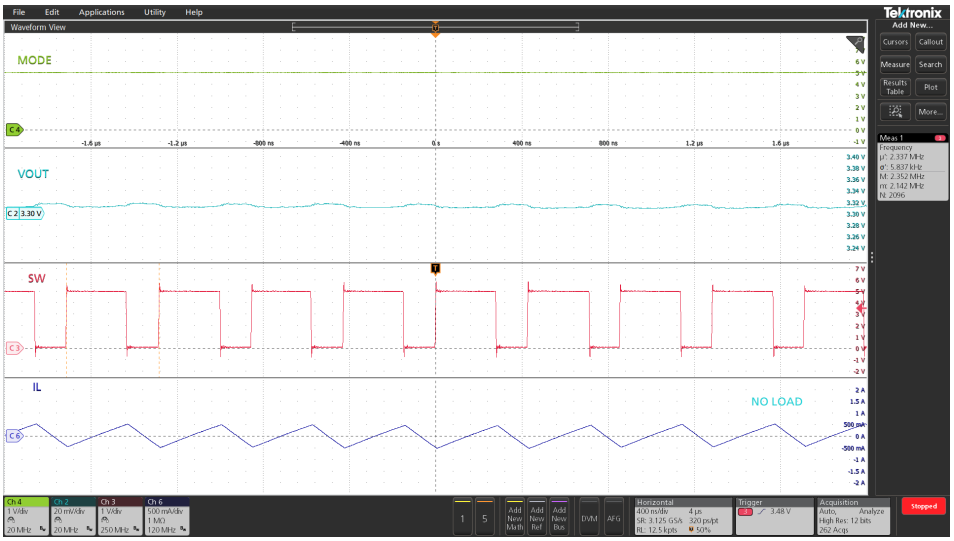


6.7 LNM/LCM selection (MODE/SIN)

Depending on the low-side power MOSFET management, the inductor current can be allowed to reverse or not. The choice can be performed during device operation by acting on the MODE/SIN pin and is effective at the end of the soft-start (refer to Section 6.4).

When the low-noise mode (LNM) operation is selected by forcing high pin MODE/SIN, the inductor current can be reversed. In this way a constant switching frequency is achieved, minimizing the output voltage ripple and providing the fastest transient response due to the peak current mode control loop.

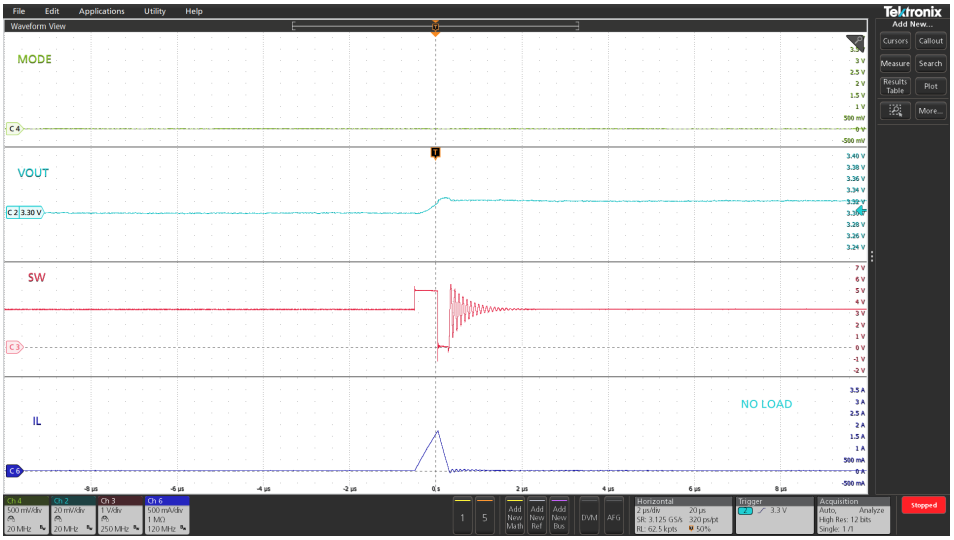
Figure 6. **LNM operation, no load**



If the MODE pin is forced low, the low-consumption mode (LCM) is selected. In this working mode, the inductor current cannot be reversed because the low-side MOSFET is turned-off when the sensed inductor current is approaching zero. The resulting switching frequency is load-dependent (i.e. SW pulses can be skipped) with a greater advantage in power conversion efficiency, above all at light load.

In LCM, the HS MOS is turned on for a fixed interval. The fixed on-time depends on the input voltage and the switching frequency is selected through FSET resistor (Table 9 for details). This control loop ensures good dynamic performance with minimum quiescent current.

Figure 7. **LCM operation, no load**



In LCM, with increasing output current, the SW frequency also increases until the continuous conduction mode (CCM) operation is achieved. When this occurs, the constant HS on-time operation is replaced by constant frequency peak current mode control, as implemented in low-noise mode (LNM).

Figure 8. **LCM operation, 100 mA load**

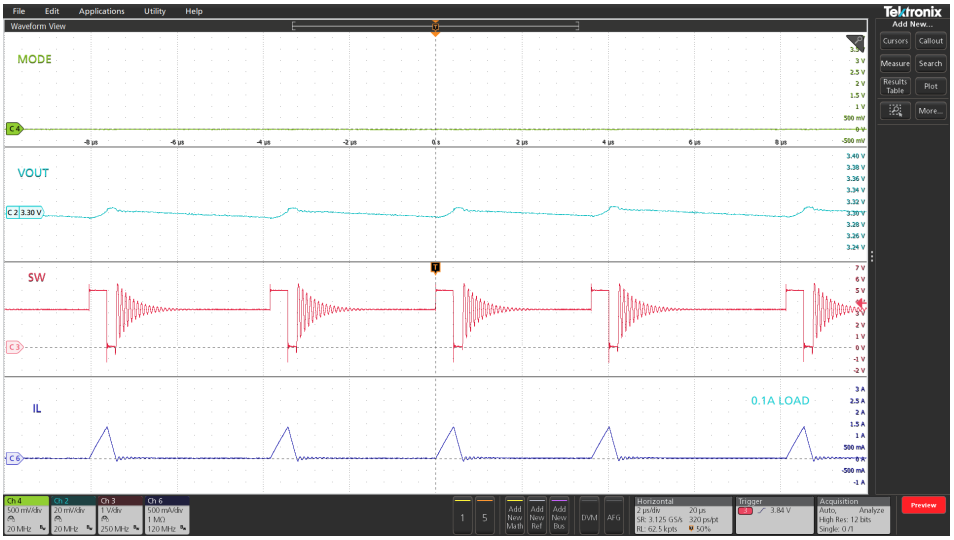


Figure 9. **LCM operation, 500 mA load**

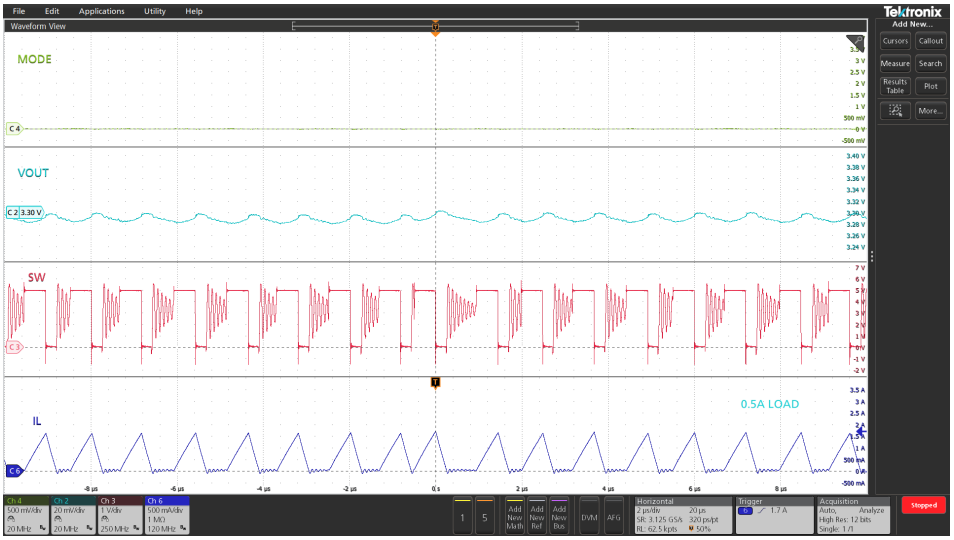
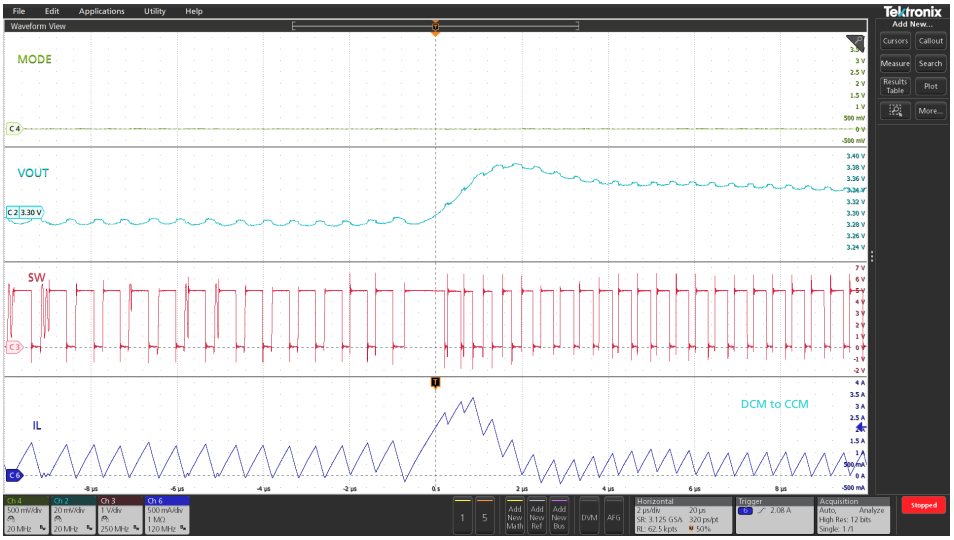
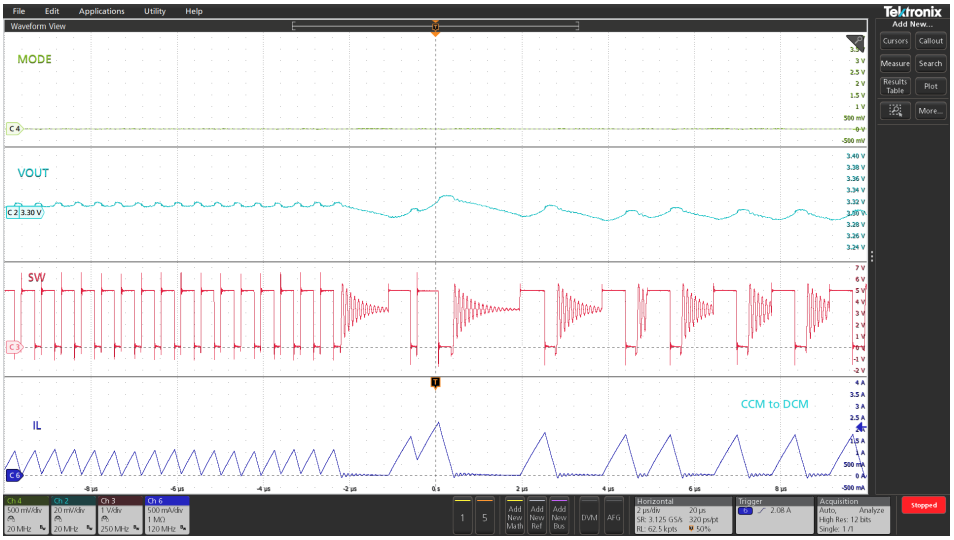


Figure 10. **LCM operation, DCM to CCM transition**



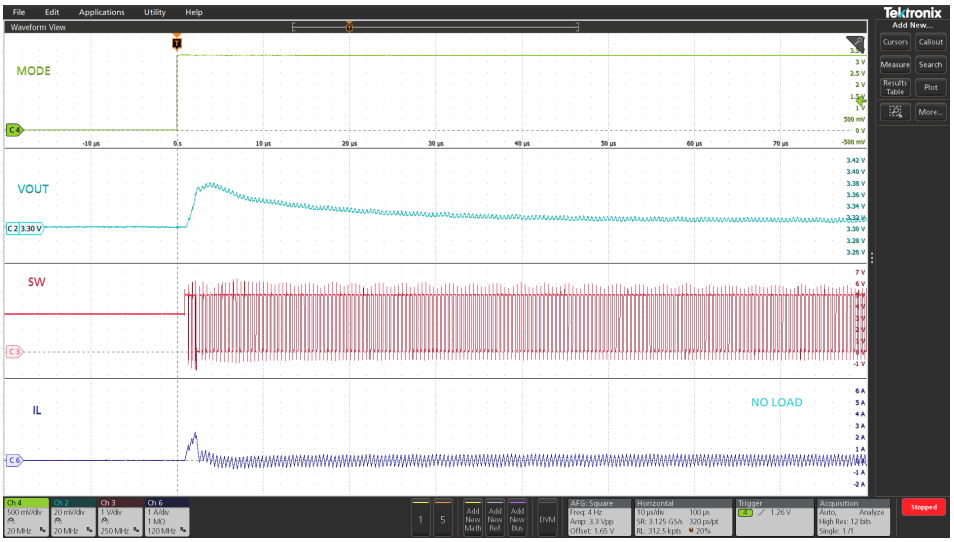
In LCM, discontinuous conduction mode (DCM) operation is automatically restored when the output load decreases below approximately half of the inductor current ripple achieved in CCM operation.

Figure 11. **LCM operation, CCM to DCM transition**



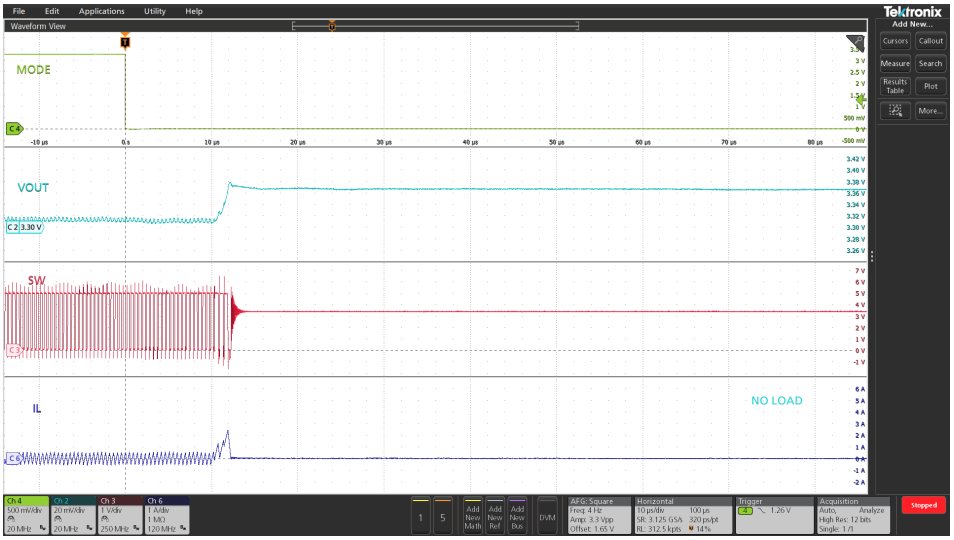
The LCM or LNM operation can be dynamically selected by toggling the MODE/SIN pin. When MODE/SIN is asserted high, the LCM to LNM transition is implemented.

Figure 12. **MODE toggle, LCM to LNM transition example**



When MODE/SIN is forced low, the LCM mode is selected and the transition is performed accordingly with the implemented architecture that optimizes the quiescent current.

Figure 13. **MODE toggle, LNM to LCM transition example**



If an external clock is applied on the MODE/SIN pin, the DCP0606Y switching activity is synchronized to the applied clock and the LNM operation is enabled. The external clock must meet the electrical requirements summarized in Table 8. The synchronization is also implemented during the soft-start sequence. However, the constant frequency operation is not allowed until the soft-start is expired. The SOUT pin provides the same clock detected on MODE pin, with a phase shift programmed by the SOUT resistor. In case no external clock is detected on MODE, the free running clock programmed on pin FSET through RFSET resistor is restored as the switching frequency and the same clock, with the programmed phase shift, is provided on SOUT.

Refer to Section 6.9 for switching frequency programming details.

If no external clock is applied on MODE/SIN, a replica of the internal clock, phase shifted, is available on SOUT as soon as the regulator is enabled and properly biased.

SOUT can be tied to another DCP0606Y MODE/SIN pin for synchronized regulators (refer to Section 6.11 for details).

6.8 Device configuration

The DCP0606Y configuration depends on the following pins configuration.

Table 9. **Device configuration**

PIN	SETUP	FEATURE
FSET	Refer to Table 10	Switching frequency and COUT range selection
MODE	Forced low (< VLCM) or high (> VLNM)	LCM or LNM working mode selection (dynamic change allowed)
	External clock applied	LNM selected, synchronization with the external clock
	Connected to SOUT provided by another DCP0606Y	LNM selected, DCP0606Ys synchronization
SOUT	Shorted to GND	Minimum quiescent current, no clock-out available
	RSOUT to GND, Refer to Table 11	Clock-out available on SOUT, to synchronize another DCP0606Y

6.9 FSET / Frequency selection table

This pin allows to set two different parameters independently:

- Internal compensation settings for the control loop
- The switching frequency in constant frequency mode, from 1.8 MHz to 4 MHz

A resistor from FSET to GND changes the compensation as well as the switching frequency.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency / compensation. Do not leave the pin floating.

The compensation range must be chosen based on the minimum capacitance used, given the following design equation:

$$C_{OUT,MIN} = \frac{K_C}{V_{OUT}}$$

Table 10. FSET configuration table

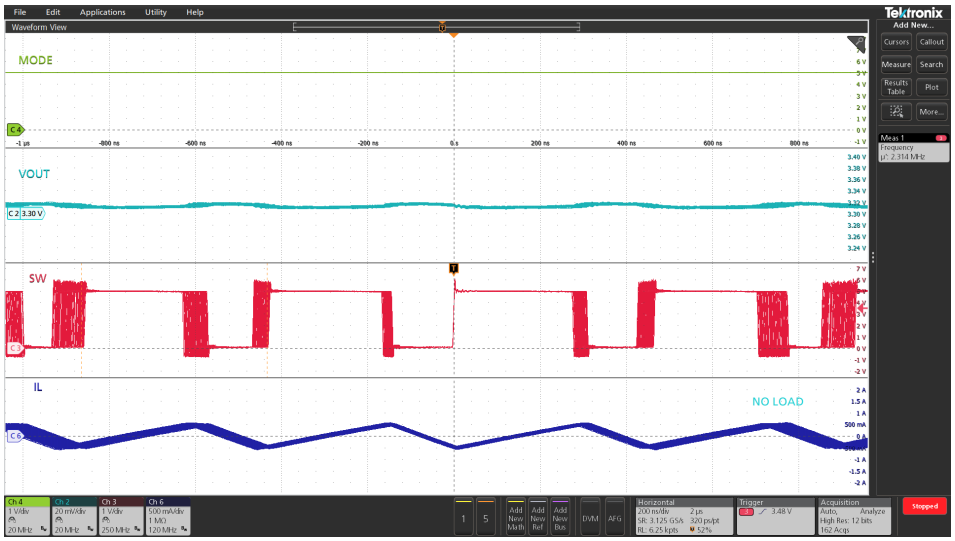
RFSET [kΩ] 1%	FSW [MHz]	KC [µF*V]
FSET=VIN	2.25 (No dithering)	100
100	1.8	200
82	2.25	200
68	3.5	200
47	4	200
33	1.8	100
27	2.25	100
22	3.5	100
15	4	100
10	1.8	50
8.2	2.25	50
6.8	3.5	50
4.7	4	50
FSET=GND	2.25 (No dithering)	50

6.10 Dithering / spread spectrum

The dithering function helps to reduce the DC-DC electromagnetic emissions, with small impact on output voltage ripple.

This feature is implemented when FSET is connected to an external resistor and it is disabled when FSET is tied to VIN or GND, as described in Section 6.9 and shown in Table 10.

Figure 14. RFSET = 27 k, dithering enabled



The internal dithering circuitry changes the switching frequency in the range of ± 5% of the nominal value.
The device updates the frequency every clock period by fixed steps:

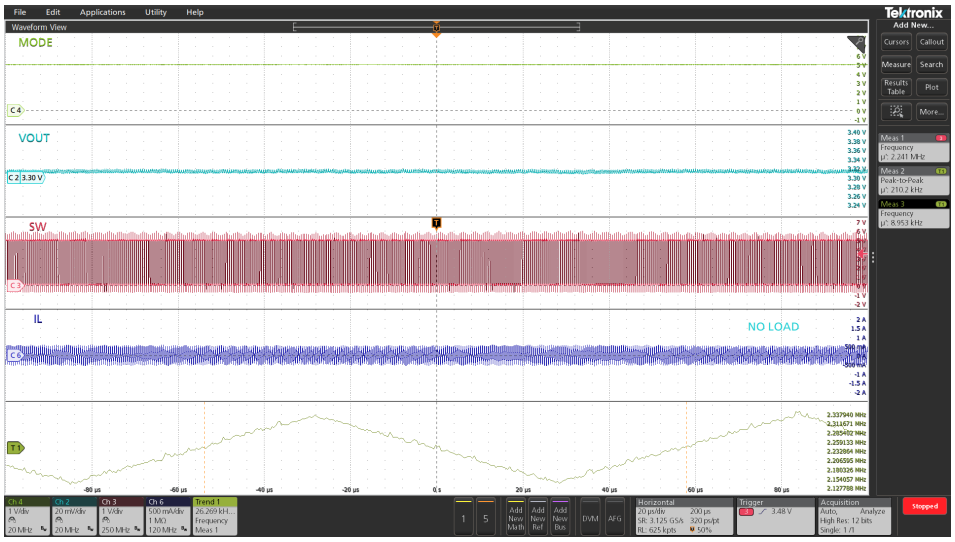
- Ramps up in 63 steps from minimum to maximum switching frequency;
- Ramps down in 63 steps from maximum to minimum switching frequency.

The resulting frequency modulation is almost triangular, with a frequency of:

$$F_{Dith} = \frac{F_{SW}}{K_{Dith} \cdot 126}$$

Given K_{Dith} in the range 1.5÷3, depending on the selected F_{SW}, the resulting F_{Dith} is close to 9 kHz.

Figure 15. RFSET = 27 k, switching frequency time trend

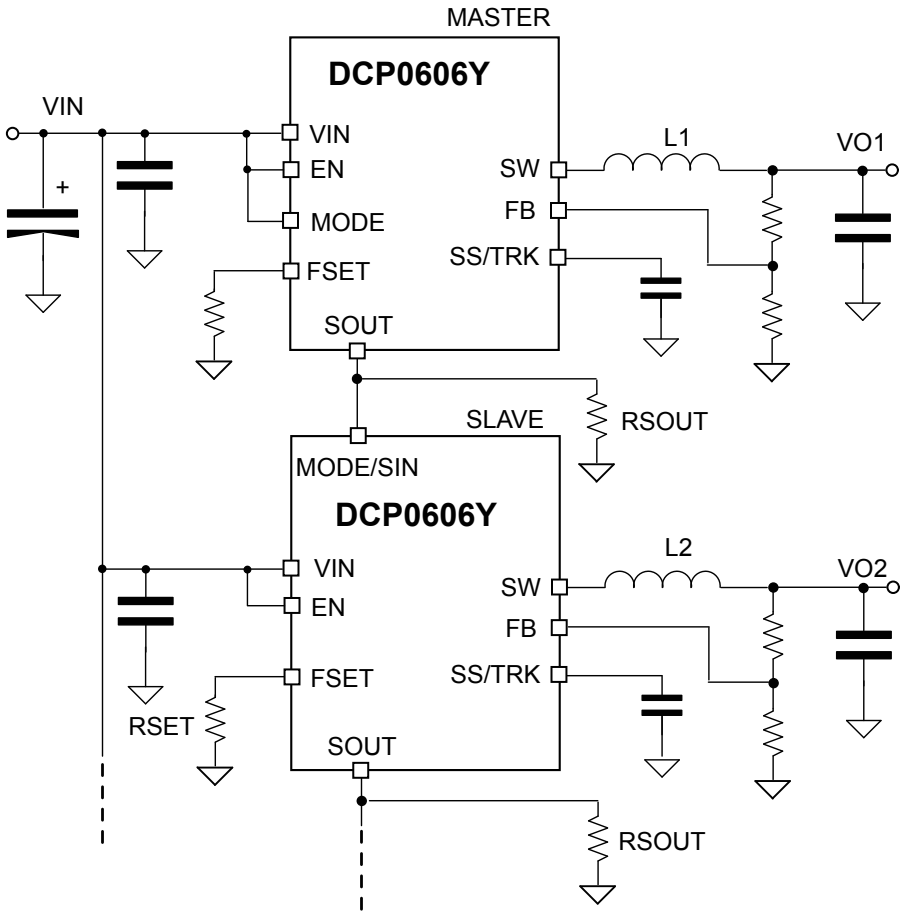


The clock provided on SOUT is implementing the dithering function, with the programmed phase shift, unless SOUT is shorted to GND or a clock-in is provided on MODE/SIN.

6.11 Synchronization

In case two or more DCP0606Y are requested to work at the same switching frequency, with phase shifting, the following configuration must be considered:

Figure 16. **Synchronization example**



The same switching frequency must be programmed for all the regulators and the MASTER SOUT pin must be connected directly to the SLAVE MODE/SIN pin. Each DCP0606Y provides independent regulation and full fault management. Based on the RSOUT resistor mounted between SOUT and GND, the following phase shifting can be programmed:

Table 11. **SOUT phase shifting programming**

RSOUT [kΩ]	Phase shift [°]	Devices
N.M.	180	Master + 1
100	120	Master + 2
75	90	Master + 3

The synchronization and constant frequency operation are implemented by the SLAVE as soon as the clock-in is available on its pin MODE/SIN. However, during the soft-start, the LCM mode is always implemented since the inductor current is not allowed to reverse, as described in Section 6.4.

The SLAVE regulator is providing on its SOUT pin the same clock detected on the MODE pin with the phase shifting programmed on its SOUT pin.

If no clock-in is provided on its MODE/SIN pin, the MASTER regulator will implement a dithering function on clock-out, including the programmed phase shift; otherwise SOUT will be a replica of clock-in with the programmed phase shift only and pulse width equal to one half of the switching period.

If the clock-out feature is not exploited, the SOUT pin can be shorted to GND before powering up the DCP0606Y to further reduce the input quiescent current.

SOUT is internally parked to GND if EN pin is forced low or VIN is below UVLO threshold, otherwise it is always available also during fault detection, overtemperature fault included, with approximately 50% duty cycle and electrical characteristics described in Table 8.

7 Fault management

The DCP0606Y fault management is continuously monitoring the inductor current, the output voltage and the device junction temperature.

Furthermore, thanks to the input UVLO (undervoltage lock-out) circuitry, the switching activity is guaranteed only with the proper VIN level. All the protections are auto-recovery (no EN or VIN toggle is required).

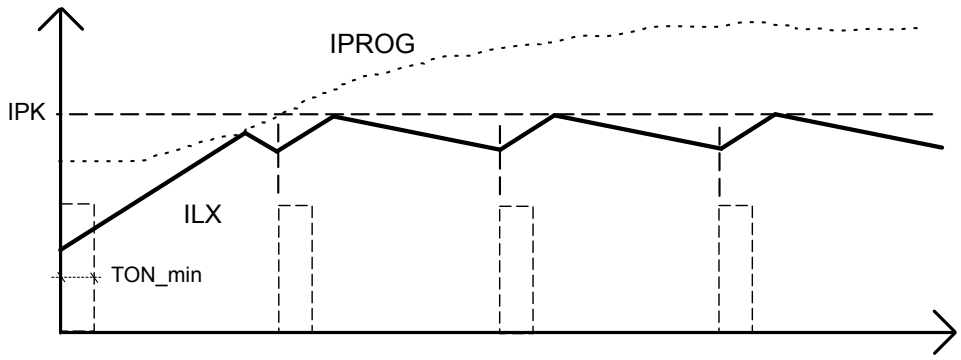
7.1 Overcurrent protection (OCP)

Overcurrent protection is active as soon as the device is enabled and VIN is above the UVLO level.

The overcurrent function protects the converter from a shorted output or overload by sensing the inductor current, cycle by cycle.

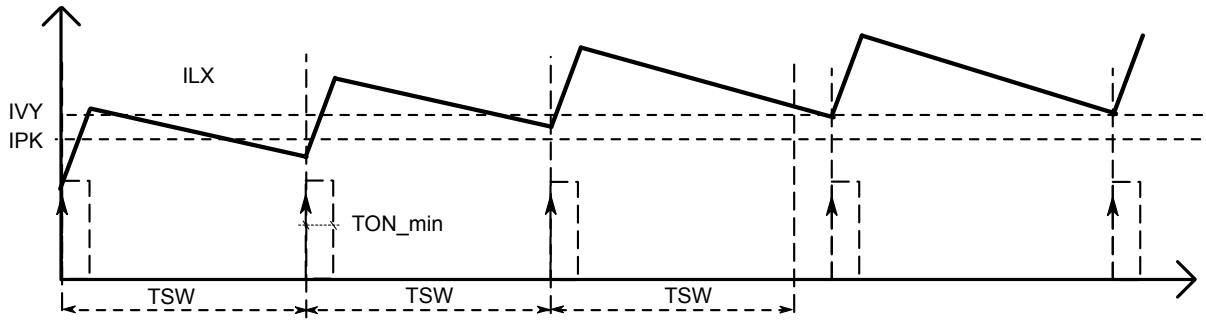
In normal operation the HS MOS is turned off when the sensed current (ILX) is equal to the current programmed by the control loop (IPROG). The maximum HS MOS peak current is limited by the internal OCP (overcurrent protection) comparator, cycle by cycle, by comparison with the IPK threshold as shown in Figure 17.

Figure 17. OCP - Peak current limit



The inductor current is also monitored during LS MOS on-time. This feature, also known as “valley current limitation”, is effective in case of current runaway due to HS MOS minimum on-time limitation and very low VOUT / VIN ratio. This protection can avoid the HS MOS turn-on if the inductor current, sensed during LS MOS on-time, is higher than the IVY threshold Figure 18.

Figure 18. OCP – Valley current limit



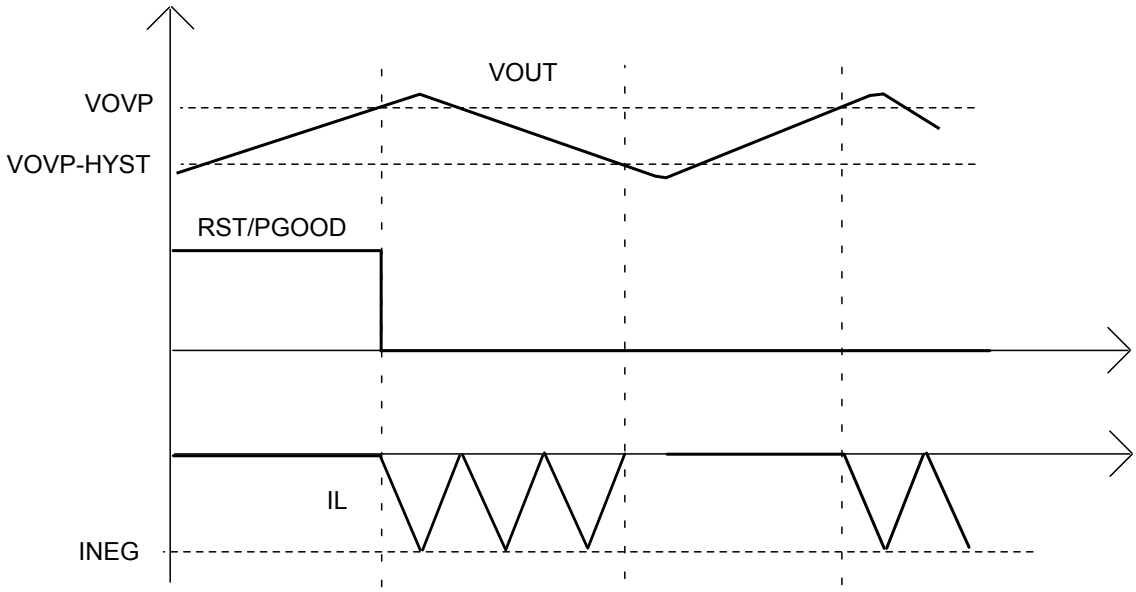
In LNM mode, the DCP0606Y can sink current from the output. However, to protect the power components and the regulator itself, a negative current limit is implemented too. If, during the LS MOS on time, the sensed current is found lower than the INEG threshold, the low-side MOS is promptly turned off and the high-side one is turned on. At the end of a fixed interval, the LS MOS can turn on again.

7.2 Output overvoltage protection (OVP)

In case the FB pin is detected above the V_{OVP} threshold, the output overvoltage protection is triggered.

When this occurs, the RST/PGOOD pin is forced low and the DCP0606Y actively discharges the output voltage by sinking current (refer to Section 7.1).

Figure 19. Output overvoltage protection



As soon as the OVP cause is removed, the proper switching activity is restored, and RST/PGOOD output is released, with the delay and threshold described in Section 6.5.

7.3 Overtemperature protection (OTP)

If the device junction temperature increases above T_{SHDWN} (170 °C typ.), the switching activity is inhibited and the RST/PGOOD pin is pulled down. As soon as the junction temperature drops of T_{HYS} (20 °C typ.) is detected, the switching activity is resumed and a new soft-start is implemented.

SOUT clock, if programmed, is also available during the thermal shutdown event.

The OTP protection is always active in LNM mode and in LCM mode with mid/high load.

7.4 Input undervoltage lockout (UVLO)

In case the input voltage is detected below the UVLO threshold (V_{IN_UVLO}), the switching activity is stopped, RST/PGOOD is asserted low and no clock-out is available on SOUT, if programmed. The switching activity is restored as soon as the input voltage is found above the UVLO threshold and the EN pin is asserted high.

When this occurs, a new soft-start sequence is implemented with the timing described in Section 6.4.

8 Application design guidelines

8.1 Switching frequency

The switching frequency can be selected among four values (1.8 – 2.25 – 3.5 – 4 MHz).

If not driven by specific requirements, F_{SW} is a trade-off between efficiency and PCB area.

In DC/DC converter, an important parameter is the HS MOS on-time interval in steady operation, theoretically given by VOUT and VIN ratio (i.e. duty cycle D), and divided by the switching frequency:

$$T_{ON} = \frac{\frac{V_{OUT}}{V_{IN}}}{F_{SW}} = \frac{D}{F_{SW}}$$

Some constraints are implemented in the HS and LS MOS timing to guarantee the proper current monitoring and reliable operation. By referring to Table 8, the maximum switching frequency that avoids TONMIN limitation in case of very low duty cycle is:

$$F_{SW} < \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{T_{ON,MIN}}$$

A similar constraint is found in case of high duty cycle to avoid the LS MOS minimum on-time limitation (TOFFMIN):

$$F_{SW} < \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \frac{1}{T_{OFF,MIN}}$$

The F_{SW} selection guidelines described above are more relevant in case constant frequency operation and minimum output voltage ripple are the key features in the target application.

8.2 Input capacitor selection

The input capacitor must be rated for the maximum input operating voltage and the maximum expected RMS input current. Since the step-down converters' input current is a sequence of pulses from 0 A to IOUT, the input capacitor must absorb the equivalent RMS current which can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors must be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency.

The RMS input current (flowing through the input capacitor) is roughly estimated by:

$$I_{CIN,RMS} \cong I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

Considering D = VOUT / VIN the theoretical DC-DC conversion ratio, the above equation provides a maximum value equal to IOUT / 2 when D = 0.5.

The amount of the input voltage ripple can be roughly estimated by:

$$V_{IN,PP} \cong \frac{D \cdot (1 - D) \cdot I_{OUT}}{C_{IN} \cdot F_{SW}} + R_{ES,IN} \cdot I_{OUT}$$

In case of MLCC ceramic input capacitors, the equivalent series resistance (RES, IN) is almost negligible and above all, if multiple components are put in parallel.

The suggested components are two or more ceramic MLCC capacitors with value 22 µF or higher, with adequate voltage rating, placed as close as possible to the VIN and GND pins.

8.3 Inductor selection

The inductance value is typically selected to keep the current ripple, ΔIL_{PP}, in the range 20% - 40% of the maximum DC output current:

$$L = \frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I_L \cdot F_{SW}}$$

To prevent the sub-harmonic instability in the peak current mode control loop, a fixed slope compensation mechanism is implemented in DCP0606Y by adding a current ramp to the sensed current (see Figure 1). This approach is effective if the inductor current ripple within the expected input voltage range is comparable with the above-mentioned added slope. By also considering this requirement, the following charts can be used as reference for selecting the proper inductance value.

Table 12. Inductor selection – 1.8 MHz

Figure 20. Lind vs. Vout - 1.8 MHz / 3.3 Vin

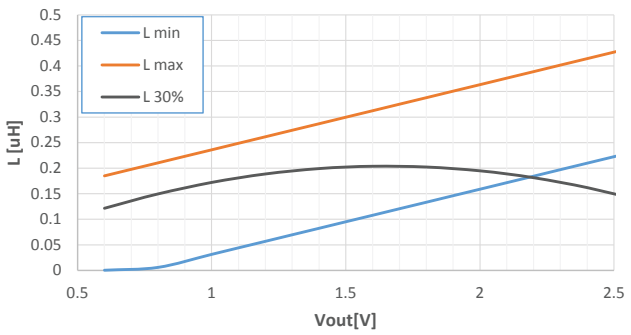


Figure 21. Lind vs. Vout - 1.8 MHz / 5 Vin

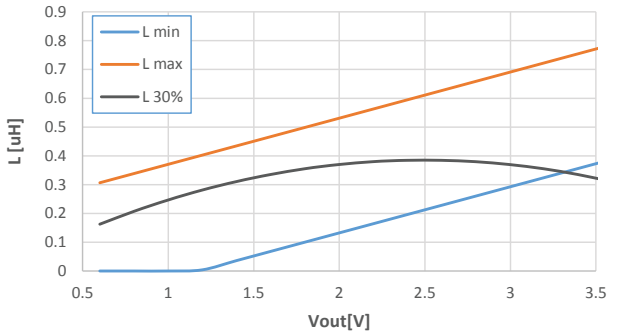


Table 13. Inductor selection – 2.25 MHz

Figure 22. Lind vs. Vout - 2.25 MHz / 3.3 Vin

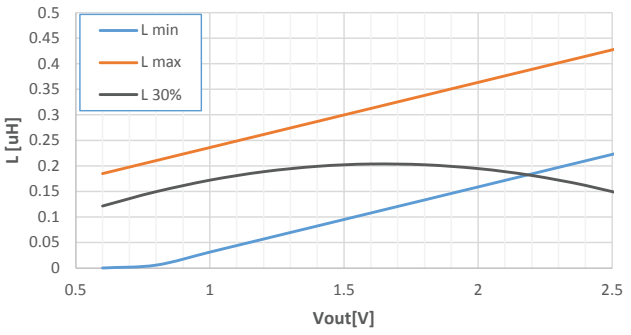


Figure 23. Lind vs. Vout - 2.25 MHz / 5 Vin

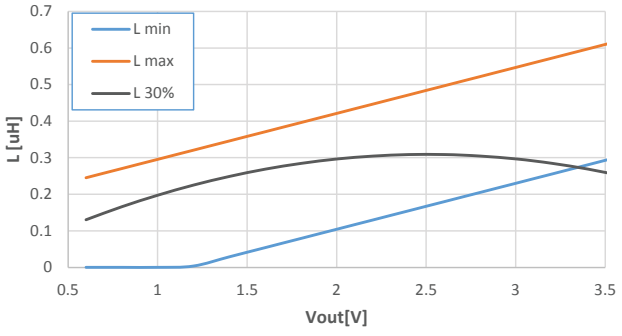


Table 14. **Inductor selection – 3.5 MHz**

Figure 24. **Lind vs. Vout - 3.5 MHz / 3.3 Vin**

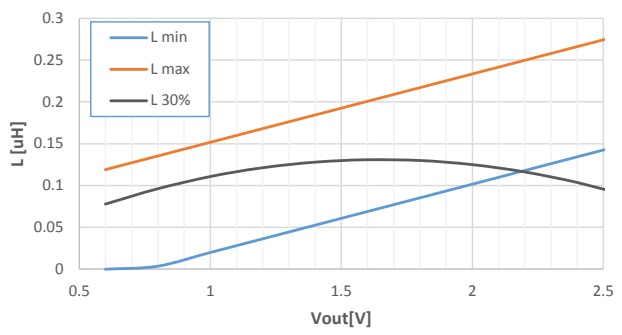


Figure 25. **Lind vs. Vout - 3.5 MHz / 5 Vin**

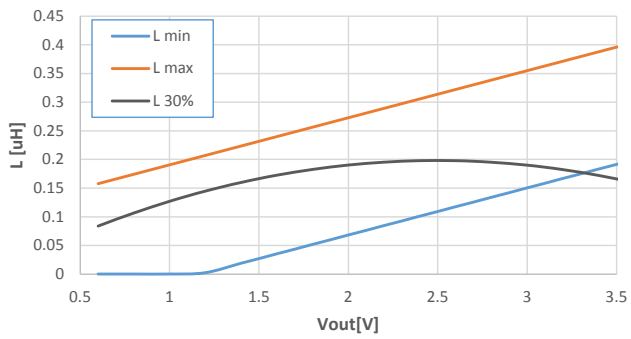


Table 15. **Inductor selection – 4 MHz**

Figure 26. **Lind vs. Vout - 4 MHz / 3.3 Vin**

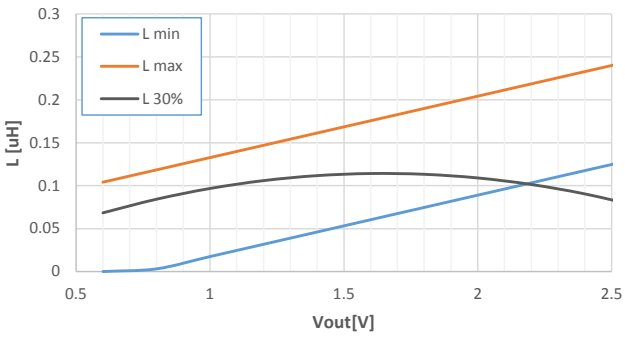
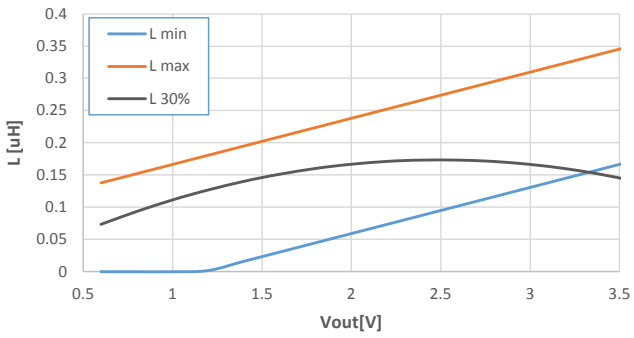


Figure 27. **Lind vs. Vout - 4 MHz / 5 Vin**



Additional features such as low DCR to improve high load efficiency and shielding to minimize EMI effects, must also be considered in the inductor choice. Care must also be taken regarding AC losses in the case of high switching frequency operation.

8.4 Output capacitor selection

The amount of the voltage ripple in LNM operation can be estimated starting from the current ripple obtained by the inductor selection. Assuming ΔIL_{PP} is the inductor current ripple and $\Delta VOUT_{PP}$ is the allowed output voltage ripple. The minimum output capacitance can be roughly estimated by:

$$C_{OUT,RIPPLE} > \frac{\Delta IL_{PP}}{8 \cdot F_{SW} \cdot \Delta VOUT_{PP}}$$

This equation does not consider the parasitic resistance ESR, typically very low in case of multi-layer ceramic capacitor (MLCC). Furthermore, this contribution is less relevant if two or more capacitors are put in parallel to achieve the total capacitance amount required.

The actual capacitance value that meets the above requirements, also considering the derating due to the applied voltage, is then used to select the proper FSET resistor (refer to Section 6.9 and Table 10).

This can be done by computing the K parameter as follows:

$$K = C_{OUT} \cdot V_{OUT}$$

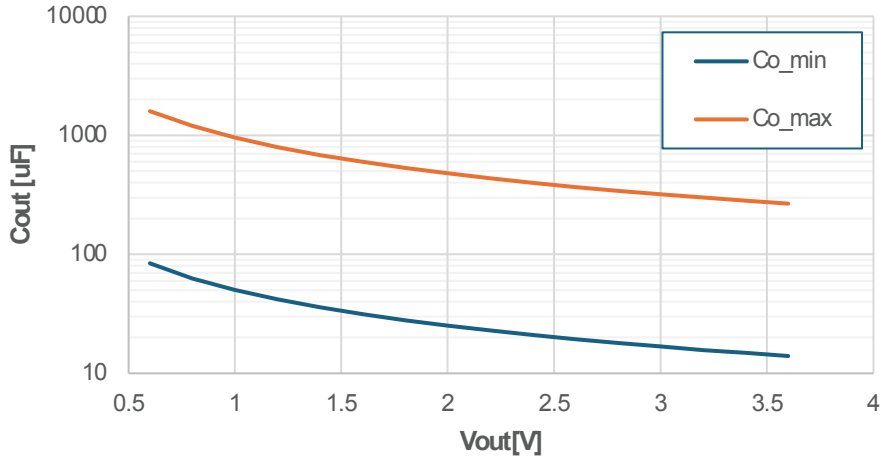
The FSET resistor is then selected considering the target switching frequency (1.8 – 2.25 – 3.5 – 4MHz) and the maximum Kc, which is lower than the K parameter computed above. With this approach, the maximum dynamic performance is achieved, and the loop bandwidth can be estimated by:

$$BW \approx \frac{K_C \cdot BW_{MAX}}{K}$$

assuming BW_{MAX} = 200 kHz and the K parameter computed above.

In the event that a very large C_{OUT} is required, the resulting loop bandwidth will be consequently reduced, which will also impact the phase margin. A feed-forward capacitor in parallel with Ru resistor can help in this case (Figure 4 for reference). This adjustment is normally not necessary if C_{OUT} is selected in the suggested range (refer to Figure 24).

Figure 28. Output capacitor suggested range



8.5 Layout considerations

The PCB layout of switching DC-DC regulators minimizes the noise injected in high impedance nodes and reduces interference generated by the high current switching loops.

In a step-down converter, the input loop (including the input capacitor, the DC-DC regulator and ground connection) is the most critical one due to high value pulsed currents flowing through it. To minimize the EMI, this loop must be as short as possible with an adequate input capacitor placed very close to DCP0606Y VIN and GND (pin 2 and 4 respectively).

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. To reduce the pick-up noise, the resistor divider must be placed very close to the device.

The PCB layout has a key role in guaranteeing the thermal performance of the DCP0606Y. The VIN and GND pins are the main path for heat removal, thus a multi-layer board with internal plane dedicated to GND and VIN is the right choice. As a general rule, the first internal layer must be dedicated to the GND plane, with multiple VIAs below and close to the converter to guarantee the heat removal.

Refer to Section 9 for an example of the PCB layout.

8.6 Thermal considerations

The thermal design prevents the thermal shutdown of the device if junction temperature goes above 170 °C (typ.). The three different sources of losses within the device can be estimated as follows:

Conduction losses due to the $R_{DS(on)}$ of the integrated power switches; these are equal to:

$$P_{COND} = R_{DS(ON)-H} \cdot D \cdot I_{OUT}^2 + R_{DS(ON)-L} \cdot (1-D) \cdot I_{OUT}^2 \approx R_{DS(ON)} \cdot I_{OUT}^2$$

where D is the duty cycle of the application and $R_{DS(ON)-H}$ and $R_{DS(ON)-L}$ are the maximum resistance over temperature of the power switches. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN} but it is higher to compensate the losses of the regulator. However, since HS and LS MOS are comparable in DCP0606Y, the P_{COND} equation can be simplified as shown above.

Switching losses due to power MOSFETs turn-ON and OFF; these can be calculated as:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW}$$

where TRISE and TFALL are the overlap times of the voltage across the high-side power switch (VDS) and the current flowing into it during turn-ON and turn-OFF phases. For this device, the typical value for the switching time is close to 1 ns.

Quiescent losses, calculated as follows:

$$P_Q = V_{IN} \cdot I_Q$$

where IQ is the DCP0606Y quiescent current.

The DCP0606Y total power losses are given by:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q$$

The junction temperature T_J can be estimated with the following equation:

$$T_J = T_A + P_{LOSS} \cdot R_{TH,JA}$$

where T_A is the ambient temperature. $R_{TH,JA}$ is the equivalent thermal resistance junction to ambient of the device. It can be calculated as the parallel of numerous heat conduction paths from the junctions to the ambient. For this device, the $R_{TH,JA}$ measured on the demonstration board described in the following section is about 42 °C/W.

9 Evaluation board

9.1 Schematic and PCB layout

Figure 29. **Evaluation board schematic**

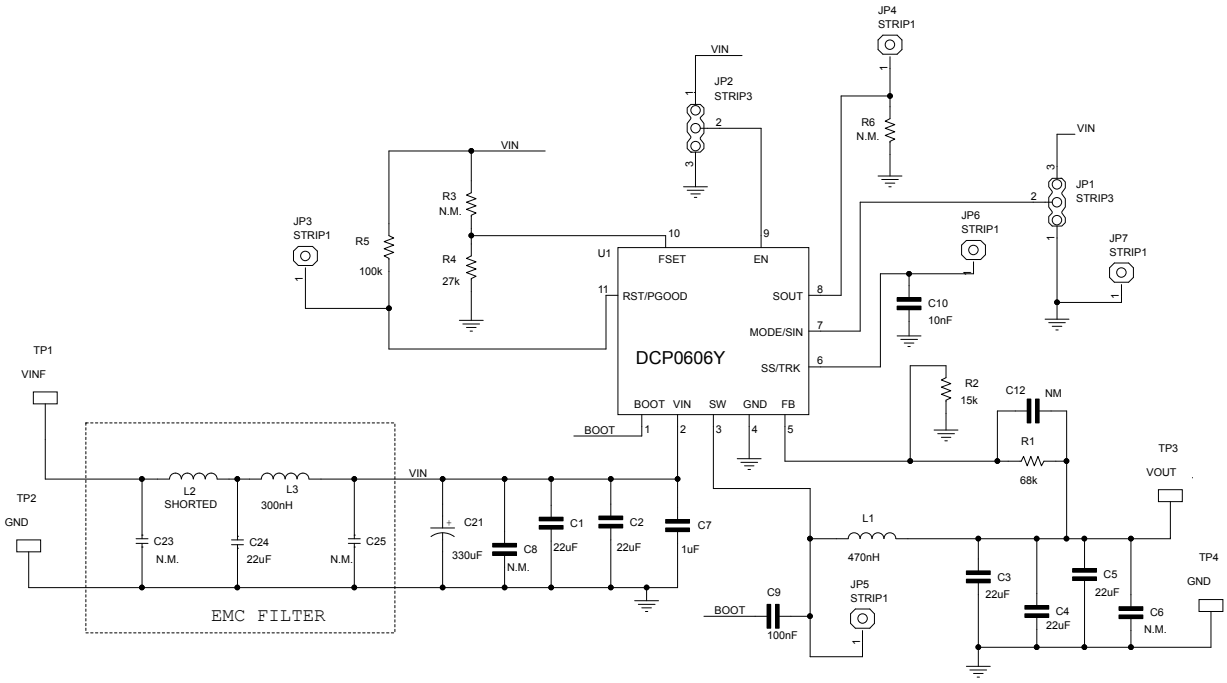


Figure 30. **Evaluation board PCB layout. Top**

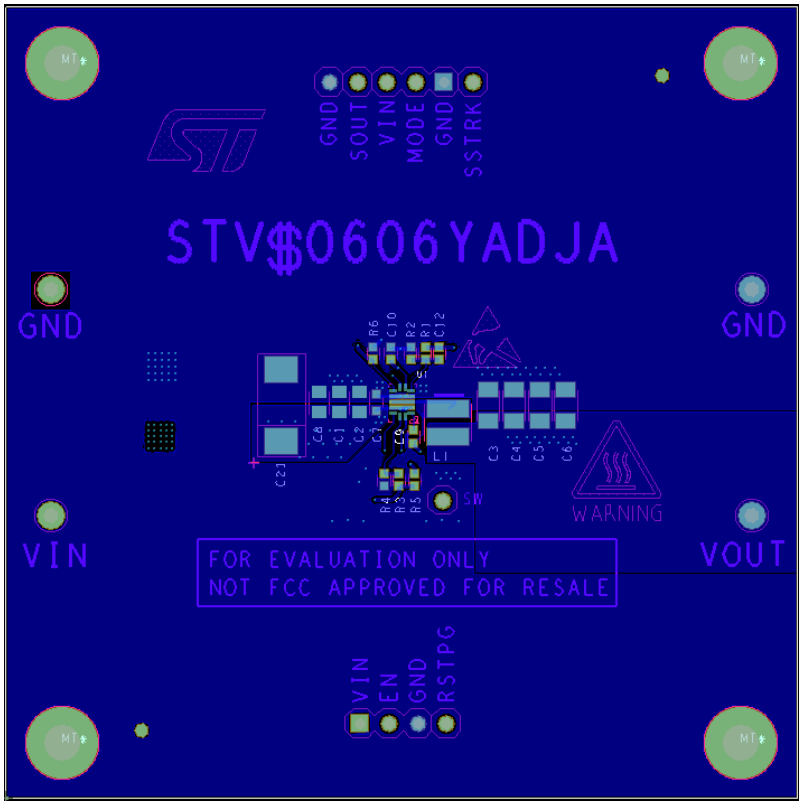


Figure 31. **Evaluation board PCB layout. Internal layer 1**

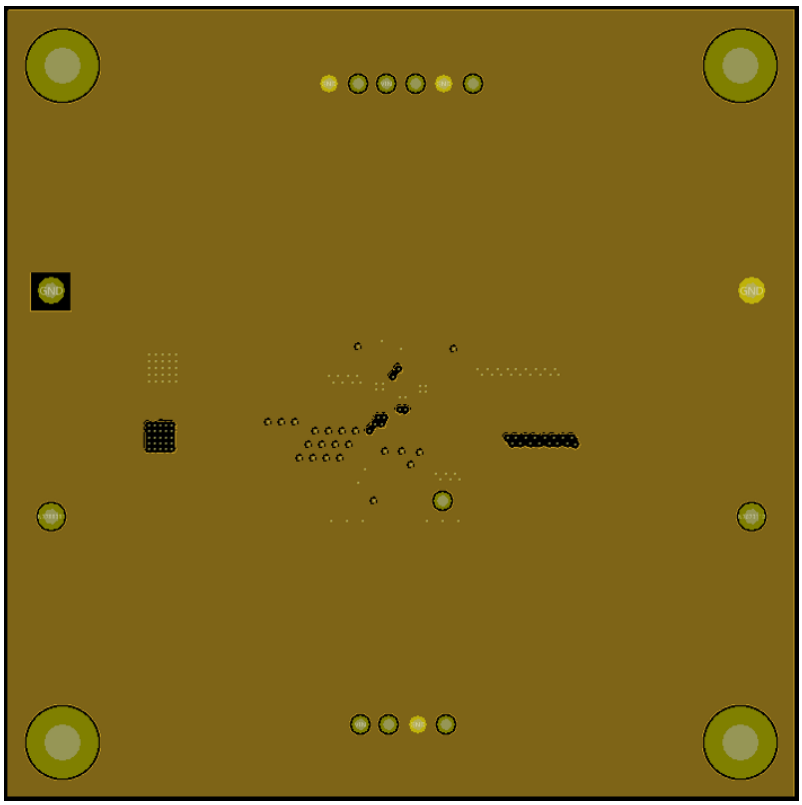


Figure 32. Evaluation board PCB layout. Internal layer 2

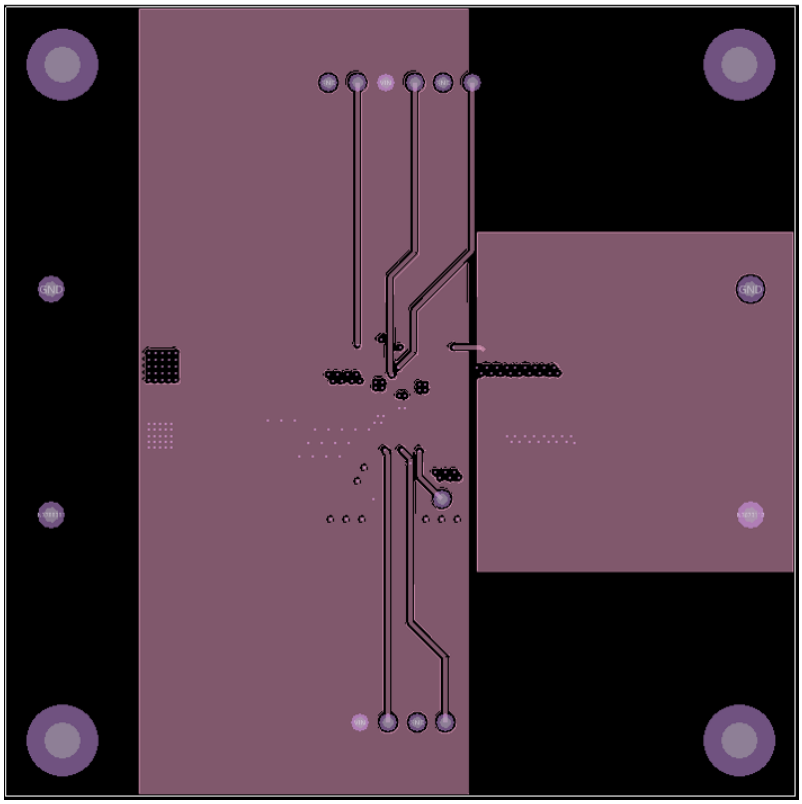
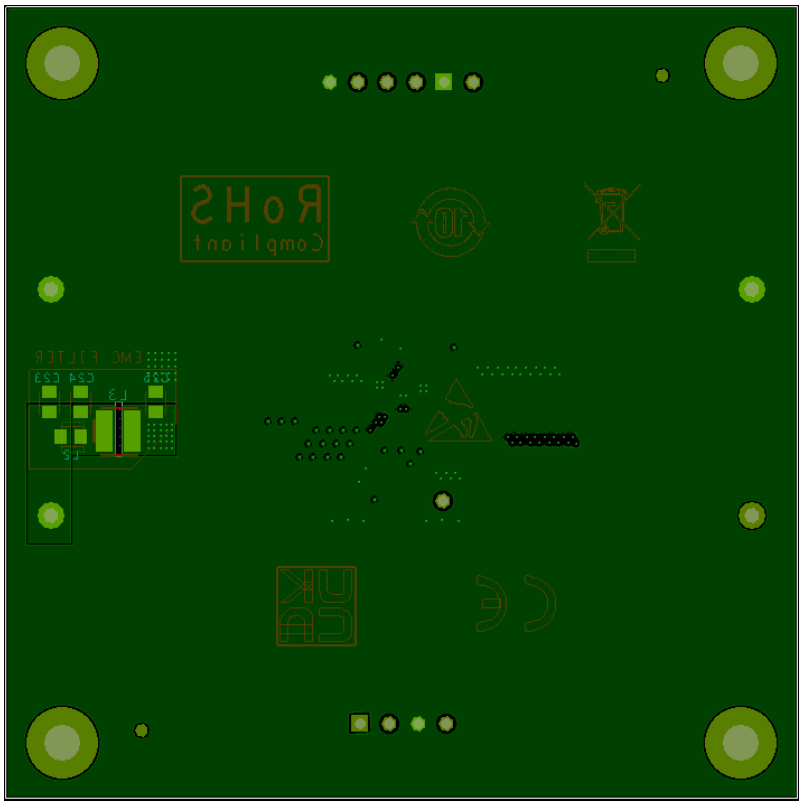


Figure 33. Evaluation board PCB layout. Bottom



9.2 DCP0606QTRY – Evaluation board

In this section the DCP0606QTRY evaluation board is described.

The board schematic is shown in Figure 29 and the PCB layout is depicted in Figure 30 and Figure 33.

The main features are:

- Programmed VOUT 3.3 V
- Max. IOUT 6 A
- Switching frequency 2.25 MHz with dithering
- Soft-start 3 ms

Table 16. BOM list

Reference	Part	Package	Details	Manufacturer P/N
C1, C2, C24	22 µF	0805	X7T/10V/20%	Murata GRT21BD71A226ME13
C3, C4, C5	22 µF	1206	X7R/10V/10%	Murata GCM31CR71A226KE
C6, C12	N.M.			
C7	1 µF	0603	X7R/25V/10%	Murata GCM188R71E105KA
C9	100 nF	0402	X7R/16V/10%	Murata GRT155R71C104KE
C10	10 nF	0402	X7R/16V/10%	
C21	330 µF	D3L	POSCAP 6.3V/105°C	Panasonic POSCAP 6TAE330ML
C23, C25	N.M.			
L1	470 nH	4 x 4	14.2 Asat / 3.9 mOhm	Coilcraft XGL4030-471
L2	N.M.		Shorted on PCB	
L3	300 nH	3 x 3	7.9 A sat / 4.7 mOhm	Coilcraft XGL3020-301M
R1	68 k	0402	1% tolerance	
R2	15 k	0402	1% tolerance	
R3, R6	N.M.			
R4	27 k	0402	1% tolerance	
R5	100 k	0402		
U1	DCP0606Y	QFN11_2x3		STM DCP0606QTRY

Figure 34. Efficiency (log. scale)

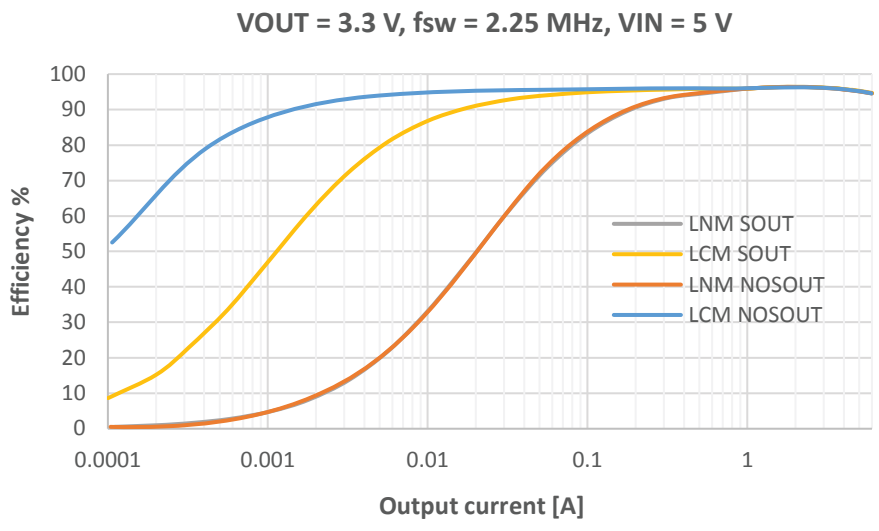


Figure 35. **Efficiency (lin. scale)**

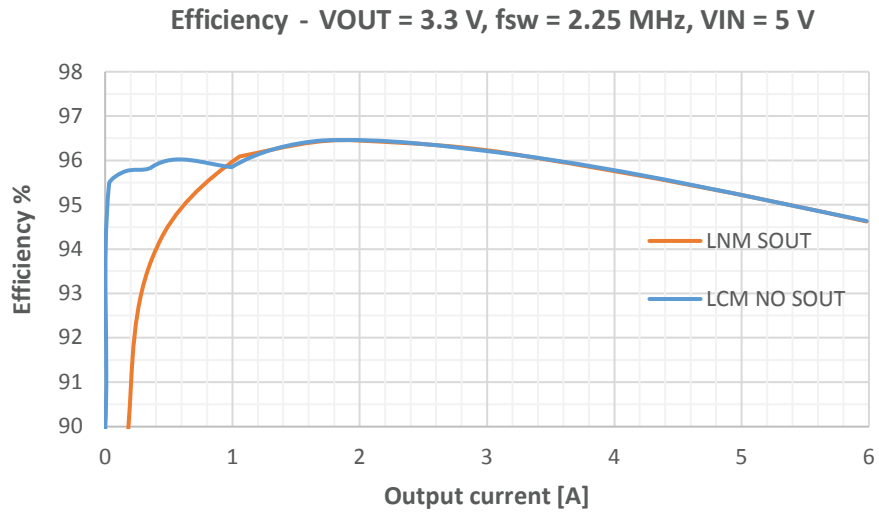


Figure 36. **Total losses (log. scale)**

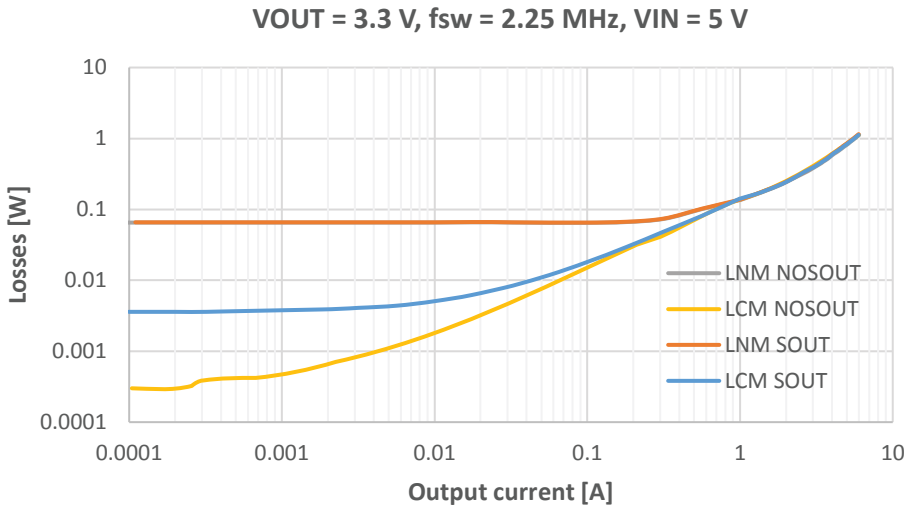
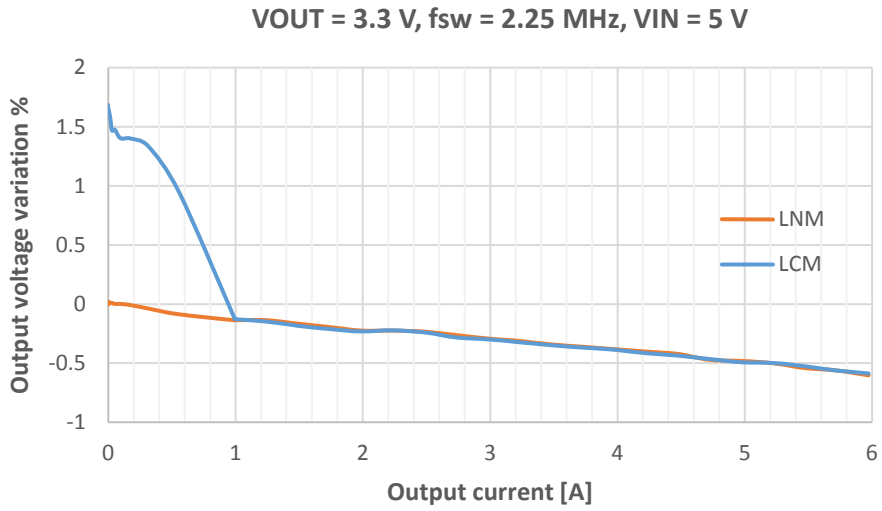


Figure 37. **Load regulation**



With minor modifications in the output filter and voltage programming divider, the following efficiency performances can be measured.

Figure 38. **Efficiency vs. VOUT – VIN = 5 V - LNM**

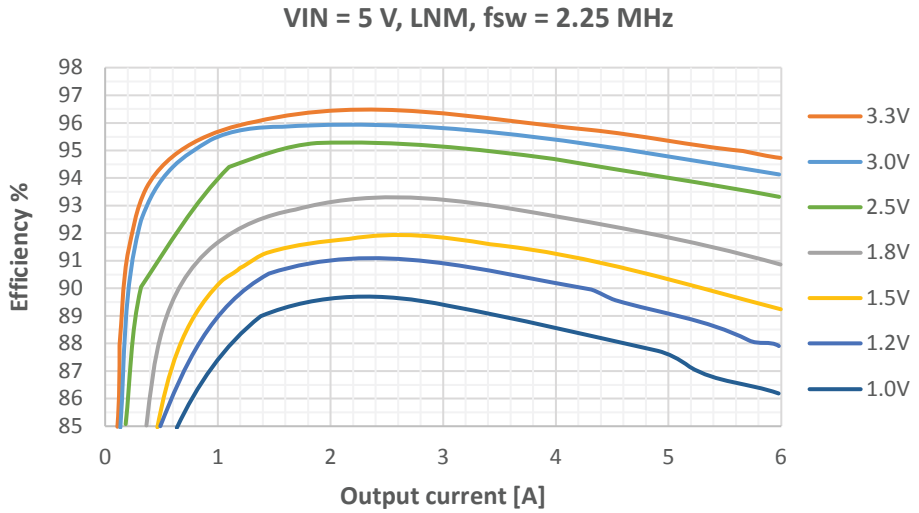


Figure 39. **Efficiency vs. VOUT – VIN = 5 V - LCM (SOUT = GND)**

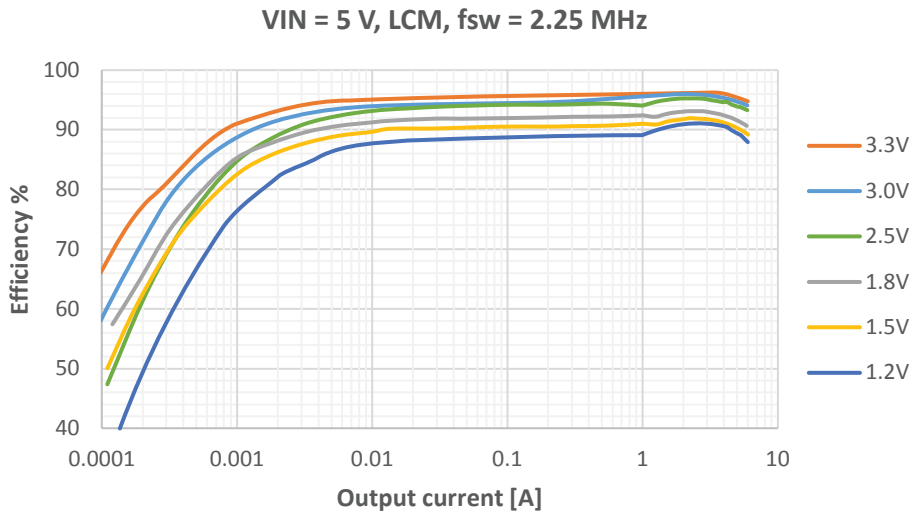


Figure 40. **Efficiency vs. VOUT – VIN = 3.3 V - LNM**

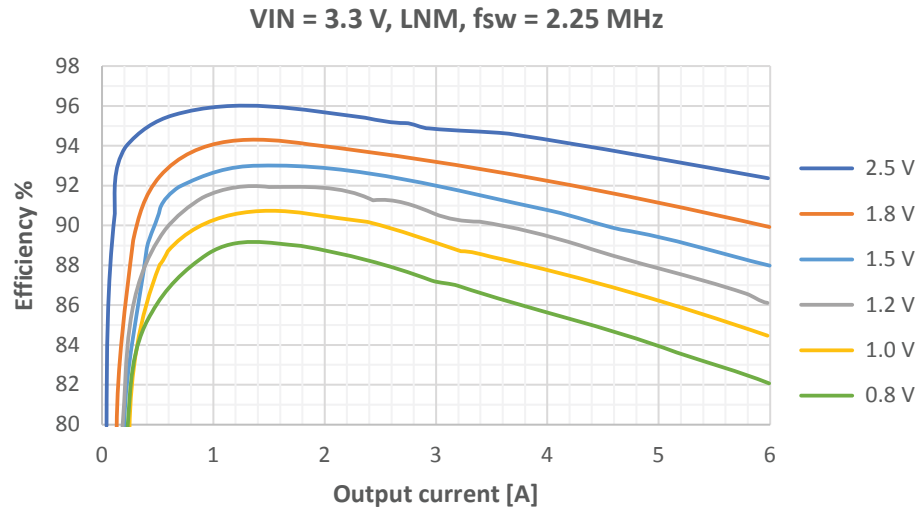
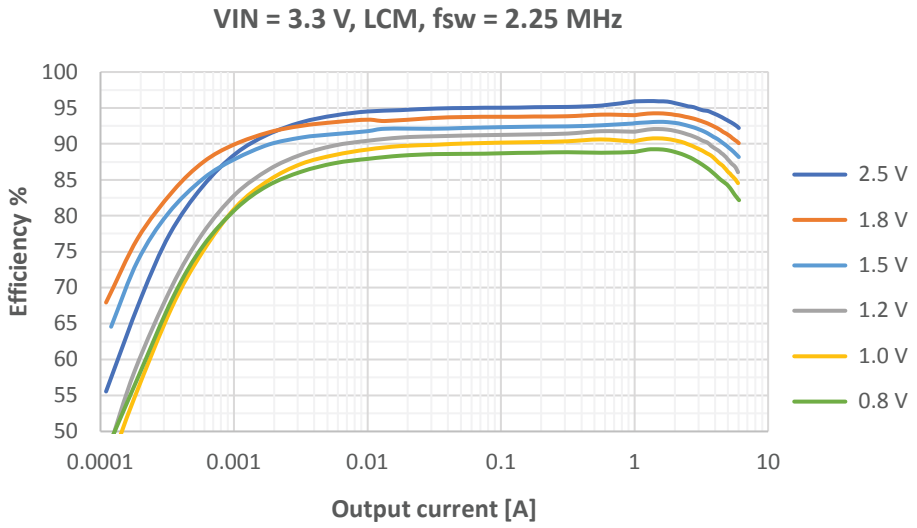


Figure 41. **Efficiency vs. VOUT – VIN = 3.3 V - LCM (SOUT = GND)**



10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN11 (2 x 3 x 0.9 mm) package information

Figure 42. QFN11 (2 x 3 x 0.9 mm) package outline

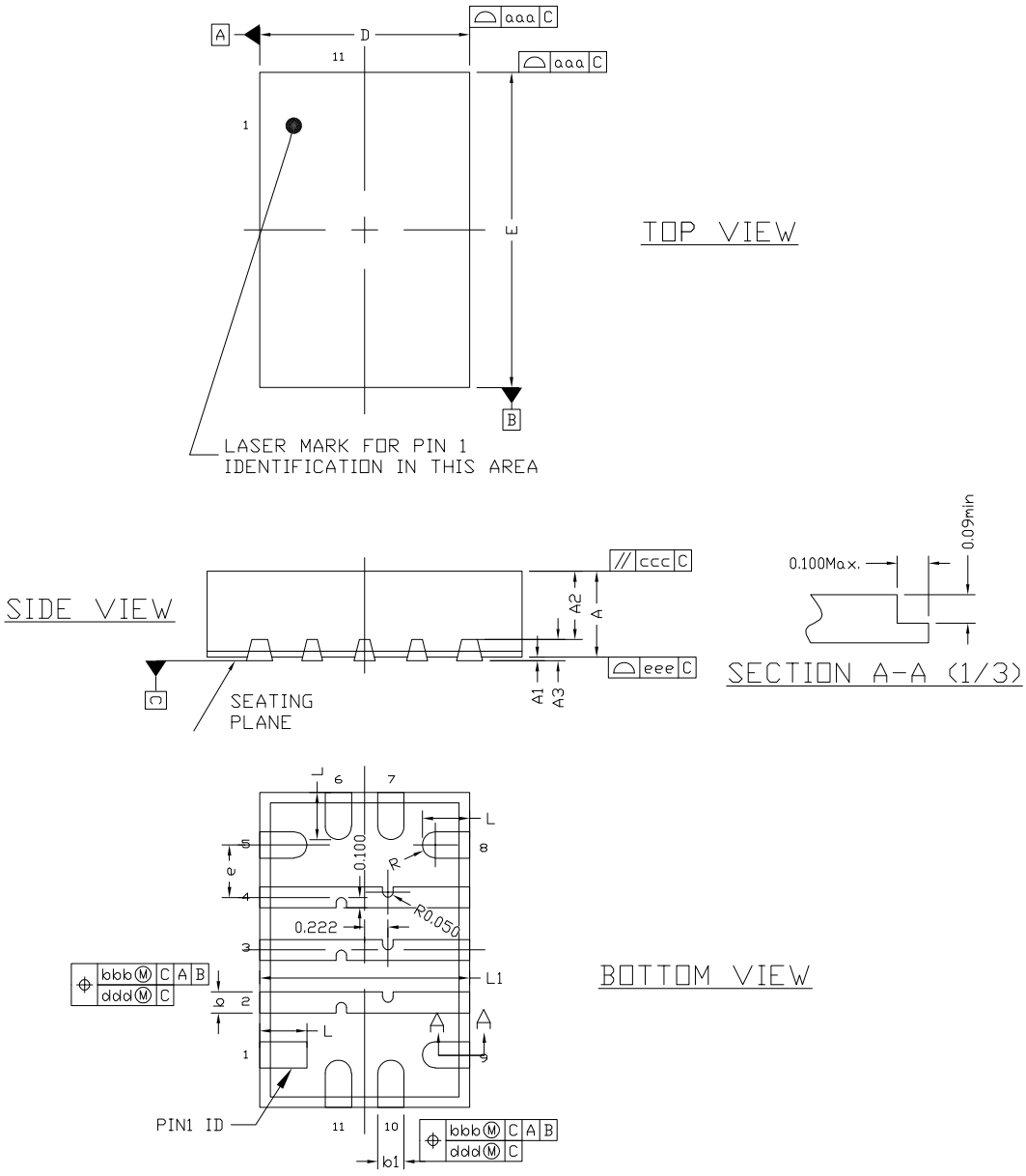
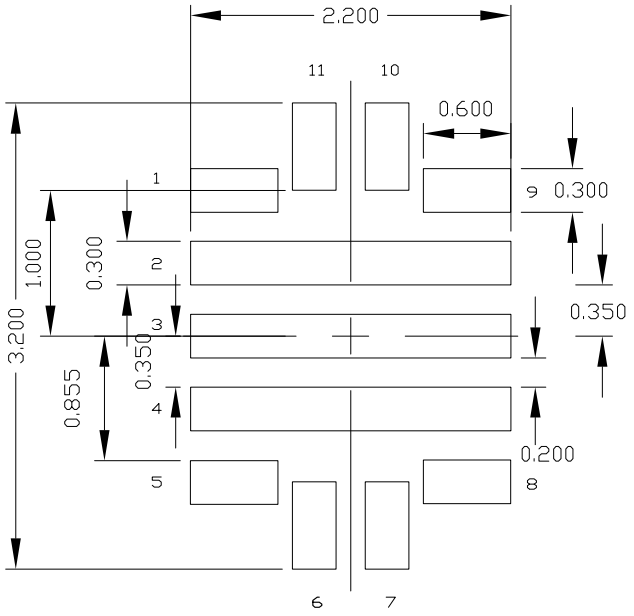


Table 17. **QFN11 (2 x 3 x 0.9 mm) mechanical data**

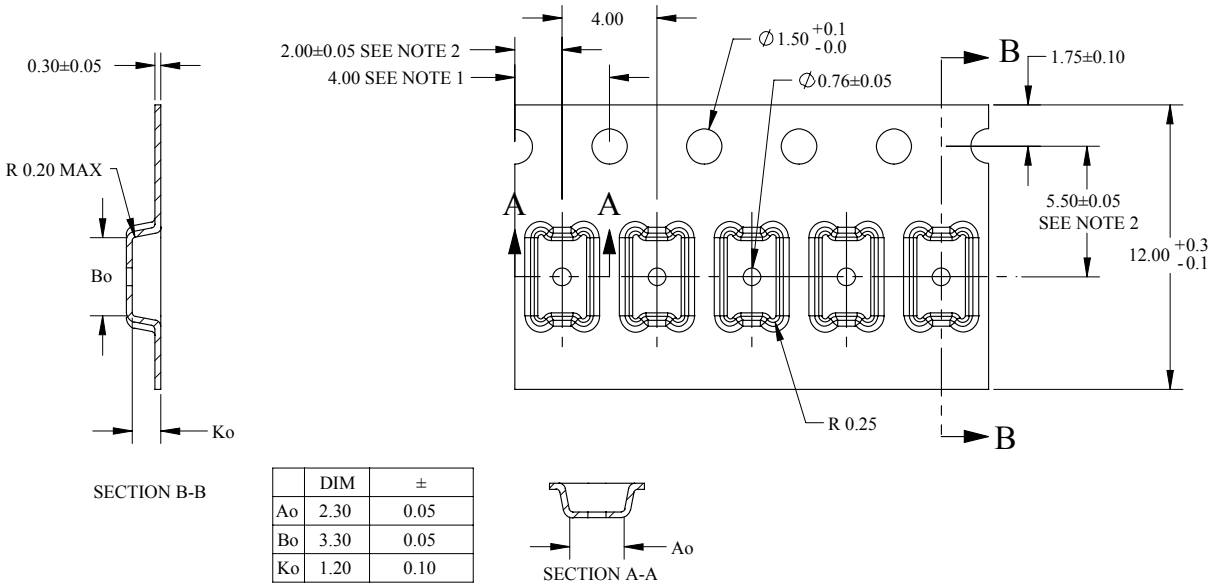
Dim.	mm		
	Min.	Typ.	Max.
A	0.800	0.850	0.900
A1	0.000		0.050
A2	0.600	0.650	0.700
A3		0.203 REF	
b	0.150	0.200	0.250
b1	0.200	0.250	0.300
D	1.900	2.000	2.100
E	2.900	3.000	3.100
L	0.350	0.450	0.550
L1	1.900	2.000	2.100
e		0.500 BSC	
R	0.100		
Tolerance			
aaa	0.100		
bbb	0.100		
ccc	0.100		
ddd	0.050		
eee	0.080		

Figure 43. **QFN11 (2 x 3 x 0.9 mm) recommended footprint - dimensions are in mm**



10.2 QFN11 (2 x 3 x 0.9 mm) packing information

Figure 44. **Carrier tape**



	DIM	±
Ao	2.30	0.05
Bo	3.30	0.05
Ko	1.20	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 45. **Pin 1 orientation. Pin 1 top right**

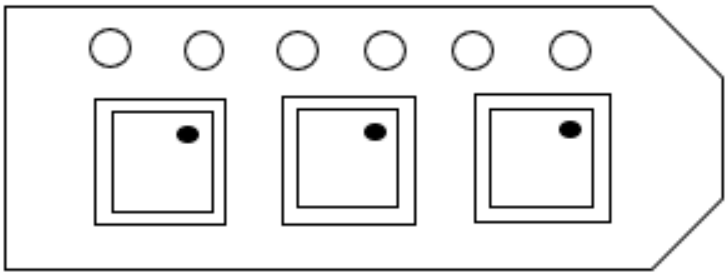


Figure 46. **Carrier reel**

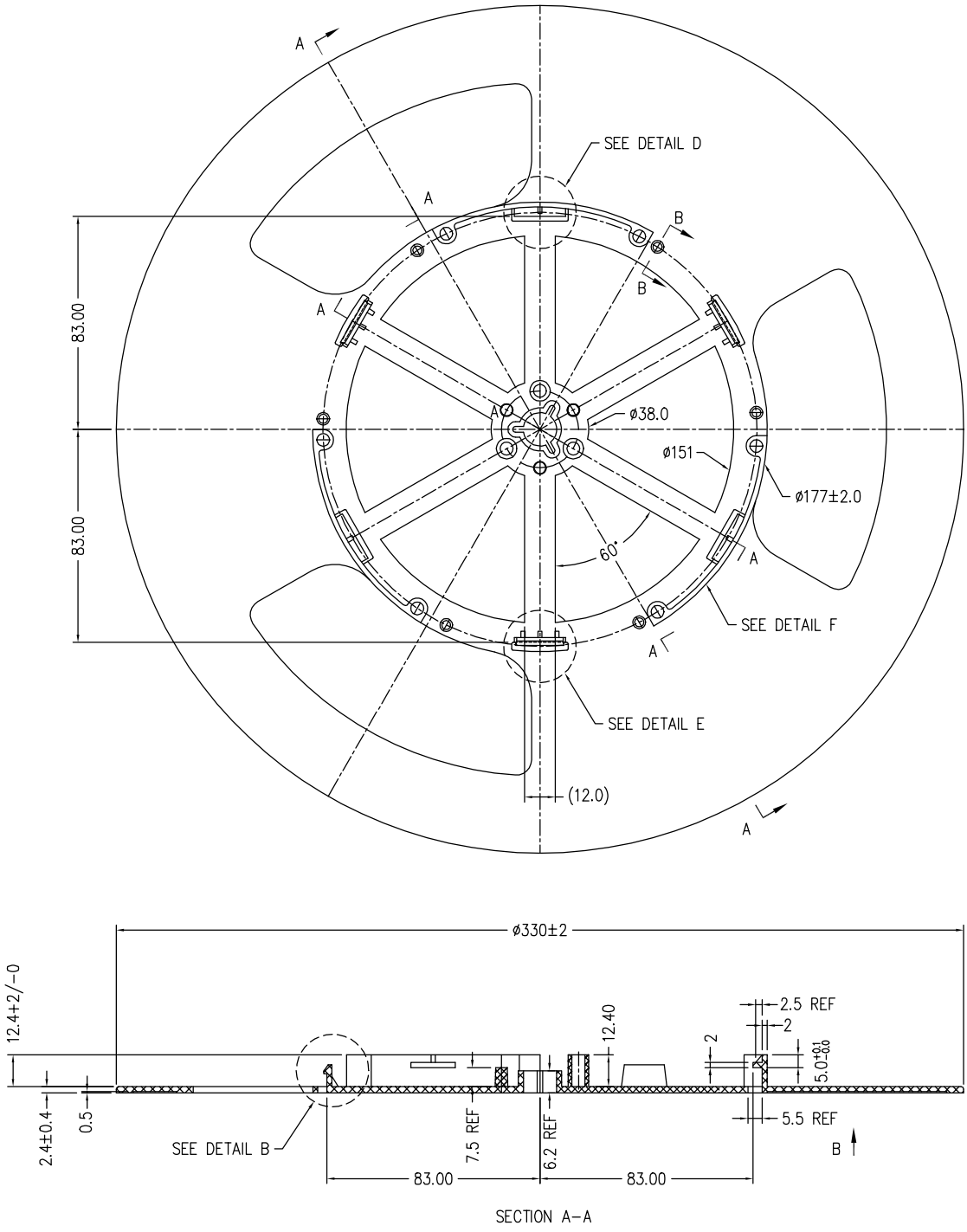
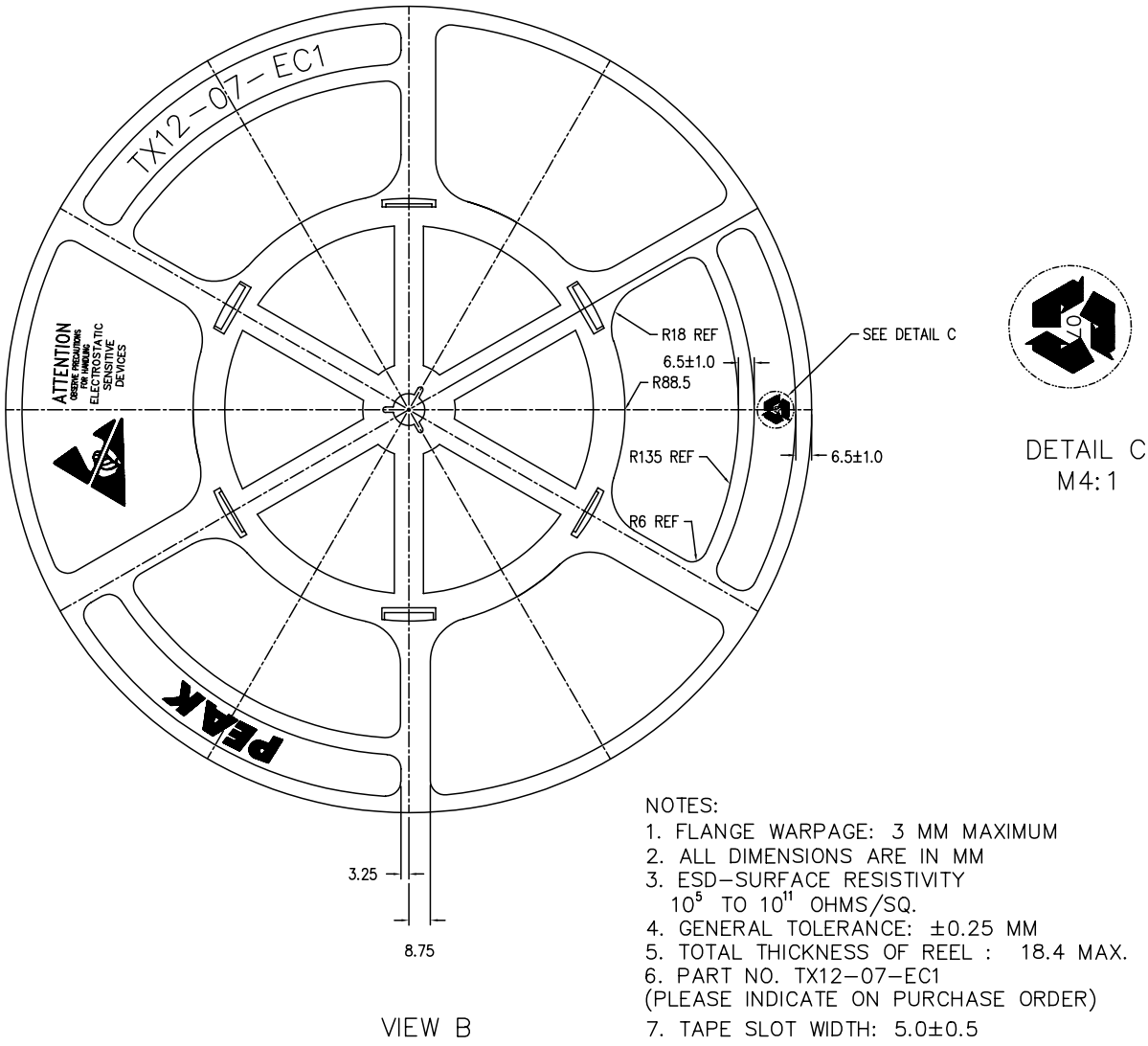


Figure 47. **Reel drawing**



11 Ordering Information

Table 18. DCP0606Y order codes

Order code	VOUT	Output discharge	Marking
DCP0606QTRY	Adjustable	NO	06Y
DCP0606DQTRY		YES	06B
DCP0606V10QTRY (1)	1.0 V	NO	
DCP0606V10DQTR (1)		YES	
DCP0606V12QTRY (1)	1.2 V	NO	
DCP0606V12DQTRY (1)		YES	
DCP0606V18QTRY (1)	1.8 V	NO	
DCP0606V18DQTRY (1)		YES	
DCP0606V30QTRY (1)	3.0 V	NO	
DCP0606V30DQTRY (1)		YES	
DCP0606V33QTRY (1)	3.3 V	NO	
DCP0606V33DQTRY (1)		YES	

1. *On request.*

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
01-Apr-2025	1	Initial release.
24-Apr-2025	2	Updated marking in Table 18.

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