DCR2630C28

Phase Control Thyristor

Replaces DS5803-4 DS5803-5 August 2023 (LN42747)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

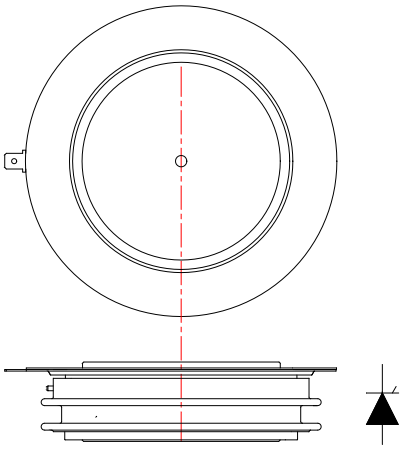
V_{DRM}	**2800V**
$I_{T(AV)}$	**2630A**
I_{TSM}	**35300A**
dV/dt*	**1500V/µs**
dI/dt	**300A/µs**

*** Higher dV/dt selections are available on request**

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} (V)	Conditions
DCR2630C28 DCR2630C26 DCR2630C24	2800 2600 2400	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 200mA, V_{DRM}, V_{RRM} tp = 10ms V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.



Outline type code: C

(See Package Details for further information)

Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2630C28

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2630	A
$I_{T(RMS)}$	RMS value	-	4130	A
I_T	Continuous (direct) on-state current	-	3940	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C V_R = 0	35.3	kA
I^2t	I^2t for fusing		6.23	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	10.1	°C/kW
		Single side cooled	Anode DC	-	17.6	°C/kW
			Cathode DC	-	23.9	°C/kW
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 37kN (with mounting compound)	Double side	-	2.5	°C/kW
			Single side	-	5.0	°C/kW
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			33	41	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	200	mA
V_{TM}	Instantaneous forward voltage	At 4000A peak, T_j = 125°C		1.40	1.65	V
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$ Gate source 30V, 10Ω t_r < 0.5µs, T_j = 125°C	Repetitive 50Hz	-	150	A/µs
			Non-repetitive	-	300	A/µs
$V_{T(TO)}$	Threshold voltage - Low level	500A to 2300A at T_{case} = 125°C		-	0.83	V
	Threshold voltage - High level	2300A to 7000A at T_{case} = 125°C		-	0.97	V
r_T	On-state slope resistance - Low level	500A to 2300A at T_{case} = 125°C		-	0.23	mΩ
	On-state slope resistance - High level	2300A to 7000A at T_{case} = 125°C		-	0.17	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear		100	250	µs
Q_S	Stored charge	I_T = 2000A, T_j = 125°C, dI/dt = 1A/µs		450	2000	µC
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	250	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

CURVES

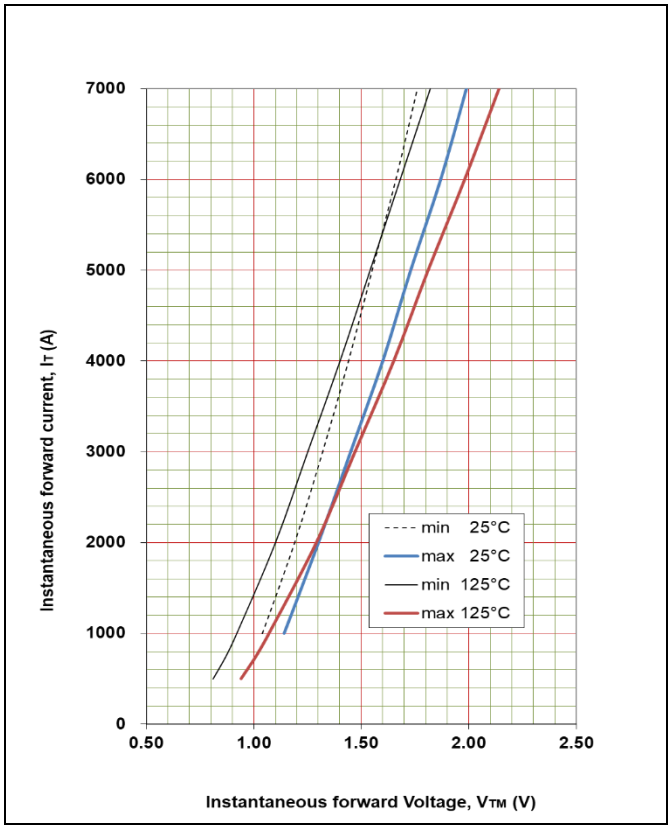


Fig. 2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B.\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.533109
B = 0.039168
C = 0.000126
D = 0.004483

These values are valid for T_j = 125°C for I_T 500A to 7000A

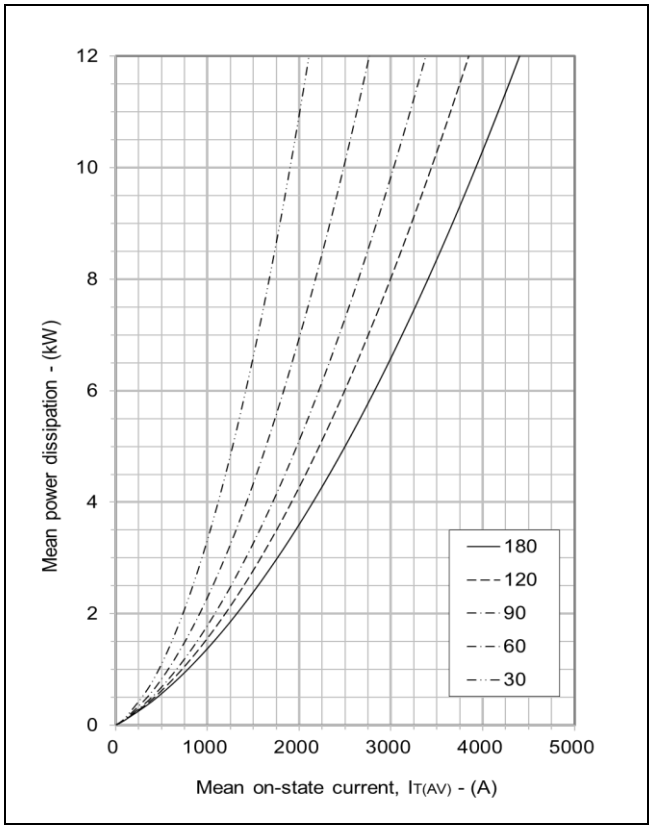


Fig. 3 On-state power dissipation - sine wave

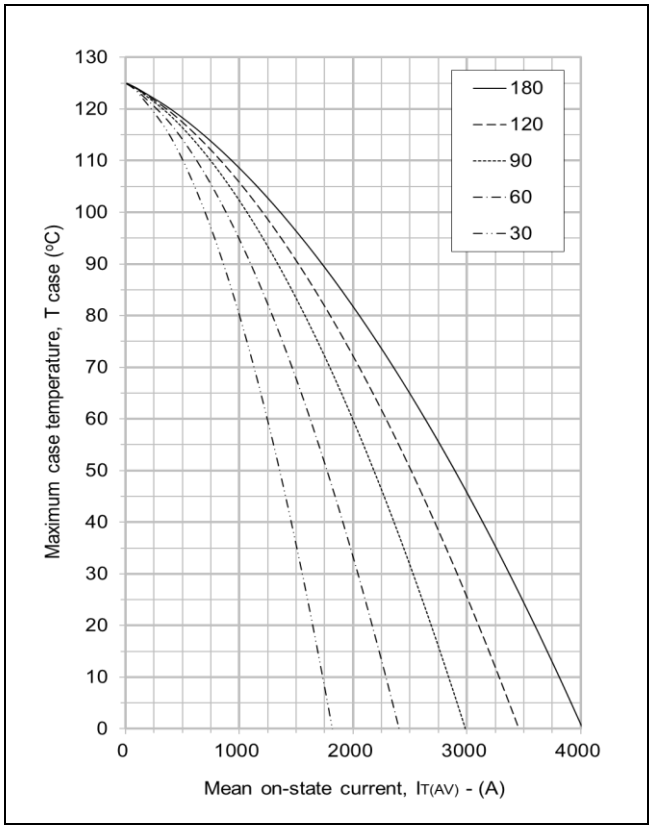


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

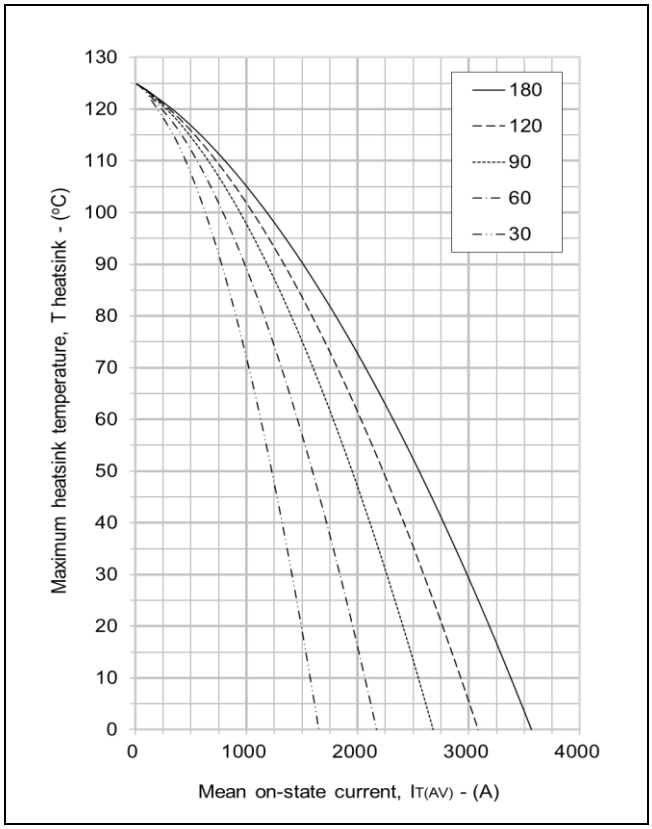


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

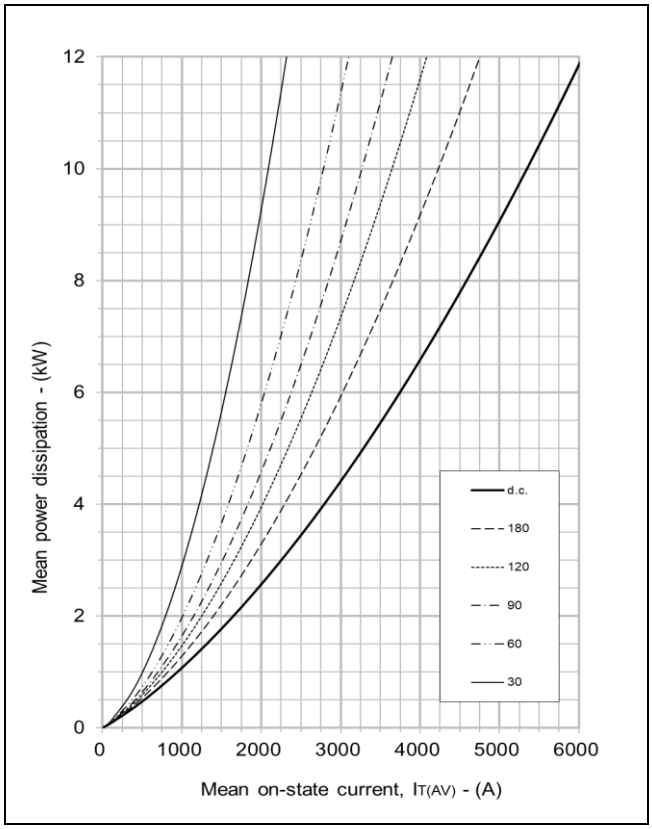


Fig. 6 On-state power dissipation - rectangular wave

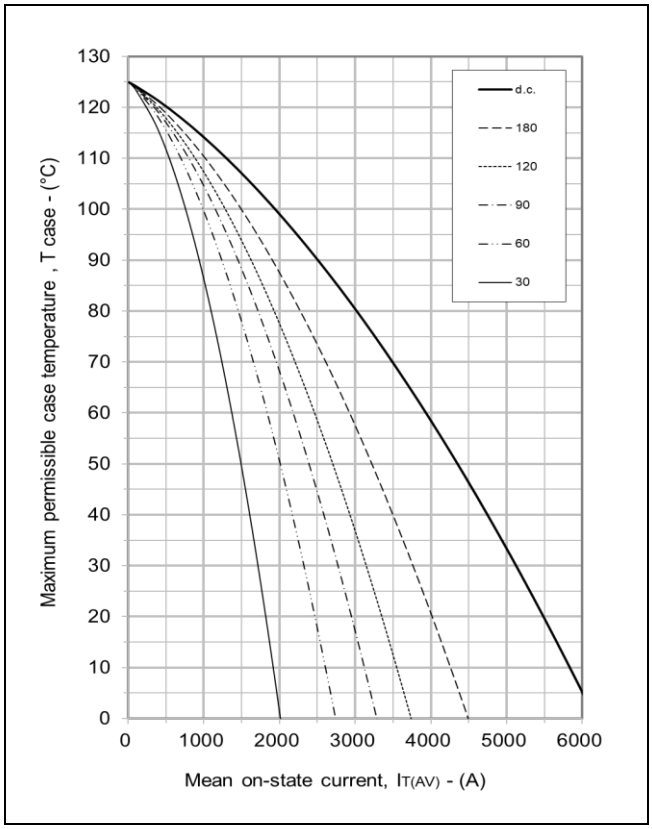


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

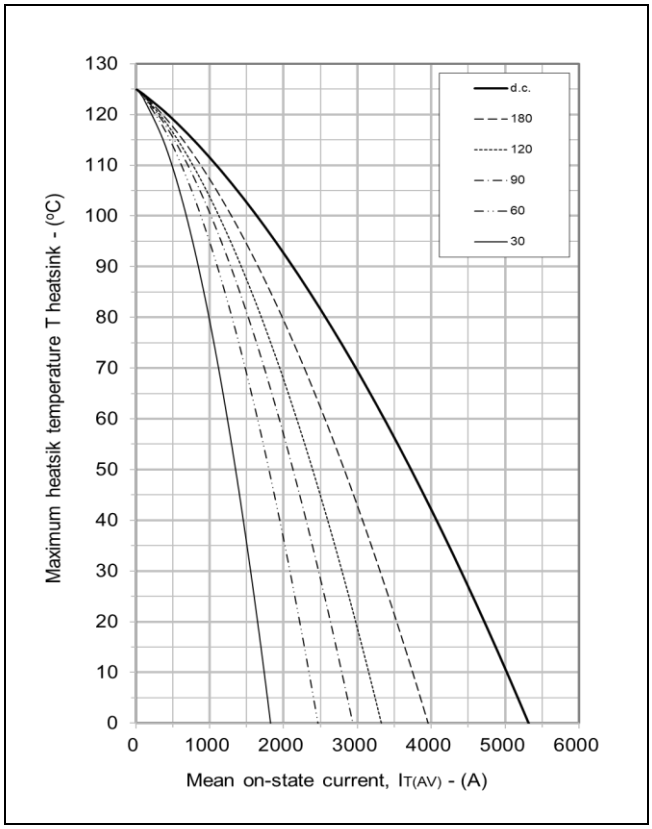
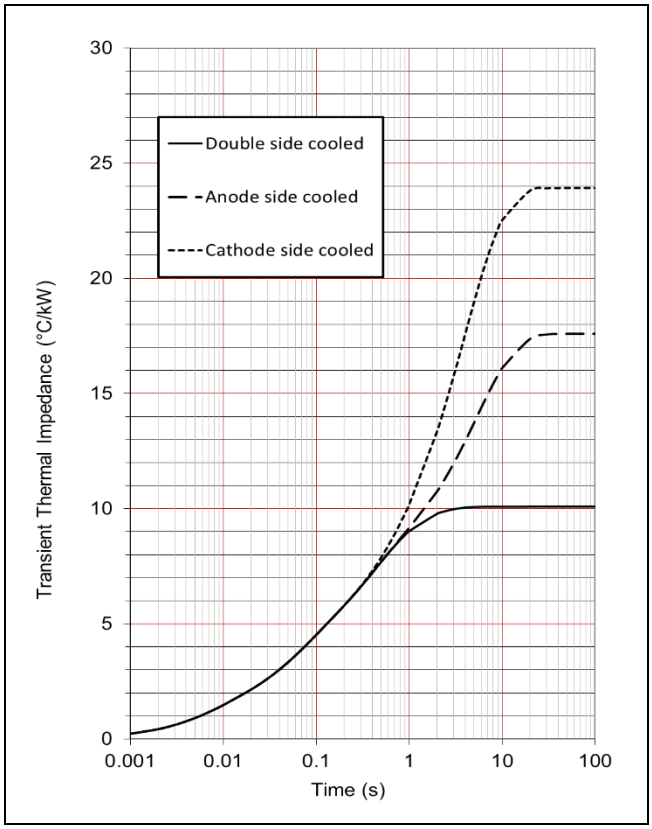


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	Ri(°C/kW)	1.104	2.576	4.510	1.901
	Ti(s)	0.006	0.052	0.382	1.060
Anode side cooled	Ri(°C/kW)	1.098	2.457	4.047	9.999
	Ti(s)	0.006	0.050	0.313	5.270
Cathode side cooled	Ri(°C/kW)	1.152	2.893	2.406	17.479
	Ti(s)	0.006	0.058	0.378	3.970

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	1.95	1.26
120	2.32	1.89
90	2.74	2.27
60	3.14	2.70
30	3.46	3.19
15	3.61	3.47

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	1.95	1.26
120	2.32	1.89
90	2.74	2.27
60	3.14	2.70
30	3.46	3.19
15	3.62	3.47

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	1.95	1.26
120	2.31	1.88
90	2.72	2.26
60	3.12	2.68
30	3.43	3.17
15	3.58	3.44

Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

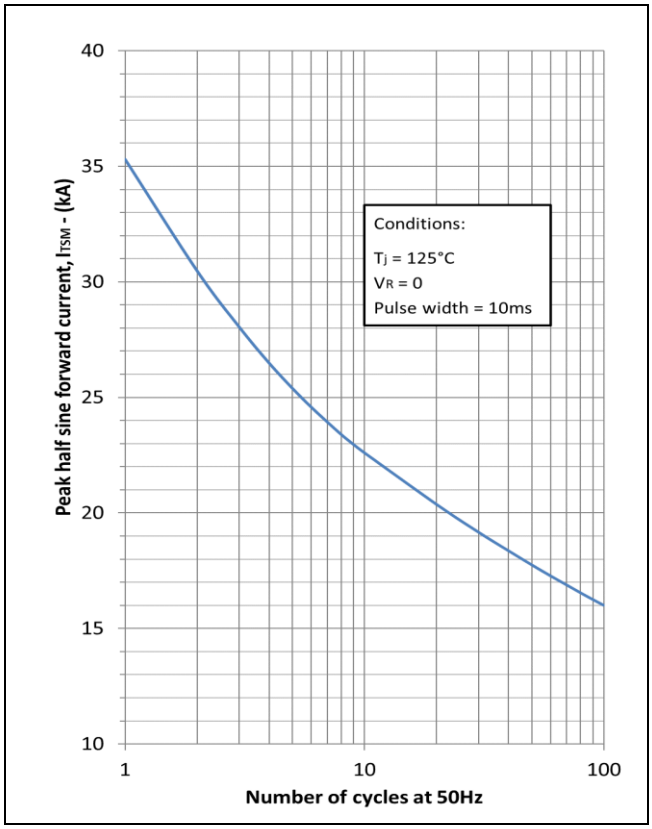


Fig. 10 Multi-cycle surge current

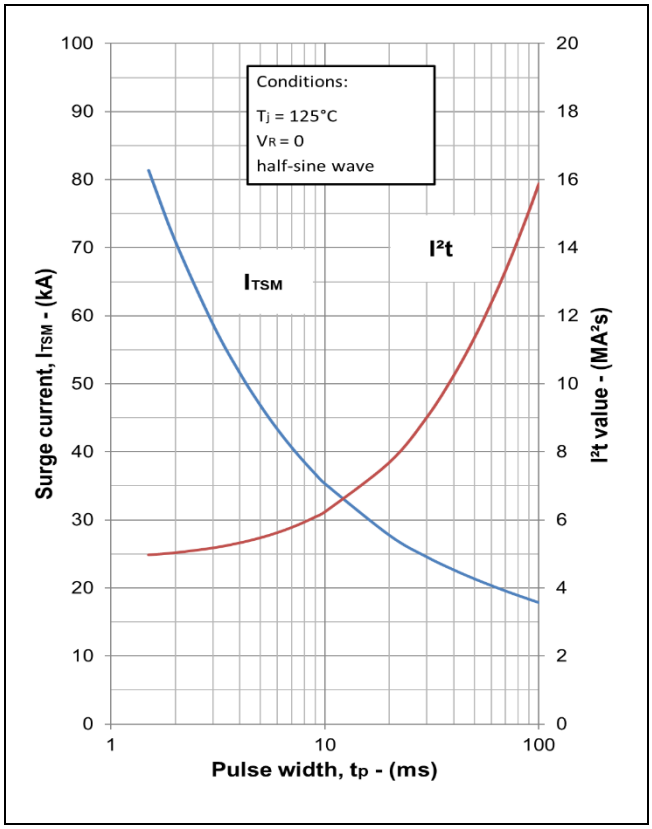


Fig. 11 Single-cycle surge current

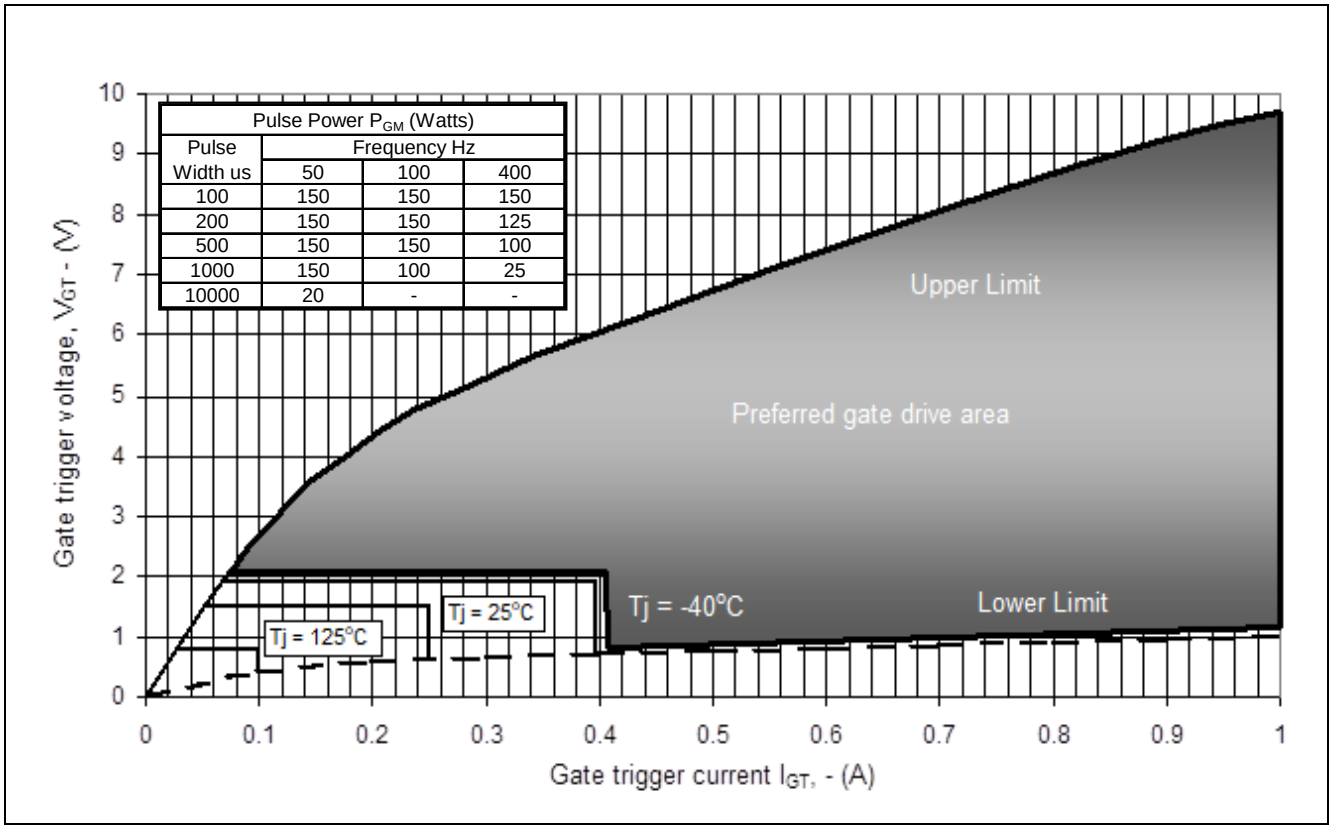


Fig. 14 Gate characteristics

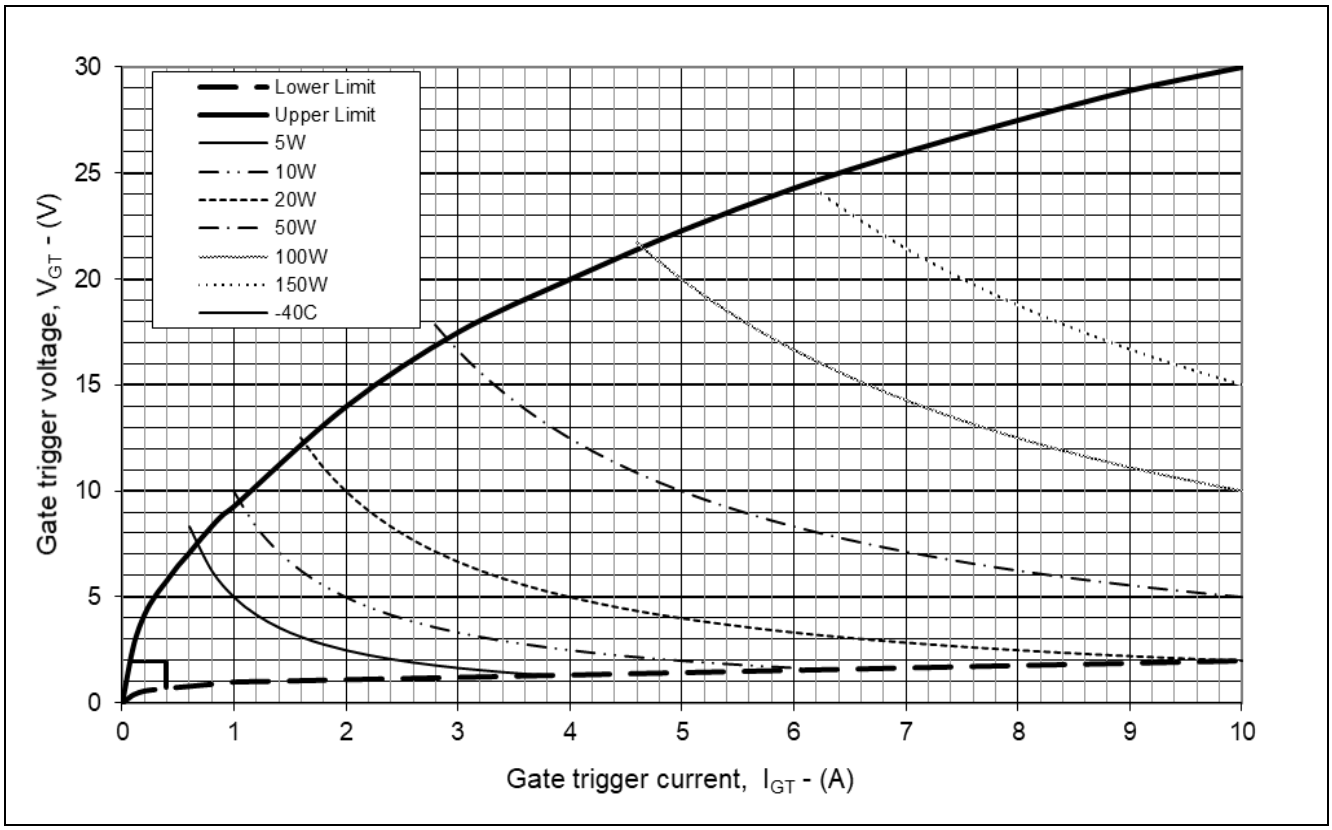


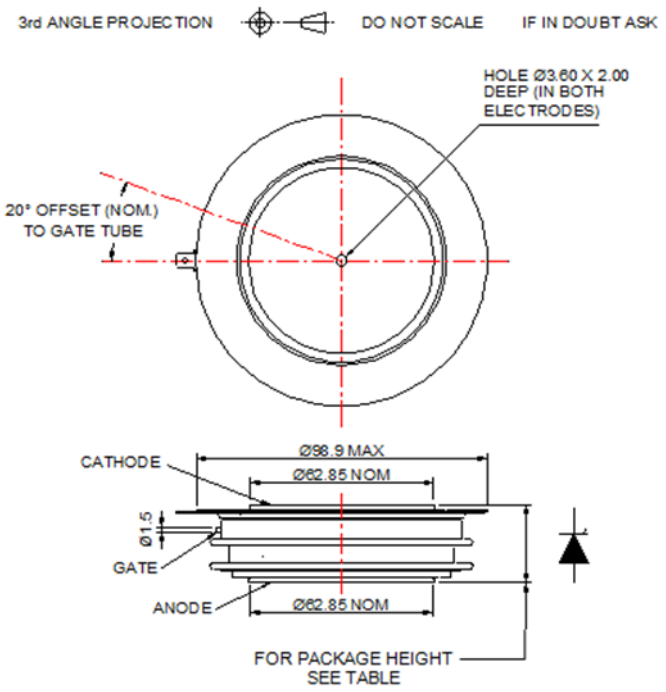
Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE



Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCR1370C85	27.4	26.9
DCR1650C65	27.1	26.6
DCR1950C52	26.9	26.3
DCR2150C42	26.7	26.2
DCR2630C28	**26.5**	**26.0**
DCR3370C22	26.4	25.9
DCR3370C18	26.3	25.8

Lead length: 420mm

Lead terminal connector: M4 ring

Package outline type code: C

Fig. 16 Package outline

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