

**FEATURES**

- Double Side Cooling
- High Surge Capability

**APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

**KEY PARAMETERS**

$V_{DRM}$	<b>2200V</b>
$I_{T(AV)}$	<b>3890A</b>
$I_{TSM}$	<b>54000A</b>
$dV/dt^*$	<b>1500V/<math>\mu</math>s</b>
$dI/dt$	<b>300A/<math>\mu</math>s</b>

\* Higher  $dV/dt$  selections are available on request

**VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ (V)	Conditions
DCR3910Y22	2200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR3910Y20	2000	
DCR3910Y18	1800	

Lower voltage grades available.

**ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

**DCR3910Y22**

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

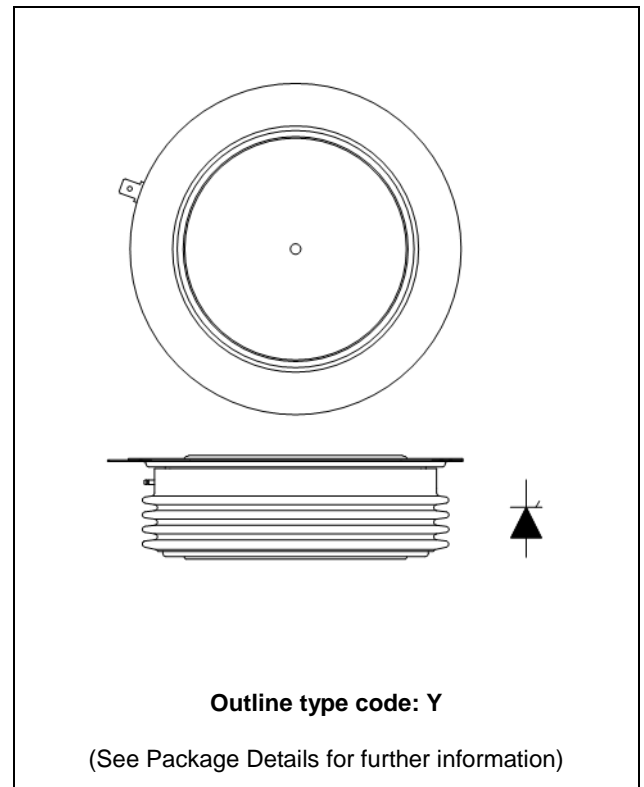


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}C$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3890	A
$I_{T(RMS)}$	RMS value	-	6110	A
$I_r$	Continuous (direct) on-state current	-	5390	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}C$	54.0	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	14.6	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	8.4	$^{\circ}C/kW$
		Single side cooled	Anode DC	-	13.4	$^{\circ}C/kW$
			Cathode DC	-	23.1	$^{\circ}C/kW$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	2.0	$^{\circ}C/kW$
			Single side	-	4.0	$^{\circ}C/kW$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}C$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}C$	
$F_m$	Clamping force		48	59	kN	

**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
<b>I<sub>RRM</sub>/I<sub>DRM</sub></b>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C	-	200	mA	
<b>V<sub>TM</sub></b>	Instantaneous forward voltage	At 4000A peak, T <sub>j</sub> = 125°C	1.15	1.30	V	
<b>dV/dt</b>	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, gate open	-	1500	V/μs	
<b>di/dt</b>	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub> Gate source 30V, 10Ω tr < 0.5μs, T <sub>j</sub> = 125°C	Repetitive 50Hz	-	150	A/μs
			Non-repetitive	-	300	A/μs
<b>V<sub>T(TO)</sub></b>	Threshold voltage - Low level	500A to 2300A at T <sub>case</sub> = 125°C	-	0.78	V	
	Threshold voltage - High level	2300A to 7000A at T <sub>case</sub> = 125°C	-	0.92	V	
<b>r<sub>T</sub></b>	On-state slope resistance - Low level	500A to 2300A at T <sub>case</sub> = 125°C	-	0.16	mΩ	
	On-state slope resistance - High level	2300A to 7000A at T <sub>case</sub> = 125°C	-	0.10	mΩ	
<b>t<sub>gd</sub></b>	Delay time	V <sub>D</sub> = 67% V <sub>DRM</sub> , gate source 30V, 10Ω tr = 0.5μs, T <sub>j</sub> = 25°C	-	3	μs	
<b>t<sub>q</sub></b>	Turn-off time	T <sub>j</sub> = 125°C, V <sub>R</sub> = 200V, di/dt = 1A/μs, dV <sub>DR</sub> /dt = 20V/μs linear	-	600	μs	
<b>Q<sub>s</sub></b>	Stored charge	I <sub>T</sub> = 2000A, T <sub>j</sub> = 125°C, di/dt = 1A/μs	390	1920	μC	
<b>I<sub>RR</sub></b>	Reverse recovery current	V <sub>R(peak)</sub> ~ 1300V, V <sub>RM</sub> ~ 900V	17	36	A	
<b>I<sub>L</sub></b>	Latching current	T <sub>j</sub> = 25°C, V <sub>D</sub> = 5V	-	3	A	
<b>I<sub>H</sub></b>	Holding current	T <sub>j</sub> = 25°C, R <sub>G-K</sub> = ∞, I <sub>TM</sub> = 500A, I <sub>T</sub> = 5A	-	300	mA	

### GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	250	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

### CURVES

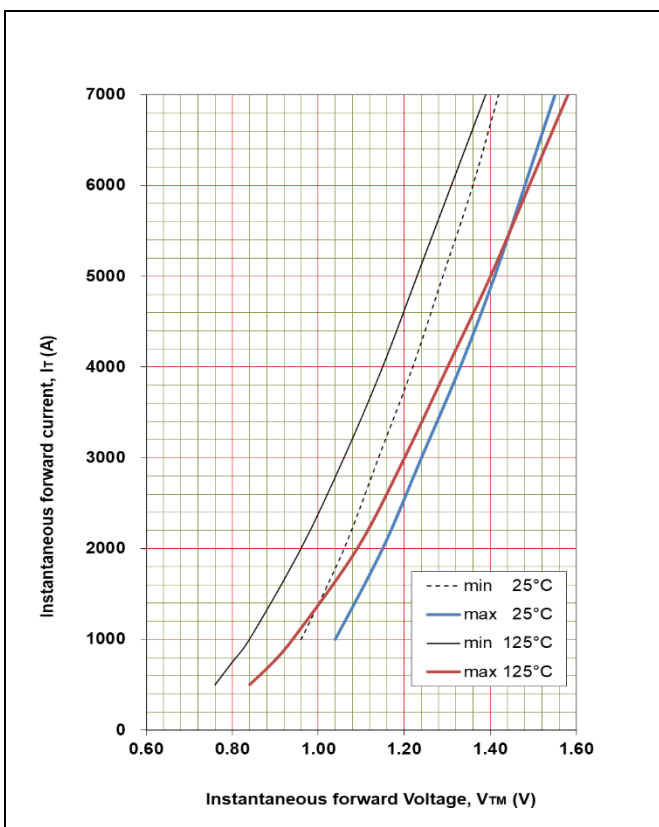


Fig. 2 Maximum & minimum on state characteristics

### V<sub>TM</sub> EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.404689

B = 0.051381

C = 0.000056

D = 0.003938

These values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 500A to 7000A

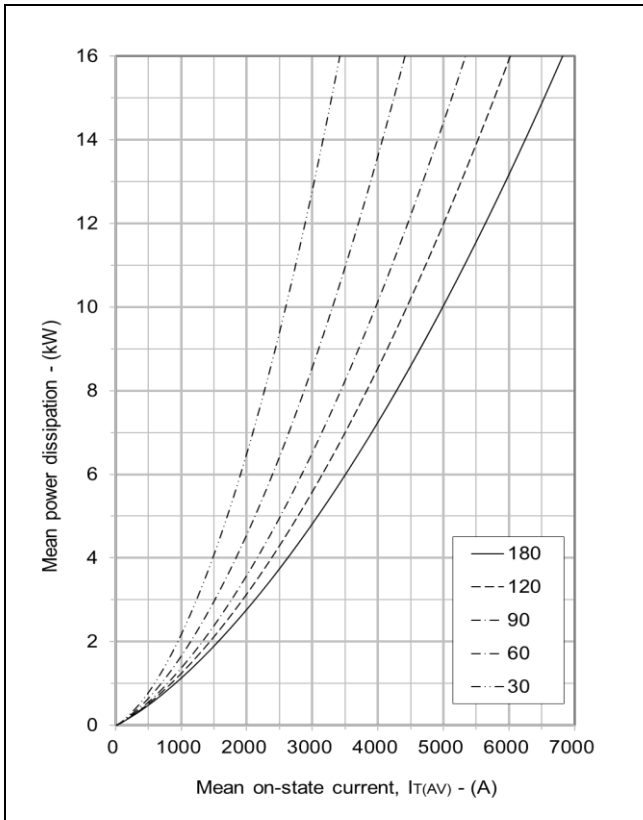


Fig. 3 On-state power dissipation - sine wave

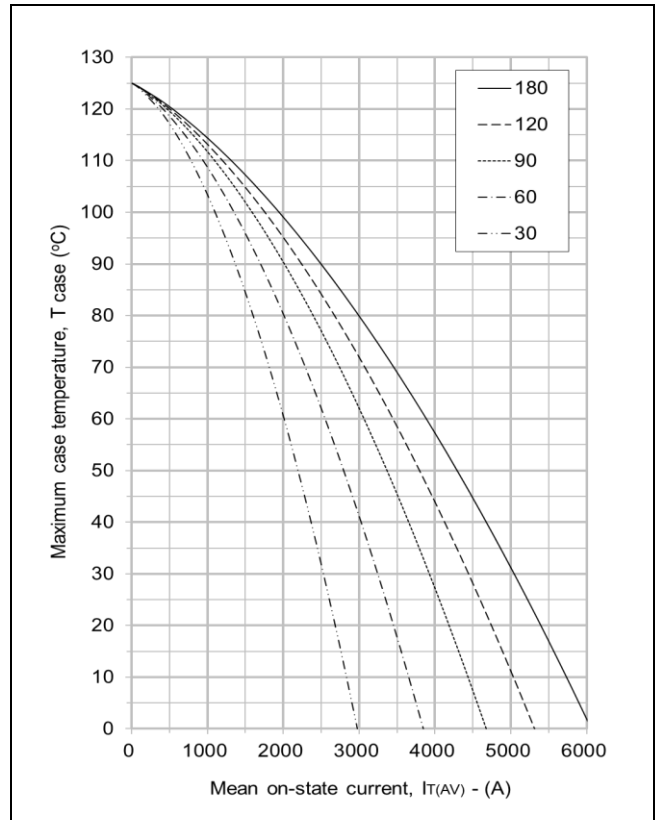


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

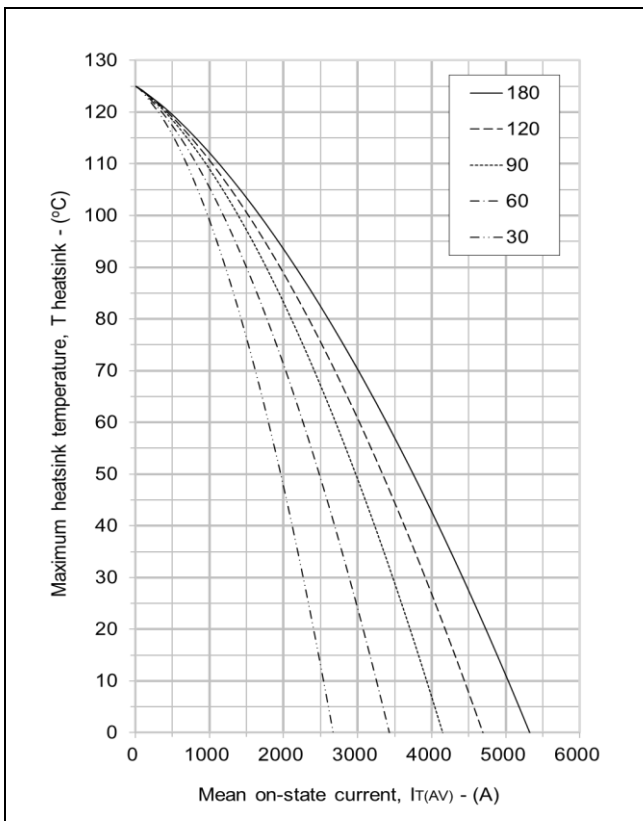


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

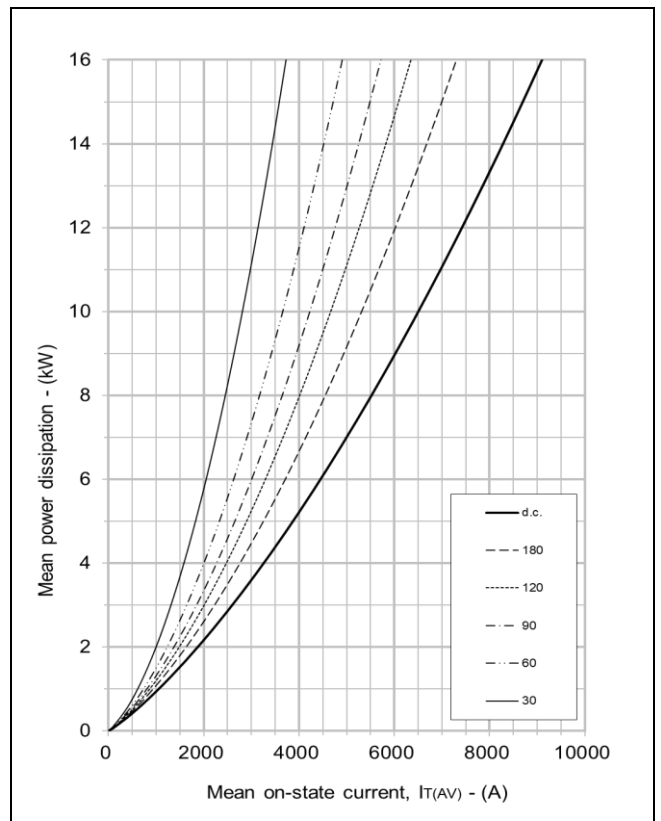


Fig. 6 On-state power dissipation - rectangular wave

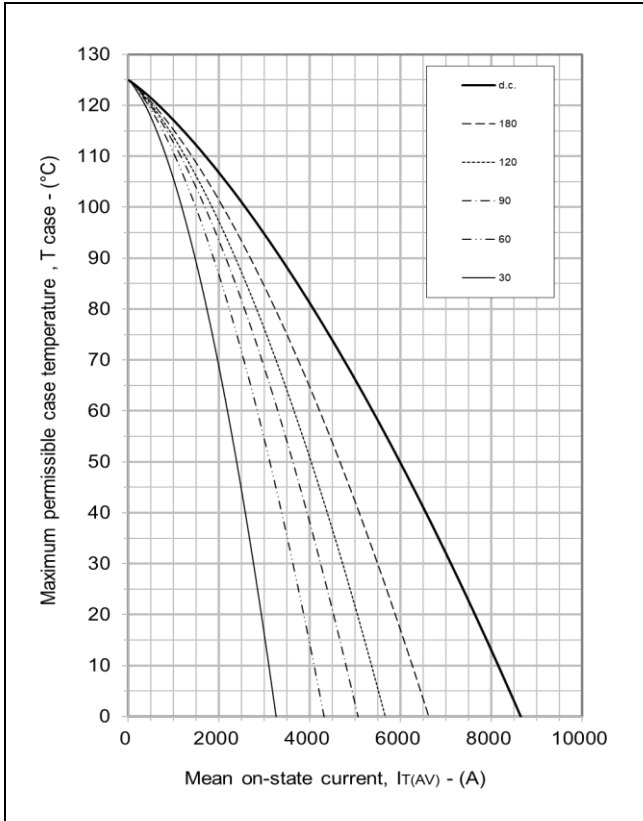


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

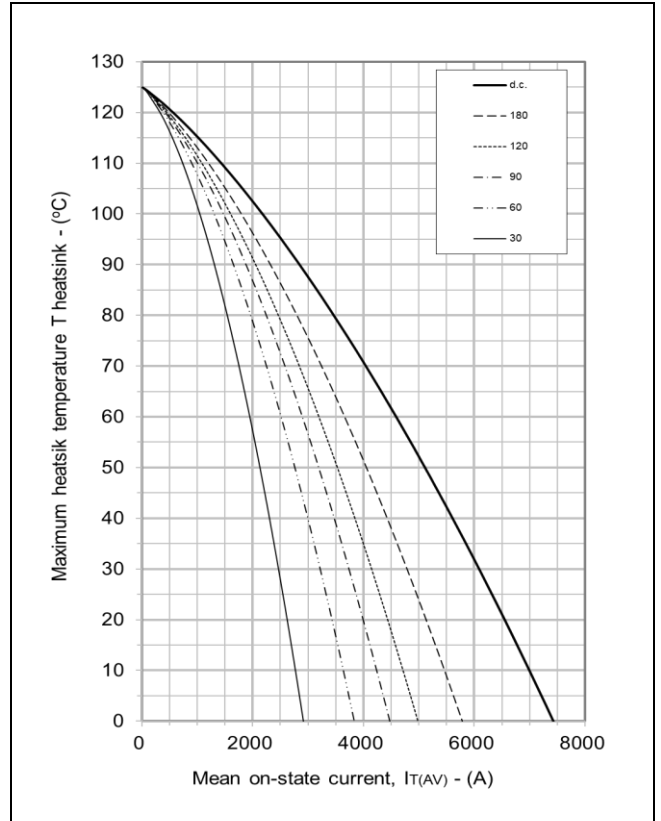


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

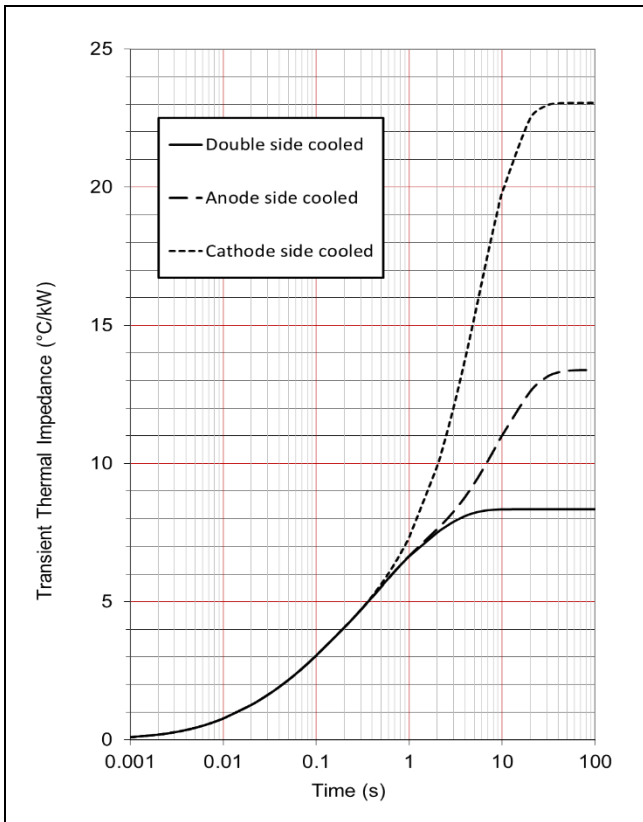


Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

		1	2	3	4
Double side cooled	Ri(°C/kW)	0.612	1.772	3.105	2.861
	Ti(s)	0.010	0.056	0.333	1.632
Anode side cooled	Ri(°C/kW)	0.701	1.939	3.610	7.138
	Ti(s)	0.011	0.066	0.420	9.061
Cathode side cooled	Ri(°C/kW)	0.673	2.017	1.731	18.639
	Ti(s)	0.011	0.066	0.304	5.727

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
$\theta^\circ$	$\Delta Z_{th} (z)$		$\theta^\circ$	$\Delta Z_{th} (z)$		$\theta^\circ$	$\Delta Z_{th} (z)$	
	sine	rect		sine	rect		sine	rect
180	0.94	0.65	180	0.94	0.64	180	0.94	0.64
120	1.09	0.92	120	1.08	0.91	120	1.08	0.91
90	1.24	1.07	90	1.23	1.06	90	1.24	1.06
60	1.38	1.23	60	1.37	1.22	60	1.37	1.22
30	1.49	1.40	30	1.47	1.38	30	1.48	1.39
15	1.54	1.49	15	1.52	1.47	15	1.53	1.48

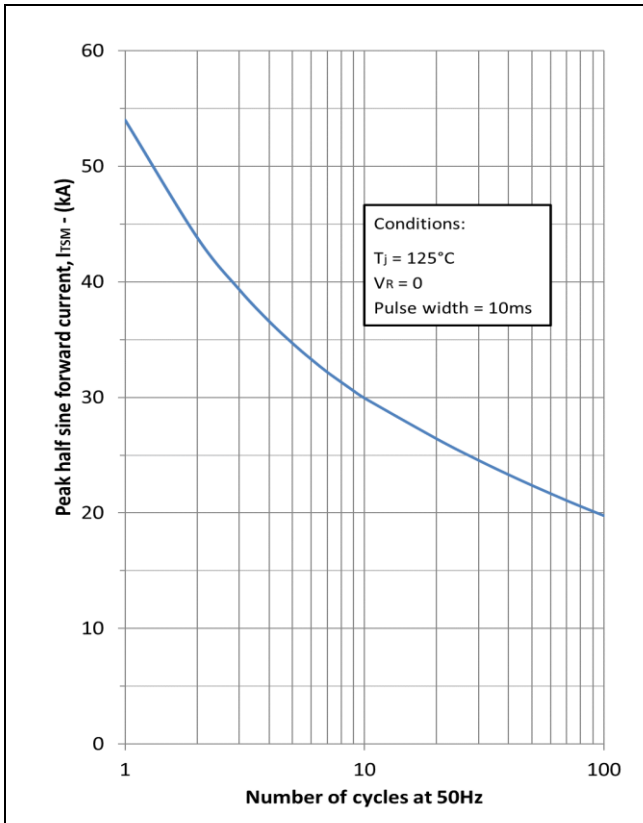


Fig. 10 Multi-cycle surge current

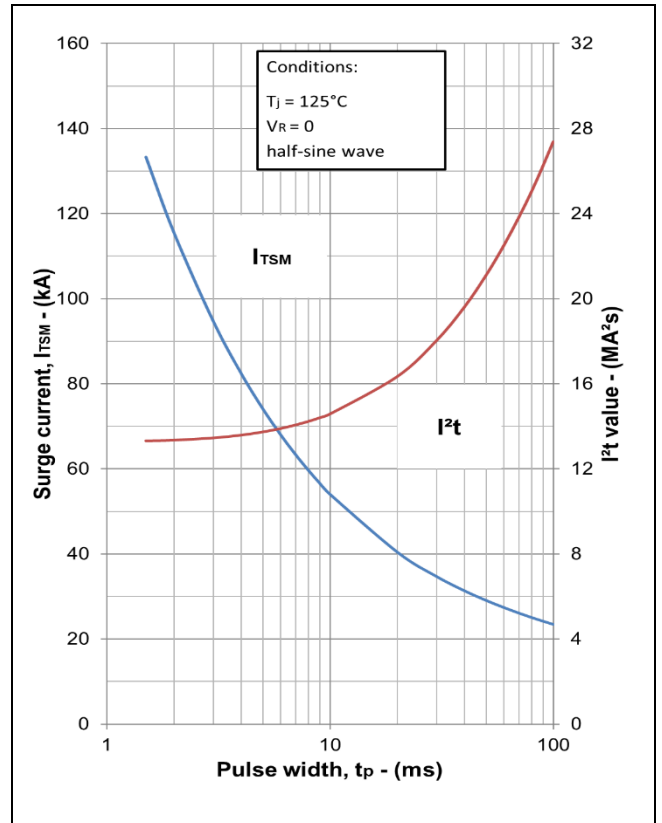


Fig. 11 Single-cycle surge current

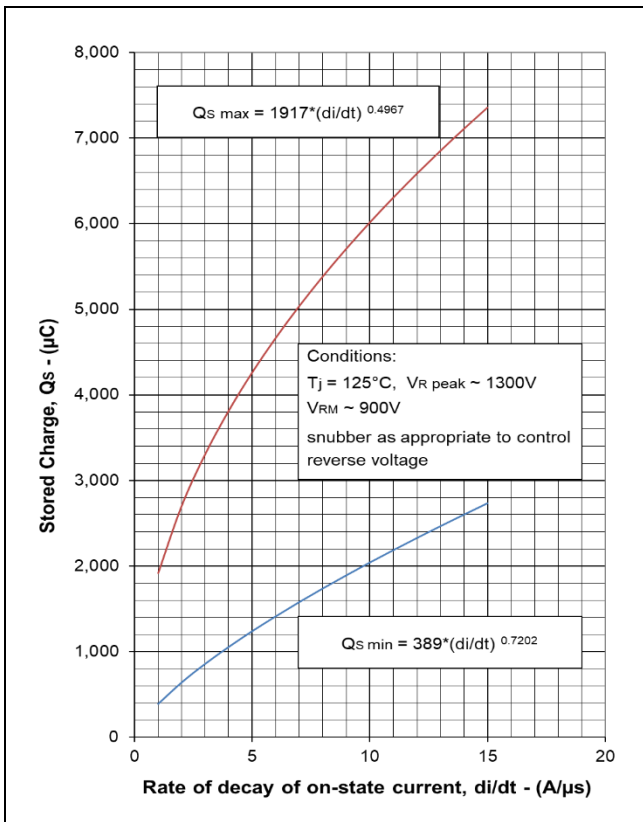


Fig. 12 Stored charge

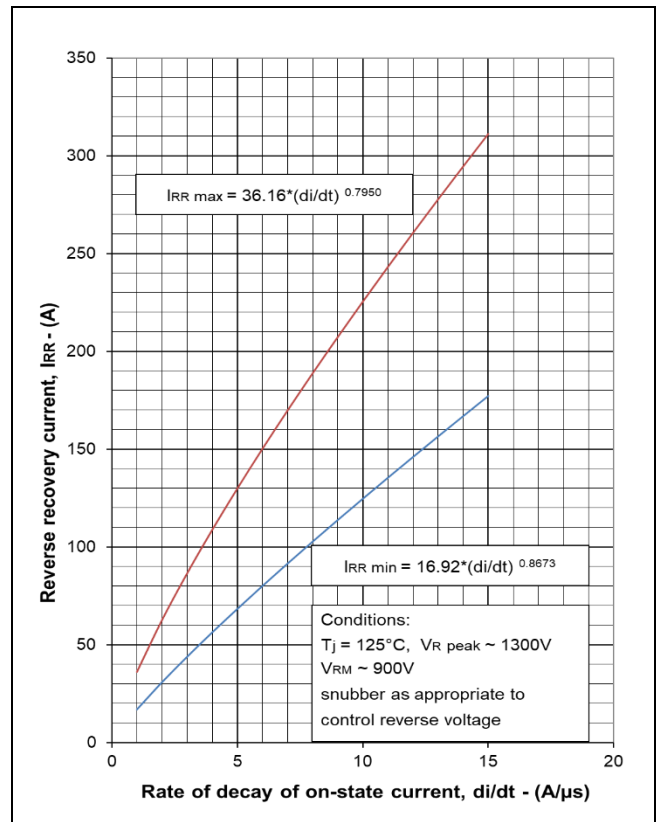


Fig. 13 Reverse recovery current

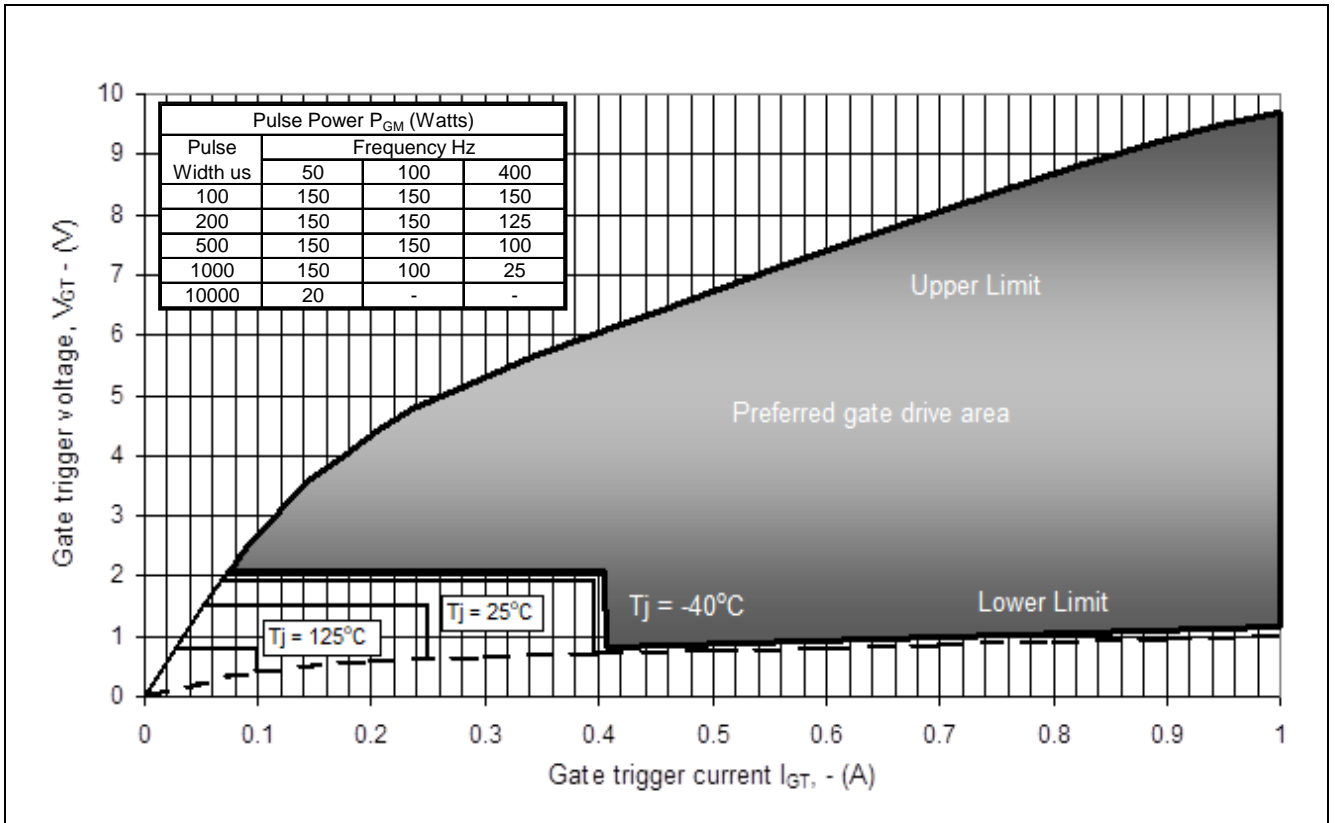


Fig. 14 Gate characteristics

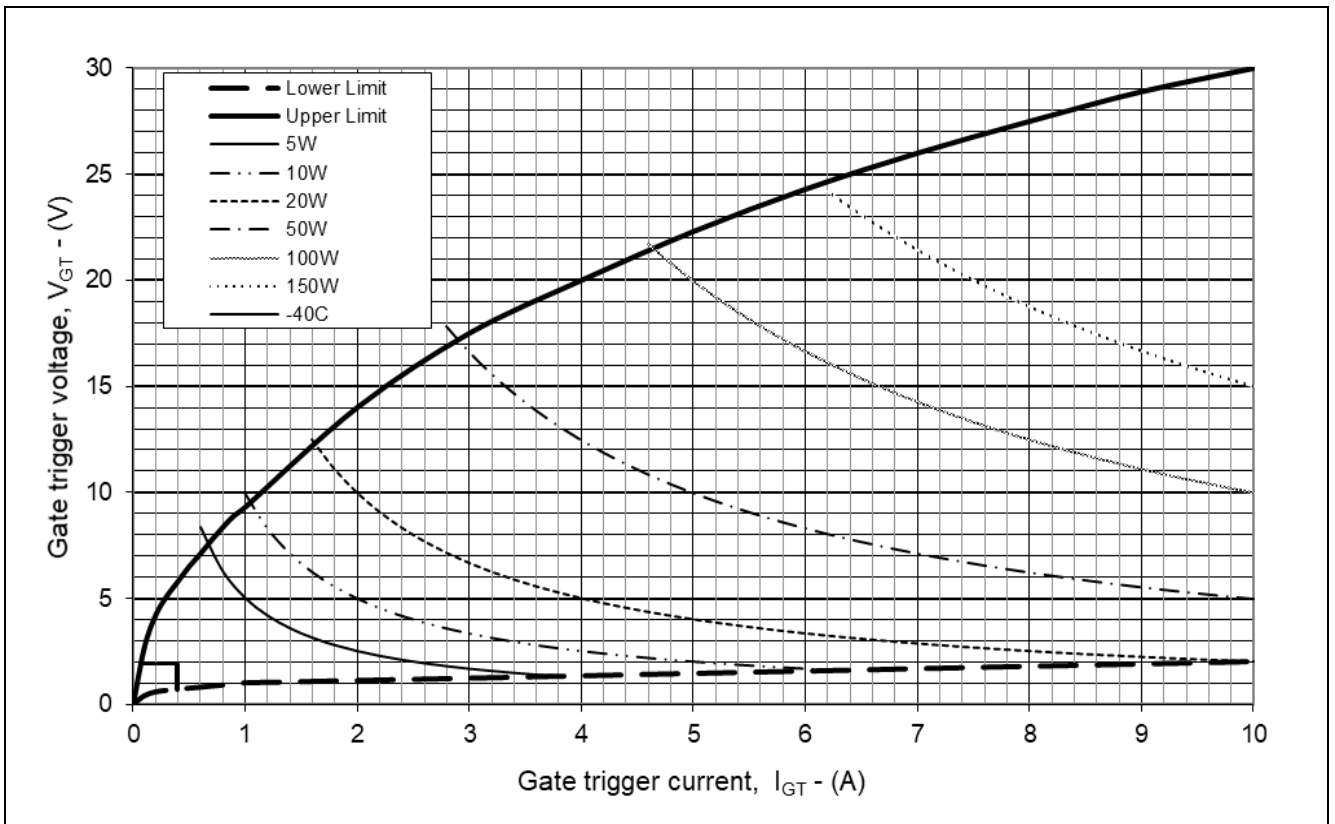


Fig. 15 Gate characteristics



**PACKAGE DETAILS**

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

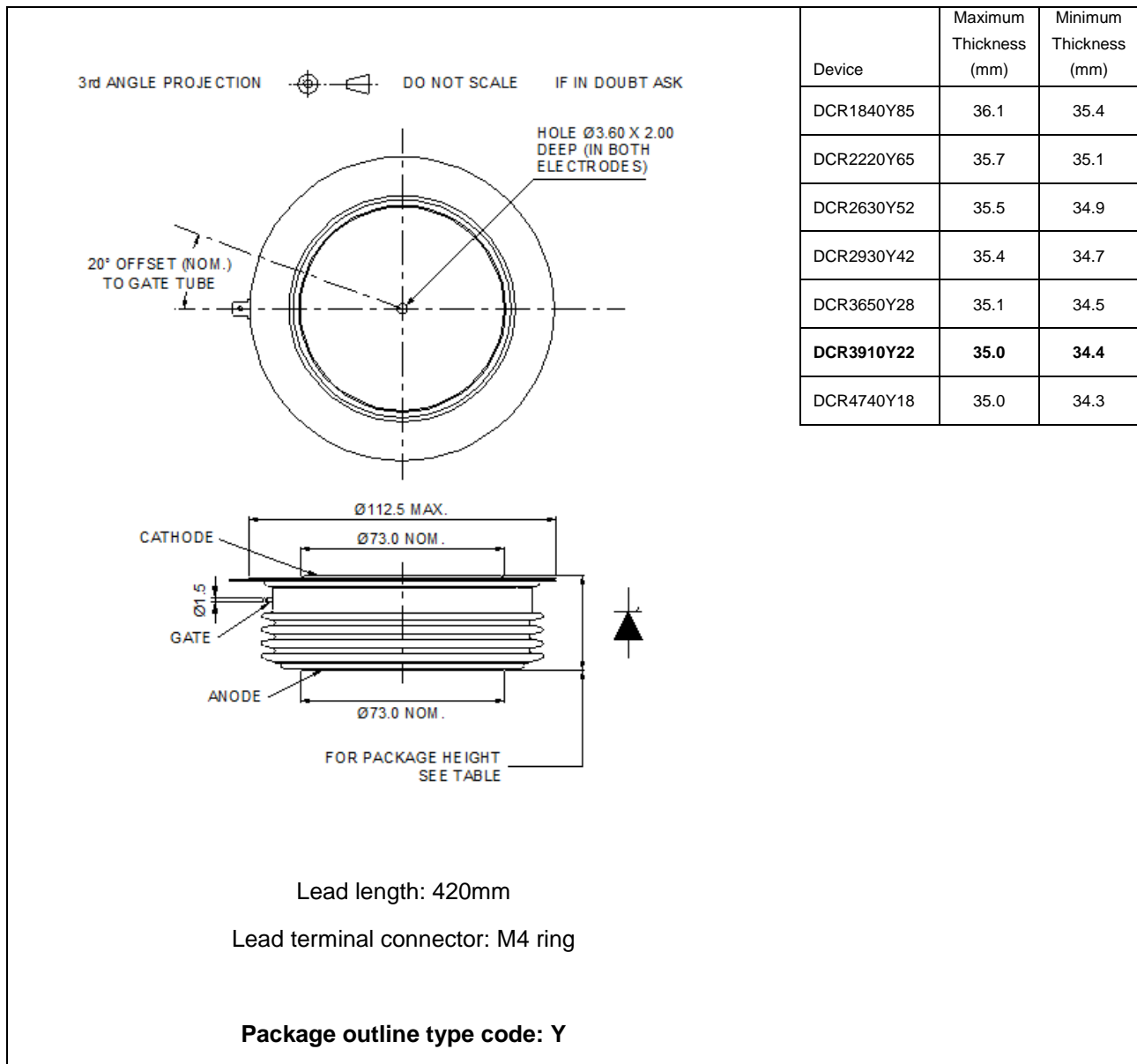


Fig. 16 Package outline

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